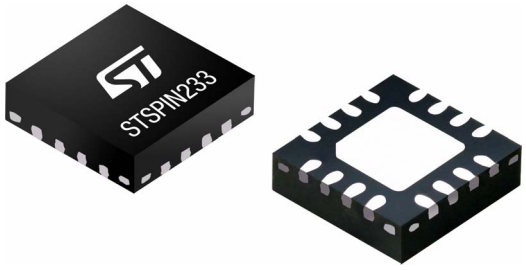
STSPIN233

Low voltage three phase and three sense motor driver

Datasheet - production data



VFQFPN 3 x 3 x 1.0 (16-pin)

Features

- Operating voltage from 1.8 to 10 V
- Maximum output current 1.3 Arms
- $R_{DS(ON)}$ HS + LS = 0.4 Ω typ.
- Full protection set
  - Non-dissipative overcurrent protection
  - Short-circuit protection
  - Thermal shutdown
- Supporting three shunt sensing topology
- Direct driving, dedicated input and enable pin for each half-bridge
- Energy saving and long battery life with standby consumption less than 80 nA

Applications

- Battery-powered 3-phase brushless (BLDC) motors in applications such as
  - Drones and portable gimbals
  - Portable health care products
  - Low voltage electronic valves
  - Portable medical equipment
  - Toys
  - Robotics

Description

The STSPIN233 device integrates a triple half-bridge low $R_{DS(ON)}$ power stage in a small VFQFPN 3 x 3 x 1.0 mm package ideal for small and space constrained applications.

The device is designed to operate in battery-powered scenarios and can be forced in a zero consumption state, allowing a significant increase in battery life.

The STSPIN233 is supporting three shunt sensing topology.

The device offers a complete set of protection including overcurrent, overtemperature and short-circuit protection.

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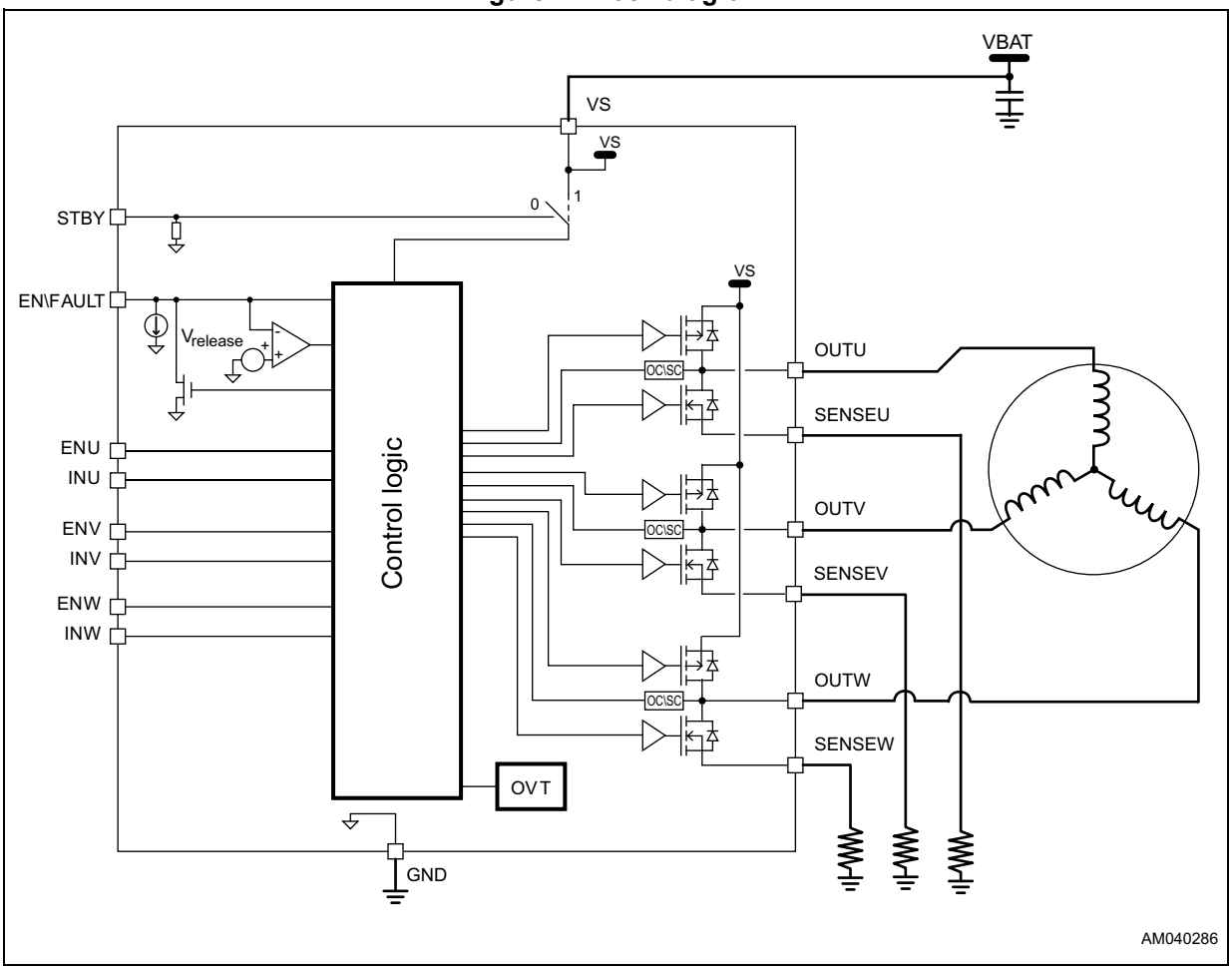
Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_S	Supply voltage	-	-0.3 to 11	V
V_{IN}	Logic input voltage	-	-0.3 to 5.5	V
V_{OUT} - V_{SENSE}	Output to sense voltage drop	-	up to 12	V
V_S - V_{OUT}	Supply to output voltage drop	-	up to 12	V
V_{SENSE}	Sense pins voltage	-	-1 to 1	V
$I_{OUT,RMS}$	Continuous power stage output current (each bridge)	-	1.3	Arms
T_j	Junction temperature	-	-40 to 150	°C
T_{STG}	Storage temperature	-	-55 to 150	°C

2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage	-	1.8	-	10	V
V_{IN}	Logic input voltage	-	0	-	5	V

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Conditions	Value	Unit
R_{thJA}	Junction to ambient thermal resistance	Natural convection, according to JESD51-2A(1)	57.1	°C/W
$R_{thJCtop}$	Junction to case thermal resistance (top side)	Simulation with cold plate on package top	67.3	°C/W
$R_{thJCbot}$	Junction to case thermal resistance (bottom side)	Simulation with cold plate on exposed pad	9.1	°C/W
R_{thJB}	Junction to board thermal resistance	according to JESD51-8(1)	23.3	°C/W
Ψ_{JT}	Junction to top characterization	According to JESD51-2A(1)	3.3	°C/W
Ψ_{JB}	Junction to board characterization	According to JESD51-2A(1)	22.6	°C/W

1. Simulated on a 21.2 x 21.2 mm board, 2s2p 1 Oz copper and four 300 µm vias below the exposed pad.

2.4 ESD protection ratings

Table 4. ESD protection ratings

Symbol	Parameter	Conditions	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	C2	750	V

3 Electrical characteristics

Testing conditions: V_S = 5 V, T_j = 25 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
$V_{Sth(ON)}$	V_S turn-on voltage	V_S rising from 0 V	1.45	1.65	1.79	V
$V_{Sth(OFF)}$	V_S turn-off voltage	V_S falling from 5 V	1.3	1.45	1.65	V
$V_{Sth(HYS)}$	V_S hysteresis voltage	-	-	180	-	mV
I_S	V_S supply current	No commutations EN = 0	-	900	1300	µA
		No commutations EN = 1	-	1500	1950	µA
$I_{S,STBY}$	V_S standby current	STBY = 0 V	-	10	80	nA
V_{STBYL}	Standby low voltage	-	-	-	0.9	V
V_{STBYH}	Standby high voltage	-	1.48	-	-	V
Power stage						
$R_{DS(ON)HS+LS}$	Total on resistance HS + LS	V_S = 10 V, I_{OUT} = 1.3 A	-	0.4	0.65	Ω
		V_S = 10 V, I_{OUT} = 1.3 A, T_j = 125 °C(1)	-	0.53	0.87	
		V_S = 3 V, I_{OUT} = 0.4 A	-	0.53	0.8	
I_{DSS}	Leakage current	OUTx = V_S	-	-	1	µA
		OUTx = GND	- 1	-	-	
V_{DF}	Freewheeling diode forward voltage	I_D = 1.3 A	-	0.9	-	V
t_{rise}	Rise time	V_S = 10 V; unloaded outputs	-	10	-	ns
t_{fall}	Fall time	V_S = 10 V; unloaded outputs	-	10	-	ns
t_{DT}	Integrated dead time		-	50	-	ns
Logic IOs						
V_{IH}	High logic level input voltage	-	1.6	-	-	V
V_{IL}	Low logic level input voltage	-	-	-	0.6	V
$V_{RELEASE}$	FAULT open-drain release voltage	-	-	-	0.4	V
V_{OL}	EN Low logic level output voltage	I_{EN} = 4 mA	-	-	0.4	V
R_{STBY}	STBY pull-down resistance	-	-	36	-	kΩ
I_{PDEN}	EN pull-down current	-	-	10.5	-	µA
t_{End}	EN input propagation delay	From EN falling edge to OUT high impedance	-	55	-	ns
$t_{IN,d(ON)}$	Turn-on propagation delay	From INx rising edge to 10% of OUTx	-	125	-	ns
$t_{IN,d(OFF)}$	Turn-off propagation delay	From INx falling edge to 90% of OUTx	-	140	-	ns

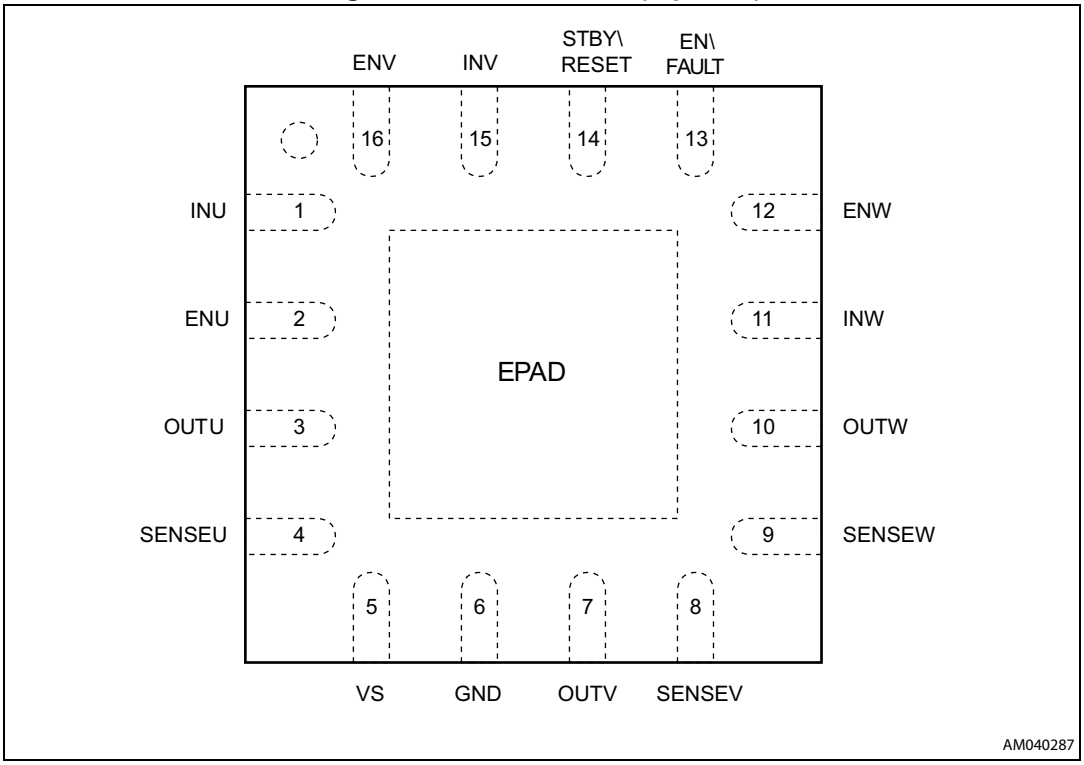
Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Protections						
T_{jSD}	Thermal shutdown threshold	-	-	160	-	°C
$T_{jSD,Hyst}$	Thermal shutdown hysteresis	-	-	40	-	°C
I_{OC}	Overcurrent threshold	See *Figure 10 on page 18*	-	2	-	A

1. Based on characterization data on a limited number of samples, not tested during production.

4 Pin description

Figure 2. Pin connection (top view)



Note: The exposed pad must be connected to ground.

Table 6. Pin description

No.	Name	Type	Function
1	INU	Logic input	Output U driving input
2	ENU	Logic input	Output U enable input
3	OUTU	Power output	Power bridge output U
4	SENSEU	Power output	Sense output bridge U
5	VS	Supply	Device supply voltage
6 EPAD	GND	Ground	Device ground
7	OUTV	Power output	Power bridge output V
8	SENSEV	Power output	Sense output bridge V
9	SENSEW	Power output	Sense output bridge W
10	OUTW	Power output	Power bridge output W
11	INW	Logic input	Output W driving input
12	ENW	Logic input	Output W enable input

Table 6. Pin description (continued)

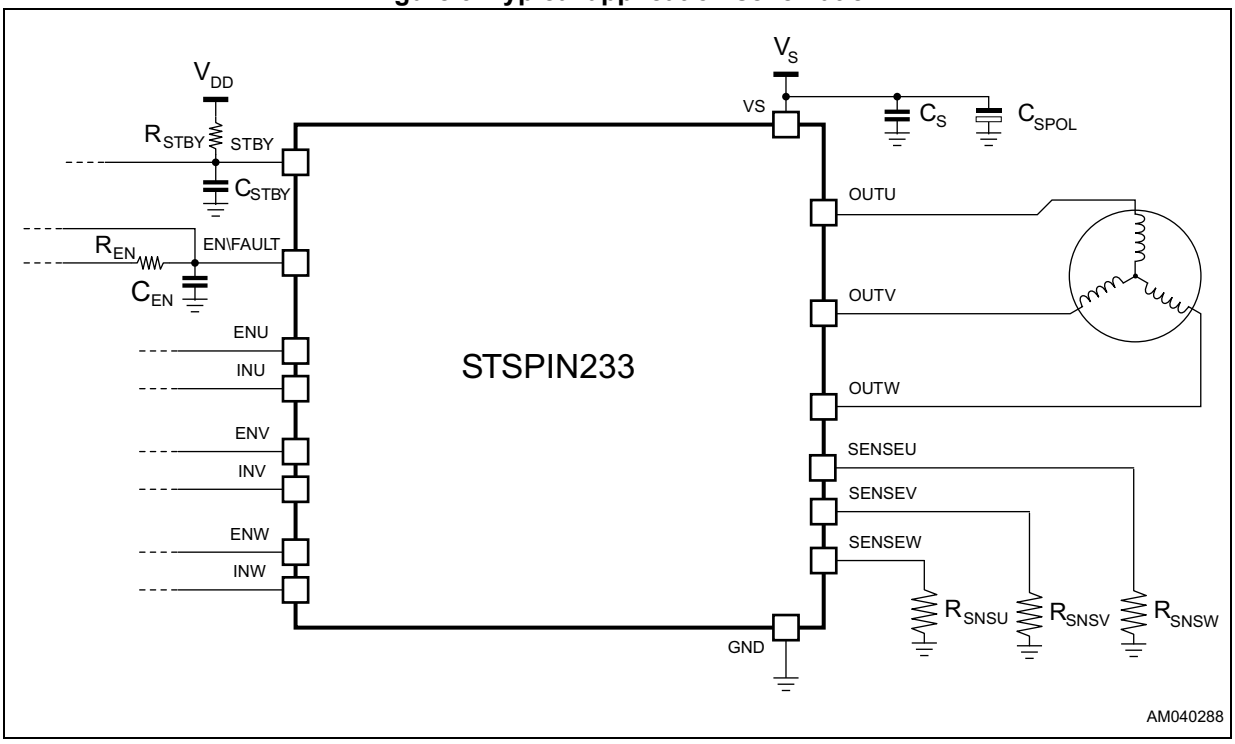
No.	Name	Type	Function
13	EN\FAULT	Logic input\ open-drain output	Logic input 5 V compliant whit and open-drain output. This is the enable of the power stage (when low, the power stage is turned off) and it is forced low through the integrated open-drain MOSFET when a failure occurs.
14	STBY\RESET	Logic input	Logic input 5 V compliant. When forced low, the device is forced in low consumption mode.
15	INV	Logic input	Output V driving input
16	ENV	Logic input	Output V enable input

5 Typical applications

Table 7. Typical application values

Name	Value
C_S	2.2 µF / 16 V
C_{SPOL}	22 µF / 16 V
R_{SNSU}, R_{SNSV}, R_{SNSW}	330 mΩ / 1 W
C_{EN}	10 nF / 6.3 V
R_{EN}	18 kΩ
C_{STBY}	1 nF / 6.3 V
R_{STBY}	18 kΩ

Figure 3. Typical application schematic



6 Description

The STSPIN233 device is a protected triple half-bridge motor driver.

6.1 Standby and power-up

The device provides a low consumption mode which is set forcing the STBY\RESET input below the V_{STBYL} threshold.

When the device is in the standby status the power stage is disabled (outputs are in high impedance) and the supply to the integrated control circuitry is cut off. When the device leaves the standby status, all the control circuitry is reset at power-up condition.

6.2 Motor driving

The outputs of the three half-bridges are directly driven through the logic input as listed in *Table 8*.

Table 8. ENx and INx truth table

EN\FAULT	ENx	INx	OUTx	'x' half-bridge condition
0	X	X	HiZ	Disabled
1	0	X	HiZ	Disabled
1	1	0	GND	Low side MOSFET ON
1	1	1	VS	High side MOSFET ON

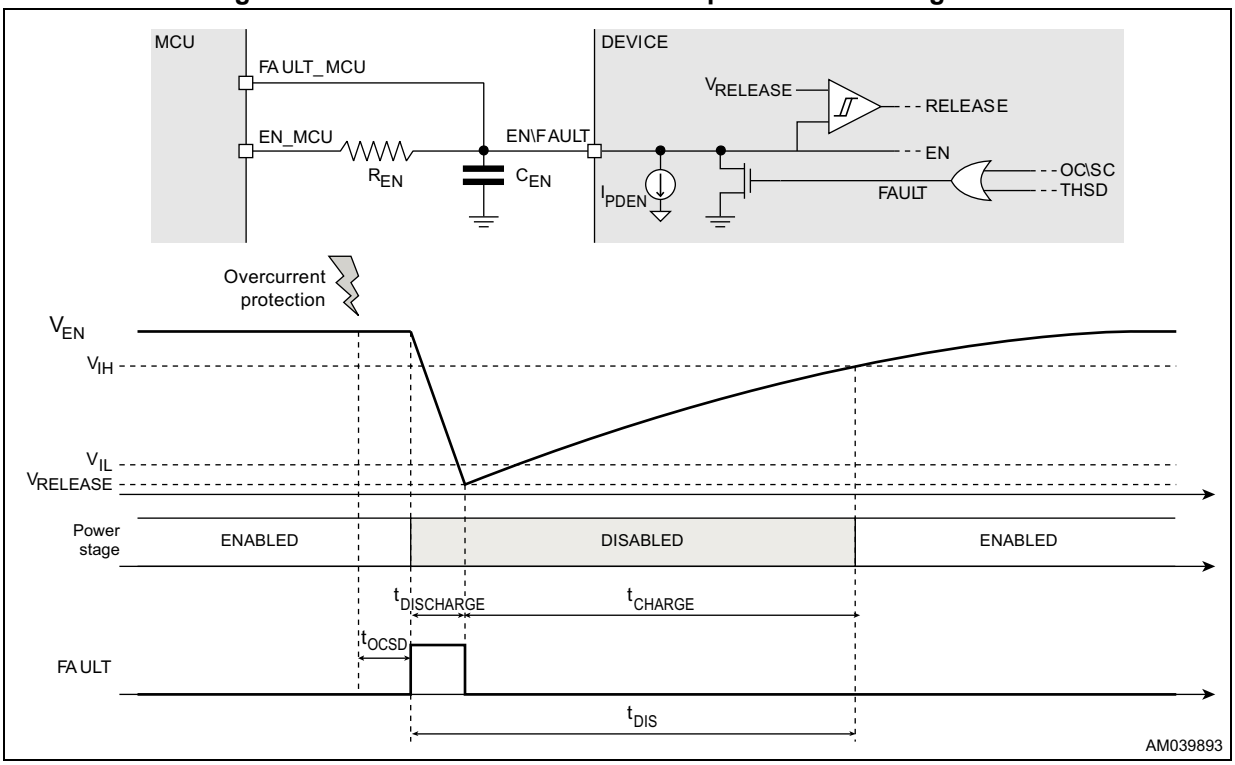
6.3 Overcurrent and short-circuit protections

The device embeds a circuitry protecting each power output against the overload and short-circuit conditions (short-circuit to ground, short-circuit to VS and short-circuit between outputs).

When the overcurrent or the short-circuit protection is triggered, the power stage is disabled and the EN\FAULT input is forced low through the integrated open-drain MOSFET discharging the external C_{EN} capacitor (refer to *Figure 4*).

The power stage is kept disabled and the open-drain MOSFET is kept ON until the EN\FAULT input falls below the $V_{RELEASE}$ threshold, then the C_{EN} capacitor is charged through the R_{EN} resistor.

Figure 4. Overcurrent and short-circuit protections management



The total disable time after an overcurrent event can be set sizing properly the external network connected to the EN\FAULT pin (refer to *Figure 4*).

Equation 1

$$t_{DIS} = t_{discharge} + t_{charge}$$

But t_{charge} is normally very higher than $t_{discharge}$, we can consider only the second one contribution:

Equation 2

$$t_{DIS} \cong R_{EN} \cdot C_{EN} \cdot \ln \frac{(V_{DD} - R_{EN} \cdot I_{PD}) - V_{RELEASE}}{(V_{DD} - R_{EN} \cdot I_{PD}) - V_{IH}}$$

Where V_{DD} is the pull-up voltage of the R_{EN} resistor.

Figure 5. Disable time versus R_{EN} and C_{EN} values (V_{DD} = 3.3 V)

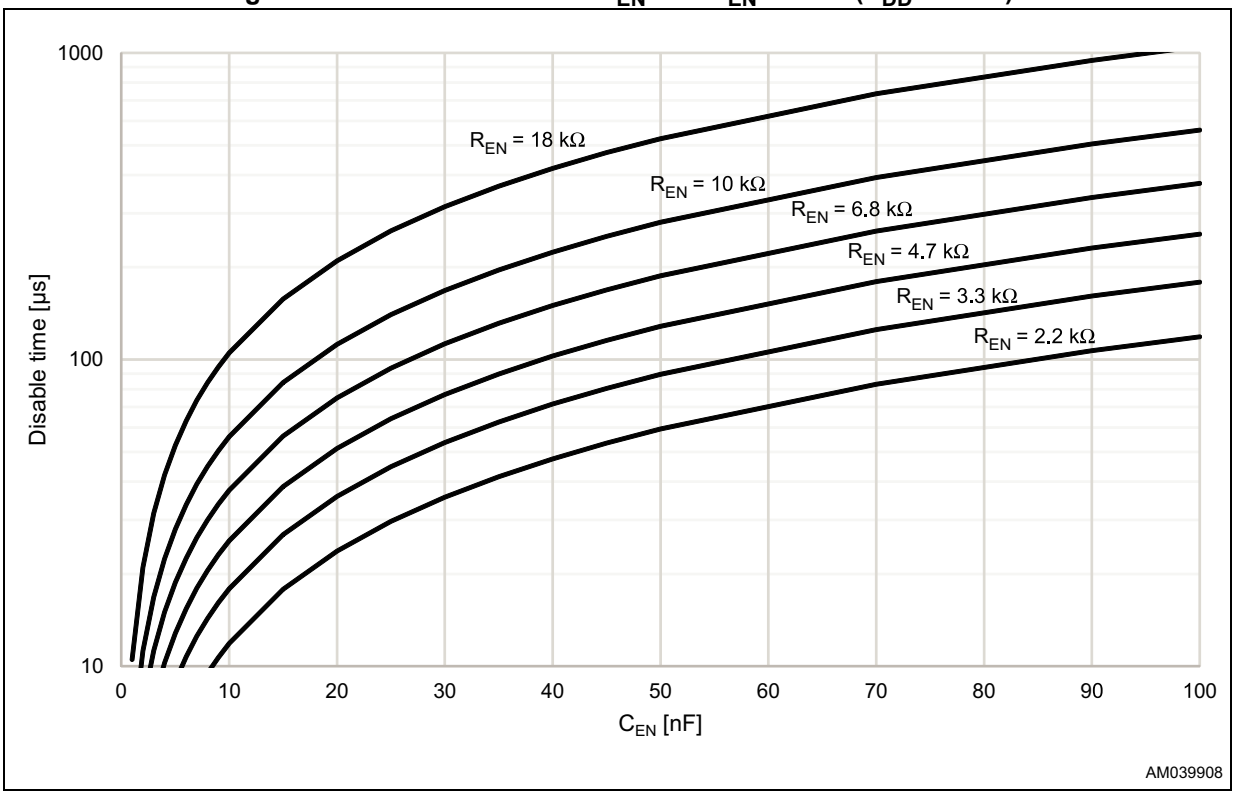
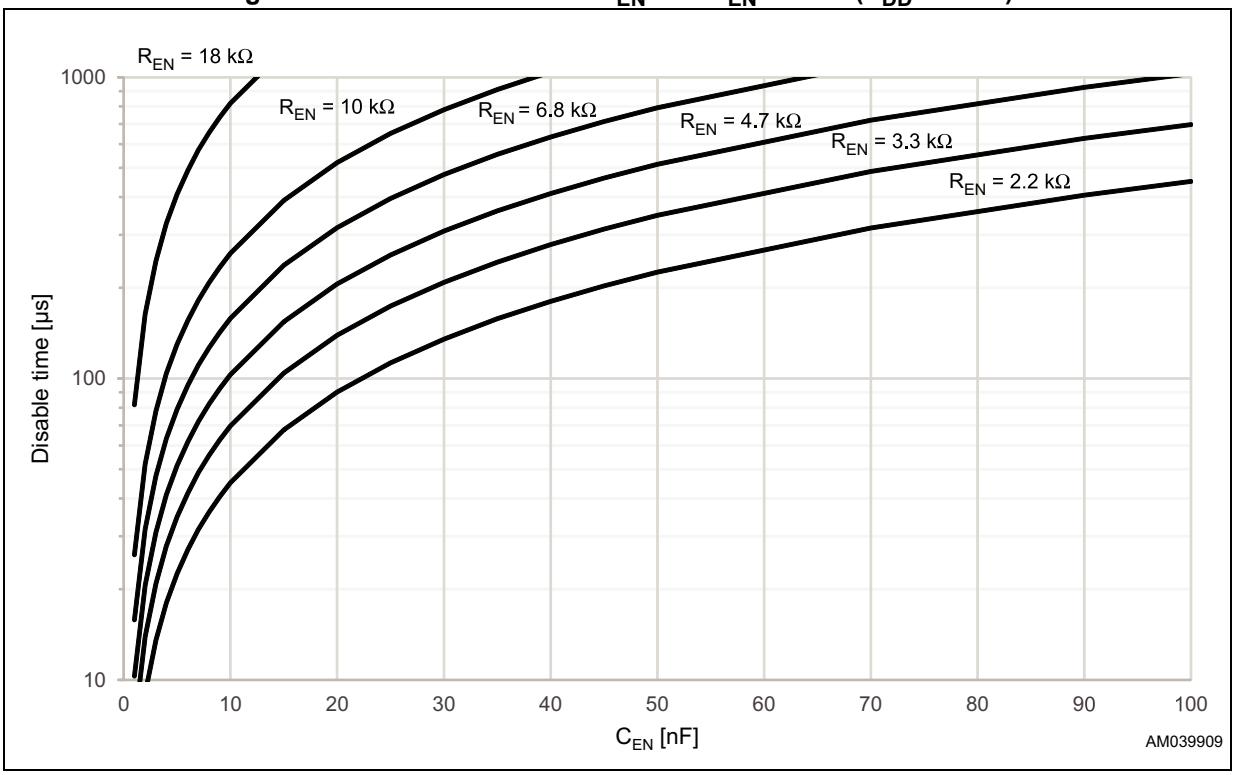


Figure 6. Disable time versus R_{EN} and C_{EN} values (V_{DD} = 1.8 V)



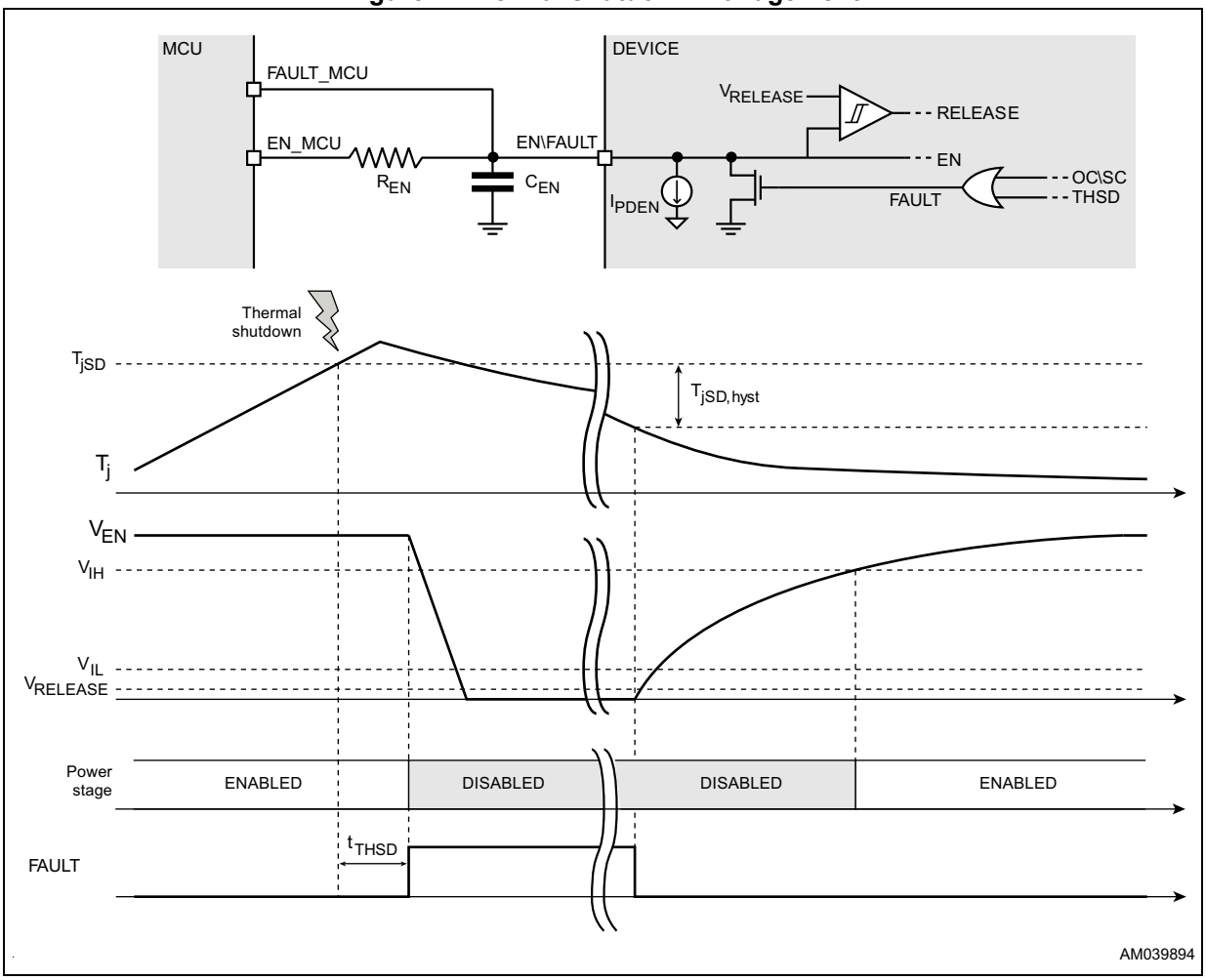
6.4 Thermal shutdown

The device embeds circuitry protecting it from the overtemperature condition.

When the thermal shutdown temperature is reached, the power stage is disabled and the EN\FAULT input is forced low through the integrated open-drain MOSFET (refer to *Figure 7*).

The protection and the EN\FAULT output are released when the IC temperature returns below a safe operating value (T_{jSD} - $T_{jSD,Hyst}$).

Figure 7. Thermal shutdown management



7 Graphs

Figure 8. Power stage resistance versus supply voltage

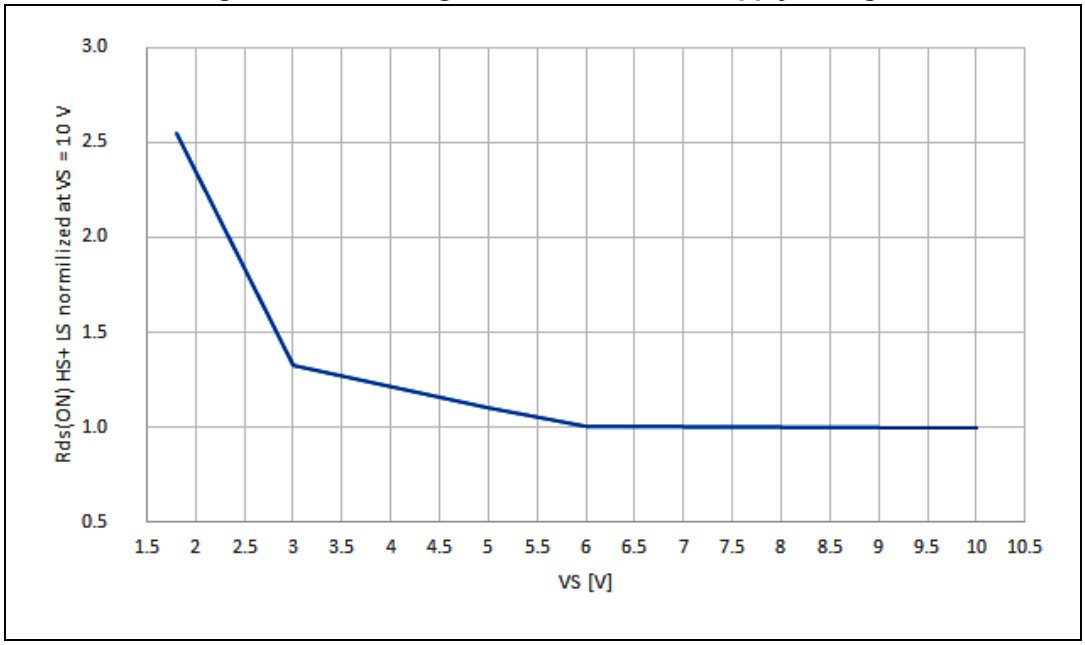


Figure 9. Power stage resistance versus temperature

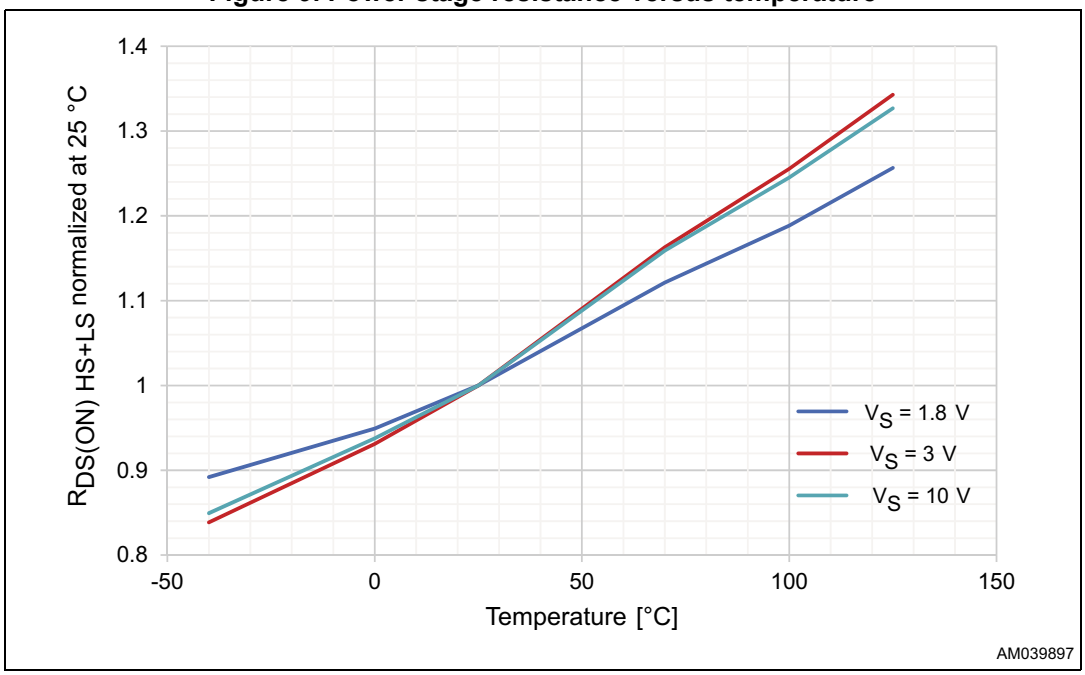
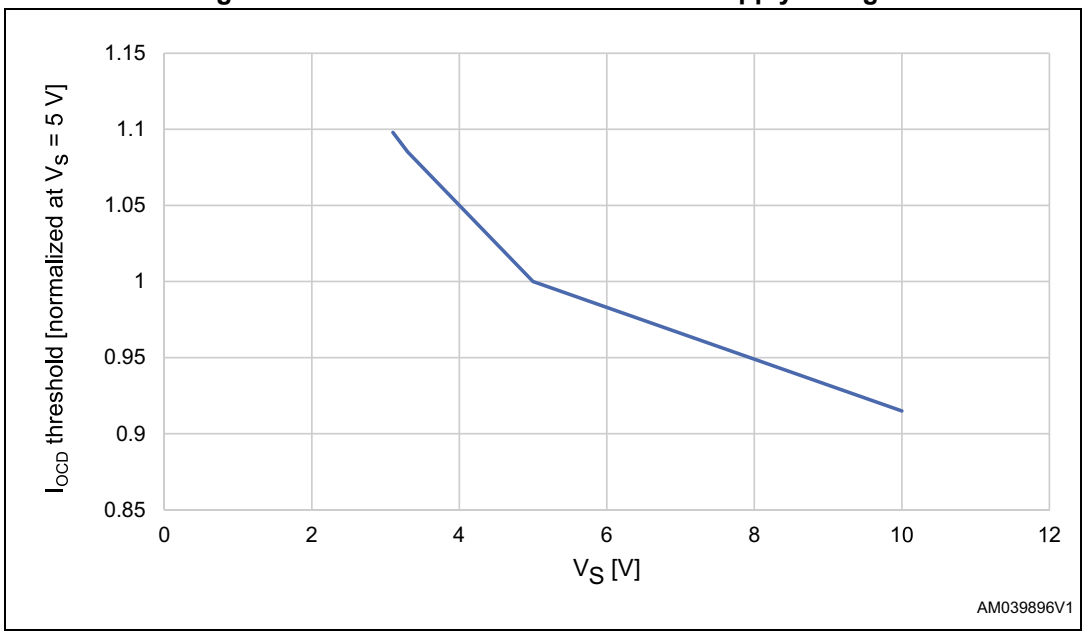


Figure 10. Overcurrent threshold versus supply voltage



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 VFQFPN 3 x 3 x 1.0 16L package information

Figure 11. VFQFPN 3 x 3 x 1.0 16L package outline

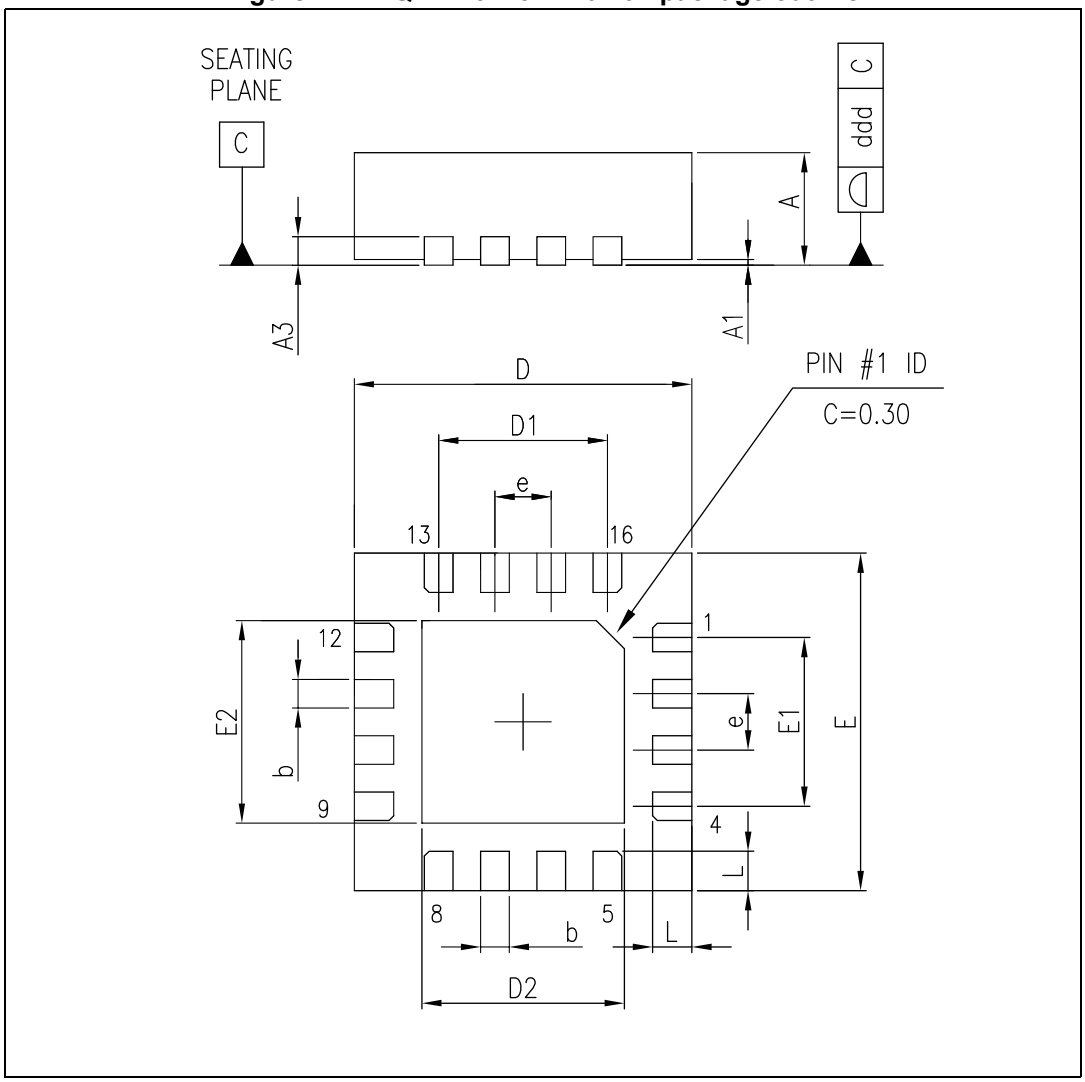
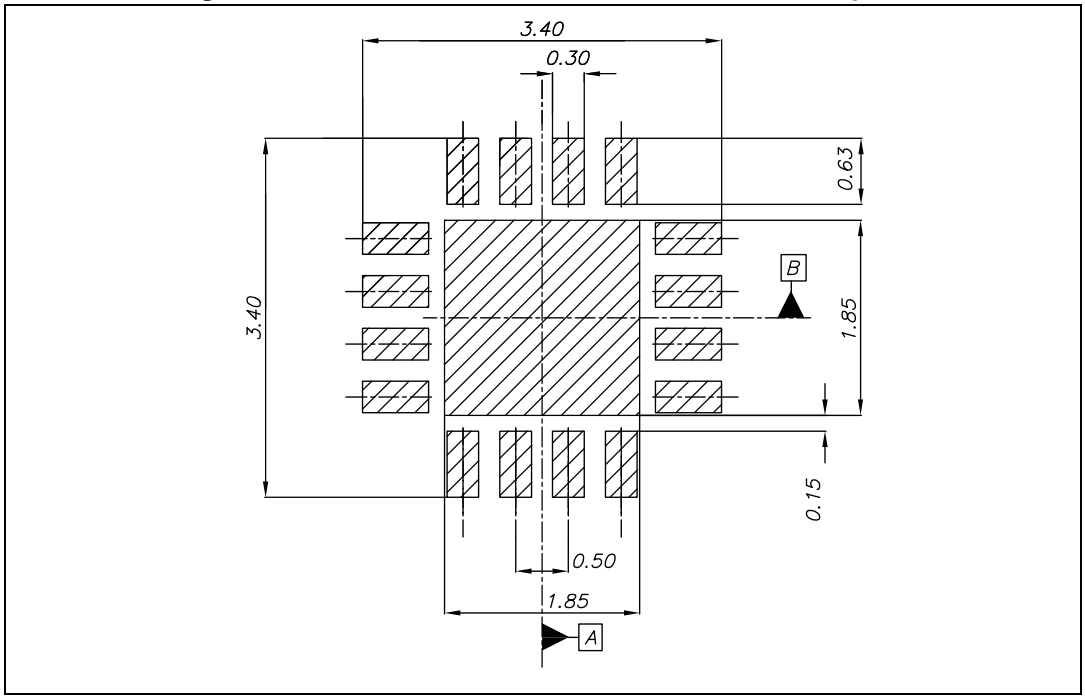


Table 9. VFQFPN 3 x 3 x 1.0 16L package mechanical data(1)

Symbol	Dimensions (mm)			Notes
	Min.	Typ.	Max.	
A	0.80	0.90	1.00	-
A1	0.00	0.02	0.005	(2)
A3	-	0.20 REF.	-	-
b	0.20	0.25	0.30	(3)
D	3.00 BSC			-
D1	1.50 BSC			-
D2	1.70	1.80	1.90	-
e	0.50 BSC			-
E	3.00 BSC			-
E1	1.50 BSC			-
E2	1.70	1.80	1.90	-
L	0.30	0.40	0.50	(3)
ddd	0.05			-

1. VFQFPN stands for thermally enhanced “Very thin Fine pitch Quad Packages No lead”. Very thin: 0.80 < A ≤ 1.00 mm / fine pitch: e < 1.00 mm. The topside terminal A1 indicator may be a molded or metalized feature. The optional indicator on the bottom surface may be a molded, marked or metalized feature.
2. A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).
3. Dimensions “b” and “L” are measured at terminal plating surface.

Figure 12. VFQFPN 3 x 3 x 1.0 16L recommended footprint



9 Ordering information

Table 10. Device summary

Order code	Package	Packaging
STSPIN233	VFQFPN 3 x 3 x 1.0 16L	Tape and reel

10 Revision history

Table 11. Document revision history

Date	Revision	Changes
17-Jan-2018	1	Initial release.