



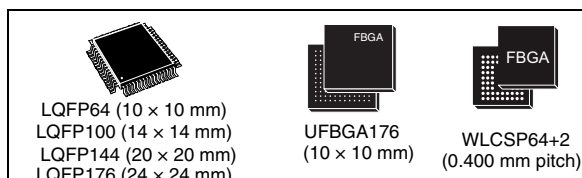
STM32F205xx STM32F207xx

ARM-based 32-bit MCU, 150DMIPs, up to 1 MB Flash/128+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Datasheet – production data

Features

- Core: ARM 32-bit Cortex™-M3 CPU (120 MHz max) with Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution performance from Flash memory, MPU, 150 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1)
- Memories
 - Up to 1 Mbyte of Flash memory
 - 512 bytes of OTP memory
 - Up to 128 + 4 Kbytes of SRAM
 - Flexible static memory controller that supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
 - LCD parallel interface, 8080/6800 modes
- CRC calculation unit
- Clock, reset and supply management
 - From 1.8 to 3.6 V application supply+I/Os
 - POR, PDR, PVD and BOR
 - 4 to 26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 20 × 32 bit backup registers, and optional 4 KB backup SRAM
- 3 × 12-bit, 0.5 μs ADCs with up to 24 channels and up to 6 MSPS in triple interleaved mode
- 2 × 12-bit D/A converters
- General-purpose DMA: 16-stream controller with centralized FIFOs and burst support
- 96-bit unique ID
- Up to 17 timers
 - Up to twelve 16-bit and two 32-bit timers, up to 120 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode: Serial wire debug (SWD), JTAG, and Cortex-M3 Embedded Trace Macrocell™



- Up to 140 I/O ports with interrupt capability:
 - Up to 136 fast I/Os up to 60 MHz
 - Up to 138 5 V-tolerant I/Os
- Up to 15 communication interfaces
 - Up to 3 × I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs and 2 UARTs (7.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
 - Up to 3 SPIs (30 Mbit/s), 2 with muxed I²S to achieve audio class accuracy via audio PLL or external PLL
 - 2 × CAN interfaces (2.0B Active)
 - SDIO interface
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface (48 Mbyte/s max)
- Analog true random number generator

Table 1. Device summary

| Reference | Part number |
|-------------|--|
| STM32F205xx | STM32F205RB, STM32F205RC, STM32F205RE, STM32F205RF, STM32F205RG, STM32F205VB, STM32F205VC, STM32F205VE, STM32F205VF, STM32F205VG, STM32F205ZC, STM32F205ZE, STM32F205ZF, STM32F205ZG |
| STM32F207xx | STM32F207IC, STM32F207IE, STM32F207IF, STM32F207IG, STM32F207ZC, STM32F207ZE, STM32F207ZF, STM32F207ZG, STM32F207VC, STM32F207VE, STM32F207VF, STM32F207VG |

Contents

| | | |
|----------|---|-----------|
| 1 | Introduction | 10 |
| 2 | Description | 11 |
| 2.1 | Full compatibility throughout the family | 15 |
| 2.2 | Device overview | 17 |
| 2.2.1 | ARM® Cortex™-M3 core with embedded Flash and SRAM | 18 |
| 2.2.2 | Adaptive real-time memory accelerator (ART Accelerator™) | 18 |
| 2.2.3 | Memory protection unit | 18 |
| 2.2.4 | Embedded Flash memory | 18 |
| 2.2.5 | CRC (cyclic redundancy check) calculation unit | 19 |
| 2.2.6 | Embedded SRAM | 19 |
| 2.2.7 | Multi-AHB bus matrix | 19 |
| 2.2.8 | DMA controller (DMA) | 20 |
| 2.2.9 | Flexible static memory controller (FSMC) | 20 |
| 2.2.10 | Nested vectored interrupt controller (NVIC) | 21 |
| 2.2.11 | External interrupt/event controller (EXTI) | 21 |
| 2.2.12 | Clocks and startup | 21 |
| 2.2.13 | Boot modes | 22 |
| 2.2.14 | Power supply schemes | 22 |
| 2.2.15 | Power supply supervisor | 22 |
| 2.2.16 | Voltage regulator | 22 |
| 2.2.17 | Real-time clock (RTC), backup SRAM and backup registers | 24 |
| 2.2.18 | Low-power modes | 25 |
| 2.2.19 | V _{BAT} operation | 26 |
| 2.2.20 | Timers and watchdogs | 26 |
| 2.2.21 | Inter-integrated circuit interface (I ² C) | 28 |
| 2.2.22 | Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs) | 28 |
| 2.2.23 | Serial peripheral interface (SPI) | 29 |
| 2.2.24 | Inter-integrated sound (I ² S) | 29 |
| 2.2.25 | SDIO | 30 |
| 2.2.26 | Ethernet MAC interface with dedicated DMA and IEEE 1588 support | 30 |
| 2.2.27 | Controller area network (CAN) | 31 |
| 2.2.28 | Universal serial bus on-the-go full-speed (OTG_FS) | 31 |

| | | |
|----------|---|-----------|
| 2.2.29 | Universal serial bus on-the-go high-speed (OTG_HS) | 31 |
| 2.2.30 | Audio PLL (PLLI2S) | 32 |
| 2.2.31 | Digital camera interface (DCMI) | 32 |
| 2.2.32 | True random number generator (RNG) | 32 |
| 2.2.33 | GPIOs (general-purpose inputs/outputs) | 33 |
| 2.2.34 | ADCs (analog-to-digital converters) | 33 |
| 2.2.35 | DAC (digital-to-analog converter) | 33 |
| 2.2.36 | Temperature sensor | 34 |
| 2.2.37 | Serial wire JTAG debug port (SWJ-DP) | 34 |
| 2.2.38 | Embedded Trace Macrocell™ | 34 |
| 3 | Pinouts and pin description | 35 |
| 4 | Memory mapping | 58 |
| 5 | Electrical characteristics | 60 |
| 5.1 | Parameter conditions | 60 |
| 5.1.1 | Minimum and maximum values | 60 |
| 5.1.2 | Typical values | 60 |
| 5.1.3 | Typical curves | 60 |
| 5.1.4 | Loading capacitor | 60 |
| 5.1.5 | Pin input voltage | 60 |
| 5.1.6 | Power supply scheme | 61 |
| 5.1.7 | Current consumption measurement | 62 |
| 5.2 | Absolute maximum ratings | 62 |
| 5.3 | Operating conditions | 63 |
| 5.3.1 | General operating conditions | 63 |
| 5.3.2 | VCAP1/VCAP2 external capacitor | 66 |
| 5.3.3 | Operating conditions at power-up / power-down (regulator ON) | 67 |
| 5.3.4 | Operating conditions at power-up / power-down (regulator OFF) | 67 |
| 5.3.5 | Embedded reset and power control block characteristics | 68 |
| 5.3.6 | Supply current characteristics | 69 |
| 5.3.7 | Wakeup time from low-power mode | 80 |
| 5.3.8 | External clock source characteristics | 81 |
| 5.3.9 | Internal clock source characteristics | 85 |
| 5.3.10 | PLL characteristics | 86 |
| 5.3.11 | PLL spread spectrum clock generation (SSCG) characteristics | 89 |

| | | |
|-------------------|--|------------|
| 5.3.12 | Memory characteristics | 90 |
| 5.3.13 | EMC characteristics | 92 |
| 5.3.14 | Absolute maximum ratings (electrical sensitivity) | 94 |
| 5.3.15 | I/O current injection characteristics | 95 |
| 5.3.16 | I/O port characteristics | 96 |
| 5.3.17 | NRST pin characteristics | 100 |
| 5.3.18 | TIM timer characteristics | 101 |
| 5.3.19 | Communications interfaces | 102 |
| 5.3.20 | 12-bit ADC characteristics | 115 |
| 5.3.21 | DAC electrical characteristics | 120 |
| 5.3.22 | Temperature sensor characteristics | 122 |
| 5.3.23 | V _{BAT} monitoring characteristics | 122 |
| 5.3.24 | Embedded reference voltage | 123 |
| 5.3.25 | FSMC characteristics | 123 |
| 5.3.26 | Camera interface (DCMI) timing specifications | 141 |
| 5.3.27 | SD/SDIO MMC card host interface (SDIO) characteristics | 141 |
| 5.3.28 | RTC characteristics | 142 |
| 6 | Package characteristics | 143 |
| 6.1 | Package mechanical data | 143 |
| 6.2 | Thermal characteristics | 154 |
| 7 | Part numbering | 155 |
| Appendix A | Application block diagrams | 156 |
| A.1 | Main applications versus package | 156 |
| A.2 | Application example with regulator OFF | 157 |
| A.3 | USB OTG full speed (FS) interface solutions | 158 |
| A.4 | USB OTG high speed (HS) interface solutions | 160 |
| A.5 | Complete audio player solutions | 161 |
| A.6 | Ethernet interface solutions | 164 |
| 8 | Revision history | 166 |

List of tables

| | | |
|-----------|--|----|
| Table 1. | Device summary | 1 |
| Table 2. | STM32F205xx features and peripheral counts | 12 |
| Table 3. | STM32F207xx features and peripheral counts | 13 |
| Table 4. | Timer feature comparison | 26 |
| Table 5. | USART feature comparison | 29 |
| Table 6. | STM32F20x pin and ball definitions | 39 |
| Table 7. | FSMC pin definition | 50 |
| Table 8. | Alternate function mapping | 53 |
| Table 9. | Voltage characteristics | 62 |
| Table 10. | Current characteristics | 63 |
| Table 11. | Thermal characteristics | 63 |
| Table 12. | General operating conditions | 63 |
| Table 13. | Limitations depending on the operating power supply range | 64 |
| Table 14. | VCAP1/VCAP2 operating conditions | 66 |
| Table 15. | Operating conditions at power-up / power-down (regulator ON) | 67 |
| Table 16. | Operating conditions at power-up / power-down (regulator OFF) | 67 |
| Table 17. | Embedded reset and power control block characteristics | 68 |
| Table 18. | Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled) | 70 |
| Table 19. | Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM | 71 |
| Table 20. | Typical and maximum current consumption in Sleep mode | 74 |
| Table 21. | Typical and maximum current consumptions in Stop mode | 76 |
| Table 22. | Typical and maximum current consumptions in Standby mode | 77 |
| Table 23. | Typical and maximum current consumptions in V _{BAT} mode | 77 |
| Table 24. | Peripheral current consumption | 78 |
| Table 25. | Low-power mode wakeup timings | 80 |
| Table 26. | High-speed external user clock characteristics | 81 |
| Table 27. | Low-speed external user clock characteristics | 81 |
| Table 28. | HSE 4-26 MHz oscillator characteristics | 83 |
| Table 29. | LSE oscillator characteristics (f _{LSE} = 32.768 kHz) | 84 |
| Table 30. | HSI oscillator characteristics | 85 |
| Table 31. | LSI oscillator characteristics | 86 |
| Table 32. | Main PLL characteristics | 86 |
| Table 33. | PLLI2S (audio PLL) characteristics | 87 |
| Table 34. | SSCG parameters constraint | 89 |
| Table 35. | Flash memory characteristics | 90 |
| Table 36. | Flash memory programming | 91 |
| Table 37. | Flash memory programming with V _{PP} | 91 |
| Table 38. | Flash memory endurance and data retention | 92 |
| Table 39. | EMS characteristics | 93 |
| Table 40. | EMI characteristics | 94 |
| Table 41. | ESD absolute maximum ratings | 94 |
| Table 42. | Electrical sensitivities | 95 |
| Table 43. | I/O current injection susceptibility | 95 |
| Table 44. | I/O static characteristics | 96 |
| Table 45. | Output voltage characteristics | 97 |
| Table 46. | I/O AC characteristics | 98 |

| | | |
|-----------|--|-----|
| Table 47. | NRST pin characteristics | 100 |
| Table 48. | Characteristics of TIMx connected to the APB1 domain | 101 |
| Table 49. | Characteristics of TIMx connected to the APB2 domain | 102 |
| Table 50. | I ² C characteristics | 103 |
| Table 51. | SCL frequency (f _{PCLK1} = 30 MHz, V _{DD} = 3.3 V) | 104 |
| Table 52. | SPI characteristics | 105 |
| Table 53. | I ² S characteristics | 108 |
| Table 54. | USB OTG FS startup time | 110 |
| Table 55. | USB OTG FS DC electrical characteristics | 110 |
| Table 56. | USB OTG FS electrical characteristics | 111 |
| Table 57. | USB HS DC electrical characteristics | 111 |
| Table 58. | Clock timing parameters | 111 |
| Table 59. | ULPI timing | 112 |
| Table 60. | Ethernet DC electrical characteristics | 112 |
| Table 61. | Dynamics characteristics: Ethernet MAC signals for SMI | 113 |
| Table 62. | Dynamics characteristics: Ethernet MAC signals for RMII | 113 |
| Table 63. | Dynamics characteristics: Ethernet MAC signals for MII | 114 |
| Table 64. | ADC characteristics | 115 |
| Table 65. | ADC accuracy | 117 |
| Table 66. | DAC characteristics | 120 |
| Table 67. | TS characteristics | 122 |
| Table 68. | V _{BAT} monitoring characteristics | 122 |
| Table 69. | Embedded internal reference voltage | 123 |
| Table 70. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings | 124 |
| Table 71. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings | 125 |
| Table 72. | Asynchronous multiplexed PSRAM/NOR read timings | 126 |
| Table 73. | Asynchronous multiplexed PSRAM/NOR write timings | 127 |
| Table 74. | Synchronous multiplexed NOR/PSRAM read timings | 129 |
| Table 75. | Synchronous multiplexed PSRAM write timings | 130 |
| Table 76. | Synchronous non-multiplexed NOR/PSRAM read timings | 131 |
| Table 77. | Synchronous non-multiplexed PSRAM write timings | 132 |
| Table 78. | Switching characteristics for PC Card/CF read and write cycles in attribute/common space | 137 |
| Table 79. | Switching characteristics for PC Card/CF read and write cycles in I/O space | 138 |
| Table 80. | Switching characteristics for NAND Flash read cycles | 140 |
| Table 81. | Switching characteristics for NAND Flash write cycles | 141 |
| Table 82. | DCMI characteristics | 141 |
| Table 83. | SD / MMC characteristics | 142 |
| Table 84. | RTC characteristics | 142 |
| Table 85. | LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data | 144 |
| Table 86. | WLCSP64+2 - 0.400 mm pitch wafer level chip size package mechanical data | 146 |
| Table 87. | LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data | 147 |
| Table 88. | LQFP144 20 x 20 mm, 144-pin low-profile quad flat package mechanical data | 149 |
| Table 89. | LQFP176 - Low profile quad flat package 24 x 24 x 1.4 mm package mechanical data | 151 |
| Table 90. | UFBGA176+25 - ultra thin fine pitch ball grid array 10 x 10 x 0.6 mm mechanical data | 153 |
| Table 91. | Package thermal characteristics | 154 |
| Table 92. | Ordering information scheme | 155 |
| Table 93. | Main applications versus package for STM32F2xxx microcontrollers | 156 |
| Table 94. | Document revision history | 166 |

List of figures

| | | |
|------------|--|-----|
| Figure 1. | Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package. | 15 |
| Figure 2. | Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package. | 16 |
| Figure 3. | Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package. | 16 |
| Figure 4. | STM32F20x block diagram. | 17 |
| Figure 5. | Multi-AHB matrix. | 19 |
| Figure 6. | Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization | 24 |
| Figure 7. | Startup in regulator OFF: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization | 24 |
| Figure 8. | STM32F20x LQFP64 pinout. | 35 |
| Figure 9. | STM32F20x WLCSP64+2 ballout. | 35 |
| Figure 10. | STM32F20x LQFP100 pinout. | 36 |
| Figure 11. | STM32F20x LQFP144 pinout. | 37 |
| Figure 12. | STM32F20x LQFP176 pinout. | 38 |
| Figure 13. | STM32F20x UFBGA176 ballout | 39 |
| Figure 14. | Memory map | 59 |
| Figure 15. | Pin loading conditions. | 60 |
| Figure 16. | Pin input voltage | 60 |
| Figure 17. | Power supply scheme | 61 |
| Figure 18. | Current consumption measurement scheme | 62 |
| Figure 19. | Number of wait states versus f_{CPU} and V_{DD} range. | 66 |
| Figure 20. | External capacitor C_{EXT} | 66 |
| Figure 21. | Typical current consumption vs temperature, Run mode, code with data processing running from RAM, and peripherals ON | 72 |
| Figure 22. | Typical current consumption vs temperature, Run mode, code with data processing running from RAM, and peripherals OFF | 72 |
| Figure 23. | Typical current consumption vs temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals ON | 73 |
| Figure 24. | Typical current consumption vs temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals OFF | 73 |
| Figure 25. | Typical current consumption vs temperature in Sleep mode, peripherals ON | 75 |
| Figure 26. | Typical current consumption vs temperature in Sleep mode, peripherals OFF | 75 |
| Figure 27. | Typical current consumption vs temperature in Stop mode | 76 |
| Figure 28. | High-speed external clock source AC timing diagram | 82 |
| Figure 29. | Low-speed external clock source AC timing diagram | 82 |
| Figure 30. | Typical application with an 8 MHz crystal | 83 |
| Figure 31. | Typical application with a 32.768 kHz crystal | 84 |
| Figure 32. | ACC_{HSI} versus temperature | 85 |
| Figure 33. | ACC_{LSI} versus temperature | 86 |
| Figure 34. | PLL output clock waveforms in center spread mode | 90 |
| Figure 35. | PLL output clock waveforms in down spread mode | 90 |
| Figure 36. | I/O AC characteristics definition | 99 |
| Figure 37. | Recommended NRST pin protection | 100 |

| | | |
|------------|---|-----|
| Figure 38. | I ² C bus AC waveforms and measurement circuit | 104 |
| Figure 39. | SPI timing diagram - slave mode and CPHA = 0 | 106 |
| Figure 40. | SPI timing diagram - slave mode and CPHA = 1 | 106 |
| Figure 41. | SPI timing diagram - master mode | 107 |
| Figure 42. | I ² S slave timing diagram (Philips protocol) ⁽¹⁾ | 109 |
| Figure 43. | I ² S master timing diagram (Philips protocol) ⁽¹⁾ | 109 |
| Figure 44. | USB OTG FS timings: definition of data signal rise and fall time | 111 |
| Figure 45. | ULPI timing diagram | 112 |
| Figure 46. | Ethernet SMI timing diagram | 113 |
| Figure 47. | Ethernet RMII timing diagram | 113 |
| Figure 48. | Ethernet MII timing diagram | 114 |
| Figure 49. | ADC accuracy characteristics | 117 |
| Figure 50. | Typical connection diagram using the ADC | 118 |
| Figure 51. | Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) | 119 |
| Figure 52. | Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) | 119 |
| Figure 53. | 12-bit buffered /non-buffered DAC | 122 |
| Figure 54. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms | 124 |
| Figure 55. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms | 125 |
| Figure 56. | Asynchronous multiplexed PSRAM/NOR read waveforms | 126 |
| Figure 57. | Asynchronous multiplexed PSRAM/NOR write waveforms | 127 |
| Figure 58. | Synchronous multiplexed NOR/PSRAM read timings | 128 |
| Figure 59. | Synchronous multiplexed PSRAM write timings | 130 |
| Figure 60. | Synchronous non-multiplexed NOR/PSRAM read timings | 131 |
| Figure 61. | Synchronous non-multiplexed PSRAM write timings | 132 |
| Figure 62. | PC Card/CompactFlash controller waveforms for common memory read access | 133 |
| Figure 63. | PC Card/CompactFlash controller waveforms for common memory write access | 134 |
| Figure 64. | PC Card/CompactFlash controller waveforms for attribute memory read access | 135 |
| Figure 65. | PC Card/CompactFlash controller waveforms for attribute memory write access | 136 |
| Figure 66. | PC Card/CompactFlash controller waveforms for I/O space read access | 136 |
| Figure 67. | PC Card/CompactFlash controller waveforms for I/O space write access | 137 |
| Figure 68. | NAND controller waveforms for read access | 139 |
| Figure 69. | NAND controller waveforms for write access | 139 |
| Figure 70. | NAND controller waveforms for common memory read access | 140 |
| Figure 71. | NAND controller waveforms for common memory write access | 140 |
| Figure 72. | SDIO high-speed mode | 141 |
| Figure 73. | SD default mode | 142 |
| Figure 74. | LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline | 144 |
| Figure 75. | Recommended footprint | 145 |
| Figure 76. | WLCSP64+2 - 0.400 mm pitch wafer level chip size package outline | 146 |
| Figure 77. | LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline | 147 |
| Figure 78. | Recommended footprint | 148 |
| Figure 79. | LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline | 149 |
| Figure 80. | Recommended footprint | 150 |
| Figure 81. | LQFP176 - Low profile quad flat package 24 x 24 x 1.4 mm, package outline | 151 |
| Figure 82. | LQFP176 recommended footprint | 152 |
| Figure 83. | UFPGA176+25 - ultra thin fine pitch ball grid array 10 x 10 x 0.6 mm, package outline | 153 |
| Figure 84. | Regulator OFF/internal reset ON | 157 |
| Figure 85. | Regulator OFF/ internal reset OFF | 157 |
| Figure 86. | USB OTG FS (full speed) device-only connection | 158 |

| | | |
|------------|--|-----|
| Figure 87. | USB OTG FS (full speed) host-only connection | 158 |
| Figure 88. | OTG FS (full speed) connection dual-role with internal PHY | 159 |
| Figure 89. | OTG HS (high speed) device connection, host and dual-role in high-speed mode with external PHY. | 160 |
| Figure 90. | Complete audio player solution 1 | 161 |
| Figure 91. | Complete audio player solution 2 | 161 |
| Figure 92. | Audio player solution using PLL, PLLI2S, USB and 1 crystal. | 162 |
| Figure 93. | Audio PLL (PLLI2S) providing accurate I2S clock | 162 |
| Figure 94. | Master clock (MCK) used to drive the external audio DAC. | 163 |
| Figure 95. | Master clock (MCK) not used to drive the external audio DAC. | 163 |
| Figure 96. | MII mode using a 25 MHz crystal | 164 |
| Figure 97. | RMII with a 50 MHz oscillator | 164 |
| Figure 98. | RMII with a 25 MHz crystal and PHY with PLL. | 165 |

1 Introduction

This datasheet provides the description of the STM32F205xx and STM32F207xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F205xx and STM32F207xx datasheet should be read in conjunction with the STM32F20x/STM32F21x reference manual. They will be referred to as STM32F20x devices throughout the document.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F20x/STM32F21x Flash programming manual (PM0059).

The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/>.

2 Description

The STM32F20x family is based on the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a frequency of up to 120 MHz. The family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 128 Kbytes of system SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

The devices also feature an adaptive real-time memory accelerator (ART Accelerator™) which allows to achieve a performance equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz. This performance has been validated using the CoreMark benchmark.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true number random generator (RNG). They also feature standard and advanced communication interfaces. New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), and a camera interface for CMOS sensors. The devices also feature standard peripherals.

- Up to three I²Cs
- Three SPIs, two I²Ss. To achieve audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external PLL to allow synchronization.
- 4 USARTs and 2 UARTs
- A USB OTG high-speed with full-speed capability (with the ULPI)
- A second USB OTG (full-speed)
- Two CANs
- An SDIO interface
- Ethernet and camera interface available on STM32F207xx devices only.

Note: The STM32F205xx and STM32F207xx devices operate in the -40 to $+105$ °C temperature range from a 1.8 V to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range and IRROFF is connected to V_{DD}.

A comprehensive set of power-saving modes allow the design of low-power applications.

STM32F205xx and STM32F207xx devices are offered in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen. These features make the STM32F205xx and STM32F207xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 4 shows the general block diagram of the device family.

**Table 2. STM32F205xx features and peripheral counts**

| Peripherals | | STM32F205Rx | | | | | STM32F205Vx | | | | | STM32F205Zx | | | |
|-------------------------|----------------------|-------------------------------|------------|--------------|-----|------|--------------------|------------|--------------|-----|------|-------------|--------------|-----|------|
| Flash memory in Kbytes | | 128 | 256 | 512 | 768 | 1024 | 128 | 256 | 512 | 768 | 1024 | 256 | 512 | 768 | 1024 |
| SRAM in Kbytes | System (SRAM1+SRAM2) | 64 (48+16) | 96 (80+16) | 128 (112+16) | | | 64 (48+16) | 96 (80+16) | 128 (112+16) | | | 96 (80+16) | 128 (112+16) | | |
| | Backup | 4 | | | | | 4 | | | | | 4 | | | |
| FSMC memory controller | | No | | | | | Yes ⁽¹⁾ | | | | | | | | |
| Ethernet | | No | | | | | | | | | | | | | |
| Timers | General-purpose | 10 | | | | | | | | | | | | | |
| | Advanced-control | 2 | | | | | | | | | | | | | |
| | Basic | 2 | | | | | | | | | | | | | |
| | IWDG | Yes | | | | | | | | | | | | | |
| | WWDG | Yes | | | | | | | | | | | | | |
| RTC | | Yes | | | | | | | | | | | | | |
| Random number generator | | Yes | | | | | | | | | | | | | |
| Comm. interfaces | SPI/I ² S | 3 (2) ⁽²⁾ | | | | | | | | | | | | | |
| | I ² C | 3 | | | | | | | | | | | | | |
| | USART | 4 | | | | | | | | | | | | | |
| | UART | 2 | | | | | | | | | | | | | |
| | USB OTG FS | Yes | | | | | | | | | | | | | |
| | USB OTG HS | Yes | | | | | | | | | | | | | |
| CAN | | 2 | | | | | | | | | | | | | |
| Camera interface | | No | | | | | | | | | | | | | |
| GPIOs | | 51 | | | | | 82 | | | | | 114 | | | |
| SDIO | | Yes | | | | | | | | | | | | | |
| 12-bit ADC | | 3 | | | | | | | | | | | | | |
| Number of channels | | 16 | | | | | 16 | | | | | 24 | | | |
| 12-bit DAC | | Yes | | | | | | | | | | | | | |
| Number of channels | | 2 | | | | | | | | | | | | | |
| Maximum CPU frequency | | 120 MHz | | | | | | | | | | | | | |
| Operating voltage | | 1.8 V to 3.6 V ⁽³⁾ | | | | | | | | | | | | | |



Table 2. STM32F205xx features and peripheral counts (continued)

| Peripherals | STM32F205Rx | | | | STM32F205Vx | STM32F205Zx |
|------------------------|--|-------------------------|-------------|--------------------------|-------------|-------------|
| Operating temperatures | Ambient temperatures: -40 to +85 °C / -40 to +105 °C | | | | | |
| | Junction temperature: -40 to + 125 °C | | | | | |
| Package | LQFP64 | LQFP64 WLCSP64 +2 | LQFP64 4 | LQFP64 WLCSP64 4+2 | LQFP100 | LQFP144 |

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD} minimum value is 1.7 V when the device operates in the 0 to 70 °C temperature range and IRROFF is set to V_{DD} .

Table 3. STM32F207xx features and peripheral counts

| Peripherals | | STM32F207Vx | | | | STM32F207Zx | | | | STM32F207Ix | | | |
|-------------------------|-------------------------|--------------------|-----|-----|------|-------------|-----|-----|------|-------------|-----|-----|------|
| Flash memory in Kbytes | | 256 | 512 | 768 | 1024 | 256 | 512 | 768 | 1024 | 256 | 512 | 768 | 1024 |
| SRAM in Kbytes | System (SRAM1+SRAM2) | 128 (112+16) | | | | | | | | | | | |
| | Backup | 4 | | | | | | | | | | | |
| FSMC memory controller | | Yes ⁽¹⁾ | | | | | | | | | | | |
| Ethernet | | Yes | | | | | | | | | | | |
| Timers | General-purpose | 10 | | | | | | | | | | | |
| | Advanced-control | 2 | | | | | | | | | | | |
| | Basic | 2 | | | | | | | | | | | |
| | IWDG | Yes | | | | | | | | | | | |
| | WWDG | Yes | | | | | | | | | | | |
| RTC | | Yes | | | | | | | | | | | |
| Random number generator | | Yes | | | | | | | | | | | |

Table 3. STM32F207xx features and peripheral counts (continued)

| Peripherals | | STM32F207Vx | STM32F207Zx | STM32F207Ix |
|----------------------------------|----------------------|--|-------------|----------------------|
| Comm. interfaces | SPI/I ² S | 3 (2) ⁽²⁾ | | |
| | I ² C | 3 | | |
| | USART UART | 4 2 | | |
| | USB OTG FS | Yes | | |
| | USB OTG HS | Yes | | |
| | CAN | 2 | | |
| Camera interface | | Yes | | |
| GPIOs | | 82 | 114 | 140 |
| SDIO | | Yes | | |
| 12-bit ADC Number of channels | | 3 | | |
| | | 16 | 24 | 24 |
| 12-bit DAC Number of channels | | Yes 2 | | |
| Maximum CPU frequency | | 120 MHz | | |
| Operating voltage | | 1.8 V to 3.6 V ⁽³⁾ | | |
| Operating temperatures | | Ambient temperatures: -40 to +85 °C/-40 to +105 °C | | |
| | | Junction temperature: -40 to + 125 °C | | |
| Package | | LQFP100 | LQFP144 | LQFP176/ UFBGA176 |

1. For the LQFP100 package, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD} minimum value is 1.7 V when the device operates in the 0 to 70 °C temperature range and IRROFF is set to V_{DD} .

2.1 Full compatibility throughout the family

The STM32F205xx and STM32F207xx constitute the STM32F20x family whose members are fully pin-to-pin, software and feature compatible, allowing the user to try different memory densities and peripherals for a greater degree of freedom during the development cycle.

The STM32F205xx and STM32F207xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F205xx and STM32F207xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F20x family remains simple as only a few pins are impacted.

Figure 3 and *Figure 1* provide compatible board designs between the STM32F20x and the STM32F10xxx family.

Figure 1. Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package

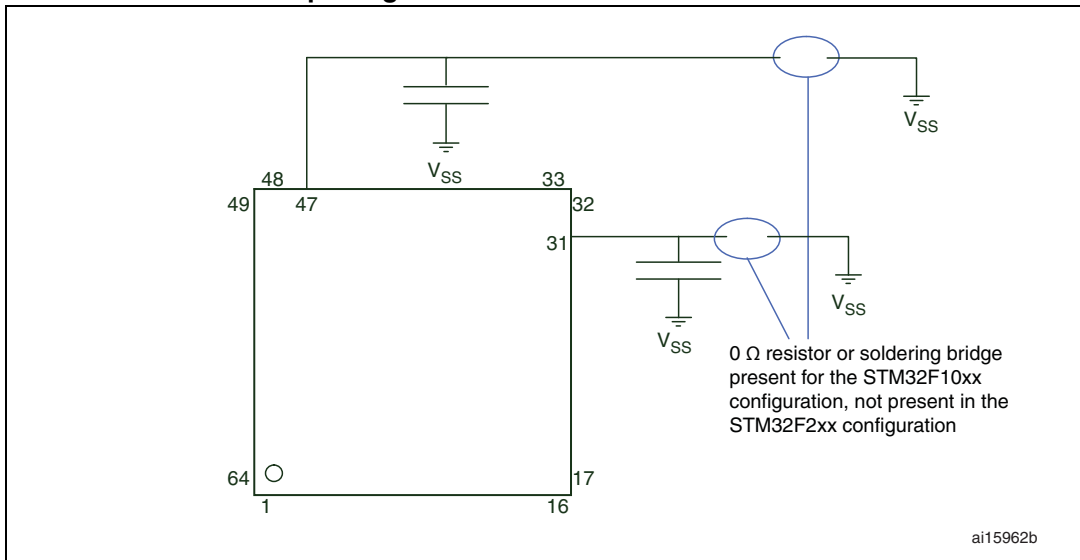


Figure 2. Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package

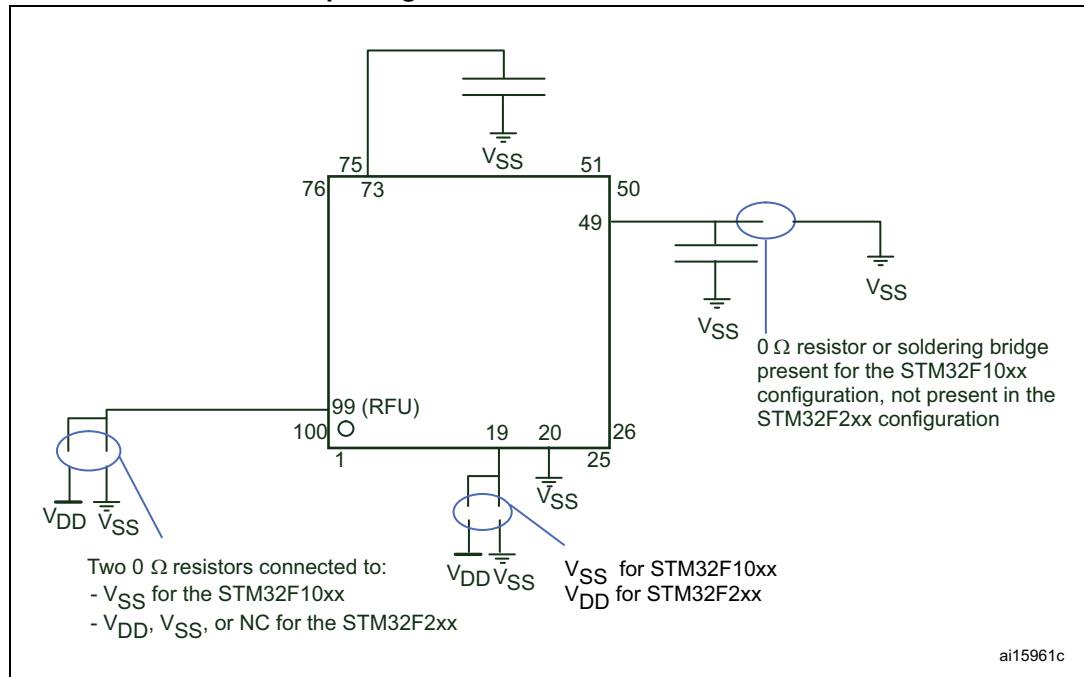
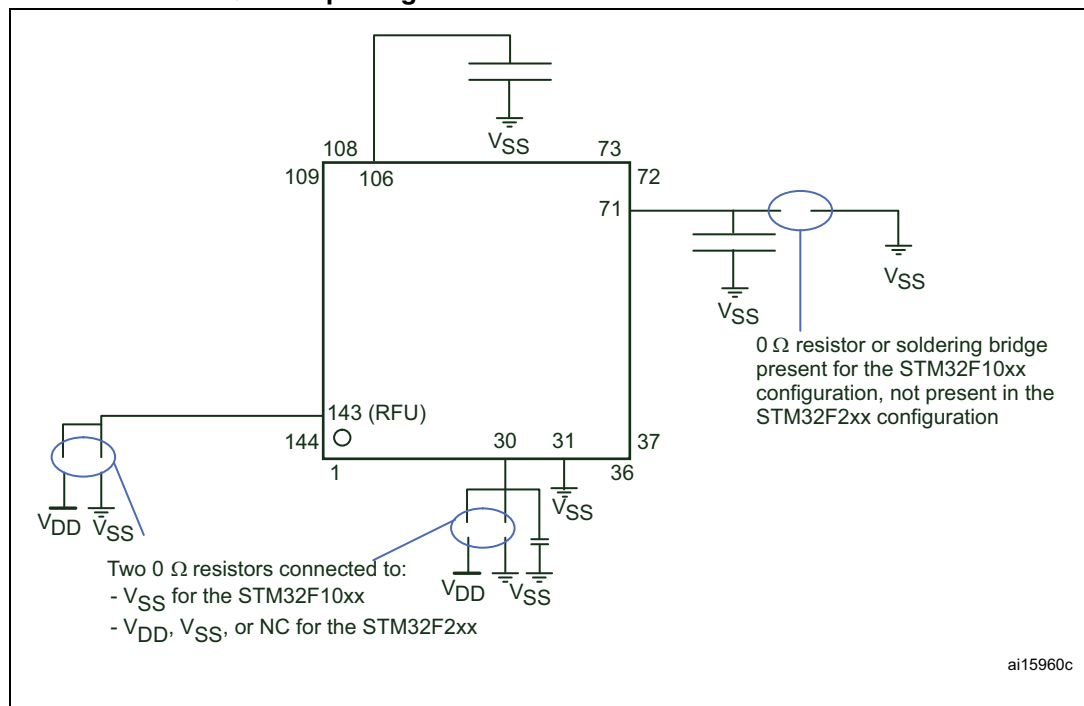


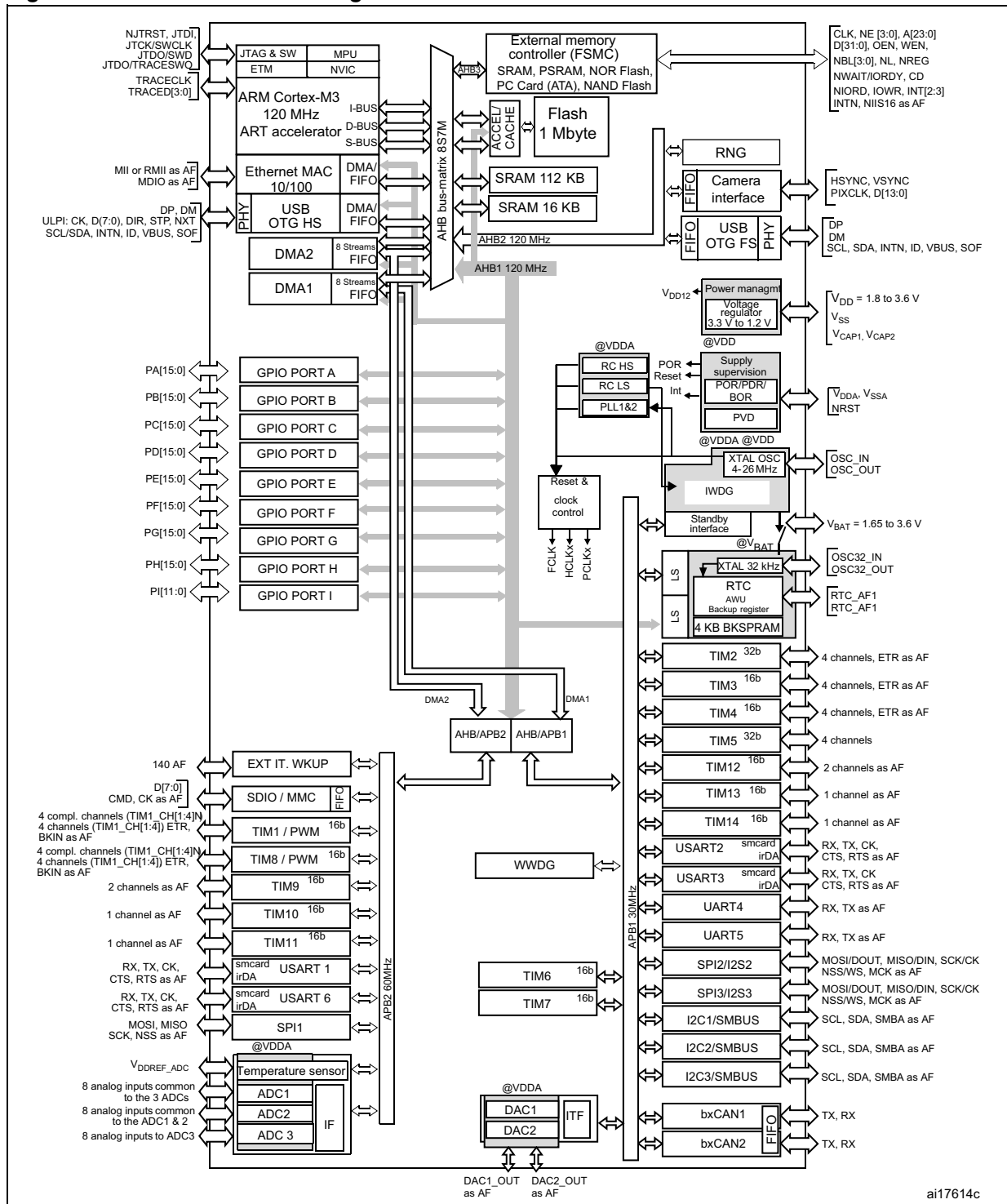
Figure 3. Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package



1. RFU = reserved for future use.

2.2 Device overview

Figure 4. STM32F20x block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 120 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 60 MHz.
2. The camera interface and Ethernet are available only in STM32F207xx devices.

2.2.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex-M3 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, the STM32F20x family is compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F20x family.

2.2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex™-M3 processors. It balances the inherent performance advantage of the ARM Cortex-M3 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher operating frequencies.

To release the processor full 150 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 120 MHz.

2.2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.4 Embedded Flash memory

The STM32F20x devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbytes available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 Embedded SRAM

All STM32F20x products embed:

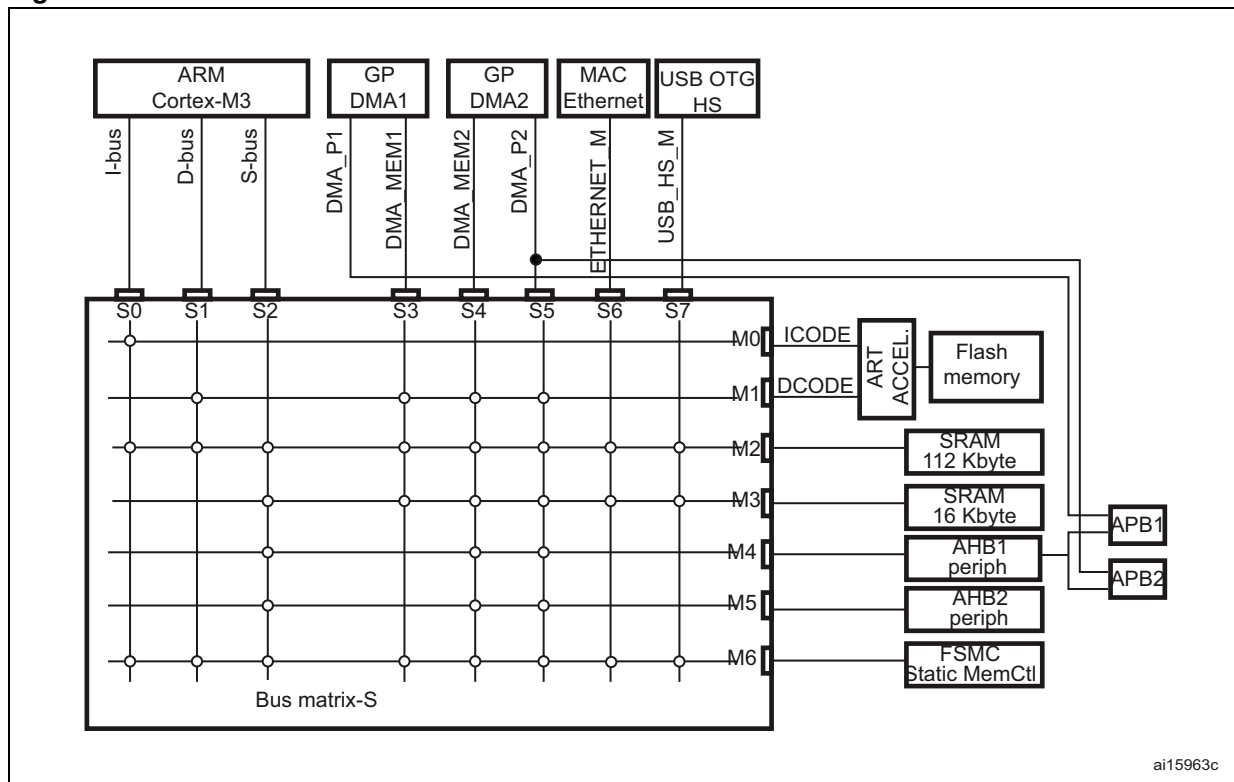
- Up to 128 Kbytes of system SRAM accessed (read/write) at CPU clock speed with 0 wait states
- 4 Kbytes of backup SRAM.

The content of this area is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

2.2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix



ai15963c

2.2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They share some centralized FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART and UART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC.

2.2.9 Flexible static memory controller (FSMC)

The FSMC is embedded in all STM32F20x devices. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- Maximum frequency (f_{HCLK}) for external access is 60 MHz

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.2.10 Nested vectored interrupt controller (NVIC)

The STM32F20x devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex™-M3.

The NVIC main features are the following:

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.2.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

2.2.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In particular, the ethernet and USB OTG FS peripherals can be clocked by the system clock.

Several prescalers and PLLs allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 120 MHz and the maximum frequency the high-speed APB domains is 60 MHz. The maximum allowed frequency of the low-speed APB domain is 30 MHz.

The devices embed a dedicate PLL (PLLI2S) which allow to achieve audio class performance. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.2.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

2.2.14 Power supply schemes

- $V_{DD} = 1.8$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins. On WLCSP package, V_{DD} ranges from 1.7 to 3.6 V.
- V_{SSA} , $V_{DDA} = 1.8$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock, 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to [Figure 17: Power supply scheme](#) for more details.

2.2.15 Power supply supervisor

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit. On devices in WLCSP package, BOR can be inactivated by setting IRROFF to V_{DD} (see [Section 2.2.16: Voltage regulator](#)).

The devices also feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.16 Voltage regulator

The regulator has five operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low power regulator (LPR)
 - Power-down
- Regulator OFF
 - Regulator OFF/internal reset ON
 - Regulator OFF/internal reset OFF

Regulator ON

The regulator ON modes are activated by default on LQFP packages. On WLCSP66 package, they are activated by connecting both REGOFF and IRROFF pins to V_{SS} , while only REGOFF must be connected to V_{SS} on UFBGA176 package (IRROFF is not available).

V_{DD} minimum value is 1.8 V^(a).

There are three regulator ON modes:

- MR is used in nominal regulation mode (Run)
- LPR is used in Stop mode
- Power-down is used in Standby mode:

The regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

Regulator OFF

- Regulator OFF/internal reset ON

On WLCSP66 package, this mode is activated by connecting REGOFF pin to V_{DD} and IRROFF pin to V_{SS} . On UFBGA176 package, only REGOFF must be connected to V_{DD} (IRROFF not available).

The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD} .

The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V^(a), then PA0 should be connected to the NRST pin (see [Figure 6](#)). Otherwise, PA0 should be asserted low externally during POR until V_{DD} reaches 1.8 V (see [Figure 7](#)).

In this mode, PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic which is not reset by the NRST pin, when the internal voltage regulator is OFF.

- Regulator OFF/internal reset OFF

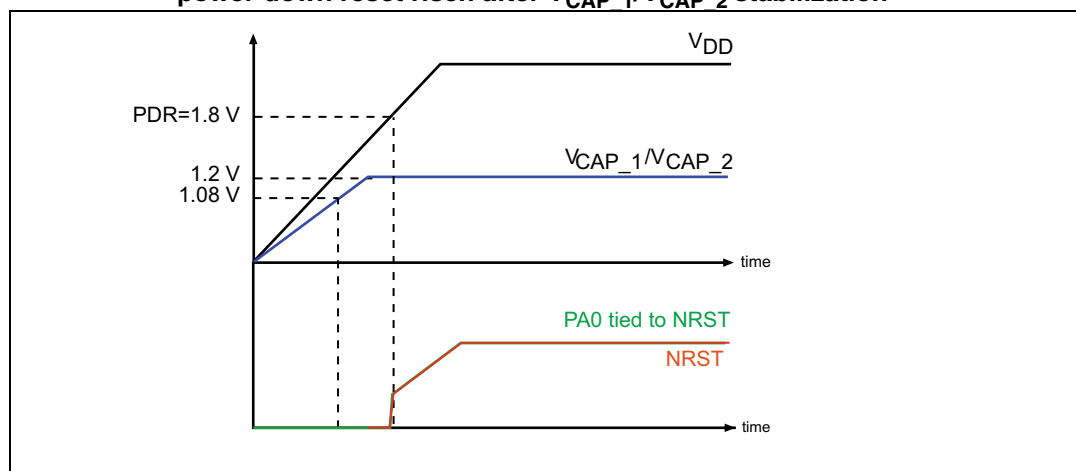
On WLCSP66 package, this mode is activated by connecting REGOFF to V_{SS} and IRROFF to V_{DD} . IRROFF cannot be activated in conjunction with REGOFF. This mode is available only on the WLCSP package. It allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD} .

The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains (see [Figure 6](#)).
- PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V, and until V_{DD} reaches 1.65 V.
- NRST should be controlled by an external reset controller to keep the device under reset when V_{DD} is below 1.65 V (see [Figure 7](#)).

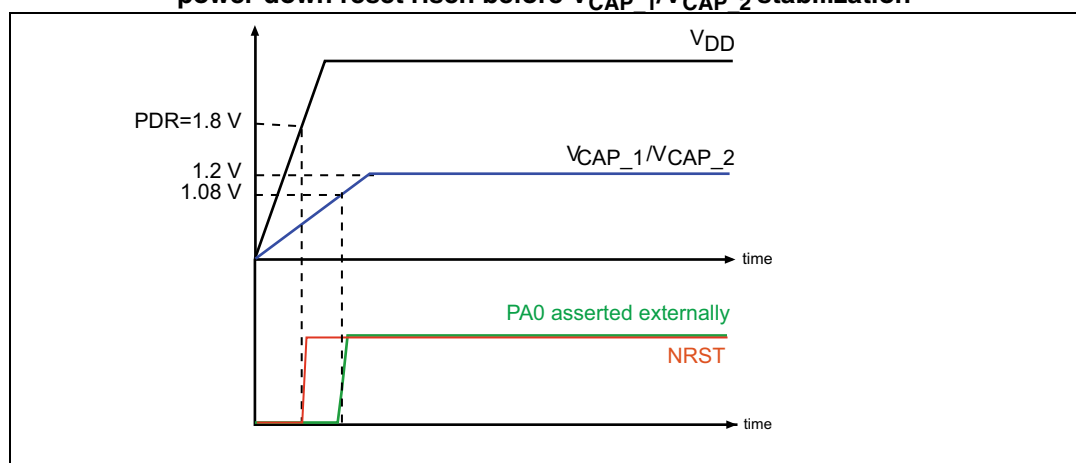
a. V_{DD} minimum value is 1.7 V when the device operates in the 0 to 70 °C temperature range and IRROFF is set to V_{DD} .

**Figure 6. Startup in regulator OFF: slow V_{DD} slope
- power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization**



1. This figure is valid both whatever the internal reset mode (ON or OFF).

**Figure 7. Startup in regulator OFF: fast V_{DD} slope
- power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization**



2.2.17 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F20x devices includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC

has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 μ s to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The 4-Kbyte backup SRAM is an EEPROM-like area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled to minimize power consumption (see [Section 2.2.18: Low-power modes](#)). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see [Section 2.2.18: Low-power modes](#)).

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or the V_{BAT} pin.

2.2.18 Low-power modes

The STM32F20x family supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped when the device enters the Stop or Standby mode.

2.2.19 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery or an external supercapacitor.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

2.2.20 Timers and watchdogs

The STM32F20x devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

[Table 4](#) compares the features of the advanced-control, general-purpose and basic timers.

Table 4. Timer feature comparison

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary output | Max interface clock | Max timer clock |
|------------------|--------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|----------------------|---------------------|-----------------|
| Advanced-control | TIM1, TIM8 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 60 MHz | 120 MHz |
| General purpose | TIM2, TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 30 MHz | 60 MHz |
| | TIM3, TIM4 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 30 MHz | 60 MHz |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 30 MHz | 60 MHz |
| General purpose | TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 60 MHz | 120 MHz |
| | TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 60 MHz | 120 MHz |
| | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 30 MHz | 60 MHz |
| | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 30 MHz | 60 MHz |

Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The TIM1 and TIM8 counters can be frozen in debug mode. Many of the advanced-control timer features are shared with those of the standard TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F20x devices (see [Table 4](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F20x include 4 full-featured general-purpose timers. TIM2 and TIM5 are 32-bit timers, and TIM3 and TIM4 are 16-bit timers. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

The counters of TIM2, TIM3, TIM4, TIM5 can be frozen in debug mode. Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM10, TIM11 and TIM9**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

- **TIM12, TIM13 and TIM14**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode

output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.21 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.22 Universal synchronous/asynchronous receiver transmitters (UARTs/USARTs)

The STM32F20x devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to

communicate at speeds of up to 7.5 Mbit/s. The other available interfaces communicate at up to 3.75 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 5. USART feature comparison

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|------------|-------------------|-----------------|-----|------------|------|----------------------|---|--|--------------------|
| USART1 | X | X | X | X | X | X | 1.87 | 7.5 | APB2 (max. 60 MHz) |
| USART2 | X | X | X | X | X | X | 1.87 | 3.75 | APB1 (max. 30 MHz) |
| USART3 | X | X | X | X | X | X | 1.87 | 3.75 | APB1 (max. 30 MHz) |
| UART4 | X | - | X | - | X | - | 1.87 | 3.75 | APB1 (max. 30 MHz) |
| UART5 | X | - | X | - | X | - | 3.75 | 3.75 | APB1 (max. 30 MHz) |
| USART6 | X | X | X | X | X | X | 3.75 | 7.5 | APB2 (max. 60 MHz) |

2.2.23 Serial peripheral interface (SPI)

The STM32F20x devices feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 30 Mbits/s, while SPI2 and SPI3 can communicate at up to 15 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

2.2.24 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, in half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx interfaces can be served by the DMA controller.

2.2.25 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.2.26 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F207xx devices.

The STM32F207xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F207xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F207xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F207xx.

The STM32F207xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F20x and STM32F21x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.2.27 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOs with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). The 256 bytes of SRAM which are allocated for each CAN are not shared with any other peripheral.

2.2.28 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support

2.2.29 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F20x devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 1024 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.2.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S application. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

2.2.31 Digital camera interface (DCMI)

The camera interface is not available in STM32F205xx devices.

STM32F207xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain up to 27 Mbyte/s at 27 MHz or 48 Mbyte/s at 48 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw Bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.2.32 True random number generator (RNG)

All STM32F2xxx products embed a true RNG that delivers 32-bit random numbers produced by an integrated analog circuit.

2.2.33 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

To provide fast I/O handling, the GPIOs are on the fast AHB1 bus with a clock up to 120 MHz that leads to a maximum I/O toggling speed of 60 MHz.

2.2.34 ADCs (analog-to-digital converters)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers TIM1, TIM2, TIM3, TIM4, TIM5 and TIM8 can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.2.35 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.2.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

2.2.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.2.38 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F20x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

3 Pinouts and pin description

Figure 8. STM32F20x LQFP64 pinout

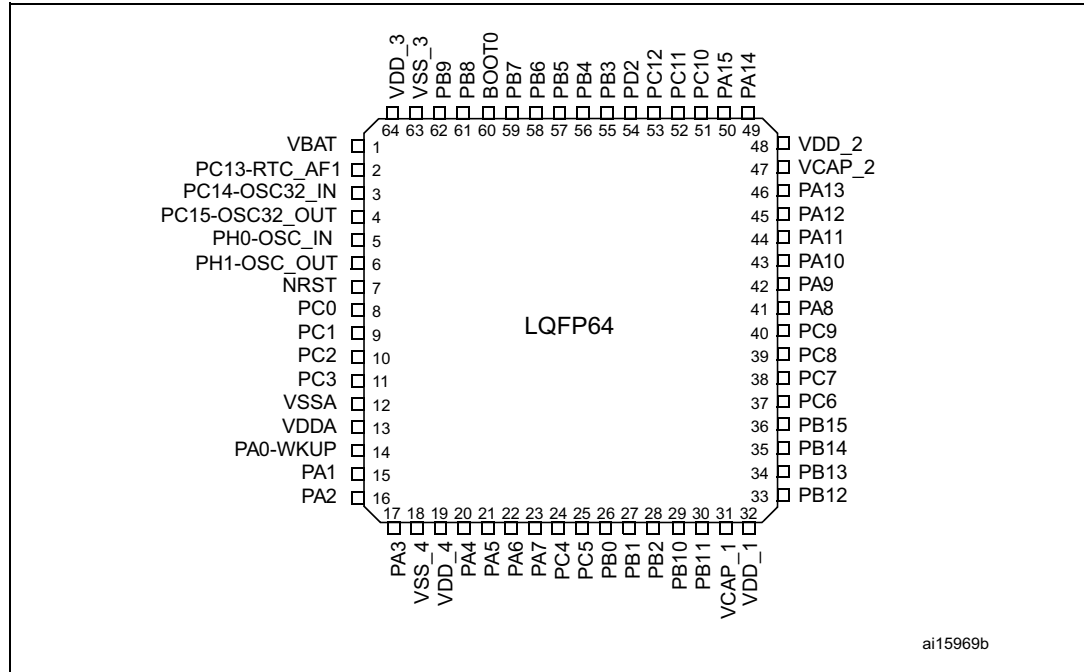


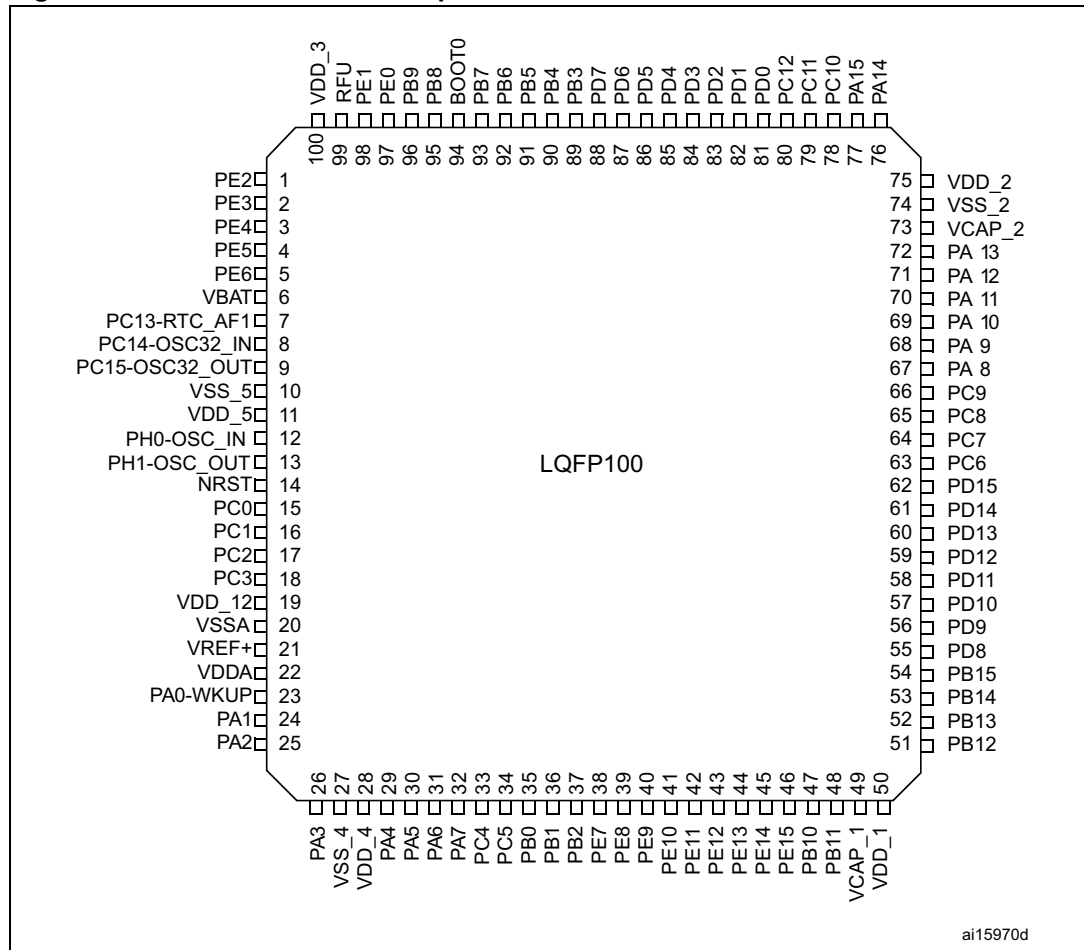
Figure 9. STM32F20x WLCSP64+2 ballout

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|-------|--------|--------|-----|-----|-------|--------|--------|------------------|
| A | PA14 | PA15 | PC12 | PB3 | PB5 | PB7 | PB9 | VDD_2 | V _{BAT} |
| B | VSS_2 | PA13 | PC10 | PB4 | PB6 | BOOT0 | PB8 | PC13 | PC14 |
| C | PA12 | VCAP_2 | PC11 | | | | PD2 | IRROFF | PC15 |
| D | PC9 | PA11 | PA10 | | | | PC2 | VSS_3 | VDD_3 |
| E | VDD_4 | PA8 | PA9 | | | | PA0 | NRST | PH0-OSC_IN |
| F | VSS_4 | PC7 | PC8 | | | | VREF+ | PC1 | PH1-OSC_OUT |
| G | PB15 | PC6 | PC5 | | | | PA3 | PC3 | PC0 |
| H | PB14 | PB13 | PB10 | PC4 | PA6 | PA5 | REGOFF | PA1 | VSS_5 |
| J | PB12 | PB11 | VCAP_1 | PB2 | PB1 | PB0 | PA7 | PA4 | PA2 |

ai18470b

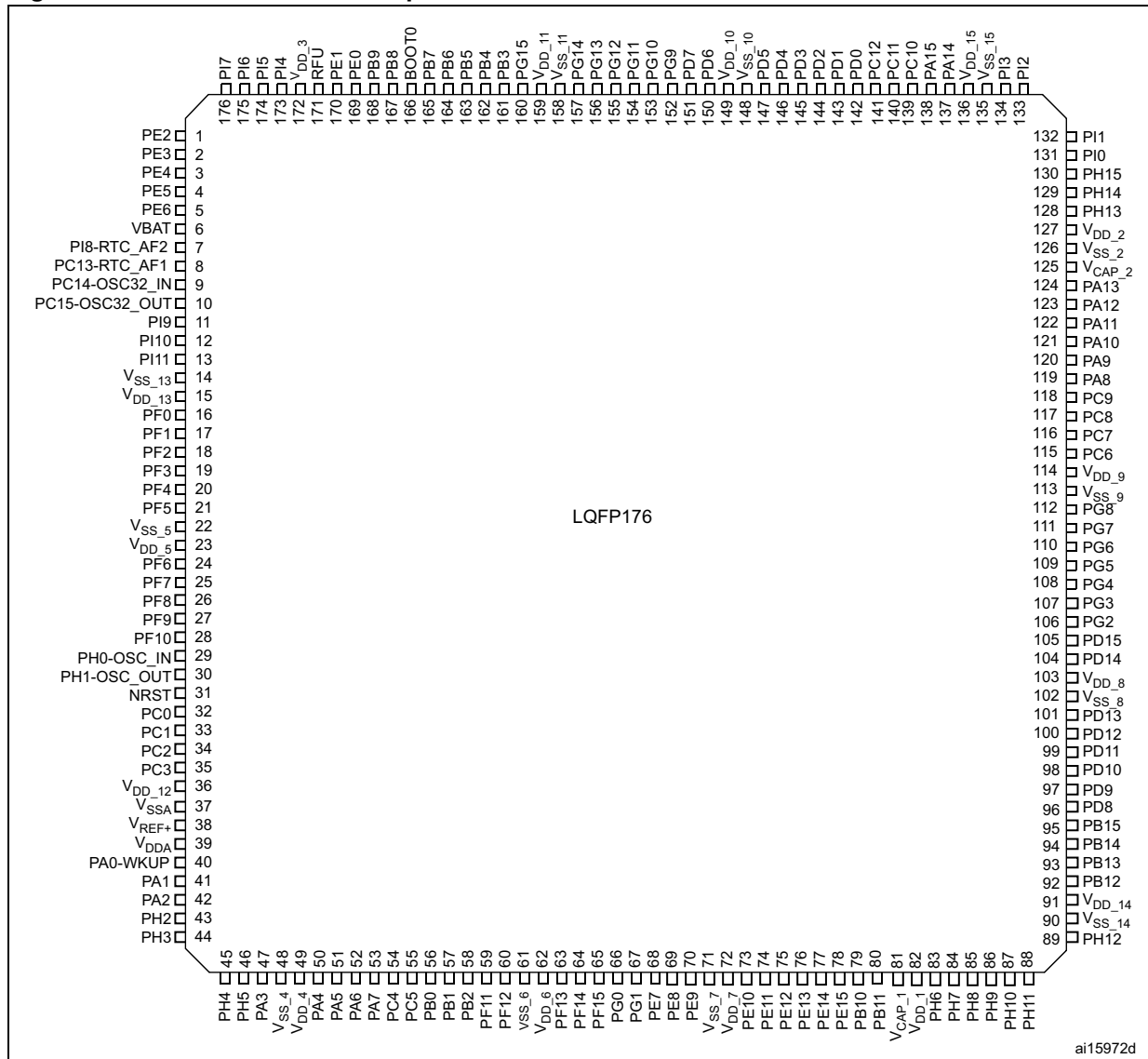
1. Top view.

Figure 10. STM32F20x LQFP100 pinout



1. RFU means "reserved for future use". This pin can be tied to V_{DD} , V_{SS} or left unconnected.

Figure 12. STM32F20x LQFP176 pinout



1. RFU means “reserved for future use”. This pin can be tied to V_{DD}, V_{SS} or left unconnected.

Figure 13. STM32F20x UFBGA176 ballout

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|----------------|-----------|----------|--------|---|-------|--------|--------|--------|-------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|-----|-----|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | PE3 | PE2 | PE1 | PE0 | PB8 | PB5 | PG14 | PG13 | PB4 | PB3 | PD7 | PC12 | PA15 | PA14 | PA13 | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | PE4 | PE5 | PE6 | PB9 | PB7 | PB6 | PG15 | PG12 | PG11 | PG10 | PD6 | PD0 | PC11 | PC10 | PA12 | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | VBAT | PI7 | PI6 | PI5 | VDD_3 | RFU | VDD_11 | VDD_10 | VDD_15 | PG9 | PD5 | PD1 | PI3 | PI2 | PA11 | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | PC13-TAMP1 | PI8-TAMP2 | PI9 | PI4 | VSS | BOOT0 | VSS_11 | VSS_10 | VSS_15 | PD4 | PD3 | PD2 | PH15 | PI1 | PA10 | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | PC14-OSC32_IN | PF0 | PI10 | PI11 | <table border="1" style="margin: auto;"> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> <tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td></tr> </table> | | | | | | | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | PH13 | PH14 | PI0 | PA9 |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSS | VSS | VSS | VSS | VSS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | PC15-OSC32_OUT | VSS_13 | VDD_13 | PH2 | VSS_2 | VCAP2 | PC9 | PA8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | PH0-OSC_IN | VSS_5 | VDD_5 | PH3 | VSS_9 | VDD_2 | PC8 | PC7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | PH1-OSC_OUT | PF2 | PF1 | PH4 | VSS_14 | VDD_9 | PG8 | PC6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | NRST | PF3 | PF4 | PH5 | VDD_14 | VDD_8 | PG7 | PG6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | PF7 | PF6 | PF5 | VDD_4 | PH12 | PG5 | PG4 | PG3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | PF10 | PF9 | PF8 | REGOFF | PH11 | PH10 | PD15 | PG2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | VSSA | PC0 | PC1 | PC2 | PC3 | PB2 | PG1 | VSS_6 | VSS_7 | VCAP1 | PH6 | PH8 | PH9 | PD14 | PD13 | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | VREF- | PA1 | PA0-WKUP | PA4 | PC4 | PF13 | PG0 | VDD_6 | VDD_7 | VDD_1 | PE13 | PH7 | PD12 | PD11 | PD10 | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | VREF+ | PA2 | PA6 | PA5 | PC5 | PF12 | PF15 | PE8 | PE9 | PE11 | PE14 | PB12 | PB13 | PD9 | PD8 | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | VDDA | PA3 | PA7 | PB1 | PB0 | PF11 | PF14 | PE7 | PE10 | PE12 | PE15 | PB10 | PB11 | PB14 | PB15 | | | | | | | | | | | | | | | | | | | | | | | | | |

ai17293b

1. RFU means "reserved for future use". This pin can be tied to V_{DD}, V_{SS} or left unconnected.
2. Top view.

Table 6. STM32F20x pin and ball definitions

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I / O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|------------------|---------------------|----------------------------|---|---|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | 1 | 1 | 1 | A2 | PE2 | I/O | FT | PE2 | TRACECLK/ FSMC_A23 / ETH_MII_TXD3 / EVENTOUT | |
| - | - | 2 | 2 | 2 | A1 | PE3 | I/O | FT | PE3 | TRACED0/FSMC_A19/ EVENTOUT | |
| - | - | 3 | 3 | 3 | B1 | PE4 | I/O | FT | PE4 | TRACED1/FSMC_A20 / DCM1_D4/ EVENTOUT | |
| - | - | 4 | 4 | 4 | B2 | PE5 | I/O | FT | PE5 | TRACED2 / FSMC_A21 / TIM9_CH1 / DCM1_D6/ EVENTOUT | |
| - | - | 5 | 5 | 5 | B3 | PE6 | I/O | FT | PE6 | TRACED3 / FSMC_A22 / TIM9_CH2 / DCM1_D7/ EVENTOUT | |
| 1 | A9 | 6 | 6 | 6 | C1 | V _{BAT} | S | | V _{BAT} | | |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|---|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | - | 7 | D2 | PI8 ⁽⁴⁾ | I/O | FT | PI8 ⁽⁵⁾ | EVENTOUT | RTC_AF2 |
| 2 | B8 | 7 | 7 | 8 | D1 | PC13 ⁽⁴⁾ | I/O | FT | PC13 ⁽⁵⁾ | EVENTOUT | RTC_AF1 |
| 3 | B9 | 8 | 8 | 9 | E1 | PC14 ⁽⁴⁾ -OSC32_IN ⁽⁶⁾ | I/O | FT | PC14 ⁽⁵⁾ | EVENTOUT | OSC32_IN |
| 4 | C9 | 9 | 9 | 10 | F1 | PC15 ⁽⁴⁾ -OSC32_OUT ⁽⁶⁾ | I/O | FT | PC15 ⁽⁵⁾ | EVENTOUT | OSC32_OUT |
| - | - | - | - | 11 | D3 | PI9 | I/O | FT | PI9 | CAN1_RX / EVENTOUT | |
| - | - | - | - | 12 | E3 | PI10 | I/O | FT | PI10 | ETH_MII_RX_ER/ EVENTOUT | |
| - | - | - | - | 13 | E4 | PI11 | I/O | FT | PI11 | OTG_HS_ULPI_DIR/ EVENTOUT | |
| - | - | - | - | 14 | F2 | V _{SS_13} | S | | V _{SS_13} | | |
| - | - | - | - | 15 | F3 | V _{DD_13} | S | | V _{DD_13} | | |
| - | - | - | 10 | 16 | E2 | PF0 | I/O | FT | PF0 | FSMC_A0 / I2C2_SDA/ EVENTOUT | |
| - | - | - | 11 | 17 | H3 | PF1 | I/O | FT | PF1 | FSMC_A1 / I2C2_SCL/ EVENTOUT | |
| - | - | - | 12 | 18 | H2 | PF2 | I/O | FT | PF2 | FSMC_A2 / I2C2_SMBA/ EVENTOUT | |
| - | - | - | 13 | 19 | J2 | PF3 ⁽⁶⁾ | I/O | FT | PF3 | FSMC_A3/ EVENTOUT | ADC3_IN9 |
| - | - | - | 14 | 20 | J3 | PF4 ⁽⁶⁾ | I/O | FT | PF4 | FSMC_A4/ EVENTOUT | ADC3_IN14 |
| - | - | - | 15 | 21 | K3 | PF5 ⁽⁶⁾ | I/O | FT | PF5 | FSMC_A5/ EVENTOUT | ADC3_IN15 |
| - | H9 | 10 | 16 | 22 | G2 | V _{SS_5} | S | | V _{SS_5} | | |
| - | - | 11 | 17 | 23 | G3 | V _{DD_5} | S | | V _{DD_5} | | |
| - | - | - | 18 | 24 | K2 | PF6 ⁽⁶⁾ | I/O | FT | PF6 | TIM10_CH1 / FSMC_NIORD/ EVENTOUT | ADC3_IN4 |
| - | - | - | 19 | 25 | K1 | PF7 ⁽⁶⁾ | I/O | FT | PF7 | TIM11_CH1/FSMC_NREG/ EVENTOUT | ADC3_IN5 |
| - | - | - | 20 | 26 | L3 | PF8 ⁽⁶⁾ | I/O | FT | PF8 | TIM13_CH1 / FSMC_NIOWR/ EVENTOUT | ADC3_IN6 |
| - | - | - | 21 | 27 | L2 | PF9 ⁽⁶⁾ | I/O | FT | PF9 | TIM14_CH1 / FSMC_CD/ EVENTOUT | ADC3_IN7 |
| - | - | - | 22 | 28 | L1 | PF10 ⁽⁶⁾ | I/O | FT | PF10 | FSMC_INTR/ EVENTOUT | ADC3_IN8 |
| 5 | E9 | 12 | 23 | 29 | G1 | PH0 ⁽⁶⁾ -OSC_IN | I/O | FT | PH0 | EVENTOUT | OSC_IN |
| 6 | F9 | 13 | 24 | 30 | H1 | PH1 ⁽⁶⁾ -OSC_OUT | I/O | FT | PH1 | EVENTOUT | OSC_OUT |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|---|---------------------|--------------------------|---|---|---------------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 7 | E8 | 14 | 25 | 31 | J1 | NRST | I/O | | NRST | | |
| 8 | G9 | 15 | 26 | 32 | M2 | PC0 ⁽⁶⁾ | I/O | FT | PC0 | OTG_HS_ULPI_STP/ EVENTOUT | ADC123_ IN10 |
| 9 | F8 | 16 | 27 | 33 | M3 | PC1 ⁽⁶⁾ | I/O | FT | PC1 | ETH_MDC/ EVENTOUT | ADC123_ IN11 |
| 10 | D7 | 17 | 28 | 34 | M4 | PC2 ⁽⁶⁾ | I/O | FT | PC2 | SPI2_MISO / OTG_HS_ULPI_DIR / ETH_MII_TXD2/ EVENTOUT | ADC123_ IN12 |
| 11 | G8 | 18 | 29 | 35 | M5 | PC3 ⁽⁶⁾ | I/O | FT | PC3 | SPI2_MOSI / I2S2_SD / OTG_HS_ULPI_NXT / ETH_MII_TX_CLK/ EVENTOUT | ADC123_ IN13 |
| - | - | 19 | 30 | 36 | - | V _{DD_12} | S | | V _{DD_12} | | |
| 12 | - | 20 | 31 | 37 | M1 | V _{SSA} | S | | V _{SSA} | | |
| - | - | - | - | - | N1 | V _{REF-} | S | | V _{REF-} | | |
| - | F7 | 21 | 32 | 38 | P1 | V _{REF+} | S | | V _{REF+} | | |
| 13 | - | 22 | 33 | 39 | R1 | V _{DDA} | S | | V _{DDA} | | |
| 14 | E7 | 23 | 34 | 40 | N3 | PA0 ⁽⁷⁾ -WKUP ⁽⁶⁾ | I/O | FT | PA0-WKUP | USART2_CTS/ UART4_TX/ ETH_MII_CRS / TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR/ EVENTOUT | ADC123_IN0/ WKUP |
| 15 | H8 | 24 | 35 | 41 | N2 | PA1 ⁽⁶⁾ | I/O | FT | PA1 | USART2_RTS / UART4_RX/ ETH_RMII_REF_CLK / ETH_MII_RX_CLK / TIM5_CH2 / TIM2_CH2/ EVENTOUT | ADC123_IN1 |
| 16 | J9 | 25 | 36 | 42 | P2 | PA2 ⁽⁶⁾ | I/O | FT | PA2 | USART2_TX/TIM5_CH3 / TIM9_CH1 / TIM2_CH3 / ETH_MDIO/ EVENTOUT | ADC123_IN2 |
| - | - | - | - | 43 | F4 | PH2 | I/O | FT | PH2 | ETH_MII_CRS/ EVENTOUT | |
| - | - | - | - | 44 | G4 | PH3 | I/O | FT | PH3 | ETH_MII_COL/ EVENTOUT | |
| - | - | - | - | 45 | H4 | PH4 | I/O | FT | PH4 | I2C2_SCL / OTG_HS_ULPI_NXT/ EVENTOUT | |
| - | - | - | - | 46 | J4 | PH5 | I/O | FT | PH5 | I2C2_SDA/ EVENTOUT | |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|---|------------------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 17 | G7 | 26 | 37 | 47 | R2 | PA3 ⁽⁶⁾ | I/O | FT | PA3 | USART2_RX/TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / OTG_HS_ULPI_D0 / ETH_MII_COL/ EVENTOUT | ADC123_IN3 |
| 18 | F1 | 27 | 38 | 48 | - | V _{SS_4} | S | | V _{SS_4} | | |
| | H7 | | | | L4 | REGOFF | I/O | | REGOFF | | |
| 19 | E1 | 28 | 39 | 49 | K4 | V _{DD_4} | S | | V _{DD_4} | | |
| 20 | J8 | 29 | 40 | 50 | N4 | PA4 ⁽⁶⁾ | I/O | TT | PA4 | SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/ EVENTOUT | ADC12_IN4 /DAC_OUT1 |
| 21 | H6 | 30 | 41 | 51 | P4 | PA5 ⁽⁶⁾ | I/O | TT | PA5 | SPI1_SCK/ OTG_HS_ULPI_CK / TIM2_CH1_ETR/ TIM8_CHIN/ EVENTOUT | ADC12_IN5 /DAC_OUT2 |
| 22 | H5 | 31 | 42 | 52 | P3 | PA6 ⁽⁶⁾ | I/O | FT | PA6 | SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/ EVENTOUT | ADC12_IN6 |
| 23 | J7 | 32 | 43 | 53 | R3 | PA7 ⁽⁶⁾ | I/O | FT | PA7 | SPI1_MOSI/ TIM8_CH1N / TIM14_CH1 TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / RMII_CRS_DV / EVENTOUT | ADC12_IN7 |
| 24 | H4 | 33 | 44 | 54 | N5 | PC4 ⁽⁶⁾ | I/O | FT | PC4 | ETH_RMII_RX_D0 / ETH_MII_RX_D0/ EVENTOUT | ADC12_IN14 |
| 25 | G3 | 34 | 45 | 55 | P5 | PC5 ⁽⁶⁾ | I/O | FT | PC5 | ETH_RMII_RX_D1 / ETH_MII_RX_D1 / EVENTOUT | ADC12_IN15 |
| 26 | J6 | 35 | 46 | 56 | R5 | PB0 ⁽⁶⁾ | I/O | FT | PB0 | TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N/ EVENTOUT | ADC12_IN8 |
| 27 | J5 | 36 | 47 | 57 | R4 | PB1 ⁽⁶⁾ | I/O | FT | PB1 | TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / TIM1_CH3N/ EVENTOUT | ADC12_IN9 |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|-------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 28 | J4 | 37 | 48 | 58 | M6 | PB2 | I/O | FT | PB2-BOOT1 | EVENTOUT | |
| - | - | - | 49 | 59 | R6 | PF11 | I/O | FT | PF11 | DCMI_12/ EVENTOUT | |
| - | - | - | 50 | 60 | P6 | PF12 | I/O | FT | PF12 | FSMC_A6/ EVENTOUT | |
| - | - | - | 51 | 61 | M8 | V _{SS_6} | S | | V _{SS_6} | | |
| - | - | - | 52 | 62 | N8 | V _{DD_6} | S | | V _{DD_6} | | |
| - | - | - | 53 | 63 | N6 | PF13 | I/O | FT | PF13 | FSMC_A7/ EVENTOUT | |
| - | - | - | 54 | 64 | R7 | PF14 | I/O | FT | PF14 | FSMC_A8/ EVENTOUT | |
| - | - | - | 55 | 65 | P7 | PF15 | I/O | FT | PF15 | FSMC_A9/ EVENTOUT | |
| - | - | - | 56 | 66 | N7 | PG0 | I/O | FT | PG0 | FSMC_A10/ EVENTOUT | |
| - | - | - | 57 | 67 | M7 | PG1 | I/O | FT | PG1 | FSMC_A11/ EVENTOUT | |
| - | - | 38 | 58 | 68 | R8 | PE7 | I/O | FT | PE7 | FSMC_D4/TIM1_ETR/ EVENTOUT | |
| - | - | 39 | 59 | 69 | P8 | PE8 | I/O | FT | PE8 | FSMC_D5/TIM1_CH1N/ EVENTOUT | |
| - | - | 40 | 60 | 70 | P9 | PE9 | I/O | FT | PE9 | FSMC_D6/TIM1_CH1/ EVENTOUT | |
| - | - | - | 61 | 71 | M9 | V _{SS_7} | S | | V _{SS_7} | | |
| - | - | - | 62 | 72 | N9 | V _{DD_7} | S | | V _{DD_7} | | |
| - | - | 41 | 63 | 73 | R9 | PE10 | I/O | FT | PE10 | FSMC_D7/TIM1_CH2N/ EVENTOUT | |
| - | - | 42 | 64 | 74 | P10 | PE11 | I/O | FT | PE11 | FSMC_D8/TIM1_CH2/ EVENTOUT | |
| - | - | 43 | 65 | 75 | R10 | PE12 | I/O | FT | PE12 | FSMC_D9/TIM1_CH3N/ EVENTOUT | |
| - | - | 44 | 66 | 76 | N11 | PE13 | I/O | FT | PE13 | FSMC_D10/TIM1_CH3/ EVENTOUT | |
| - | - | 45 | 67 | 77 | P11 | PE14 | I/O | FT | PE14 | FSMC_D11/TIM1_CH4/ EVENTOUT | |
| - | - | 46 | 68 | 78 | R11 | PE15 | I/O | FT | PE15 | FSMC_D12/TIM1_BKIN/ EVENTOUT | |
| 29 | H3 | 47 | 69 | 79 | R12 | PB10 | I/O | FT | PB10 | SPI2_SCK/ I2S2_SCK/ I2C2_SCL / USART3_TX / OTG_HS_ULPI_D3 / ETH_MII_RX_ER / TIM2_CH3/ EVENTOUT | |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 30 | J2 | 48 | 70 | 80 | R13 | PB11 | I/O | FT | PB11 | I2C2_SDA/USART3_RX/ OTG_HS_ULPI_D4 / ETH_RMII_TX_EN/ ETH_MII_TX_EN / TIM2_CH4/ EVENTOUT | |
| 31 | J3 | 49 | 71 | 81 | M10 | V _{CAP_1} | S | | V _{CAP_1} | | |
| 32 | - | 50 | 72 | 82 | N10 | V _{DD_1} | S | | V _{DD_1} | | |
| - | - | - | - | 83 | M11 | PH6 | I/O | FT | PH6 | I2C2_SMBA / TIM12_CH1 / ETH_MII_RXD2/ EVENTOUT | |
| - | - | - | - | 84 | N12 | PH7 | I/O | FT | PH7 | I2C3_SCL / ETH_MII_RXD3/ EVENTOUT | |
| - | - | - | - | 85 | M12 | PH8 | I/O | FT | PH8 | I2C3_SDA / DCMI_HSYNC/ EVENTOUT | |
| - | - | - | - | 86 | M13 | PH9 | I/O | FT | PH9 | I2C3_SMBA / TIM12_CH2/ DCMI_D0/ EVENTOUT | |
| - | - | - | - | 87 | L13 | PH10 | I/O | FT | PH10 | TIM5_CH1 / DCMI_D1/ EVENTOUT | |
| - | - | - | - | 88 | L12 | PH11 | I/O | FT | PH11 | TIM5_CH2 / DCMI_D2/ EVENTOUT | |
| - | - | - | - | 89 | K12 | PH12 | I/O | FT | PH12 | TIM5_CH3 / DCMI_D3/ EVENTOUT | |
| - | - | - | - | 90 | H12 | V _{SS_14} | S | | V _{SS_14} | | |
| - | - | - | - | 91 | J12 | V _{DD_14} | S | | V _{DD_14} | | |
| 33 | J1 | 51 | 73 | 92 | P12 | PB12 | I/O | FT | PB12 | SPI2_NSS/I2S2_WS/ I2C2_SMBA/ USART3_CK/ TIM1_BKIN / CAN2_RX / OTG_HS_ULPI_D5/ ETH_RMII_TXD0 / ETH_MII_TXD0/ OTG_HS_ID/ EVENTOUT | |
| 34 | H2 | 52 | 74 | 93 | P13 | PB13 | I/O | FT | PB13 | SPI2_SCK / I2S2_SCK / USART3_CTS/ TIM1_CH1N /CAN2_TX / OTG_HS_ULPI_D6 / ETH_RMII_TXD1 / ETH_MII_TXD1/ EVENTOUT | OTG_HS_VBUS |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|-------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 35 | H1 | 53 | 75 | 94 | R14 | PB14 | I/O | FT | PB14 | SPI2_MISO/ TIM1_CH2N / TIM12_CH1 / OTG_HS_DM USART3_RTS/ TIM8_CH2N/ EVENTOUT | |
| 36 | G1 | 54 | 76 | 95 | R15 | PB15 | I/O | FT | PB15 | SPI2_MOSI / I2S2_SD / TIM1_CH3N / TIM8_CH3N / TIM12_CH2 / OTG_HS_DP / RTC_50Hz/ EVENTOUT | |
| - | - | 55 | 77 | 96 | P15 | PD8 | I/O | FT | PD8 | FSMC_D13 / USART3_TX/ EVENTOUT | |
| - | - | 56 | 78 | 97 | P14 | PD9 | I/O | FT | PD9 | FSMC_D14 / USART3_RX/ EVENTOUT | |
| - | - | 57 | 79 | 98 | N15 | PD10 | I/O | FT | PD10 | FSMC_D15 / USART3_CK/ EVENTOUT | |
| - | - | 58 | 80 | 99 | N14 | PD11 | I/O | FT | PD11 | FSMC_A16/USART3_CTS/ EVENTOUT | |
| - | - | 59 | 81 | 100 | N13 | PD12 | I/O | FT | PD12 | FSMC_A17/TIM4_CH1 / USART3_RTS/ EVENTOUT | |
| - | - | 60 | 82 | 101 | M15 | PD13 | I/O | FT | PD13 | FSMC_A18/TIM4_CH2/ EVENTOUT | |
| - | - | - | 83 | 102 | - | V _{SS_8} | S | | V _{SS_8} | | |
| - | - | - | 84 | 103 | J13 | V _{DD_8} | S | | V _{DD_8} | | |
| - | - | 61 | 85 | 104 | M14 | PD14 | I/O | FT | PD14 | FSMC_D0/TIM4_CH3/ EVENTOUT | |
| - | - | 62 | 86 | 105 | L14 | PD15 | I/O | FT | PD15 | FSMC_D1/TIM4_CH4/ EVENTOUT | |
| - | - | - | 87 | 106 | L15 | PG2 | I/O | FT | PG2 | FSMC_A12/ EVENTOUT | |
| - | - | - | 88 | 107 | K15 | PG3 | I/O | FT | PG3 | FSMC_A13/ EVENTOUT | |
| - | - | - | 89 | 108 | K14 | PG4 | I/O | FT | PG4 | FSMC_A14/ EVENTOUT | |
| - | - | - | 90 | 109 | K13 | PG5 | I/O | FT | PG5 | FSMC_A15/ EVENTOUT | |
| - | - | - | 91 | 110 | J15 | PG6 | I/O | FT | PG6 | FSMC_INT2/ EVENTOUT | |
| - | - | - | 92 | 111 | J14 | PG7 | I/O | FT | PG7 | FSMC_INT3/USART6_CK/ EVENTOUT | |
| - | - | - | 93 | 112 | H14 | PG8 | I/O | FT | PG8 | USART6_RTS / ETH_PPS_OUT/ EVENTOUT | |
| - | - | - | 94 | 113 | G12 | V _{SS_9} | S | | V _{SS_9} | | |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | 95 | 114 | H13 | V _{DD_9} | S | | V _{DD_9} | | |
| 37 | G2 | 63 | 96 | 115 | H15 | PC6 | I/O | FT | PC6 | I2S2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1/ EVENTOUT | |
| 38 | F2 | 64 | 97 | 116 | G15 | PC7 | I/O | FT | PC7 | I2S3_MCK / TIM8_CH2/SDIO_D7 / USART6_RX / DCMI_D1/TIM3_CH2/ EVENTOUT | |
| 39 | F3 | 65 | 98 | 117 | G14 | PC8 | I/O | FT | PC8 | TIM8_CH3/SDIO_D0 /TIM3_CH3/ USART6_CK / DCMI_D2/ EVENTOUT | |
| 40 | D1 | 66 | 99 | 118 | F14 | PC9 | I/O | FT | PC9 | I2S2_CKIN/ I2S3_CKIN/ MCO2 / TIM8_CH4/SDIO_D1 / /I2C3_SDA / DCMI_D3 / TIM3_CH4/ EVENTOUT | |
| 41 | E2 | 67 | 100 | 119 | F15 | PA8 | I/O | FT | PA8 | MCO1 / USART1_CK/ TIM1_CH1/ I2C3_SCL/ OTG_FS_SOF/ EVENTOUT | |
| 42 | E3 | 68 | 101 | 120 | E15 | PA9 | I/O | FT | PA9 | USART1_TX/ TIM1_CH2 / I2C3_SMBA / DCMI_D0/ EVENTOUT | OTG_FS_ VBUS |
| 43 | D3 | 69 | 102 | 121 | D15 | PA10 | I/O | FT | PA10 | USART1_RX/ TIM1_CH3/ OTG_FS_ID/DCMI_D1/ EVENTOUT | |
| 44 | D2 | 70 | 103 | 122 | C15 | PA11 | I/O | FT | PA11 | USART1_CTS / CAN1_RX/ TIM1_CH4 / OTG_FS_DM/ EVENTOUT | |
| 45 | C1 | 71 | 104 | 123 | B15 | PA12 | I/O | FT | PA12 | USART1_RTS / CAN1_TX/ TIM1_ETR/ OTG_FS_DP/ EVENTOUT | |
| 46 | B2 | 72 | 105 | 124 | A15 | PA13 | I/O | FT | JTMS- SWDIO | JTMS-SWDIO/ EVENTOUT | |
| 47 | C2 | 73 | 106 | 125 | F13 | V _{CAP_2} | S | | V _{CAP_2} | | |
| - | B1 | 74 | 107 | 126 | F12 | V _{SS_2} | S | | V _{SS_2} | | |
| 48 | A8 | 75 | 108 | 127 | G13 | V _{DD_2} | S | | V _{DD_2} | | |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|---|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | - | 128 | E12 | PH13 | I/O | FT | PH13 | TIM8_CH1N / CAN1_TX/ EVENTOUT | |
| - | - | - | - | 129 | E13 | PH14 | I/O | FT | PH14 | TIM8_CH2N / DCMI_D4/ EVENTOUT | |
| - | - | - | - | 130 | D13 | PH15 | I/O | FT | PH15 | TIM8_CH3N / DCMI_D11/ EVENTOUT | |
| - | - | - | - | 131 | E14 | PI0 | I/O | FT | PI0 | TIM5_CH4 / SPI2_NSS / I2S2_WS / DCMI_D13/ EVENTOUT | |
| - | - | - | - | 132 | D14 | PI1 | I/O | FT | PI1 | SPI2_SCK / I2S2_SCK / DCMI_D8/ EVENTOUT | |
| - | - | - | - | 133 | C14 | PI2 | I/O | FT | PI2 | TIM8_CH4 / SPI2_MISO / DCMI_D9/ EVENTOUT | |
| - | - | - | - | 134 | C13 | PI3 | I/O | FT | PI3 | TIM8_ETR / SPI2_MOSI / I2S2_SD / DCMI_D10/ EVENTOUT | |
| - | - | - | - | 135 | D9 | V _{SS_15} | S | | V _{SS_15} | | |
| - | - | - | - | 136 | C9 | V _{DD_15} | S | | V _{DD_15} | | |
| 49 | A1 | 76 | 109 | 137 | A14 | PA14 | I/O | FT | JTCK- SWCLK | JTCK-SWCLK/ EVENTOUT | |
| 50 | A2 | 77 | 110 | 138 | A13 | PA15 | I/O | FT | JTDI | JTDI/ SPI3_NSS/ I2S3_WS/TIM2_CH1_ETR / SPI1_NSS/ EVENTOUT | |
| 51 | B3 | 78 | 111 | 139 | B14 | PC10 | I/O | FT | PC10 | SPI3_SCK / I2S3_SCK / UART4_TX / SDIO_D2 / DCMI_D8 / USART3_TX/ EVENTOUT | |
| 52 | C3 | 79 | 112 | 140 | B13 | PC11 | I/O | FT | PC11 | UART4_RX/ SPI3_MISO / SDIO_D3 / DCMI_D4/USART3_RX/ EVENTOUT | |
| 53 | A3 | 80 | 113 | 141 | A12 | PC12 | I/O | FT | PC12 | UART5_TX/SDIO_CK / DCMI_D9 / SPI3_MOSI / I2S3_SD / USART3_CK/ EVENTOUT | |
| - | - | 81 | 114 | 142 | B12 | PD0 | I/O | FT | PD0 | FSMC_D2/CAN1_RX/ EVENTOUT | |
| - | - | 82 | 115 | 143 | C12 | PD1 | I/O | FT | PD1 | FSMC_D3 / CAN1_TX/ EVENTOUT | |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|--|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 54 | C7 | 83 | 116 | 144 | D12 | PD2 | I/O | FT | PD2 | TIM3_ETR/UART5_RX SDIO_CMD / DCMI_D11/ EVENTOUT | |
| - | - | 84 | 117 | 145 | D11 | PD3 | I/O | FT | PD3 | FSMC_CLK/USART2_CTS/ EVENTOUT | |
| - | - | 85 | 118 | 146 | D10 | PD4 | I/O | FT | PD4 | FSMC_NOE/USART2_RTS / EVENTOUT | |
| - | - | 86 | 119 | 147 | C11 | PD5 | I/O | FT | PD5 | FSMC_NWE/USART2_TX/ EVENTOUT | |
| - | - | - | 120 | 148 | D8 | V _{SS_10} | S | | V _{SS_10} | | |
| - | - | - | 121 | 149 | C8 | V _{DD_10} | S | | V _{DD_10} | | |
| - | - | 87 | 122 | 150 | B11 | PD6 | I/O | FT | PD6 | FSMC_NWAIT/ USART2_RX/ EVENTOUT | |
| - | - | 88 | 123 | 151 | A11 | PD7 | I/O | FT | PD7 | USART2_CK/FSMC_NE1/ FSMC_NCE2/ EVENTOUT | |
| - | - | - | 124 | 152 | C10 | PG9 | I/O | FT | PG9 | USART6_RX / FSMC_NE2/FSMC_NCE3/ EVENTOUT | |
| - | - | - | 125 | 153 | B10 | PG10 | I/O | FT | PG10 | FSMC_NCE4_1/ FSMC_NE3/ EVENTOUT | |
| - | - | - | 126 | 154 | B9 | PG11 | I/O | FT | PG11 | FSMC_NCE4_2 / ETH_MII_TX_EN / ETH_RMII_TX_EN/ EVENTOUT | |
| - | - | - | 127 | 155 | B8 | PG12 | I/O | FT | PG12 | FSMC_NE4 / USART6_RTS/ EVENTOUT | |
| - | - | - | 128 | 156 | A8 | PG13 | I/O | FT | PG13 | FSMC_A24 / USART6_CTS /ETH_MII_TXD0/ ETH_RMII_TXD0/ EVENTOUT | |
| - | - | - | 129 | 157 | A7 | PG14 | I/O | FT | PG14 | FSMC_A25 / USART6_TX /ETH_MII_TXD1/ ETH_RMII_TXD1/ EVENTOUT | |
| - | - | - | 130 | 158 | D7 | V _{SS_11} | S | | V _{SS_11} | | |
| - | - | - | 131 | 159 | C7 | V _{DD_11} | S | | V _{DD_11} | | |
| - | - | - | 132 | 160 | B7 | PG15 | I/O | FT | PG15 | USART6_CTS / DCMI_D13/ EVENTOUT | |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|--------------------|---------------------|--------------------------|---|---|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| 55 | A4 | 89 | 133 | 161 | A10 | PB3 | I/O | FT | JTDO/ TRACESWO | JTDO/ TRACESWO/ SPI3_SCK / I2S3_SCK / TIM2_CH2 / SPI1_SCK/ EVENTOUT | |
| 56 | B4 | 90 | 134 | 162 | A9 | PB4 | I/O | FT | NJTRST | NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO/ EVENTOUT | |
| 57 | A5 | 91 | 135 | 163 | A6 | PB5 | I/O | FT | PB5 | I2C1_SMBA/ CAN2_RX / OTG_HS_ULPI_D7 / ETH_PPS_OUT/TIM3_CH2 / SPI1_MOSI/ SPI3_MOSI / DCMI_D10 / I2S3_SD/ EVENTOUT | |
| 58 | B5 | 92 | 136 | 164 | B6 | PB6 | I/O | FT | PB6 | I2C1_SCL/ TIM4_CH1 / CAN2_TX / DCMI_D5/USART1_TX/ EVENTOUT | |
| 59 | A6 | 93 | 137 | 165 | B5 | PB7 | I/O | FT | PB7 | I2C1_SDA / FSMC_NL ⁽⁸⁾ / DCMI_VSYNC / USART1_RX/ TIM4_CH2/ EVENTOUT | |
| 60 | B6 | 94 | 138 | 166 | D6 | BOOT0 | I | | BOOT0 | | V _{PP} |
| 61 | B7 | 95 | 139 | 167 | A5 | PB8 | I/O | FT | PB8 | TIM4_CH3/SDIO_D4/ TIM10_CH1 / DCMI_D6 / ETH_MII_TXD3 / I2C1_SCL/ CAN1_RX/ EVENTOUT | |
| 62 | A7 | 96 | 140 | 168 | B4 | PB9 | I/O | FT | PB9 | SPI2_NSS/ I2S2_WS/ TIM4_CH4/ TIM11_CH1/ SDIO_D5 / DCMI_D7 / I2C1_SDA / CAN1_TX/ EVENTOUT | |
| - | - | 97 | 141 | 169 | A4 | PE0 | I/O | FT | PE0 | TIM4_ETR / FSMC_NBL0 / DCMI_D2/ EVENTOUT | |
| - | - | 98 | 142 | 170 | A3 | PE1 | I/O | FT | PE1 | FSMC_NBL1 / DCMI_D3/ EVENTOUT | |
| - | - | - | - | - | D5 | V _{SS} | S | | V _{SS} | | |
| 63 | D8 | - | - | - | - | V _{SS_3} | S | | V _{SS_3} | | |
| - | - | 99 | 143 | 171 | C6 | RFU ⁽⁹⁾ | | | | | |
| 64 | D9 | 100 | 144 | 172 | C5 | V _{DD_3} | S | | V _{DD_3} | | |

Table 6. STM32F20x pin and ball definitions (continued)

| Pins | | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | Other functions |
|--------|-----------|---------|---------|---------|----------|----------|---------------------|--------------------------|---|------------------------------------|-----------------|
| LQFP64 | WLCSP64+2 | LQFP100 | LQFP144 | LQFP176 | UFBGA176 | | | | | | |
| - | - | - | - | 173 | D4 | PI4 | I/O | FT | PI4 | TIM8_BKIN / DCMI_D5/ EVENTOUT | |
| - | - | - | - | 174 | C4 | PI5 | I/O | FT | PI5 | TIM8_CH1 / DCMI_VSYNC/ EVENTOUT | |
| - | - | - | - | 175 | C3 | PI6 | I/O | FT | PI6 | TIM8_CH2 / DCMI_D6/ EVENTOUT | |
| - | - | - | - | 176 | C2 | PI7 | I/O | FT | PI7 | TIM8_CH3 / DCMI_D7/ EVENTOUT | |
| - | C8 | - | - | - | - | IRROFF | I/O | | IRROFF | | |

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant; TT = 3.6 V tolerant.
3. Function availability depends on the chosen device.
4. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F20x and STM32F21x reference manual, available from the STMicroelectronics website: www.st.com.
6. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
7. If the device is delivered in a UFBGA176 package and if the REGOFF pin is set to V_{DD} (Regulator OFF), then PA0 is used as an internal Reset (active low).
8. FSMC_NL pin is also named FSMC_NADV on memory devices.
9. RFU means “reserved for future use”. This pin can be tied to V_{DD}, V_{SS} or left unconnected.

Table 7. FSMC pin definition

| Pins | FSMC | | | | LQFP100 |
|------|------|--------------------|---------------|-------------|---------|
| | CF | NOR/PSRAM/S RAM | NOR/PSRAM Mux | NAND 16 bit | |
| PE2 | | A23 | A23 | | Yes |
| PE3 | | A19 | A19 | | Yes |
| PE4 | | A20 | A20 | | Yes |
| PE5 | | A21 | A21 | | Yes |
| PE6 | | A22 | A22 | | Yes |
| PF0 | A0 | A0 | | | - |
| PF1 | A1 | A1 | | | - |
| PF2 | A2 | A2 | | | - |
| PF3 | A3 | A3 | | | - |

Table 7. FSMC pin definition (continued)

| Pins | FSMC | | | | LQFP100 |
|------|-------|----------------|---------------|-------------|---------|
| | CF | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND 16 bit | |
| PF4 | A4 | A4 | | | - |
| PF5 | A5 | A5 | | | - |
| PF6 | NIORD | | | | - |
| PF7 | NREG | | | | - |
| PF8 | NIOWR | | | | - |
| PF9 | CD | | | | - |
| PF10 | INTR | | | | - |
| PF12 | A6 | A6 | | | - |
| PF13 | A7 | A7 | | | - |
| PF14 | A8 | A8 | | | - |
| PF15 | A9 | A9 | | | - |
| PG0 | A10 | A10 | | | - |
| PG1 | | A11 | | | - |
| PE7 | D4 | D4 | DA4 | D4 | Yes |
| PE8 | D5 | D5 | DA5 | D5 | Yes |
| PE9 | D6 | D6 | DA6 | D6 | Yes |
| PE10 | D7 | D7 | DA7 | D7 | Yes |
| PE11 | D8 | D8 | DA8 | D8 | Yes |
| PE12 | D9 | D9 | DA9 | D9 | Yes |
| PE13 | D10 | D10 | DA10 | D10 | Yes |
| PE14 | D11 | D11 | DA11 | D11 | Yes |
| PE15 | D12 | D12 | DA12 | D12 | Yes |
| PD8 | D13 | D13 | DA13 | D13 | Yes |
| PD9 | D14 | D14 | DA14 | D14 | Yes |
| PD10 | D15 | D15 | DA15 | D15 | Yes |
| PD11 | | A16 | A16 | CLE | Yes |
| PD12 | | A17 | A17 | ALE | Yes |
| PD13 | | A18 | A18 | | Yes |
| PD14 | D0 | D0 | DA0 | D0 | Yes |
| PD15 | D1 | D1 | DA1 | D1 | Yes |
| PG2 | | A12 | | | - |
| PG3 | | A13 | | | - |
| PG4 | | A14 | | | - |

Table 7. FSMC pin definition (continued)

| Pins | FSMC | | | | LQFP100 |
|------|--------|----------------|---------------|-------------|---------|
| | CF | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND 16 bit | |
| PG5 | | A15 | | | - |
| PG6 | | | | INT2 | - |
| PG7 | | | | INT3 | - |
| PD0 | D2 | D2 | DA2 | D2 | Yes |
| PD1 | D3 | D3 | DA3 | D3 | Yes |
| PD3 | | CLK | CLK | | Yes |
| PD4 | NOE | NOE | NOE | NOE | Yes |
| PD5 | NWE | NWE | NWE | NWE | Yes |
| PD6 | NWAIT | NWAIT | NWAIT | NWAIT | Yes |
| PD7 | | NE1 | NE1 | NCE2 | Yes |
| PG9 | | NE2 | NE2 | NCE3 | - |
| PG10 | NCE4_1 | NE3 | NE3 | | - |
| PG11 | NCE4_2 | | | | - |
| PG12 | | NE4 | NE4 | | - |
| PG13 | | A24 | A24 | | - |
| PG14 | | A25 | A25 | | - |
| PB7 | | NADV | NADV | | Yes |
| PE0 | | NBL0 | NBL0 | | Yes |
| PE1 | | NBL1 | NBL1 | | Yes |



Table 8. Alternate function mapping

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|----------|-------------------|----------------------|----------|--------------|----------------|----------------------|----------------------|------------|--------------------|---------------------------|----------------|--|----------------------|------------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_HS | DCMI | | |
| PA0-WKUP | | TIM2_CH1_ETR | TIM5_CH1 | TIM8_ETR | | | | USART2_CTS | UART4_TX | | | ETH_MII_CRD | | | | EVENTOUT |
| PA1 | | TIM2_CH2 | TIM5_CH2 | | | | | USART2_RTS | UART4_RX | | | ETH_MII_RX_CLK ETH_RMII _REF_CLK | | | | EVENTOUT |
| PA2 | | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | | | | USART2_TX | | | | ETH_MDIO | | | | EVENTOUT |
| PA3 | | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | | | | USART2_RX | | | OTG_HS_ULPI_D0 | ETH_MII_COL | | | | EVENTOUT |
| PA4 | | | | | | SPI1_NSS | SPI3_NSS I2S3_WS | USART2_CK | | | | | OTG_HS_SOF | DCMI_HSYNC | | EVENTOUT |
| PA5 | | TIM2_CH1_ETR | | TIM8_CH1N | | SPI1_SCK | | | | | OTG_HS_ULPI_CK | | | | | EVENTOUT |
| PA6 | | TIM1_BKIN | TIM3_CH1 | TIM8_BKIN | | SPI1_MISO | | | | TIM13_CH1 | | | | DCMI_PIXCK | | EVENTOUT |
| PA7 | | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | | SPI1_MOSI | | | | TIM14_CH1 | | ETH_MII_RX_DV ETH_RMII _CRS_DV | | | | EVENTOUT |
| PA8 | MCO1 | TIM1_CH1 | | | I2C3_SCL | | | USART1_CK | | | OTG_FS_SOF | | | | | EVENTOUT |
| PA9 | | TIM1_CH2 | | | I2C3_SMBA | | | USART1_TX | | | | | | DCMI_D0 | | EVENTOUT |
| PA10 | | TIM1_CH3 | | | | | | USART1_RX | | | OTG_FS_ID | | | DCMI_D1 | | EVENTOUT |
| PA11 | | TIM1_CH4 | | | | | | USART1_CTS | | CAN1_RX | OTG_FS_DM | | | | | EVENTOUT |
| PA12 | | TIM1_ETR | | | | | | USART1_RTS | | CAN1_TX | OTG_FS_DP | | | | | EVENTOUT |
| PA13 | JTMS-SWDIO | | | | | | | | | | | | | | | EVENTOUT |
| PA14 | JTCK-SWCLK | | | | | | | | | | | | | | | EVENTOUT |
| PA15 | JTDI | TIM2_CH1 TIM2_ETR | | | | SPI1_NSS | SPI3_NSS I2S3_WS | | | | | | | | | EVENTOUT |
| PB0 | | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | | | | | | | OTG_HS_ULPI_D1 | ETH_MII_RXD2 | | | | EVENTOUT |
| PB1 | | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | | | | | | | OTG_HS_ULPI_D2 | ETH_MII_RXD3 | | | | EVENTOUT |
| PB2 | | | | | | | | | | | | | | | | EVENTOUT |
| PB3 | JTDO/ TRACESWO | TIM2_CH2 | | | | SPI1_SCK | SPI3_SCK I2S3_SCK | | | | | | | | | EVENTOUT |
| PB4 | JTRST | | TIM3_CH1 | | | SPI1_MISO | SPI3_MISO | | | | | | | | | EVENTOUT |
| PB5 | | | TIM3_CH2 | | I2C1_SMBA | SPI1_MOSI | SPI3_MOSI I2S3_SD | | | CAN2_RX | OTG_HS_ULPI_D7 | ETH_PPS_OUT | | DCMI_D10 | | EVENTOUT |
| PB6 | | | TIM4_CH1 | | I2C1_SCL | | | USART1_TX | | CAN2_TX | | | | DCMI_D5 | | EVENTOUT |
| PB7 | | | TIM4_CH2 | | I2C1_SDA | | | USART1_RX | | | | | FSMC_NL | DCMI_VSYNC | | EVENTOUT |
| PB8 | | | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | | | | | CAN1_RX | | ETH_MII_TXD3 | SDIO_D4 | DCMI_D6 | | EVENTOUT |
| PB9 | | | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS I2S2_WS | | | | CAN1_TX | | | SDIO_D5 | DCMI_D7 | | EVENTOUT |
| PB10 | | TIM2_CH3 | | | I2C2_SCL | SPI2_SCK I2S2_SCK | | USART3_TX | | | OTG_HS_ULPI_D3 | ETH_MII_RX_ER | | | | EVENTOUT |
| PB11 | | TIM2_CH4 | | | I2C2_SDA | | | USART3_RX | | | OTG_HS_ULPI_D4 | ETH_MII_TX_EN ETH_RMII_TX_EN | | | | EVENTOUT |
| PB12 | | TIM1_BKIN | | | I2C2_SMBA | SPI2_NSS I2S2_WS | | USART3_CK | | CAN2_RX | OTG_HS_ULPI_D5 | ETH_MII_TXD0 ETH_RMII_TXD0 | OTG_HS_ID | | | EVENTOUT |
| PB13 | | TIM1_CH1N | | | | SPI2_SCK I2S2_SCK | | USART3_CTS | | CAN2_TX | OTG_HS_ULPI_D6 | ETH_MII_TXD1 ETH_RMII_TXD1 | | | | EVENTOUT |


Table 8. Alternate function mapping (continued)

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|----------------|----------|-----------|----------|--------------|----------------|----------------------|----------------------|------------|--------------------|---------------------------|-----------------|-------------------------------|------------------------|----------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_HS | DCMI | | |
| PB14 | | TIM1_CH2N | | TIM8_CH2N | | SPI2_MISO | | USART3_RTS | | TIM12_CH1 | | | OTG_HS_DM | | | EVENTOUT |
| PB15 | RTC_50Hz | TIM1_CH3N | | TIM8_CH3N | | SPI2_MOSI I2S2_SD | | | | TIM12_CH2 | | | OTG_HS_DP | | | EVENTOUT |
| PC0 | | | | | | | | | | | OTG_HS_ULPI_STP | | | | | EVENTOUT |
| PC1 | | | | | | | | | | | | ETH_MDC | | | | EVENTOUT |
| PC2 | | | | | | SPI2_MISO | | | | | OTG_HS_ULPI_DIR | ETH_MII_TXD2 | | | | EVENTOUT |
| PC3 | | | | | | SPI2_MOSI | | | | | OTG_HS_ULPI_NXT | ETH_MII_TX_CLK | | | | EVENTOUT |
| PC4 | | | | | | | | | | | | ETH_MII_RXD0 ETH_RMII_RXD0 | | | | EVENTOUT |
| PC5 | | | | | | | | | | | | ETH_MII_RXD1 ETH_RMII_RXD1 | | | | EVENTOUT |
| PC6 | | | TIM3_CH1 | TIM8_CH1 | | I2S2_MCK | | | USART6_TX | | | | SDIO_D6 | DCMI_D0 | | EVENTOUT |
| PC7 | | | TIM3_CH2 | TIM8_CH2 | | | I2S3_MCK | | USART6_RX | | | | SDIO_D7 | DCMI_D1 | | EVENTOUT |
| PC8 | | | TIM3_CH3 | TIM8_CH3 | | | | | USART6_CK | | | | SDIO_D0 | DCMI_D2 | | EVENTOUT |
| PC9 | MCO2 | | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S2_CKIN | I2S3_CKIN | | | | | | SDIO_D1 | DCMI_D3 | | EVENTOUT |
| PC10 | | | | | | | SPI3_SCK I2S3_SCK | USART3_TX | UART4_TX | | | | SDIO_D2 | DCMI_D8 | | EVENTOUT |
| PC11 | | | | | | | SPI3_MISO | USART3_RX | UART4_RX | | | | SDIO_D3 | DCMI_D4 | | EVENTOUT |
| PC12 | | | | | | | SPI3_MOSI I2S3_SD | USART3_CK | UART5_TX | | | | SDIO_CK | DCMI_D9 | | EVENTOUT |
| PC13 | | | | | | | | | | | | | | | | |
| PC14-OSC32_IN | | | | | | | | | | | | | | | | |
| PC15-OSC32_OUT | | | | | | | | | | | | | | | | |
| PD0 | | | | | | | | | | CAN1_RX | | | FSMC_D2 | | | EVENTOUT |
| PD1 | | | | | | | | | | CAN1_TX | | | FSMC_D3 | | | EVENTOUT |
| PD2 | | | TIM3_ETR | | | | | | UART5_RX | | | | SDIO_CMD | DCMI_D11 | | EVENTOUT |
| PD3 | | | | | | | | USART2_CTS | | | | | FSMC_CLK | | | EVENTOUT |
| PD4 | | | | | | | | USART2_RTS | | | | | FSMC_NOE | | | EVENTOUT |
| PD5 | | | | | | | | USART2_TX | | | | | FSMC_NWE | | | EVENTOUT |
| PD6 | | | | | | | | USART2_RX | | | | | FSMC_NWAIT | | | EVENTOUT |
| PD7 | | | | | | | | USART2_CK | | | | | FSMC_NE1/ FSMC_NCE2 | | | EVENTOUT |
| PD8 | | | | | | | | USART3_TX | | | | | FSMC_D13 | | | EVENTOUT |
| PD9 | | | | | | | | USART3_RX | | | | | FSMC_D14 | | | EVENTOUT |
| PD10 | | | | | | | | USART3_CK | | | | | FSMC_D15 | | | EVENTOUT |
| PD11 | | | | | | | | USART3_CTS | | | | | FSMC_A16 | | | EVENTOUT |
| PD12 | | | TIM4_CH1 | | | | | USART3_RTS | | | | | FSMC_A17 | | | EVENTOUT |
| PD13 | | | TIM4_CH2 | | | | | | | | | | FSMC_A18 | | | EVENTOUT |



Table 8. Alternate function mapping (continued)

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|------|----------|-----------|----------|--------------|----------------|----------------|-----------|------------|--------------------|---------------------------|----------------|--------------|----------------------|----------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_HS | DCMI | | |
| PD14 | | | TIM4_CH3 | | | | | | | | | | FSMC_D0 | | | EVENTOUT |
| PD15 | | | TIM4_CH4 | | | | | | | | | | FSMC_D1 | | | EVENTOUT |
| PE0 | | | TIM4_ETR | | | | | | | | | | FSMC_NBL0 | DCMI_D2 | | EVENTOUT |
| PE1 | | | | | | | | | | | | | FSMC_BLN1 | DCMI_D3 | | EVENTOUT |
| PE2 | TRACECLK | | | | | | | | | | | ETH_MII_TXD3 | FSMC_A23 | | | EVENTOUT |
| PE3 | TRACED0 | | | | | | | | | | | | FSMC_A19 | | | EVENTOUT |
| PE4 | TRACED1 | | | | | | | | | | | | FSMC_A20 | DCMI_D4 | | EVENTOUT |
| PE5 | TRACED2 | | | TIM9_CH1 | | | | | | | | | FSMC_A21 | DCMI_D6 | | EVENTOUT |
| PE6 | TRACED3 | | | TIM9_CH2 | | | | | | | | | FSMC_A22 | DCMI_D7 | | EVENTOUT |
| PE7 | | TIM1_ETR | | | | | | | | | | | FSMC_D4 | | | EVENTOUT |
| PE8 | | TIM1_CH1N | | | | | | | | | | | FSMC_D5 | | | EVENTOUT |
| PE9 | | TIM1_CH1 | | | | | | | | | | | FSMC_D6 | | | EVENTOUT |
| PE10 | | TIM1_CH2N | | | | | | | | | | | FSMC_D7 | | | EVENTOUT |
| PE11 | | TIM1_CH2 | | | | | | | | | | | FSMC_D8 | | | EVENTOUT |
| PE12 | | TIM1_CH3N | | | | | | | | | | | FSMC_D9 | | | EVENTOUT |
| PE13 | | TIM1_CH3 | | | | | | | | | | | FSMC_D10 | | | EVENTOUT |
| PE14 | | TIM1_CH4 | | | | | | | | | | | FSMC_D11 | | | EVENTOUT |
| PE15 | | TIM1_BKIN | | | | | | | | | | | FSMC_D12 | | | EVENTOUT |
| PF0 | | | | | I2C2_SDA | | | | | | | | FSMC_A0 | | | EVENTOUT |
| PF1 | | | | | I2C2_SCL | | | | | | | | FSMC_A1 | | | EVENTOUT |
| PF2 | | | | | I2C2_SMBA | | | | | | | | FSMC_A2 | | | EVENTOUT |
| PF3 | | | | | | | | | | | | | FSMC_A3 | | | EVENTOUT |
| PF4 | | | | | | | | | | | | | FSMC_A4 | | | EVENTOUT |
| PF5 | | | | | | | | | | | | | FSMC_A5 | | | EVENTOUT |
| PF6 | | | | TIM10_CH1 | | | | | | | | | FSMC_NIORD | | | EVENTOUT |
| PF7 | | | | TIM11_CH1 | | | | | | | | | FSMC_NREG | | | EVENTOUT |
| PF8 | | | | | | | | | | TIM13_CH1 | | | FSMC_NIOWR | | | EVENTOUT |
| PF9 | | | | | | | | | | TIM14_CH1 | | | FSMC_CD | | | EVENTOUT |
| PF10 | | | | | | | | | | | | | FSMC_INTR | | | EVENTOUT |
| PF11 | | | | | | | | | | | | | | DCMI_D12 | | EVENTOUT |
| PF12 | | | | | | | | | | | | | FSMC_A6 | | | EVENTOUT |
| PF13 | | | | | | | | | | | | | FSMC_A7 | | | EVENTOUT |
| PF14 | | | | | | | | | | | | | FSMC_A8 | | | EVENTOUT |

Table 8. Alternate function mapping (continued)

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|---------------|-----|--------|----------|--------------|----------------|----------------|-----------|------------|--------------------|---------------------------|-------------------|---------------------------------|--------------------------|------------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_HS | DCMI | | |
| PF15 | | | | | | | | | | | | | FSMC_A9 | | | EVENTOUT |
| PG0 | | | | | | | | | | | | | FSMC_A10 | | | EVENTOUT |
| PG1 | | | | | | | | | | | | | FSMC_A11 | | | EVENTOUT |
| PG2 | | | | | | | | | | | | | FSMC_A12 | | | EVENTOUT |
| PG3 | | | | | | | | | | | | | FSMC_A13 | | | EVENTOUT |
| PG4 | | | | | | | | | | | | | FSMC_A14 | | | EVENTOUT |
| PG5 | | | | | | | | | | | | | FSMC_A15 | | | EVENTOUT |
| PG6 | | | | | | | | | | | | | FSMC_INT2 | | | EVENTOUT |
| PG7 | | | | | | | | | USART6_CK | | | | FSMC_INT3 | | | EVENTOUT |
| PG8 | | | | | | | | | USART6_RTS | | | ETH_PPS_OUT | | | | EVENTOUT |
| PG9 | | | | | | | | | USART6_RX | | | | FSMC_NE2/ FSMC_NCE3 | | | EVENTOUT |
| PG10 | | | | | | | | | | | | | FSMC_NCE4_1/ FSMC_NE3 | | | EVENTOUT |
| PG11 | | | | | | | | | | | | ETH_MII_TX_EN ETH_RMII_TX_EN | FSMC_NCE4_2 | | | EVENTOUT |
| PG12 | | | | | | | | | USART6_RTS | | | | FSMC_NE4 | | | EVENTOUT |
| PG13 | | | | | | | | | UART6_CTS | | | ETH_MII_TXD0 ETH_RMII_TXD0 | FSMC_A24 | | | EVENTOUT |
| PG14 | | | | | | | | | USART6_TX | | | ETH_MII_TXD1 ETH_RMII_TXD1 | FSMC_A25 | | | EVENTOUT |
| PG15 | | | | | | | | | USART6_CTS | | | | | DCMI_D13 | | EVENTOUT |
| PH0 - OSC_IN | | | | | | | | | | | | | | | | |
| PH1 - OSC_OUT | | | | | | | | | | | | | | | | |
| PH2 | | | | | | | | | | | | ETH_MII_CRS | | | | EVENTOUT |
| PH3 | | | | | | | | | | | | ETH_MII_COL | | | | EVENTOUT |
| PH4 | | | | | I2C2_SCL | | | | | | OTG_HS_ULPI_NXT | | | | | EVENTOUT |
| PH5 | | | | | I2C2_SDA | | | | | | | | | | | EVENTOUT |
| PH6 | | | | | I2C2_SMBA | | | | | TIM12_CH1 | | ETH_MII_RXD2 | | | | EVENTOUT |
| PH7 | | | | | I2C3_SCL | | | | | | | ETH_MII_RXD3 | | | | EVENTOUT |
| PH8 | | | | | I2C3_SDA | | | | | | | | | DCMI_HSYNC | | EVENTOUT |
| PH9 | | | | | I2C3_SMBA | | | | | TIM12_CH2 | | | | DCMI_D0 | | EVENTOUT |
| PH10 | | | TIM5_CH1 | | | | | | | | | | | DCMI_D1 | | EVENTOUT |
| PH11 | | | TIM5_CH2 | | | | | | | | | | | DCMI_D2 | | EVENTOUT |
| PH12 | | | TIM5_CH3 | | | | | | | | | | | DCMI_D3 | | EVENTOUT |
| PH13 | | | | TIM8_CH1N | | | | | | CAN1_TX | | | | | | EVENTOUT |



Table 8. Alternate function mapping (continued)

| Port | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF014 | AF15 |
|------|-----|--------|----------|--------------|----------------|----------------------|-----------|------------|--------------------|---------------------------|-----------------|---------------|----------------------|------------|-------|----------|
| | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | USART1/2/3 | UART4/5/ USART6 | CAN1/CAN2/ TIM12/13/14 | OTG_FS/ OTG_HS | ETH | FSMC/SDIO/ OTG_HS | DCMI | | |
| PH14 | | | | TIM8_CH2N | | | | | | | | | | DCMI_D4 | | EVENTOUT |
| PH15 | | | | TIM8_CH3N | | | | | | | | | | DCMI_D11 | | EVENTOUT |
| PI0 | | | TIM5_CH4 | | | SPI2_NSS I2S2_WS | | | | | | | | DCMI_D13 | | EVENTOUT |
| PI1 | | | | | | SPI2_SCK I2S2_SCK | | | | | | | | DCMI_D8 | | EVENTOUT |
| PI2 | | | | TIM8_CH4 | | SPI2_MISO | | | | | | | | DCMI_D9 | | EVENTOUT |
| PI3 | | | | TIM8_ETR | | SPI2_MOSI I2S2_SD | | | | | | | | DCMI_D10 | | EVENTOUT |
| PI4 | | | | TIM8_BKIN | | | | | | | | | | DCMI_D5 | | EVENTOUT |
| PI5 | | | | TIM8_CH1 | | | | | | | | | | DCMI_VSYNC | | EVENTOUT |
| PI6 | | | | TIM8_CH2 | | | | | | | | | | DCMI_D6 | | EVENTOUT |
| PI7 | | | | TIM8_CH3 | | | | | | | | | | DCMI_D7 | | EVENTOUT |
| PI8 | | | | | | | | | | | | | | | | |
| PI9 | | | | | | | | | | CAN1_RX | | | | | | EVENTOUT |
| PI10 | | | | | | | | | | | | ETH_MII_RX_ER | | | | EVENTOUT |
| PI11 | | | | | | | | | | | OTG_HS_ULPI_DIR | | | | | EVENTOUT |

4 Memory mapping

The memory map is shown in [Figure 14](#).

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^\circ\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$ (for the $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 15](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 16](#).

Figure 15. Pin loading conditions

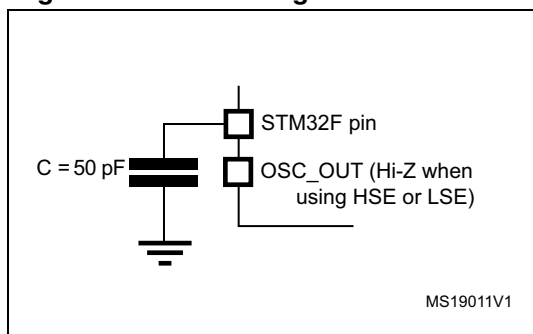
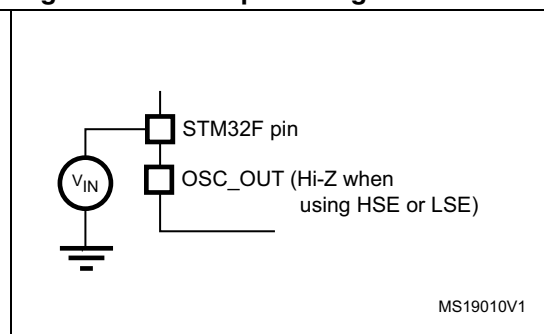
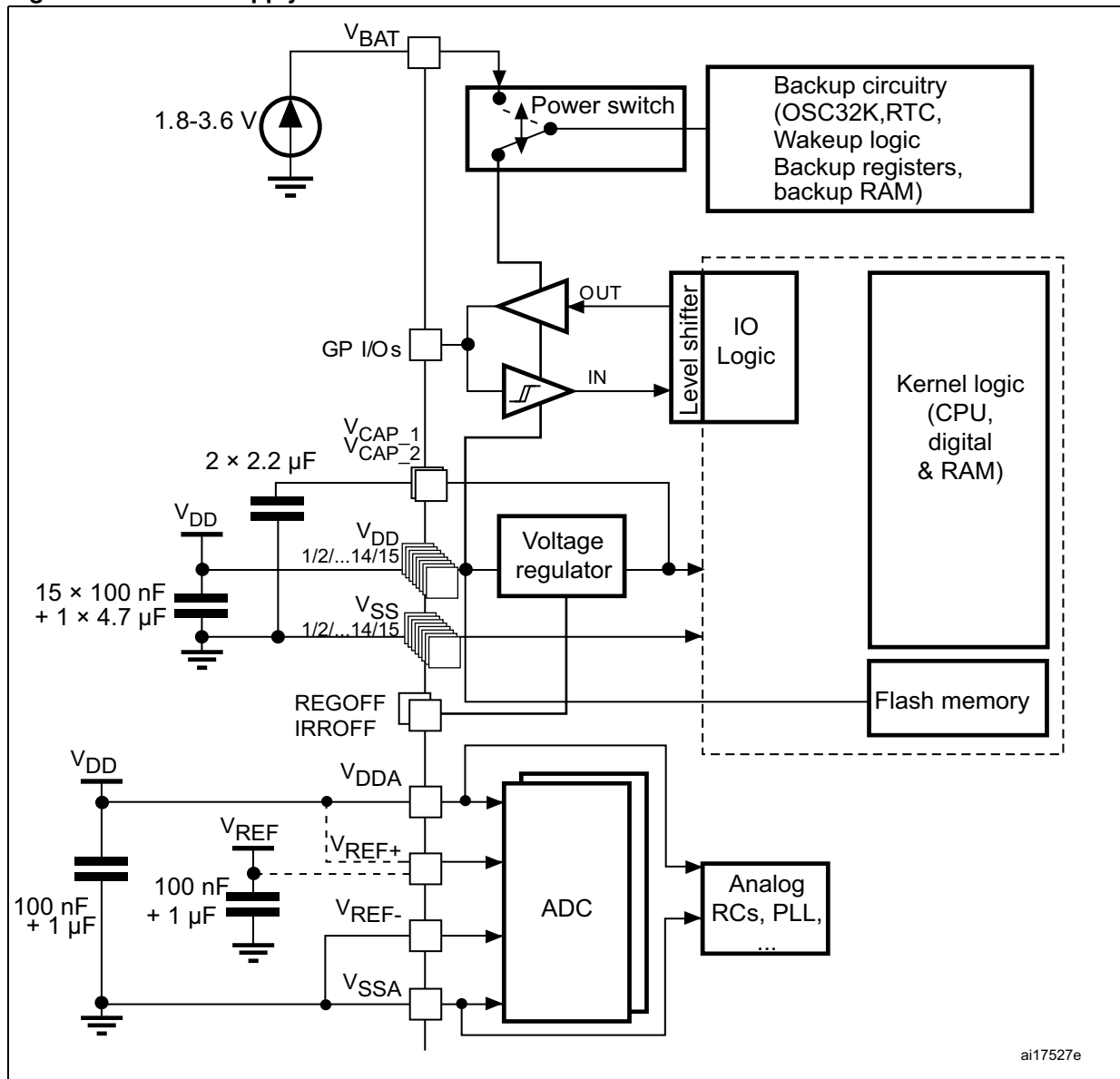


Figure 16. Pin input voltage



5.1.6 Power supply scheme

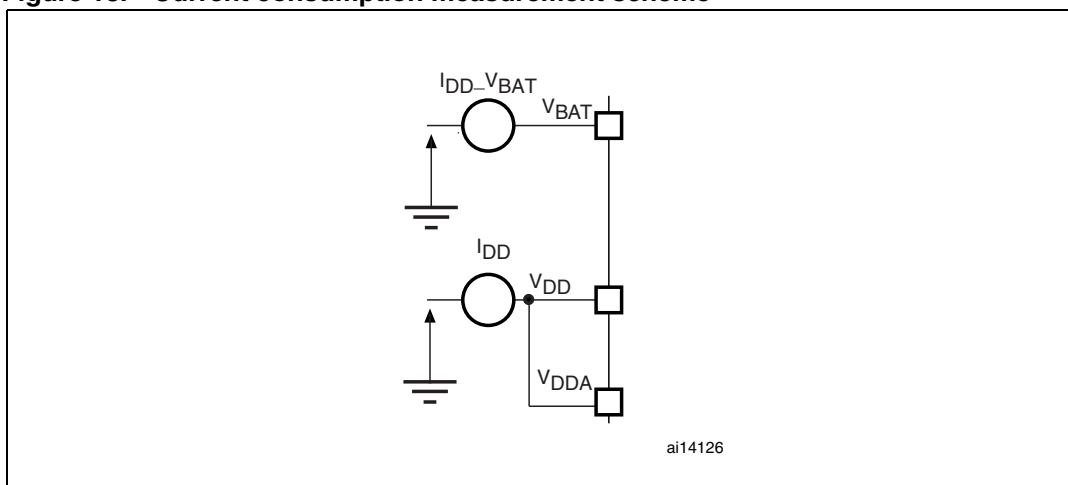
Figure 17. Power supply scheme



1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. To connect REGOFF and IRROFF pins, refer to [Section 2.2.16: Voltage regulator](#).
3. The two 2.2 μF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
4. The 4.7 μF ceramic capacitor must be connected to one of the V_{DD} pin.

5.1.7 Current consumption measurement

Figure 18. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 9: Voltage characteristics](#), [Table 10: Current characteristics](#), and [Table 11: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Voltage characteristics

| Symbol | Ratings | Min | Max | Unit |
|----------------------|---|---|------------|------|
| $V_{DD}-V_{SS}$ | External main supply voltage (including V_{DDA} , V_{DD}) ⁽¹⁾ | -0.3 | 4.0 | V |
| V_{IN} | Input voltage on five-volt tolerant pin ⁽²⁾ | $V_{SS}-0.3$ | $V_{DD}+4$ | |
| | Input voltage on any other pin | $V_{SS}-0.3$ | 4.0 | |
| $ ΔV_{DDx} $ | Variations between different V_{DD} power pins | - | 50 | mV |
| $ V_{SSx} - V_{SS} $ | Variations between all the different ground pins | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see Section 5.3.14: Absolute maximum ratings (electrical sensitivity) | | |

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to [Table 10](#) for the values of the maximum allowed injected current.

Table 10. Current characteristics

| Symbol | Ratings | Max. | Unit |
|--------------------------------------|---|-------|------|
| I_{VDD} | Total current into V_{DD} power lines (source) ⁽¹⁾ | 120 | mA |
| I_{VSS} | Total current out of V_{SS} ground lines (sink) ⁽¹⁾ | 120 | |
| I_{IO} | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | 25 | |
| $I_{INJ(PIN)}$ ⁽²⁾ | Injected current on five-volt tolerant I/O ⁽³⁾ | -5/+0 | |
| | Injected current on any other pin ⁽⁴⁾ | ±5 | |
| $\Sigma I_{INJ(PIN)}$ ⁽⁴⁾ | Total injected current (sum of all I/O and control pins) ⁽⁵⁾ | ±25 | |

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in [Section 5.3.20: 12-bit ADC characteristics](#).
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 9](#) for the values of the maximum allowed input voltage.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 9](#) for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 11. Thermal characteristics

| Symbol | Ratings | Value | Unit |
|-----------|------------------------------|-------------|------|
| T_{STG} | Storage temperature range | -65 to +150 | °C |
| T_J | Maximum junction temperature | 125 | °C |

5.3 Operating conditions

5.3.1 General operating conditions

Table 12. General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------------------|---|---|--------------------|-----|------|
| f_{HCLK} | Internal AHB clock frequency | | 0 | 120 | MHz |
| f_{PCLK1} | Internal APB1 clock frequency | | 0 | 30 | |
| f_{PCLK2} | Internal APB2 clock frequency | | 0 | 60 | |
| V_{DD} | Standard operating voltage | | 1.8 ⁽¹⁾ | 3.6 | V |
| V_{DDA} ⁽²⁾ | Analog operating voltage (ADC limited to 1 M samples) | Must be the same potential as V_{DD} ⁽³⁾ | 1.8 ⁽¹⁾ | 3.6 | V |
| | Analog operating voltage (ADC limited to 2 M samples) | | 2.4 | 3.6 | |
| V_{BAT} | Backup operating voltage | | 1.65 | 3.6 | V |

Table 12. General operating conditions (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|---|--------------------------------------|-----|-----|------|
| V_{CAP1} | Internal core voltage to be supplied externally in REGOFF mode | | 1.1 | 1.3 | V |
| V_{CAP2} | | | | | |
| P_D | Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 ⁽⁴⁾ | LQFP64 | - | 444 | mW |
| | | WLCSP66 | - | 392 | |
| | | LQFP100 | - | 434 | |
| | | LQFP144 | - | 500 | |
| | | LQFP176 | - | 526 | |
| | | UFBGA176 | - | 513 | |
| T_A | Ambient temperature for 6 suffix version | Maximum power dissipation | -40 | 85 | °C |
| | | Low power dissipation ⁽⁵⁾ | -40 | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | -40 | 105 | °C |
| | | Low power dissipation ⁽⁵⁾ | -40 | 125 | |
| T_J | Junction temperature range | 6 suffix version | -40 | 105 | °C |
| | | 7 suffix version | -40 | 125 | |

1. IRROFF is set to V_{DD} , this value can be lowered to 1.7 V when the device operates in the 0 to 70 °C temperature range. a reduced temperature range.
2. When the ADC is used, refer to [Table 64: ADC characteristics](#).
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} .
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} .

Table 13. Limitations depending on the operating power supply range

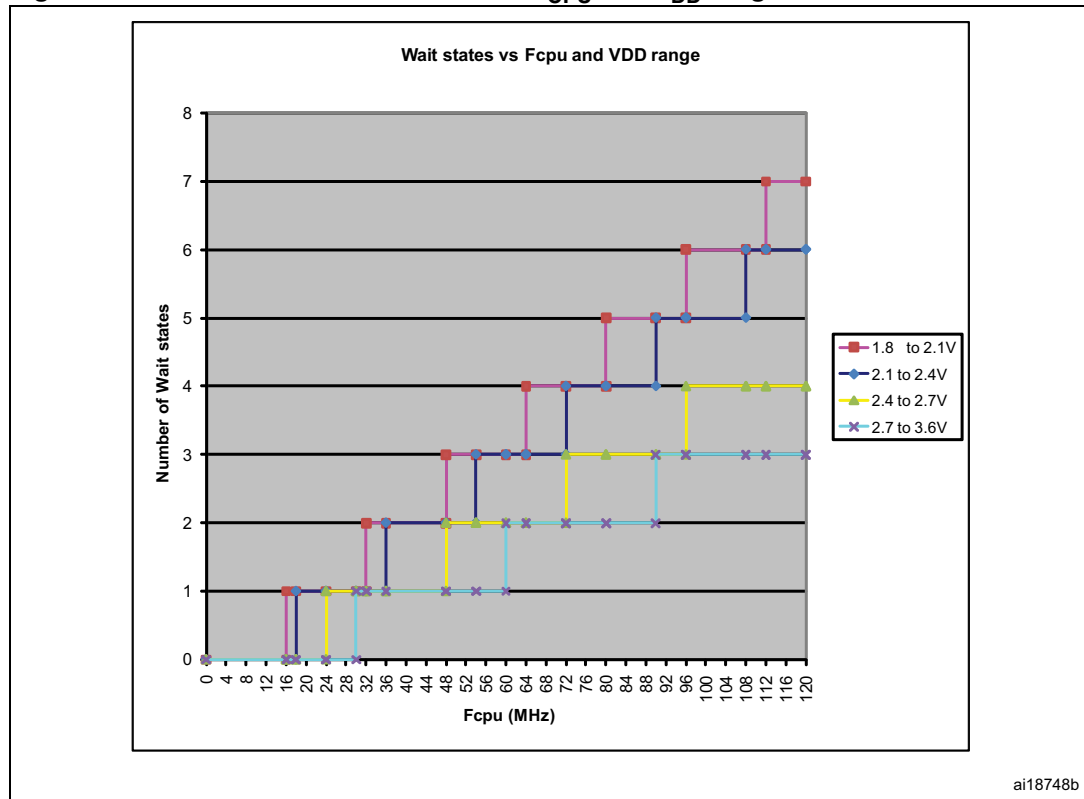
| Operating power supply range | ADC operation | Maximum Flash memory access frequency ($f_{Flashmax}$) | Number of wait states at maximum CPU frequency ($f_{CPUmax} = 120\text{ MHz}$) ⁽¹⁾ | I/O operation | FSMC_CLK frequency for synchronous accesses | Possible Flash memory operations |
|---|------------------------------|--|---|---|---|---|
| $V_{DD} = 1.8$ to 2.1 V ⁽²⁾ | Conversion time up to 1 Msps | 16 MHz with no Flash memory wait state | 7 ⁽³⁾ | - Degraded speed performance - No I/O compensation | up to 30 MHz | 8-bit erase and program operations only |
| $V_{DD} = 2.1$ to 2.4 V | Conversion time up to 1 Msps | 18 MHz with no Flash memory wait state | 6 ⁽³⁾ | - Degraded speed performance - No I/O compensation | up to 30 MHz | 16-bit erase and program operations |

Table 13. Limitations depending on the operating power supply range

| Operating power supply range | ADC operation | Maximum Flash memory access frequency (f _{Flashmax}) | Number of wait states at maximum CPU frequency (f _{CPUMax} =120 MHz) ⁽¹⁾ | I/O operation | FSMC_CLK frequency for synchronous accesses | Possible Flash memory operations |
|---|------------------------------|--|--|--|--|-------------------------------------|
| V _{DD} = 2.4 to 2.7 V | Conversion time up to 2 Msps | 24 MHz with no Flash memory wait state | 4 ⁽³⁾ | <ul style="list-style-type: none"> – Degraded speed performance – I/O compensation works | up to 48 MHz | 16-bit erase and program operations |
| V _{DD} = 2.7 to 3.6 V ⁽⁴⁾ | Conversion time up to 2 Msps | 30 MHz with no Flash memory wait state | 3 ⁽³⁾ | <ul style="list-style-type: none"> – Full-speed operation – I/O compensation works | <ul style="list-style-type: none"> – up to 60 MHz when V_{DD} = 3.0 to 3.6 V – up to 48 MHz when V_{DD} = 2.7 to 3.0 V | 32-bit erase and program operations |

1. The number of wait states can be reduced by reducing the CPU frequency (see [Figure 19](#)).
2. If IRROFF is set to V_{DD}, this value can be lowered to 1.7 V when the device operates in the 0 to 70 °C temperature range.
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

Figure 19. Number of wait states versus f_{CPU} and V_{DD} range

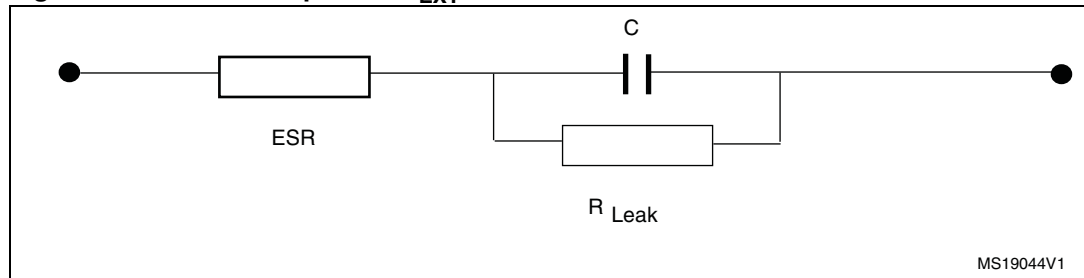


1. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range and IRROFF is set to V_{DD} .

5.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor to the VCAP1/VCAP2 pins. C_{EXT} is specified in Table 14.

Figure 20. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 14. VCAP1/VCAP2 operating conditions⁽¹⁾

| Symbol | Parameter | Conditions |
|------------------|-----------------------------------|--------------|
| C _{EXT} | Capacitance of external capacitor | 2.2 μ F |
| ESR | ESR of external capacitor | < 2 Ω |

1. When bypassing the voltage regulator, the two 2.2 μ F V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A .

Table 15. Operating conditions at power-up / power-down (regulator ON)

| Symbol | Parameter | Min | Max | Unit |
|-----------|-------------------------|-----|----------|-----------------|
| t_{VDD} | V_{DD} rise time rate | 20 | ∞ | $\mu\text{s/V}$ |
| | V_{DD} fall time rate | 20 | ∞ | |

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A .

Table 16. Operating conditions at power-up / power-down (regulator OFF)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|--|------------|-----|----------|-----------------|
| t_{VDD} | V_{DD} rise time rate | Power-up | 20 | ∞ | $\mu\text{s/V}$ |
| | V_{DD} fall time rate | Power-down | 20 | ∞ | |
| t_{VCAP} | V_{CAP_1} and V_{CAP_2} rise time rate | Power-up | 20 | ∞ | |
| | V_{CAP_1} and V_{CAP_2} fall time rate | Power-down | 20 | ∞ | |

5.3.5 Embedded reset and power control block characteristics

The parameters given in [Table 17](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 12](#).

Table 17. Embedded reset and power control block characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|---|-----------------------------|---------------------|------|------|------|
| V_{PVD} | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.09 | 2.14 | 2.19 | V |
| | | PLS[2:0]=000 (falling edge) | 1.98 | 2.04 | 2.08 | V |
| | | PLS[2:0]=001 (rising edge) | 2.23 | 2.30 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.13 | 2.19 | 2.25 | V |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.45 | 2.51 | V |
| | | PLS[2:0]=010 (falling edge) | 2.29 | 2.35 | 2.39 | V |
| | | PLS[2:0]=011 (rising edge) | 2.54 | 2.60 | 2.65 | V |
| | | PLS[2:0]=011 (falling edge) | 2.44 | 2.51 | 2.56 | V |
| | | PLS[2:0]=100 (rising edge) | 2.70 | 2.76 | 2.82 | V |
| | | PLS[2:0]=100 (falling edge) | 2.59 | 2.66 | 2.71 | V |
| | | PLS[2:0]=101 (rising edge) | 2.86 | 2.93 | 2.99 | V |
| | | PLS[2:0]=101 (falling edge) | 2.65 | 2.84 | 3.02 | V |
| | | PLS[2:0]=110 (rising edge) | 2.96 | 3.03 | 3.10 | V |
| | | PLS[2:0]=110 (falling edge) | 2.85 | 2.93 | 2.99 | V |
| | | PLS[2:0]=111 (rising edge) | 3.07 | 3.14 | 3.21 | V |
| PLS[2:0]=111 (falling edge) | 2.95 | 3.03 | 3.09 | V | | |
| $V_{PVDhyst}^{(2)}$ | PVD hysteresis | | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Falling edge | 1.60 ⁽¹⁾ | 1.68 | 1.76 | V |
| | | Rising edge | 1.64 | 1.72 | 1.80 | V |
| $V_{PDRhyst}^{(2)}$ | PDR hysteresis | | - | 40 | - | mV |

Table 17. Embedded reset and power control block characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------|---|---|------|------|------|---------------|
| V_{BOR1} | Brownout level 1 threshold | Falling edge | 2.13 | 2.19 | 2.24 | V |
| | | Rising edge | 2.23 | 2.29 | 2.33 | V |
| V_{BOR2} | Brownout level 2 threshold | Falling edge | 2.44 | 2.50 | 2.56 | V |
| | | Rising edge | 2.53 | 2.59 | 2.63 | V |
| V_{BOR3} | Brownout level 3 threshold | Falling edge | 2.75 | 2.83 | 2.88 | V |
| | | Rising edge | 2.85 | 2.92 | 2.97 | |
| $V_{BORhyst}^{(2)}$ | BOR hysteresis | | - | 100 | - | mV |
| $T_{RSTTEMPO}^{(2)(3)}$ | Reset temporization | | 0.5 | 1.5 | 3.0 | ms |
| $I_{RUSH}^{(2)}$ | InRush current on voltage regulator power-on (POR or wakeup from Standby) | | - | 160 | 200 | mA |
| $E_{RUSH}^{(2)}$ | InRush energy on voltage regulator power-on (POR or wakeup from Standby) | $V_{DD} = 1.8\text{ V}$, $T_A = 105\text{ °C}$, $I_{RUSH} = 171\text{ mA}$ for $31\text{ }\mu\text{s}$ | - | - | 5.4 | μC |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.
3. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 18: Current consumption measurement scheme](#).

All Run mode current consumption measurements given in this section are performed using CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz and 3 wait states from 90 to 120 MHz).
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$, except is explicitly mentioned.
- The maximum values are obtained for $V_{DD} = 3.6\text{ V}$ and maximum ambient temperature (T_A), and the typical values for $T_A = 25\text{ °C}$ and $V_{DD} = 3.3\text{ V}$ unless otherwise specified.

Table 18. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

| Symbol | Parameter | Conditions | f_{HCLK} | Typ | Max ⁽¹⁾ | | Unit |
|----------|----------------------------|--|-----------------------|----------------------|----------------------|-----------------------|------|
| | | | | $T_A = 25\text{ °C}$ | $T_A = 85\text{ °C}$ | $T_A = 105\text{ °C}$ | |
| I_{DD} | Supply current in Run mode | External clock ⁽²⁾ , all peripherals enabled ⁽³⁾ | 120 MHz | 61 | 81 | 93 | mA |
| | | | 90 MHz | 48 | 68 | 80 | |
| | | | 60 MHz | 33 | 53 | 65 | |
| | | | 30 MHz | 18 | 38 | 50 | |
| | | | 25 MHz | 14 | 34 | 46 | |
| | | | 16 MHz ⁽⁴⁾ | 10 | 30 | 42 | |
| | | | 8 MHz | 6 | 26 | 38 | |
| | | | 4 MHz | 4 | 24 | 36 | |
| | | 2 MHz | 3 | 23 | 35 | | |
| | | External clock ⁽²⁾ , all peripherals disabled | 120 MHz | 33 | 54 | 66 | |
| | | | 90 MHz | 27 | 47 | 59 | |
| | | | 60 MHz | 19 | 39 | 51 | |
| | | | 30 MHz | 11 | 31 | 43 | |
| | | | 25 MHz | 8 | 28 | 41 | |
| | | | 16 MHz ⁽⁴⁾ | 6 | 26 | 38 | |
| | | | 8 MHz | 4 | 24 | 36 | |
| 4 MHz | 3 | | 23 | 35 | | | |
| 2 MHz | 2 | 23 | 34 | | | | |

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when $f_{HCLK} > 25\text{ MHz}$.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.



Table 19. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM ⁽¹⁾

| Symbol | Parameter | Conditions | f _{HCLK} | Typ | Max ⁽²⁾ | | Unit |
|-----------------|----------------------------|--|-----------------------|------------------------|------------------------|-------------------------|------|
| | | | | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Run mode | External clock ⁽³⁾ , all peripherals enabled ⁽⁴⁾ | 120 MHz | 49 | 63 | 72 | mA |
| | | | 90 MHz | 38 | 51 | 61 | |
| | | | 60 MHz | 26 | 39 | 49 | |
| | | | 30 MHz | 14 | 27 | 37 | |
| | | | 25 MHz | 11 | 24 | 34 | |
| | | | 16 MHz ⁽⁵⁾ | 8 | 21 | 30 | |
| | | | 8 MHz | 5 | 17 | 27 | |
| | | | 4 MHz | 3 | 16 | 26 | |
| | | 2 MHz | 2 | 15 | 25 | | |
| | | External clock ⁽³⁾ , all peripherals disabled | 120 MHz | 21 | 34 | 44 | |
| | | | 90 MHz | 17 | 30 | 40 | |
| | | | 60 MHz | 12 | 25 | 35 | |
| | | | 30 MHz | 7 | 20 | 30 | |
| | | | 25 MHz | 5 | 18 | 28 | |
| | | | 16 MHz ⁽⁵⁾ | 4.0 | 17.0 | 27.0 | |
| | | | 8 MHz | 2.5 | 15.5 | 25.5 | |
| 4 MHz | 2.0 | | 14.7 | 24.8 | | | |
| 2 MHz | 1.6 | 14.5 | 24.6 | | | | |

- Code and data processing running from SRAM1 using boot pins.
- Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
- External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
- When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
- In this case HCLK = system clock/2.

Figure 21. Typical current consumption vs temperature, Run mode, code with data processing running from RAM, and peripherals ON

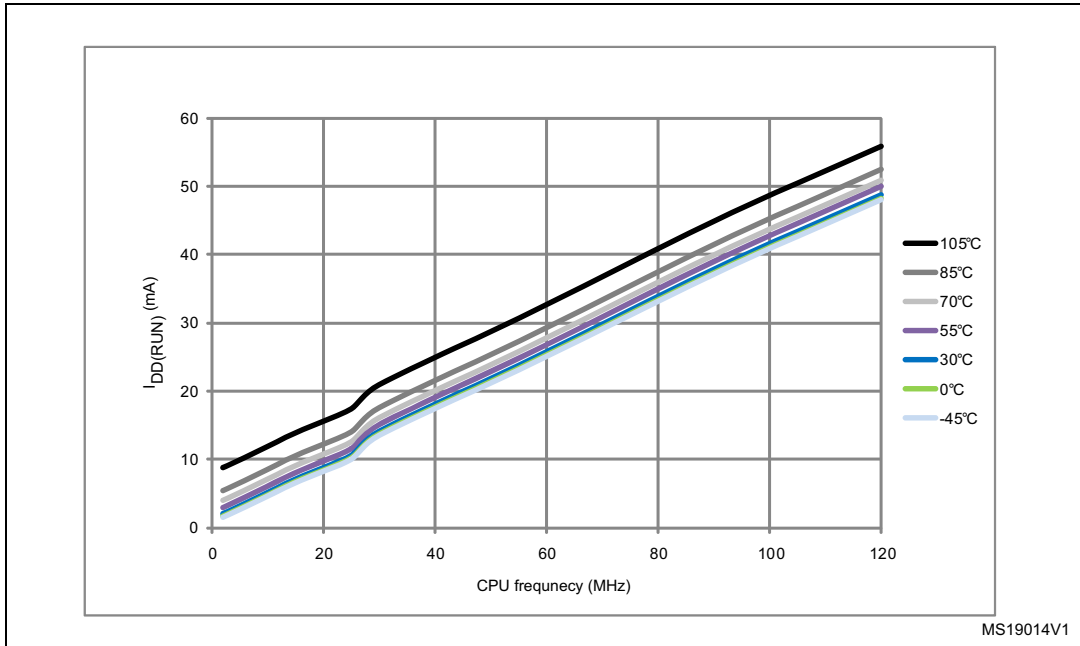


Figure 22. Typical current consumption vs temperature, Run mode, code with data processing running from RAM, and peripherals OFF

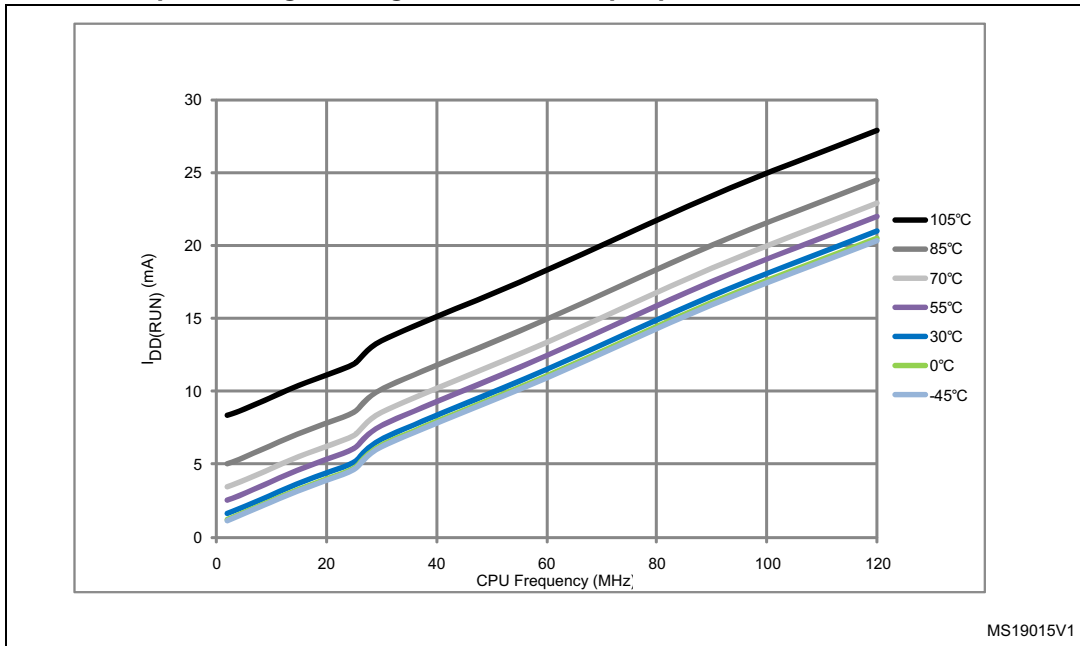


Figure 23. Typical current consumption vs temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals ON

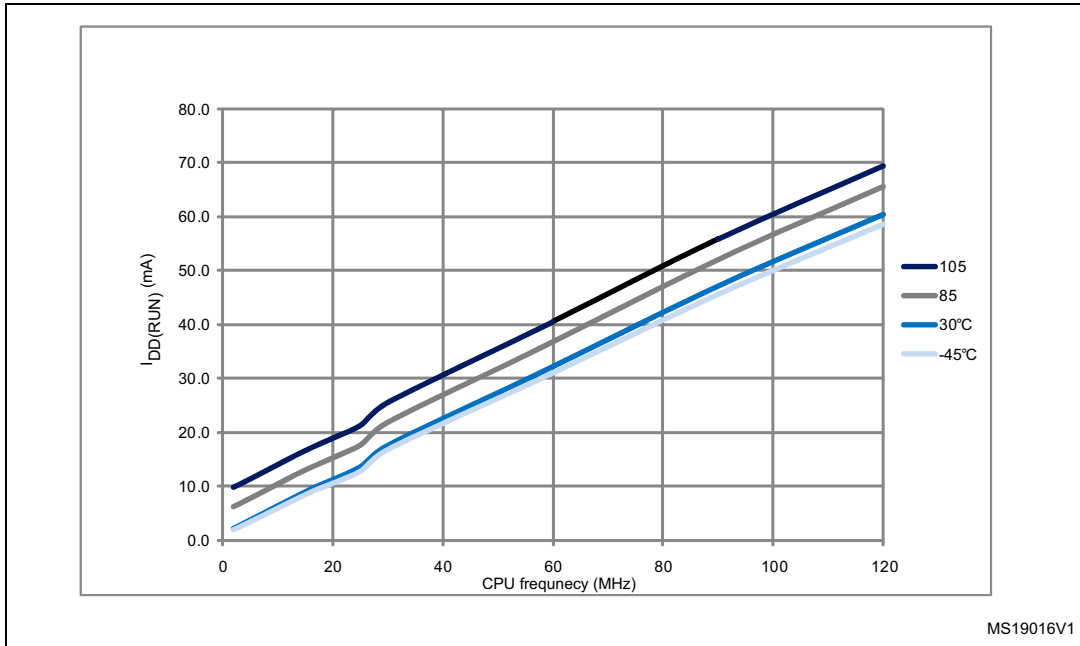


Figure 24. Typical current consumption vs temperature, Run mode, code with data processing running from Flash, ART accelerator OFF, peripherals OFF

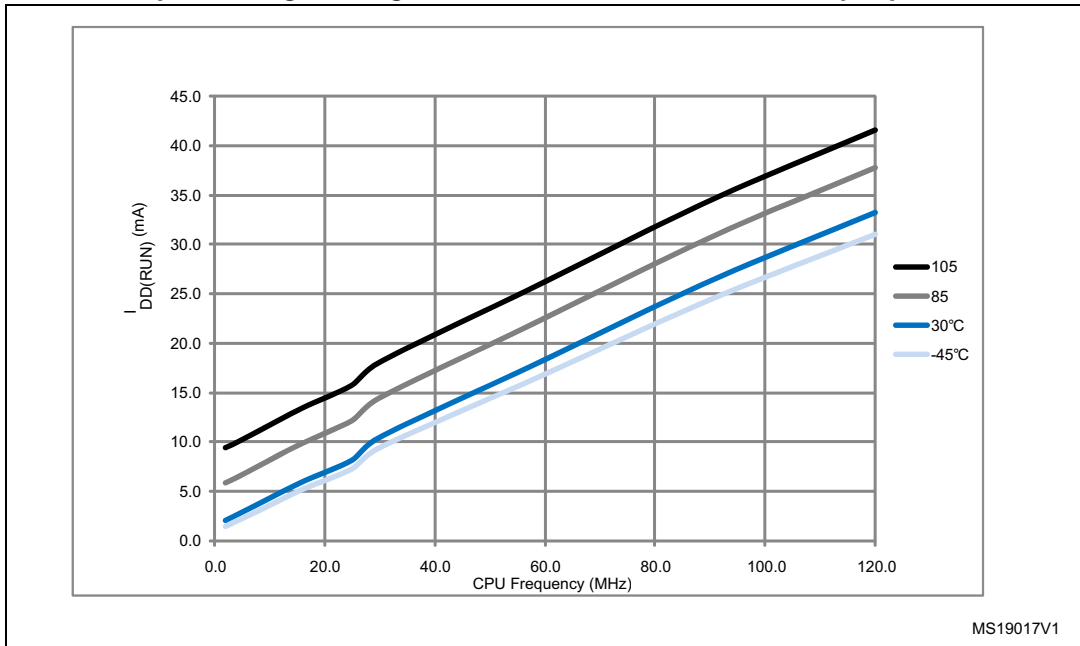


Table 20. Typical and maximum current consumption in Sleep mode

| Symbol | Parameter | Conditions | f _{HCLK} | Typ | Max ⁽¹⁾ | | Unit |
|-----------------|------------------------------|--|-------------------|------------------------|------------------------|-------------------------|------|
| | | | | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Sleep mode | External clock ⁽²⁾ , all peripherals enabled ⁽³⁾ | 120 MHz | 38 | 51 | 61 | mA |
| | | | 90 MHz | 30 | 43 | 53 | |
| | | | 60 MHz | 20 | 33 | 43 | |
| | | | 30 MHz | 11 | 25 | 35 | |
| | | | 25 MHz | 8 | 21 | 31 | |
| | | | 16 MHz | 6 | 19 | 29 | |
| | | | 8 MHz | 3.6 | 17.0 | 27.0 | |
| | | | 4 MHz | 2.4 | 15.4 | 25.3 | |
| | | 2 MHz | 1.9 | 14.9 | 24.7 | | |
| | | External clock ⁽²⁾ , all peripherals disabled | 120 MHz | 8 | 21 | 31 | |
| | | | 90 MHz | 7 | 20 | 30 | |
| | | | 60 MHz | 5 | 18 | 28 | |
| | | | 30 MHz | 3.5 | 16.0 | 26.0 | |
| | | | 25 MHz | 2.5 | 16.0 | 25.0 | |
| | | | 16 MHz | 2.1 | 15.1 | 25.0 | |
| | | | 8 MHz | 1.7 | 15.0 | 25.0 | |
| 4 MHz | 1.5 | | 14.6 | 24.6 | | | |
| 2 MHz | 1.4 | 14.2 | 24.3 | | | | |

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Figure 25. Typical current consumption vs temperature in Sleep mode, peripherals ON

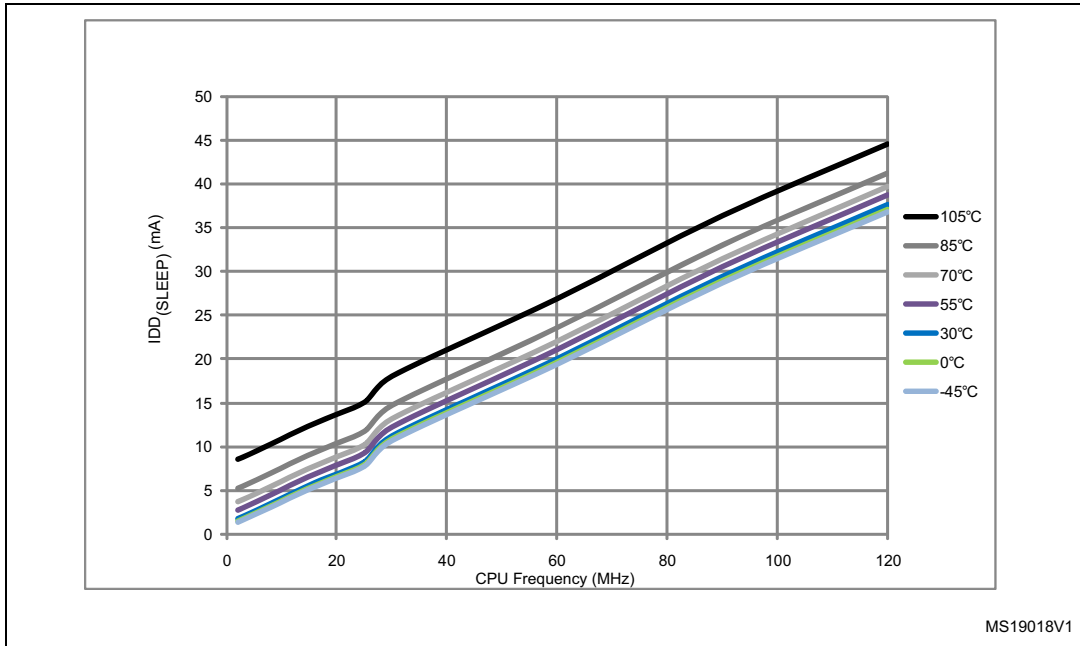


Figure 26. Typical current consumption vs temperature in Sleep mode, peripherals OFF

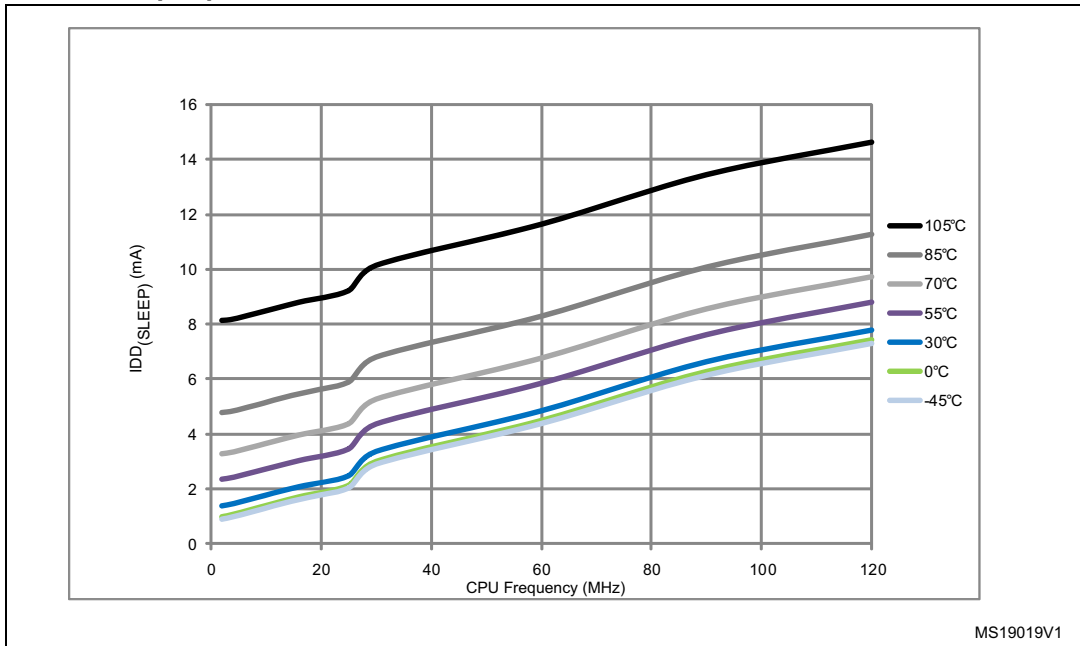
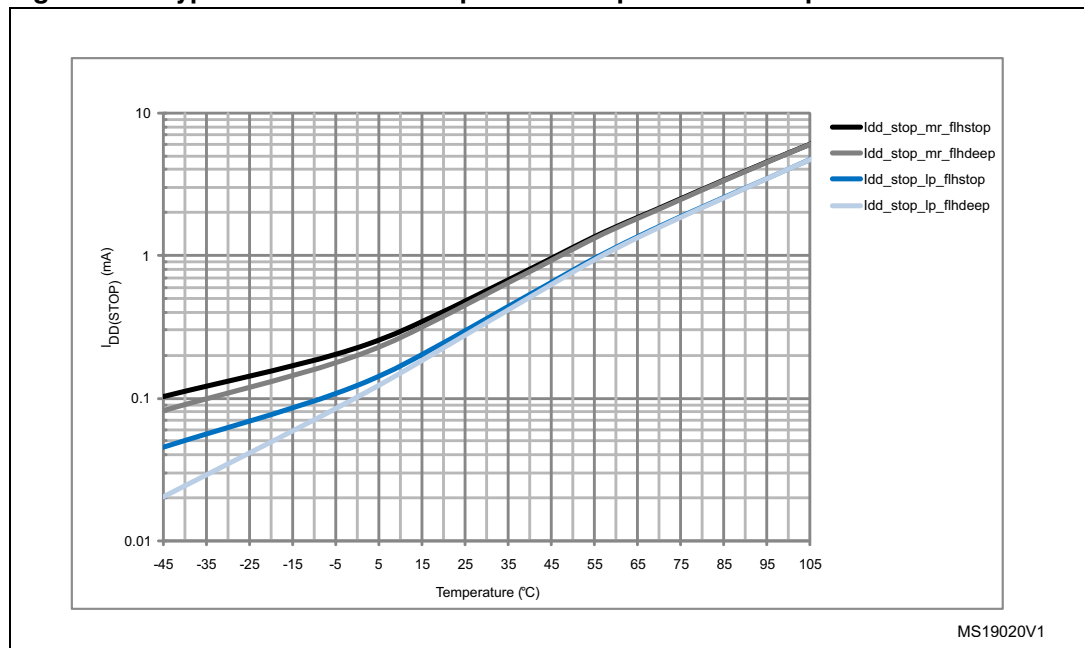


Table 21. Typical and maximum current consumptions in Stop mode⁽¹⁾

| Symbol | Parameter | Conditions | Typ | | Max | | Unit |
|----------------------|---|---|------------------------|------------------------|------------------------|-------------------------|------|
| | | | T _A = 25 °C | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | |
| I _{DD_STOP} | Supply current in Stop mode with main regulator in Run mode | Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.55 | 1.2 | 11.00 | 20.00 | mA |
| | | Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.50 | 1.2 | 11.00 | 20.00 | |
| | Supply current in Stop mode with main regulator in Low Power mode | Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.35 | 1.1 | 8.00 | 15.00 | |
| | | Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.30 | 1.1 | 8.00 | 15.00 | |

1. All typical and maximum values will be further reduced by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes.

Figure 27. Typical current consumption vs temperature in Stop mode



1. All typical and maximum values from table 18 and figure 26 will be reduced over time by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes

Table 22. Typical and maximum current consumptions in Standby mode

| Symbol | Parameter | Conditions | Typ | | | Max ⁽¹⁾ | | Unit |
|----------------------|--------------------------------|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| | | | T _A = 25 °C | | | T _A = 85 °C | T _A = 105 °C | |
| | | | V _{DD} = 1.8 V | V _{DD} = 2.4 V | V _{DD} = 3.3 V | V _{DD} = 3.6 V | | |
| I _{DD_STBY} | Supply current in Standby mode | Backup SRAM ON, low-speed oscillator and RTC ON | 3.0 | 3.4 | 4.0 | 15.1 | 25.8 | µA |
| | | Backup SRAM OFF, low-speed oscillator and RTC ON | 2.4 | 2.7 | 3.3 | 12.4 | 20.5 | |
| | | Backup SRAM ON, RTC OFF | 2.4 | 2.6 | 3.0 | 12.5 | 24.8 | |
| | | Backup SRAM OFF, RTC OFF | 1.7 | 1.9 | 2.2 | 9.8 | 19.2 | |

1. Based on characterization, not tested in production.

Table 23. Typical and maximum current consumptions in V_{BAT} mode

| Symbol | Parameter | Conditions | Typ | | | Max ⁽¹⁾ | | Unit |
|----------------------|------------------------------|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| | | | T _A = 25 °C | | | T _A = 85 °C | T _A = 105 °C | |
| | | | V _{DD} = 1.8 V | V _{DD} = 2.4 V | V _{DD} = 3.3 V | V _{DD} = 3.6 V | | |
| I _{DD_VBAT} | Backup domain supply current | Backup SRAM ON, low-speed oscillator and RTC ON | 1.29 | 1.42 | 1.68 | 12 | 19 | µA |
| | | Backup SRAM OFF, low-speed oscillator and RTC ON | 0.62 | 0.73 | 0.96 | 8 | 10 | |
| | | Backup SRAM ON, RTC OFF | 0.79 | 0.81 | 0.86 | 9 | 16 | |
| | | Backup SRAM OFF, RTC OFF | 0.10 | 0.10 | 0.10 | 5 | 7 | |

1. Based on characterization, not tested in production.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 24](#). The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with one peripheral clocked on (with only the clock applied)
- The code is running from Flash memory and the Flash memory access time is equal to 3 wait states at 120 MHz
- Prefetch and Cache ON
- When the peripherals are enabled, HCLK = 120MHz, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$
- The typical values are obtained for $V_{DD} = 3.3\text{ V}$ and $T_A = 25\text{ °C}$, unless otherwise specified.

Table 24. Peripheral current consumption

| Peripheral ⁽¹⁾ | | Typical consumption at 25 °C | Unit |
|--|---------------|------------------------------|------|
| AHB1 | GPIO A | 0.45 | mA |
| | GPIO B | 0.43 | |
| | GPIO C | 0.46 | |
| | GPIO D | 0.44 | |
| | GPIO E | 0.44 | |
| | GPIO F | 0.42 | |
| | GPIO G | 0.44 | |
| | GPIO H | 0.42 | |
| | GPIO I | 0.43 | |
| | OTG_HS + ULPI | 3.64 | |
| | CRC | 1.17 | |
| | BKPSRAM | 0.21 | |
| | DMA1 | 2.76 | |
| | DMA2 | 2.85 | |
| ETH_MAC + ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP | 2.99 | | |
| AHB2 | OTG_FS | 3.16 | |
| | DCMI | 0.60 | |
| AHB3 | FSMC | 1.74 | |

Table 24. Peripheral current consumption (continued)

| Peripheral ⁽¹⁾ | | Typical consumption at 25 °C | Unit |
|------------------------------|------------------------------|------------------------------|------|
| APB1 | TIM2 | 0.61 | mA |
| | TIM3 | 0.49 | |
| | TIM4 | 0.54 | |
| | TIM5 | 0.62 | |
| | TIM6 | 0.20 | |
| | TIM7 | 0.20 | |
| | TIM12 | 0.36 | |
| | TIM13 | 0.28 | |
| | TIM14 | 0.25 | |
| | USART2 | 0.25 | |
| | USART3 | 0.25 | |
| | UART4 | 0.25 | |
| | UART5 | 0.26 | |
| | I2C1 | 0.25 | |
| | I2C2 | 0.25 | |
| | I2C3 | 0.25 | |
| | SPI2 | 0.20/0.10 | |
| | SPI3 | 0.18/0.09 | |
| | CAN1 | 0.31 | |
| | CAN2 | 0.30 | |
| | DAC channel 1 ⁽²⁾ | 1.11 | |
| DAC channel 1 ⁽³⁾ | 1.11 | | |
| PWR | 0.15 | | |
| WWDG | 0.15 | | |

Table 24. Peripheral current consumption (continued)

| Peripheral ⁽¹⁾ | | Typical consumption at 25 °C | Unit |
|---------------------------|---------------------|------------------------------|------|
| APB2 | SDIO | 0.69 | mA |
| | TIM1 | 1.06 | |
| | TIM8 | 1.03 | |
| | TIM9 | 0.58 | |
| | TIM10 | 0.37 | |
| | TIM11 | 0.39 | |
| | ADC1 ⁽⁴⁾ | 2.13 | |
| | ADC2 ⁽⁴⁾ | 2.04 | |
| | ADC3 ⁽⁴⁾ | 2.12 | |
| | SPI1 | 1.20 | |
| | USART1 | 0.38 | |
| | USART6 | 0.37 | |

- External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
- EN1 bit is set in DAC_CR register.
- EN2 bit is set in DAC_CR register.
- $f_{ADC} = f_{PCLK2}/2$, ADON bit set in ADC_CR2 register.

5.3.7 Wakeup time from low-power mode

The wakeup times given in [Table 25](#) is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 12](#).

Table 25. Low-power mode wakeup timings

| Symbol | Parameter | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|------------------------|--|--------------------|--------------------|--------------------|------|
| $t_{WUSLEEP}^{(2)}$ | Wakeup from Sleep mode | - | 1 | - | μs |
| $t_{WUSTOP}^{(2)}$ | Wakeup from Stop mode (regulator in Run mode) | - | 13 | - | μs |
| | Wakeup from Stop mode (regulator in low power mode) | - | 17 | 40 | |
| | Wakeup from Stop mode (regulator in low power mode and Flash memory in Deep power down mode) | - | 110 | - | |
| $t_{WUSTDBY}^{(2)(3)}$ | Wakeup from Standby mode | 260 | 375 | 480 | μs |

- Based on characterization, not tested in production.
- The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
- $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and -45 °C, respectively.

5.3.8 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in [Table 26](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 12](#).

Table 26. High-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---|----------------------------------|-------------|-----|-------------|---------|
| f_{HSE_ext} | External user clock source frequency ⁽¹⁾ | | 1 | - | 26 | MHz |
| V_{HSEH} | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | - | V_{DD} | V |
| V_{HSEL} | OSC_IN input pin low level voltage | | V_{SS} | - | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{f(HSE)}$ | OSC_IN high or low time ⁽¹⁾ | | 5 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time ⁽¹⁾ | | - | - | 20 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance ⁽¹⁾ | | - | 5 | - | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | 45 | - | 55 | % |
| I_L | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ± 1 | μA |

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

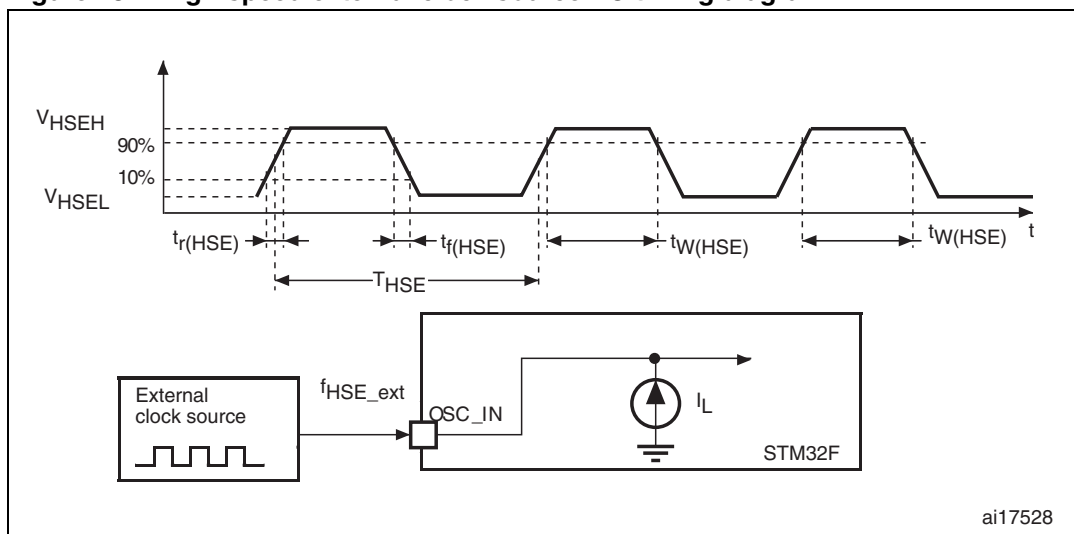
The characteristics given in [Table 27](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 12](#).

Table 27. Low-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---|----------------------------------|-------------|--------|-------------|---------|
| f_{LSE_ext} | User External clock source frequency ⁽¹⁾ | | - | 32.768 | 1000 | kHz |
| V_{LSEH} | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | V_{DD} | V |
| V_{LSEL} | OSC32_IN input pin low level voltage | | V_{SS} | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{f(LSE)}$ | OSC32_IN high or low time ⁽¹⁾ | | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time ⁽¹⁾ | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance ⁽¹⁾ | | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | 30 | - | 70 | % |
| I_L | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ± 1 | μA |

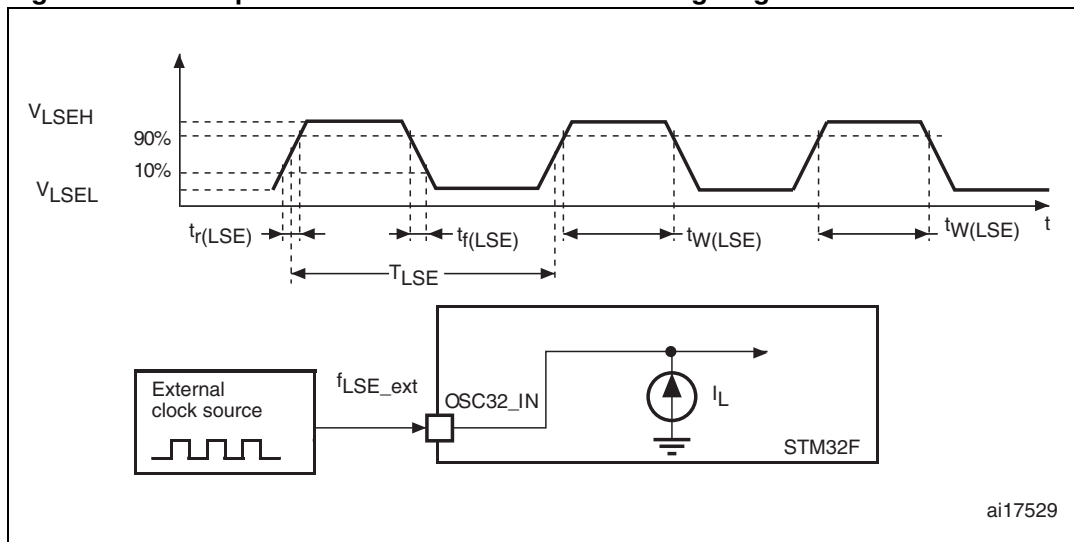
1. Guaranteed by design, not tested in production.

Figure 28. High-speed external clock source AC timing diagram



ai17528

Figure 29. Low-speed external clock source AC timing diagram



ai17529

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 28](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 28. HSE 4-26 MHz oscillator characteristics^{(1) (2)}

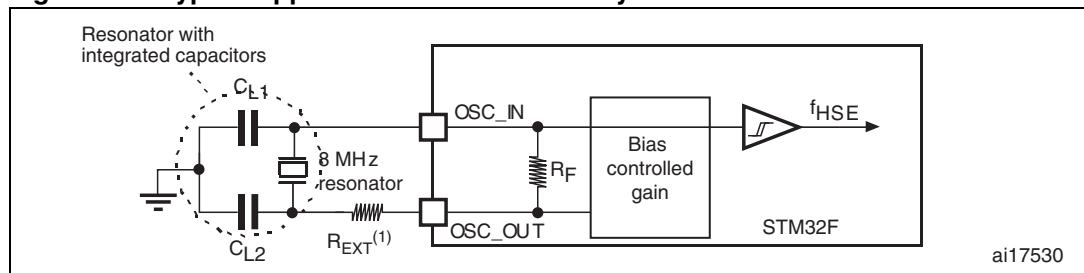
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-----------------------------|--|-----|-----|-----|---------------|
| f_{OSC_IN} | Oscillator frequency | | 4 | - | 26 | MHz |
| R_F | Feedback resistor | | - | 200 | - | k Ω |
| I_{DD} | HSE current consumption | $V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=5\text{ pF@25 MHz}$ | - | 449 | - | μA |
| | | $V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=10\text{ pF@25 MHz}$ | - | 532 | - | |
| g_m | Oscillator transconductance | Startup | 5 | - | - | mA/V |
| $t_{SU(HSE)}^{(3)}$ | Startup time | V_{DD} is stabilized | - | 2 | - | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 30](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on electing the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 30. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 29](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz) ⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|-----------------------------|------------------------|-----|------|-----|------------|
| R_F | Feedback resistor | | - | 18.4 | - | M Ω |
| I_{DD} | LSE current consumption | | - | - | 1 | μ A |
| g_m | Oscillator Transconductance | | 2.8 | - | - | μ A/V |
| $t_{SU(LSE)}$ ⁽²⁾ | startup time | V_{DD} is stabilized | - | 2 | - | s |

1. Guaranteed by design, not tested in production.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

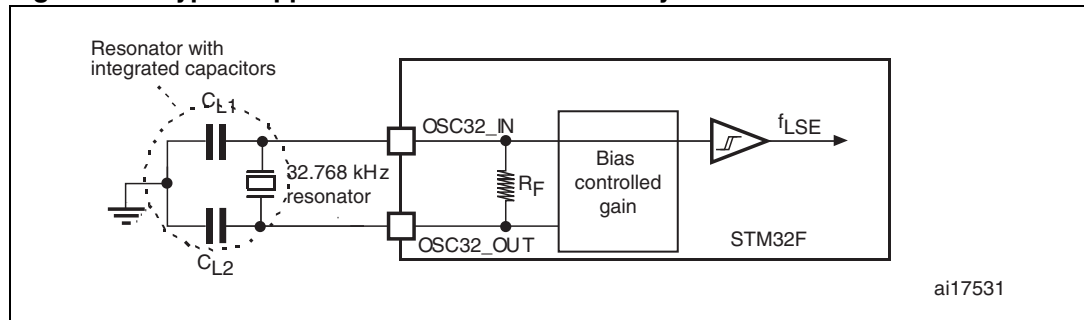
Note: For C_{L1} and C_{L2} it is recommended to use high-quality external ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 31). C_{L1} and C_{L2} , are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Note: For information on electing the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of $C_L = 6$ pF, and $C_{stray} = 2$ pF, then $C_{L1} = C_{L2} = 8$ pF.

Figure 31. Typical application with a 32.768 kHz crystal



5.3.9 Internal clock source characteristics

The parameters given in [Table 30](#) and [Table 31](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 12](#).

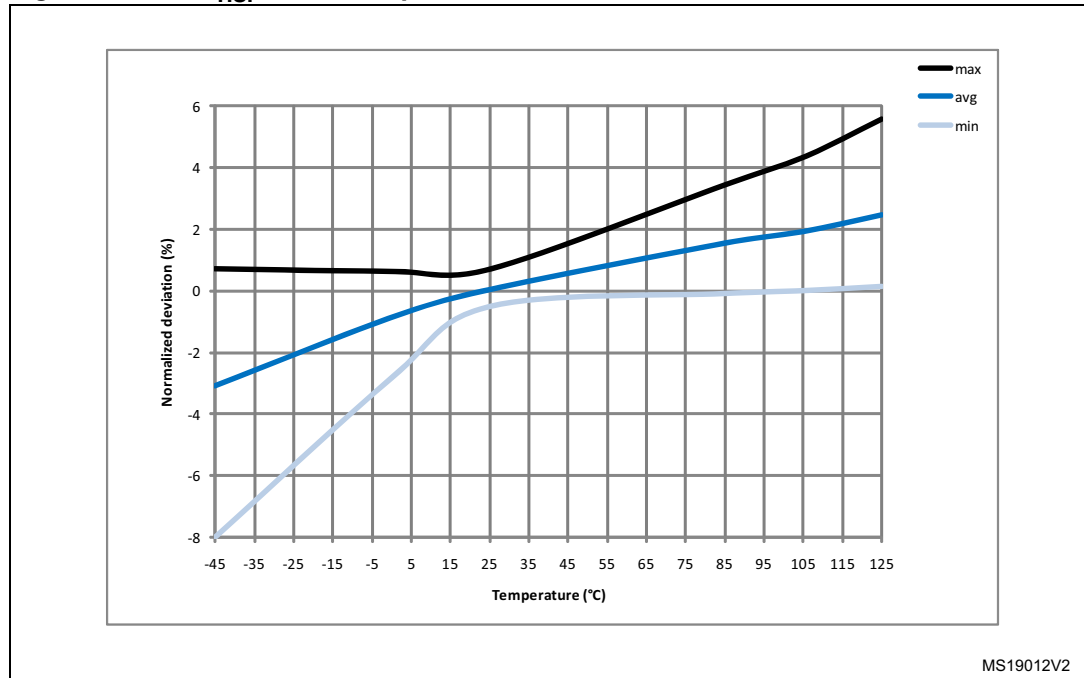
High-speed internal (HSI) RC oscillator

Table 30. HSI oscillator characteristics ⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|------------------------------|----------------------------------|--|-------------------------|-----|-----|------|---|
| f_{HSI} | Frequency | | - | 16 | - | MHz | |
| ACC_{HSI} | Accuracy of the HSI oscillator | User-trimmed with the RCC_CR register ⁽²⁾ | - | - | 1 | % | |
| | | Factory-calibrated | $T_A = -40$ to 105 °C | -8 | - | 4.5 | % |
| | | | $T_A = -10$ to 85 °C | -4 | - | 4 | % |
| | | | $T_A = 25$ °C | -1 | - | 1 | % |
| $t_{su(HSI)}$ ⁽³⁾ | HSI oscillator startup time | | - | 2.2 | 4 | µs | |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | - | 60 | 80 | µA | |

- $V_{DD} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.
- Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.
- Guaranteed by design, not tested in production.

Figure 32. ACC_{HSI} versus temperature



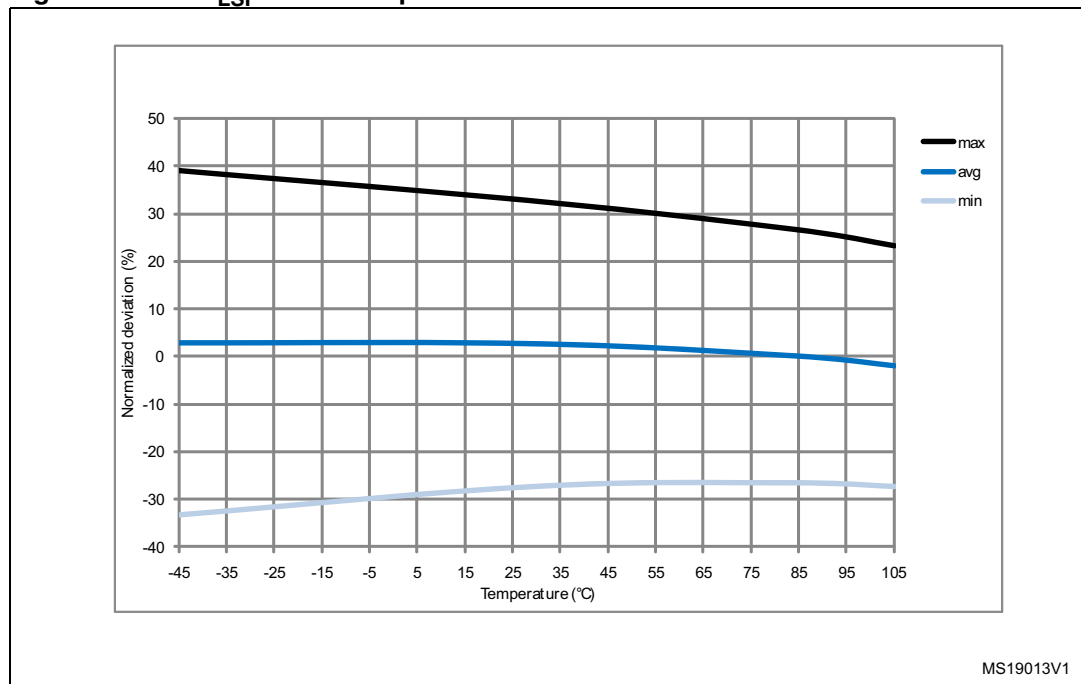
Low-speed internal (LSI) RC oscillator

Table 31. LSI oscillator characteristics (1)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|----------------------------------|-----|-----|-----|---------|
| $f_{LSI}^{(2)}$ | Frequency | 17 | 32 | 47 | kHz |
| $t_{su(LSI)}^{(3)}$ | LSI oscillator startup time | - | 15 | 40 | μs |
| $I_{DD(LSI)}^{(3)}$ | LSI oscillator power consumption | - | 0.4 | 0.6 | μA |

- $V_{DD} = 3 V, T_A = -40$ to $105\text{ }^\circ C$ unless otherwise specified.
- Based on characterization, not tested in production.
- Guaranteed by design, not tested in production.

Figure 33. ACC_{LSI} versus temperature



5.3.10 PLL characteristics

The parameters given in [Table 32](#) and [Table 33](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 12](#).

Table 32. Main PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|------------------------------------|------------|---------------------|-----|---------------------|------|
| f_{PLL_IN} | PLL input clock ⁽¹⁾ | | 0.95 ⁽²⁾ | 1 | 2.10 ⁽²⁾ | MHz |
| f_{PLL_OUT} | PLL multiplier output clock | | 24 | - | 120 | MHz |
| f_{PLL48_OUT} | 48 MHz PLL multiplier output clock | | - | - | 48 | MHz |
| f_{VCO_OUT} | PLL VCO output | | 192 | - | 432 | MHz |

Table 32. Main PLL characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--------------------------------------|-------------------------------|--|--|--|------|------|----|
| t _{LOCK} | PLL lock time | VCO freq = 192 MHz | 75 | - | 200 | µs | |
| | | VCO freq = 432 MHz | 100 | - | 300 | | |
| Jitter ⁽³⁾ | Cycle-to-cycle jitter | System clock 120 MHz | RMS | - | 25 | - | ps |
| | | | peak to peak | - | ±150 | - | |
| | RMS | | - | 15 | - | | |
| | peak to peak | | - | ±200 | - | | |
| | Period Jitter | Main clock output (MCO) for RMI Ethernet | Cycle to cycle at 50 MHz on 1000 samples | - | 32 | - | |
| | | | Main clock output (MCO) for MII Ethernet | Cycle to cycle at 25 MHz on 1000 samples | - | 40 | |
| | Bit Time CAN jitter | Cycle to cycle at 1 MHz on 1000 samples | - | 330 | - | | |
| I _{DD(PLL)} ⁽⁴⁾ | PLL power consumption on VDD | VCO freq = 192 MHz | 0.15 | - | 0.40 | mA | |
| | | VCO freq = 432 MHz | 0.45 | - | 0.75 | | |
| I _{DDA(PLL)} ⁽⁴⁾ | PLL power consumption on VDDA | VCO freq = 192 MHz | 0.30 | - | 0.40 | mA | |
| | | VCO freq = 432 MHz | 0.55 | - | 0.85 | | |

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design, not tested in production.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Based on characterization, not tested in production.

Table 33. PLLI2S (audio PLL) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------|-----------------------------------|--------------------|---------------------|-----|---------------------|------|
| f _{PLLI2S_IN} | PLLI2S input clock ⁽¹⁾ | | 0.95 ⁽²⁾ | 1 | 2.10 ⁽²⁾ | MHz |
| f _{PLLI2S_OUT} | PLLI2S multiplier output clock | | - | - | 216 | MHz |
| f _{VCO_OUT} | PLLI2S VCO output | | 192 | - | 432 | MHz |
| t _{LOCK} | PLLI2S lock time | VCO freq = 192 MHz | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | 100 | - | 300 | |

Table 33. PLLI2S (audio PLL) characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---|--|--|--------------|-----|--------------|------|----|
| Jitter ⁽³⁾ | Master I2S clock jitter | Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5 | RMS | - | 90 | - | |
| | | | peak to peak | - | ±280 | - | ps |
| | | Average frequency of 12.288 MHz N=432, R=5 on 1000 samples | - | 90 | - | ps | |
| | WS I2S clock jitter | Cycle to cycle at 48 KHz on 1000 samples | - | 400 | - | ps | |
| I _{DD(PLLI2S)} ⁽⁴⁾ | PLLI2S power consumption on V _{DD} | VCO freq = 192 MHz VCO freq = 432 MHz | 0.15 0.45 | - | 0.40 0.75 | mA | |
| I _{DDA(PLLI2S)} ⁽⁴⁾ | PLLI2S power consumption on V _{DDA} | VCO freq = 192 MHz VCO freq = 432 MHz | 0.30 0.55 | - | 0.40 0.85 | mA | |

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Based on characterization, not tested in production.

5.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 40: EMI characteristics](#)). It is available only on the main PLL.

Table 34. SSCG parameters constraint

| Symbol | Parameter | Min | Typ | Max ⁽¹⁾ | Unit |
|-------------------|-----------------------|------|-----|--------------------|------|
| f _{Mod} | Modulation frequency | - | - | 10 | KHz |
| md | Peak modulation depth | 0.25 | - | 2 | % |
| MODEPER * INCSTEP | | - | - | 2 ¹⁵ -1 | - |

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL_IN}} / (4 \times f_{\text{Mod}})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$\text{MODEPER} = \text{round}[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times \text{md} \times \text{PLL}_N / (100 \times 5 \times \text{MODEPER})]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLL_N = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times 2 \times 240 / (100 \times 5 \times 250)] = 126 \text{md}(\text{quantitized})\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = (\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \text{PLL}_N)$$

As a result:

$$\text{md}_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.0002\%(\text{peak})$$

Figure 34 and Figure 35 show the main PLL output clock waveforms in center spread and down spread modes, where:

- F0 is f_{PLL_OUT} nominal.
- T_{mode} is the modulation period.
- md is the modulation depth.

Figure 34. PLL output clock waveforms in center spread mode

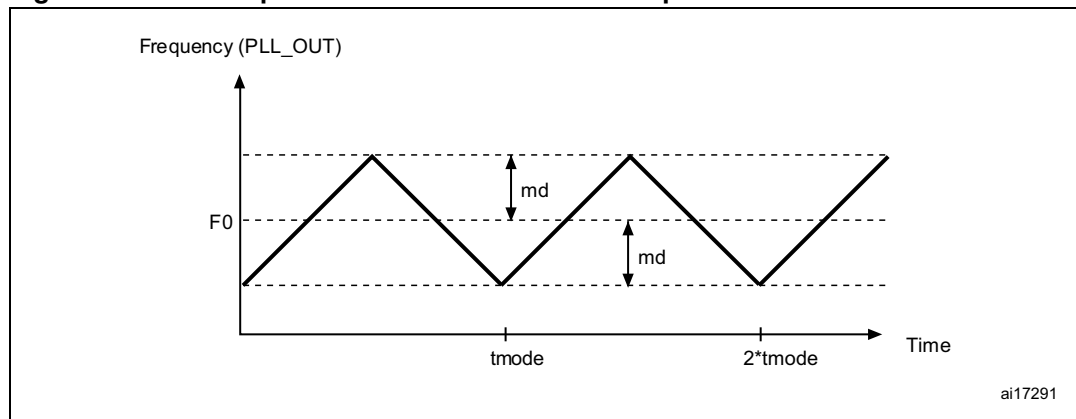
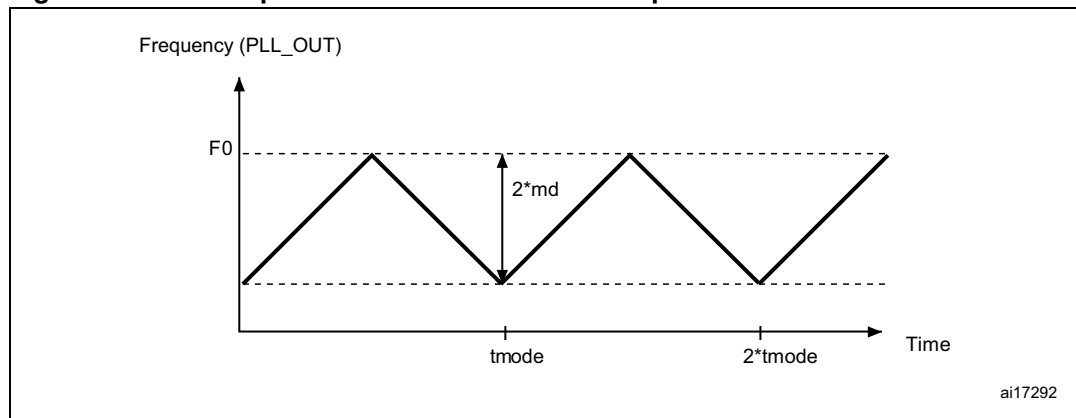


Figure 35. PLL output clock waveforms in down spread mode



5.3.12 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 35. Flash memory characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|----------------|---|-----|-----|-----|------|
| I_{DD} | Supply current | Write / Erase 8-bit mode $V_{DD} = 1.8$ V | - | 5 | - | mA |
| | | Write / Erase 16-bit mode $V_{DD} = 2.1$ V | - | 8 | - | |
| | | Write / Erase 32-bit mode $V_{DD} = 3.3$ V | - | 12 | - | |

Table 36. Flash memory programming

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit |
|-------------------------|----------------------------|---|--------------------|------|--------------------|------|
| t _{prog} | Word programming time | Program/erase parallelism (PSIZE) = x 8/16/32 | - | 16 | 100 ⁽²⁾ | μs |
| t _{ERASE16KB} | Sector (16 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 400 | 800 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 300 | 600 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 250 | 500 | |
| t _{ERASE64KB} | Sector (64 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 1200 | 2400 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 700 | 1400 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 550 | 1100 | |
| t _{ERASE128KB} | Sector (128 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 2 | 4 | s |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 1.3 | 2.6 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 1 | 2 | |
| t _{ME} | Mass erase time | Program/erase parallelism (PSIZE) = x 8 | - | 16 | 32 | s |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 11 | 22 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 8 | 16 | |
| V _{prog} | Programming voltage | 32-bit program operation | 2.7 | - | 3.6 | V |
| | | 16-bit program operation | 2.1 | - | 3.6 | V |
| | | 8-bit program operation | 1.8 | - | 3.6 | V |

1. Based on characterization, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

Table 37. Flash memory programming with V_{pp}

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit |
|-------------------------|----------------------------|--|--------------------|-----|--------------------|------|
| t _{prog} | Double word programming | T _A = 0 to +40 °C V _{DD} = 3.3 V V _{PP} = 8.5 V | - | 16 | 100 ⁽²⁾ | μs |
| t _{ERASE16KB} | Sector (16 KB) erase time | | - | 230 | - | ms |
| t _{ERASE64KB} | Sector (64 KB) erase time | | - | 490 | - | |
| t _{ERASE128KB} | Sector (128 KB) erase time | | - | 875 | - | |
| t _{ME} | Mass erase time | | - | 6.9 | - | s |
| V _{prog} | Programming voltage | | 2.7 | - | 3.6 | V |

Table 37. Flash memory programming with V_{PP} (continued)

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit |
|-----------------|--|------------|--------------------|-----|--------------------|------|
| V_{PP} | V_{PP} voltage range | | 7 | - | 9 | V |
| I_{PP} | Minimum current sunk on the V_{PP} pin | | 10 | - | - | mA |
| $t_{VPP}^{(3)}$ | Cumulative time during which V_{PP} is applied | | - | - | 1 | hour |

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 38. Flash memory endurance and data retention

| Symbol | Parameter | Conditions | Value | Unit |
|-----------|----------------|---|--------------------|---------|
| | | | Min ⁽¹⁾ | |
| N_{END} | Endurance | $T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions) | 10 | kcycles |
| t_{RET} | Data retention | 1 kcycle ⁽²⁾ at $T_A = 85$ °C | 30 | Years |
| | | 1 kcycle ⁽²⁾ at $T_A = 105$ °C | 10 | |
| | | 10 kcycles ⁽²⁾ at $T_A = 55$ °C | 20 | |

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 39](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 39. EMS characteristics

| Symbol | Parameter | Conditions | Level/ Class |
|------------|---|---|-----------------|
| V_{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$, LQFP100, $T_A = +25\text{ °C}$, $f_{HCLK} = 75\text{ MHz}$, conforms to IEC 61000-4-2 | 2B |
| V_{EFTB} | Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$, LQFP100, $T_A = +25\text{ °C}$, $f_{HCLK} = 75\text{ MHz}$, conforms to IEC 61000-4-2 | 4A |

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC[®] code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 40. EMI characteristics

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [f _{HSE} /f _{CPU}] | Unit |
|------------------|------------|---|--------------------------|---|------|
| | | | | 8/120 MHz | |
| S _{EMI} | Peak level | V _{DD} = 3.3 V, T _A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled | 0.1 to 30 MHz | 21 | dBμV |
| | | | 30 to 130 MHz | 28 | |
| | | | 130 MHz to 1GHz | 31 | |
| | | | SAE EMI Level | 4 | - |
| | | V _{DD} = 3.3 V, T _A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, PLL spread spectrum enabled | 0.1 to 30 MHz | 21 | dBμV |
| | | | 30 to 130 MHz | 15 | |
| | | | 130 MHz to 1GHz | 14 | |
| | | | SAE EMI level | 3.5 | - |

5.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 41. ESD absolute maximum ratings

| Symbol | Ratings | Conditions | Class | Maximum value ⁽¹⁾ | Unit |
|-----------------------|---|---|-------|------------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (human body model) | T _A = +25 °C conforming to JESD22-A114 | 2 | 2000 ⁽²⁾ | V |
| V _{ESD(CDM)} | Electrostatic discharge voltage (charge device model) | T _A = +25 °C conforming to JESD22-C101 | II | 500 | |

1. Based on characterization results, not tested in production.
2. On V_{BAT} pin, V_{ESD(HBM)} is limited to 1000 V.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 42. Electrical sensitivities

| Symbol | Parameter | Conditions | Class |
|--------|-----------------------|--|------------|
| LU | Static latch-up class | T _A = +105 °C conforming to JESD78A | II level A |

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in [Table 43](#).

Table 43. I/O current injection susceptibility

| Symbol | Description | Functional susceptibility | | Unit |
|------------------|-----------------------------------|---------------------------|--------------------|------|
| | | Negative injection | Positive injection | |
| I _{INJ} | Injected current on all FT pins | -5 | +0 | mA |
| | Injected current on any other pin | -5 | +5 | |

5.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 44](#) are derived from tests performed under the conditions summarized in [Table 12](#). All I/Os are CMOS and TTL compliant.

Table 44. I/O static characteristics

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|----------------|---|-----------------------------------|--|--------------------|-----|--------------|---------------|
| V_{IL} | Input low level voltage | | TTL ports $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | $V_{SS}-0.3$ | - | 0.8 | V |
| $V_{IH}^{(1)}$ | TT ⁽²⁾ I/O input high level voltage | | | 2.0 | - | $V_{DD}+0.3$ | |
| | FT ⁽³⁾ I/O input high level voltage | | | 2.0 | - | 5.5 | |
| V_{IL} | Input low level voltage | | CMOS ports $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | $V_{SS}-0.3$ | - | $0.3V_{DD}$ | V |
| $V_{IH}^{(1)}$ | TT I/O input high level voltage | | | $0.7V_{DD}$ | - | $3.6^{(4)}$ | |
| | FT I/O input high level voltage | | | | - | $5.2^{(4)}$ | |
| V_{hys} | I/O Schmitt trigger voltage hysteresis ⁽⁵⁾ | | CMOS ports $2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | - | 200 | - | mV |
| | IO FT Schmitt trigger voltage hysteresis ⁽⁵⁾ | | | $5\% V_{DD}^{(4)}$ | - | - | |
| I_{lkg} | I/O input leakage current ⁽⁶⁾ | | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ± 1 | μA |
| | I/O FT input leakage current ⁽⁶⁾ | | $V_{IN} = 5\text{ V}$ | - | - | 3 | |
| R_{PU} | Weak pull-up equivalent resistor ⁽⁷⁾ | All pins except for PA10 and PB12 | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | k Ω |
| | | PA10 and PB12 | | 8 | 11 | 15 | |
| R_{PD} | Weak pull-down equivalent resistor | All pins except for PA10 and PB12 | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | |
| | | PA10 and PB12 | | 8 | 11 | 15 | |
| $C_{IO}^{(8)}$ | I/O pin capacitance | | | | 5 | | pF |

1. If V_{IH} maximum value cannot be respected, the injection current must be limited externally to $I_{INJ(PIN)}$ maximum value.
2. TT = 3.6 V tolerant.
3. FT = 5 V tolerant.
4. With a minimum of 100 mV.
5. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
6. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).
8. Guaranteed by design, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 10](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 10](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 45](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 12](#). All I/Os are CMOS and TTL compliant.

Table 45. Output voltage characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|---|--|--------------|-----|------|
| $V_{OL}^{(2)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | CMOS ports $I_{IO} = +8$ mA 2.7 V < $V_{DD} < 3.6$ V | - | 0.4 | V |
| $V_{OH}^{(3)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-0.4$ | - | |
| $V_{OL}^{(2)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | TTL ports $I_{IO} = +8$ mA 2.7 V < $V_{DD} < 3.6$ V | - | 0.4 | V |
| $V_{OH}^{(3)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | 2.4 | - | |
| $V_{OL}^{(2)(4)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO} = +20$ mA 2.7 V < $V_{DD} < 3.6$ V | - | 1.3 | V |
| $V_{OH}^{(3)(4)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-1.3$ | - | |
| $V_{OL}^{(2)(4)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO} = +6$ mA 2 V < $V_{DD} < 2.7$ V | - | 0.4 | V |
| $V_{OH}^{(3)(4)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-0.4$ | - | |

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 10](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 10](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .

4. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 36](#) and [Table 46](#), respectively.

Unless otherwise specified, the parameters given in [Table 46](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 12](#).

Table 46. I/O AC characteristics⁽¹⁾⁽²⁾

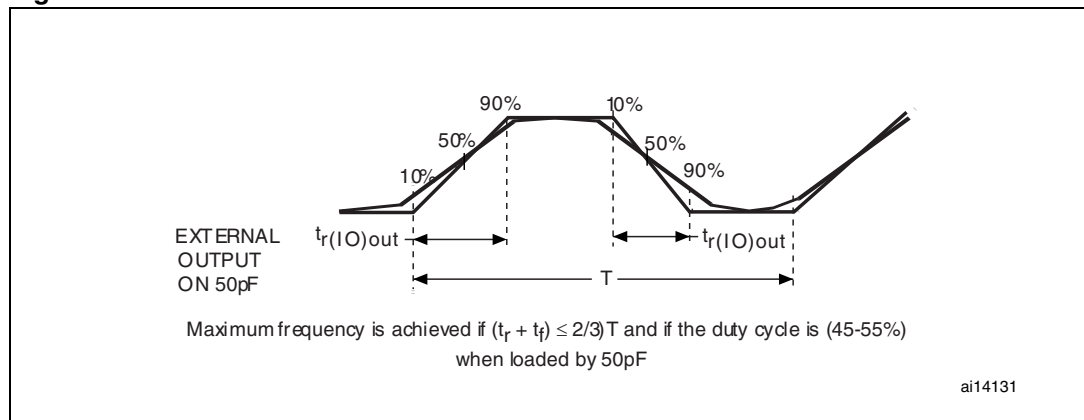
| OSPEEDRy [1:0] bit value ⁽¹⁾ | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|------------------------------------|------------------------------------|--|-----|-----|---------------------|------|
| 00 | f _{max(IO)out} | Maximum frequency ⁽³⁾ | C _L = 50 pF, V _{DD} > 2.70 V | - | - | 2 | MHz |
| | | | C _L = 50 pF, V _{DD} > 1.8 V | - | - | 2 | |
| | | | C _L = 10 pF, V _{DD} > 2.70 V | - | - | TBD | |
| | | | C _L = 10 pF, V _{DD} > 1.8 V | - | - | TBD | |
| | t _{f(IO)out} | Output high to low level fall time | C _L = 50 pF, V _{DD} = 1.8 V to 3.6 V | - | - | TBD | ns |
| t _{r(IO)out} | Output low to high level rise time | - | | - | TBD | | |
| 01 | f _{max(IO)out} | Maximum frequency ⁽³⁾ | C _L = 50 pF, V _{DD} > 2.70 V | - | - | 25 | MHz |
| | | | C _L = 50 pF, V _{DD} > 1.8 V | - | - | 12.5 ⁽⁴⁾ | |
| | | | C _L = 10 pF, V _{DD} > 2.70 V | - | - | 50 ⁽⁴⁾ | |
| | | | C _L = 10 pF, V _{DD} > 1.8 V | - | - | TBD | |
| | t _{f(IO)out} | Output high to low level fall time | C _L = 50 pF, V _{DD} < 2.7 V | - | - | TBD | ns |
| | | | C _L = 10 pF, V _{DD} > 2.7 V | - | - | TBD | |
| | t _{r(IO)out} | Output low to high level rise time | C _L = 50 pF, V _{DD} < 2.7 V | - | - | TBD | ns |
| C _L = 10 pF, V _{DD} > 2.7 V | | | - | - | TBD | | |
| 10 | f _{max(IO)out} | Maximum frequency ⁽³⁾ | C _L = 40 pF, V _{DD} > 2.70 V | - | - | 50 ⁽⁴⁾ | MHz |
| | | | C _L = 40 pF, V _{DD} > 1.8 V | - | - | 25 | |
| | | | C _L = 10 pF, V _{DD} > 2.70 V | - | - | 100 ⁽⁴⁾ | |
| | | | C _L = 10 pF, V _{DD} > 1.8 V | - | - | TBD | |
| | t _{f(IO)out} | Output high to low level fall time | C _L = 50 pF, 2.4 < V _{DD} < 2.7 V | - | - | TBD | ns |
| | | | C _L = 10 pF, V _{DD} > 2.7 V | - | - | TBD | |
| | t _{r(IO)out} | Output low to high level rise time | C _L = 50 pF, 2.4 < V _{DD} < 2.7 V | - | - | TBD | ns |
| C _L = 10 pF, V _{DD} > 2.7 V | | | - | - | TBD | | |

Table 46. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

| OSPEEDRy [1:0] bit value ⁽¹⁾ | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-------------------------|---|---|-----|-----|--------------------|------|
| 11 | F _{max(IO)out} | Maximum frequency ⁽³⁾ | C _L = 30 pF, V _{DD} > 2.70 V | - | - | 100 ⁽⁴⁾ | MHz |
| | | | C _L = 30 pF, V _{DD} > 1.8 V | - | - | 50 ⁽⁴⁾ | |
| | | | C _L = 10 pF, V _{DD} > 2.70 V | - | - | 200 ⁽⁴⁾ | |
| | | | C _L = 10 pF, V _{DD} > 1.8 V | - | - | TBD | |
| | t _{r(IO)out} | Output high to low level fall time | C _L = 20 pF, 2.4 < V _{DD} < 2.7 V | - | - | TBD | ns |
| | | | C _L = 10 pF, V _{DD} > 2.7 V | - | - | TBD | |
| | t _{r(IO)out} | Output low to high level rise time | C _L = 20 pF, 2.4 < V _{DD} < 2.7 V | - | - | TBD | ns |
| | | | C _L = 10 pF, V _{DD} > 2.7 V | - | - | TBD | |
| - | t _{EXTIpw} | Pulse width of external signals detected by the EXTI controller | | 10 | - | - | ns |

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F20/21xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
2. TBD stands for "to be defined".
3. The maximum frequency is defined in [Figure 36](#).
4. For maximum frequencies above 50 MHz, the compensation cell should be used.

Figure 36. I/O AC characteristics definition



5.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 44](#)).

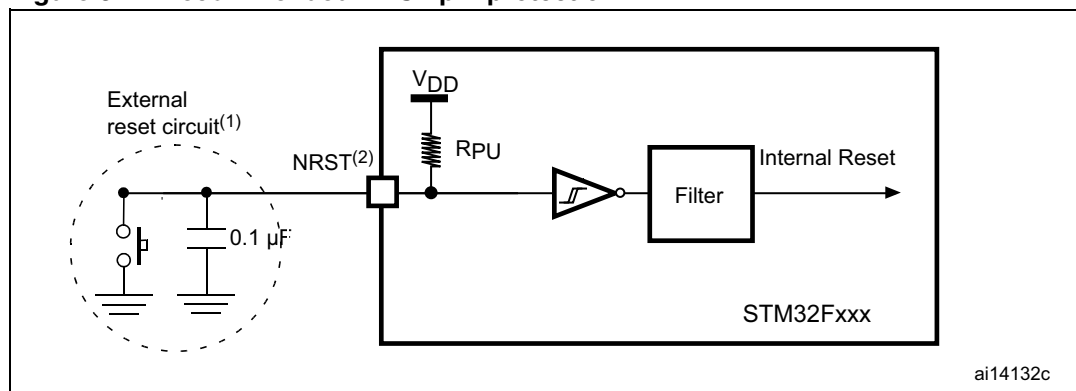
Unless otherwise specified, the parameters given in [Table 47](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 12](#).

Table 47. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|---|--|--------------|-----|--------------|---------------|
| $V_{IL(NRST)}^{(1)}$ | NRST input low level voltage | TTL ports $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | $V_{SS}-0.3$ | - | 0.8 | V |
| $V_{IH(NRST)}^{(1)}$ | NRST input high level voltage | | 2 | - | $V_{DD}+0.3$ | |
| $V_{IL(NRST)}^{(1)}$ | NRST input low level voltage | CMOS ports $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | $V_{SS}-0.3$ | - | $0.3V_{DD}$ | V |
| $V_{IH(NRST)}^{(1)}$ | NRST input high level voltage | | $0.7V_{DD}$ | - | $V_{DD}+0.3$ | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | - | 200 | - | mV |
| R_{PU} | Weak pull-up equivalent resistor ⁽²⁾ | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | k Ω |
| $V_{F(NRST)}^{(1)}$ | NRST Input filtered pulse | | - | - | 100 | ns |
| $V_{NF(NRST)}^{(1)}$ | NRST Input not filtered pulse | $V_{DD} > 2.7\text{ V}$ | 300 | - | - | ns |
| T_{NRST_OUT} | Generated reset pulse duration | Internal Reset source | 20 | - | - | μs |

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 37. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 47](#). Otherwise the reset is not taken into account by the device.

5.3.18 TIM timer characteristics

The parameters given in [Table 48](#) and [Table 49](#) are guaranteed by design.

Refer to [Section 5.3.16: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 48. Characteristics of TIMx connected to the APB1 domain⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------------|---|--|--------|----------------------|---------------|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APB1 prescaler distinct from 1, $f_{TIMxCLK} = 60$ MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 16.7 | - | ns |
| | | AHB/APB1 prescaler = 1, $f_{TIMxCLK} = 30$ MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 33.3 | - | ns |
| f_{EXT} | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK} = 60$ MHz APB1 = 30 MHz | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | | 0 | 30 | MHz |
| Res _{TIM} | Timer resolution | | - | 16/32 | bit |
| | | | 1 | 65536 | $t_{TIMxCLK}$ |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | | 0.0167 | 1092 | μ s |
| | | | 1 | - | $t_{TIMxCLK}$ |
| | 32-bit counter clock period when internal clock is selected | | 0.0167 | 71582788 | μ s |
| | | | - | 65536×65536 | $t_{TIMxCLK}$ |
| t_{MAX_COUNT} | Maximum possible count | - | 71.6 | s | |
| | | - | - | - | |

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.

Table 49. Characteristics of TIMx connected to the APB2 domain⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---|--|--------|----------------------|---------------|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APB2 prescaler distinct from 1, $f_{TIMxCLK} = 120\text{ MHz}$ | 1 | - | $t_{TIMxCLK}$ |
| | | | 8.3 | - | ns |
| | | AHB/APB2 prescaler = 1, $f_{TIMxCLK} = 60\text{ MHz}$ | 1 | - | $t_{TIMxCLK}$ |
| | | | 16.7 | - | ns |
| f_{EXT} | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK} = 120\text{ MHz}$ $APB2 = 60\text{ MHz}$ | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | | 0 | 60 | MHz |
| Res_{TIM} | Timer resolution | | - | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | | 0.0083 | 546 | μs |
| t_{MAX_COUNT} | Maximum possible count | | - | 65536×65536 | $t_{TIMxCLK}$ |
| | | - | 35.79 | s | |

1. TIMx is used as a general term to refer to the TIM1, TIM8, TIM9, TIM10, and TIM11 timers.

5.3.19 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in [Table 50](#) are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in [Table 12](#).

STM32F205xx and STM32F207xx I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

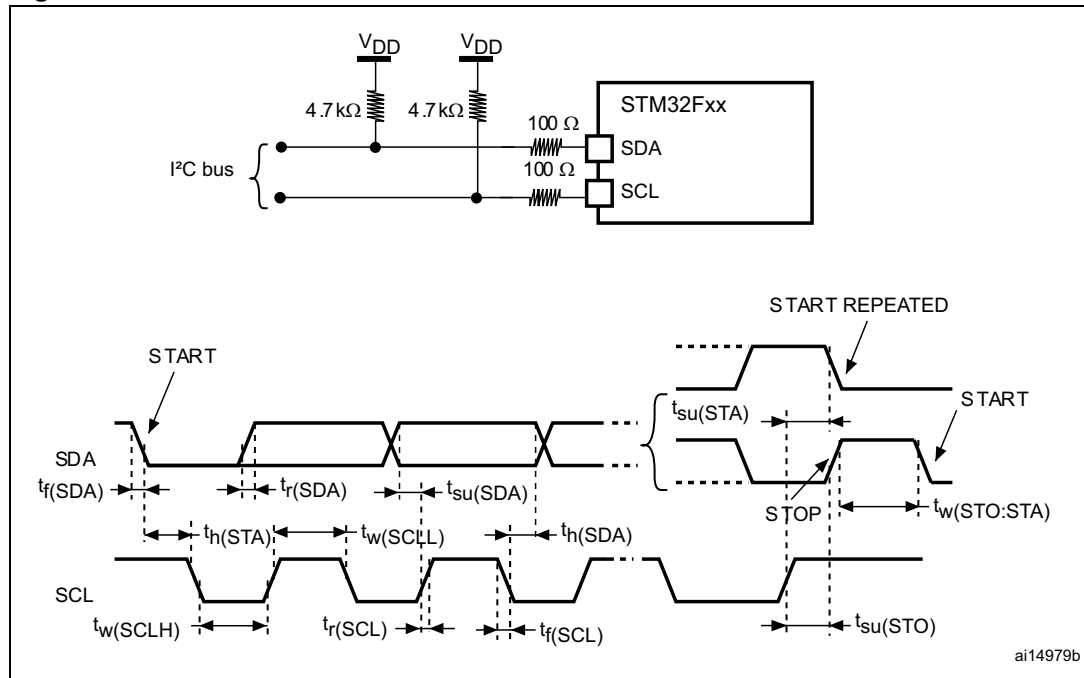
The I²C characteristics are described in [Table 50](#). Refer also to [Section 5.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 50. I²C characteristics

| Symbol | Parameter | Standard mode I ² C ⁽¹⁾ | | Fast mode I ² C ⁽¹⁾⁽²⁾ | | Unit |
|--|---|---|------|--|--------------------|------|
| | | Min | Max | Min | Max | |
| t _{w(SCLL)} | SCL clock low time | 4.7 | - | 1.3 | - | μs |
| t _{w(SCLH)} | SCL clock high time | 4.0 | - | 0.6 | - | |
| t _{su(SDA)} | SDA setup time | 250 | - | 100 | - | ns |
| t _{h(SDA)} | SDA data hold time | 0 | - | 0 | 900 ⁽³⁾ | |
| t _{r(SDA)} t _{r(SCL)} | SDA and SCL rise time | - | 1000 | 20 + 0.1C _b | 300 | |
| t _{f(SDA)} t _{f(SCL)} | SDA and SCL fall time | - | 300 | - | 300 | |
| t _{h(STA)} | Start condition hold time | 4.0 | - | 0.6 | - | μs |
| t _{su(STA)} | Repeated Start condition setup time | 4.7 | - | 0.6 | - | |
| t _{su(STO)} | Stop condition setup time | 4.0 | - | 0.6 | - | μs |
| t _{w(STO:STA)} | Stop to Start condition time (bus free) | 4.7 | - | 1.3 | - | μs |
| C _b | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. Guaranteed by design, not tested in production.
2. f_{CLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of the SCL signal.

Figure 38. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 51. SCL frequency ($f_{PCLK1} = 30 \text{ MHz}, V_{DD} = 3.3 \text{ V}$)⁽¹⁾⁽²⁾

| f _{SCL} (kHz) | I2C_CCR value |
|------------------------|-------------------------|
| | R _p = 4.7 kΩ |
| 400 | 0x8019 |
| 300 | 0x8021 |
| 200 | 0x8032 |
| 100 | 0x0096 |
| 50 | 0x012C |
| 20 | 0x02EE |

1. R_p = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I²S - SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 52](#) for SPI or in [Table 53](#) for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 12](#).

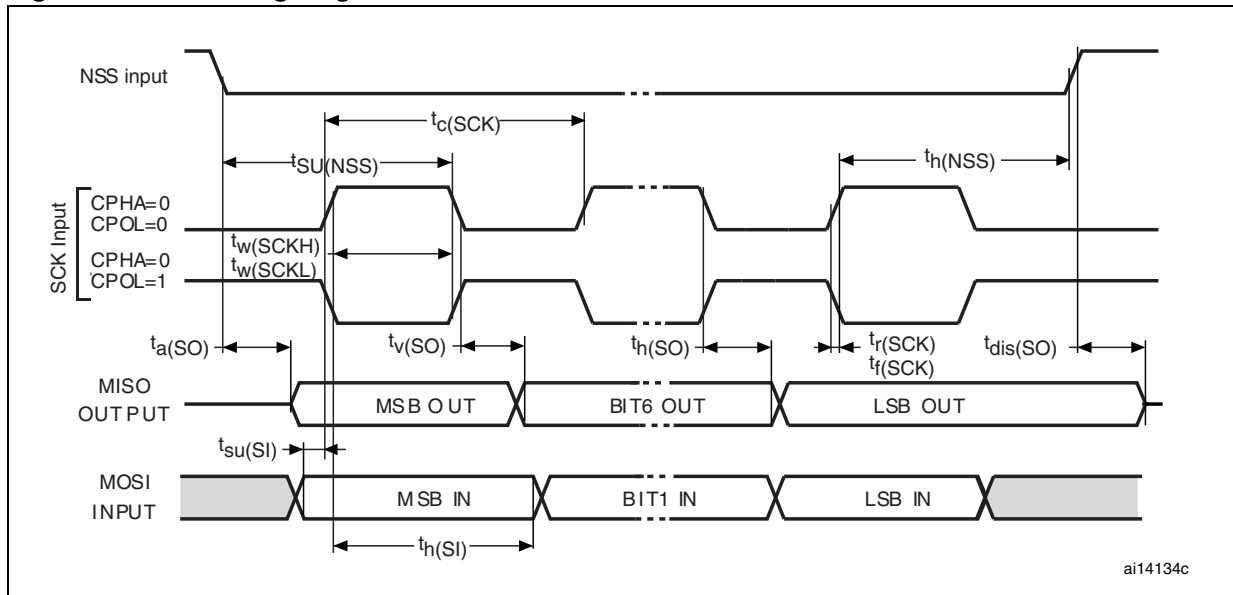
Refer to [Section 5.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 52. SPI characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|----------------------------------|--|--------------|--------------|------|
| f_{SCK} $1/t_{c(SCK)}$ | SPI clock frequency | SPI1 master/slave mode | - | 30 | MHz |
| | | SPI2/SPI3 master/slave mode | - | 15 | |
| $t_{r(SCL)}$ $t_{f(SCL)}$ | SPI clock rise and fall time | Capacitive load: $C = 30$ pF, $f_{PCLK} = 30$ MHz | - | 8 | ns |
| $DuCy(SCK)$ | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}^{(1)}$ | NSS setup time | Slave mode | $4t_{PCLK}$ | - | ns |
| $t_{h(NSS)}^{(1)}$ | NSS hold time | Slave mode | $2t_{PCLK}$ | - | |
| $t_{w(SCLH)}^{(1)}$ $t_{w(SCLL)}^{(1)}$ | SCK high and low time | Master mode, $f_{PCLK} = 30$ MHz, presc = 2 | $t_{PCLK}-3$ | $t_{PCLK}+3$ | |
| $t_{su(MI)}^{(1)}$ $t_{su(SI)}^{(1)}$ | Data input setup time | Master mode | 5 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}^{(1)}$ $t_{h(SI)}^{(1)}$ | Data input hold time | Master mode | 5 | - | |
| | | Slave mode | 4 | - | |
| $t_{a(SO)}^{(1)(2)}$ | Data output access time | Slave mode, $f_{PCLK} = 30$ MHz | 0 | $3t_{PCLK}$ | |
| $t_{dis(SO)}^{(1)(3)}$ | Data output disable time | Slave mode | 2 | 10 | |
| $t_{v(SO)}^{(1)}$ | Data output valid time | Slave mode (after enable edge) | - | 25 | |
| $t_{v(MO)}^{(1)}$ | Data output valid time | Master mode (after enable edge) | - | 5 | |
| $t_{h(SO)}^{(1)}$ $t_{h(MO)}^{(1)}$ | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| | | Master mode (after enable edge) | 2 | - | |

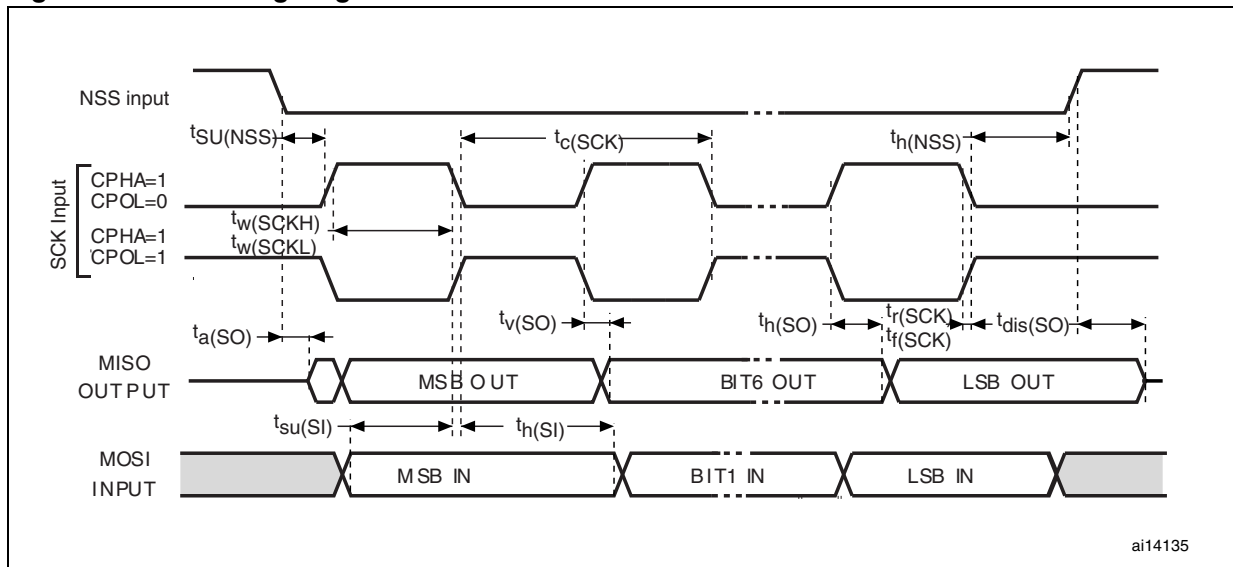
1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 39. SPI timing diagram - slave mode and CPHA = 0



ai14134c

Figure 40. SPI timing diagram - slave mode and CPHA = 1



ai14135

Figure 41. SPI timing diagram - master mode

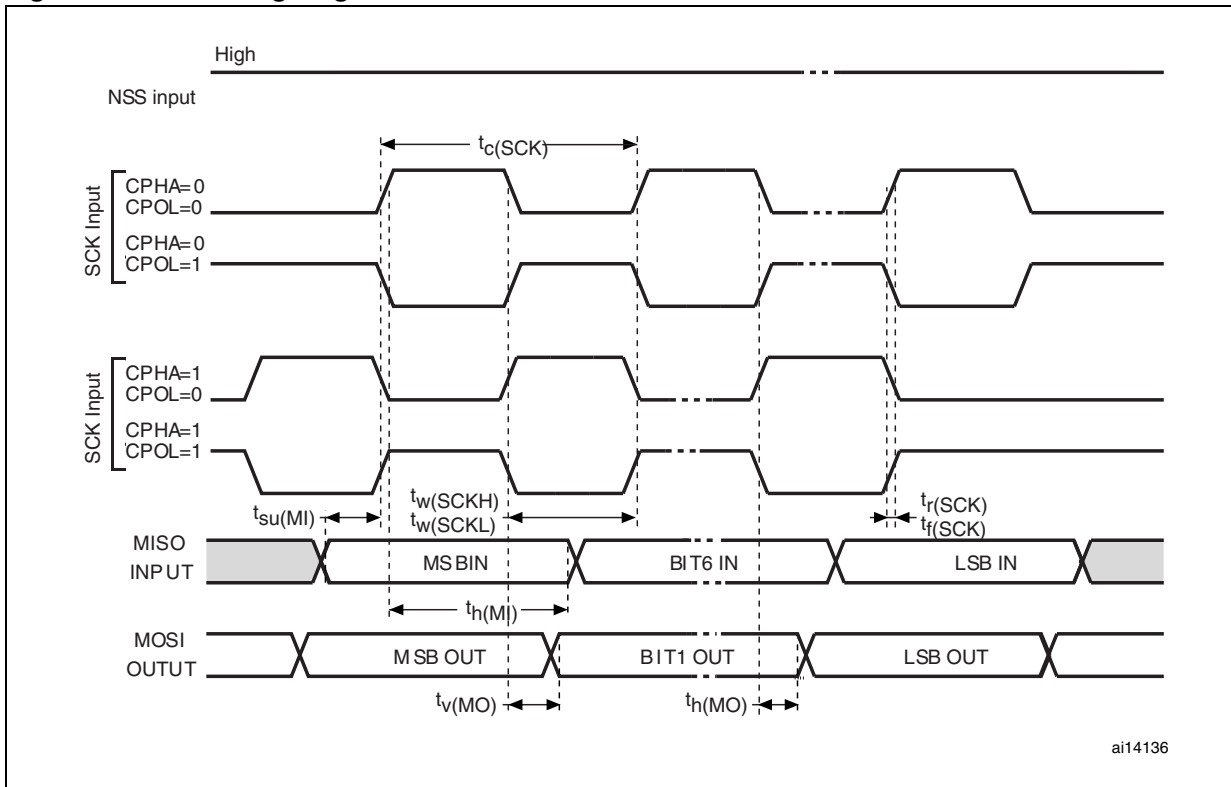
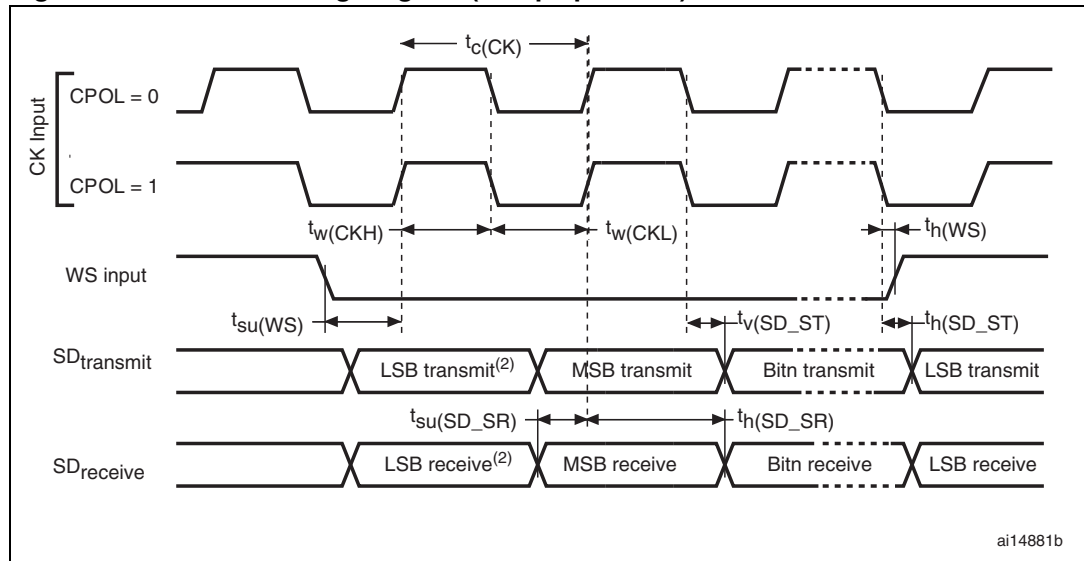


Table 53. I²S characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|---|--|---------|---------------|------|
| f_{CK} $1/t_{c(CK)}$ | I ² S clock frequency | Master, 16-bit data, audio frequency = 48 kHz, main clock disabled | 1.23 | 1.24 | MHz |
| | | Slave | 0 | $64F_S^{(1)}$ | |
| $t_{r(CK)}$ $t_{f(CK)}$ | I ² S clock rise and fall time | capacitive load $C_L = 50$ pF | - | (2) | ns |
| $t_{V(WS)}^{(3)}$ | WS valid time | Master | 0.3 | - | |
| $t_{h(WS)}^{(3)}$ | WS hold time | Master | 0 | - | |
| $t_{su(WS)}^{(3)}$ | WS setup time | Slave | 3 | - | |
| $t_{h(WS)}^{(3)}$ | WS hold time | Slave | 0 | - | |
| $t_{w(CKH)}^{(3)}$ $t_{w(CKL)}^{(3)}$ | CK high and low time | Master $f_{PCLK} = 30$ MHz | 396 | - | |
| $t_{su(SD_MR)}^{(3)}$ $t_{su(SD_SR)}^{(3)}$ | Data input setup time | Master receiver Slave receiver | 45 0 | - | |
| $t_{h(SD_MR)}^{(3)(4)}$ $t_{h(SD_SR)}^{(3)(4)}$ | Data input hold time | Master receiver: $f_{PCLK} = 30$ MHz, Slave receiver: $f_{PCLK} = 30$ MHz | 13 0 | - | |
| $t_{V(SD_ST)}^{(3)(4)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 30 | |
| $t_{h(SD_ST)}^{(3)}$ | Data output hold time | Slave transmitter (after enable edge) | 10 | - | |
| $t_{V(SD_MT)}^{(3)(4)}$ | Data output valid time | Master transmitter (after enable edge) | - | 6 | |
| $t_{h(SD_MT)}^{(3)}$ | Data output hold time | Master transmitter (after enable edge) | 0 | - | |

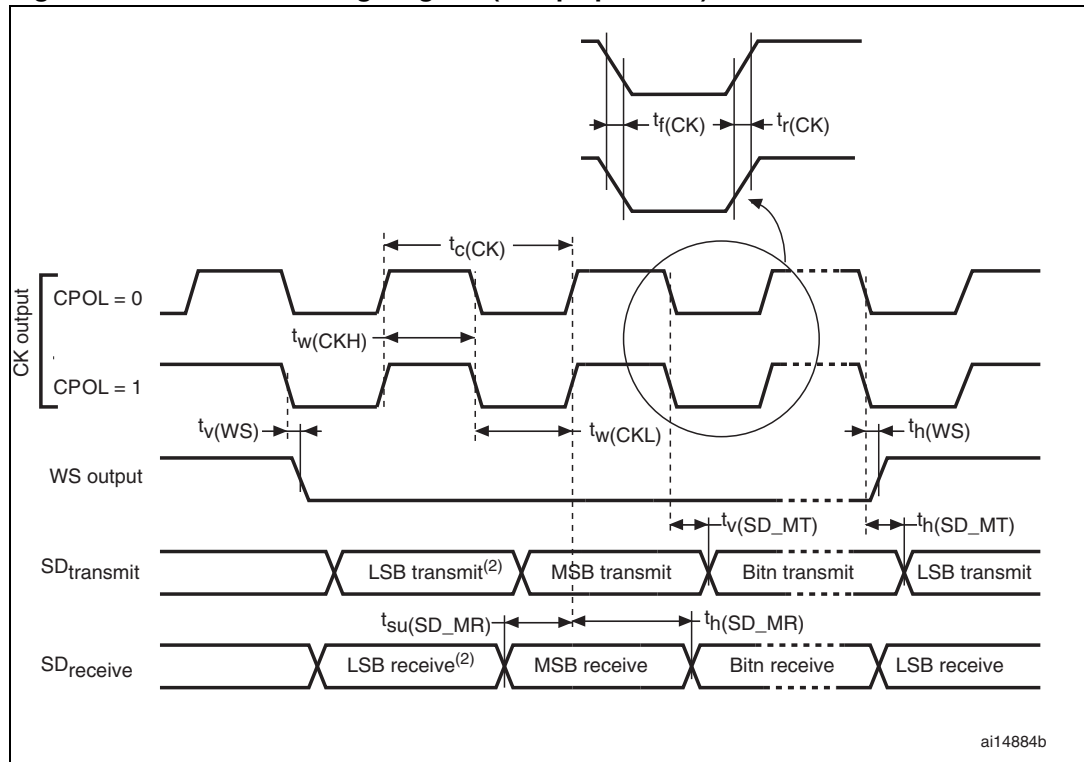
- F_S is the sampling frequency. Refer to the I²S section of the STM32F20xxx/21xxx reference manual for more details. f_{CK} values reflect only the digital peripheral behavior which leads to a minimum of $(I2SDIV/(2*I2SDIV+ODD))$, a maximum of $(I2SDIV+ODD)/(2*I2SDIV+ODD)$ and F_S maximum values for each mode/condition.
- Refer to [Table 46: I/O AC characteristics](#).
- Based on design simulation and/or characterization results, not tested in production.
- Depends on f_{PCLK} . For example, if $f_{PCLK} = 8$ MHz, then $T_{PCLK} = 1/f_{PCLK} = 125$ ns.

Figure 42. I²S slave timing diagram (Philips protocol)⁽¹⁾



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 43. I²S master timing diagram (Philips protocol)⁽¹⁾



1. Based on characterization, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 54. USB OTG FS startup time

| Symbol | Parameter | Max | Unit |
|---------------------|-------------------------------------|-----|---------|
| $t_{STARTUP}^{(1)}$ | USB OTG FS transceiver startup time | 1 | μs |

1. Guaranteed by design, not tested in production.

Table 55. USB OTG FS DC electrical characteristics

| Symbol | Parameter | Conditions | Min. ⁽¹⁾ | Typ. | Max. ⁽¹⁾ | Unit | |
|---------------|---|---------------------------------|---|------|---------------------|------------|---|
| Input levels | V_{DD} | USB OTG FS operating voltage | 3.0 ⁽²⁾ | - | 3.6 | V | |
| | $V_{DI}^{(3)}$ | Differential input sensitivity | I(USB_FS_DP/DM, USB_HS_DP/DM) | 0.2 | - | - | V |
| | $V_{CM}^{(3)}$ | Differential common mode range | Includes V_{DI} range | 0.8 | - | 2.5 | |
| | $V_{SE}^{(3)}$ | Single ended receiver threshold | | 1.3 | - | 2.0 | |
| Output levels | V_{OL} | Static output level low | R_L of 1.5 k Ω to 3.6 V ⁽⁴⁾ | - | - | 0.3 | V |
| | V_{OH} | Static output level high | R_L of 15 k Ω to $V_{SS}^{(4)}$ | 2.8 | - | 3.6 | |
| R_{PD} | PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM) | $V_{IN} = V_{DD}$ | 17 | 21 | 24 | k Ω | |
| | PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS) | | 0.65 | 1.1 | 2.0 | | |
| R_{PU} | PA12, PB15 (USB_FS_DP, USB_HS_DP) | $V_{IN} = V_{SS}$ | 1.5 | 1.8 | 2.1 | | |
| | PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS) | $V_{IN} = V_{SS}$ | 0.25 | 0.37 | 0.55 | | |

1. All the voltages are measured from the local ground potential.
2. The STM32F205xx and STM32F207xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers

Figure 44. USB OTG FS timings: definition of data signal rise and fall time

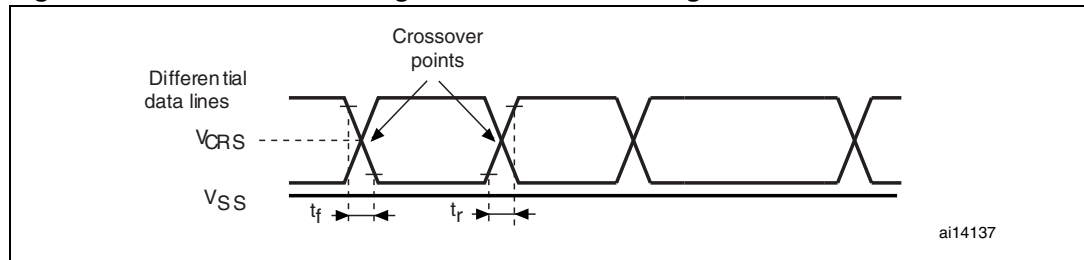


Table 56. USB OTG FS electrical characteristics⁽¹⁾

| Driver characteristics | | | | | |
|------------------------|---------------------------------|-----------------------|-----|-----|------|
| Symbol | Parameter | Conditions | Min | Max | Unit |
| t_r | Rise time ⁽²⁾ | $C_L = 50 \text{ pF}$ | 4 | 20 | ns |
| t_f | Fall time ⁽²⁾ | $C_L = 50 \text{ pF}$ | 4 | 20 | ns |
| t_{rfm} | Rise/ fall time matching | t_r/t_f | 90 | 110 | % |
| V_{CRS} | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

[Table 57](#) shows the USB HS operating voltage.

Table 57. USB HS DC electrical characteristics

| Symbol | Parameter | Min. ⁽¹⁾ | Max. ⁽¹⁾ | Unit |
|-------------|---------------------------------------|---------------------|---------------------|------|
| Input level | V_{DD} USB OTG HS operating voltage | 2.7 | 3.6 | V |

1. All the voltages are measured from the local ground potential.

Table 58. Clock timing parameters

| Parameter ⁽¹⁾ | | Symbol | Min | Nominal | Max | Unit |
|--|-----------------------|-------------------|--------|---------|--------|---------------|
| Frequency (first transition) | 8-bit $\pm 10\%$ | F_{START_8BIT} | 54 | 60 | 66 | MHz |
| Frequency (steady state) | $\pm 500 \text{ ppm}$ | F_{STEADY} | 59.97 | 60 | 60.03 | MHz |
| Duty cycle (first transition) | 8-bit $\pm 10\%$ | D_{START_8BIT} | 40 | 50 | 60 | % |
| Duty cycle (steady state) | $\pm 500 \text{ ppm}$ | D_{STEADY} | 49.975 | 50 | 50.025 | % |
| Time to reach the steady state frequency and duty cycle after the first transition | | T_{STEADY} | - | - | 1.4 | ms |
| Clock startup time after the de-assertion of SuspendM | Peripheral | T_{START_DEV} | - | - | 5.6 | ms |
| | Host | T_{START_HOST} | - | - | - | |
| PHY preparation time after the first transition of the input clock | | T_{PREP} | - | - | - | μs |

1. Guaranteed by design, not tested in production.

Figure 45. ULPI timing diagram

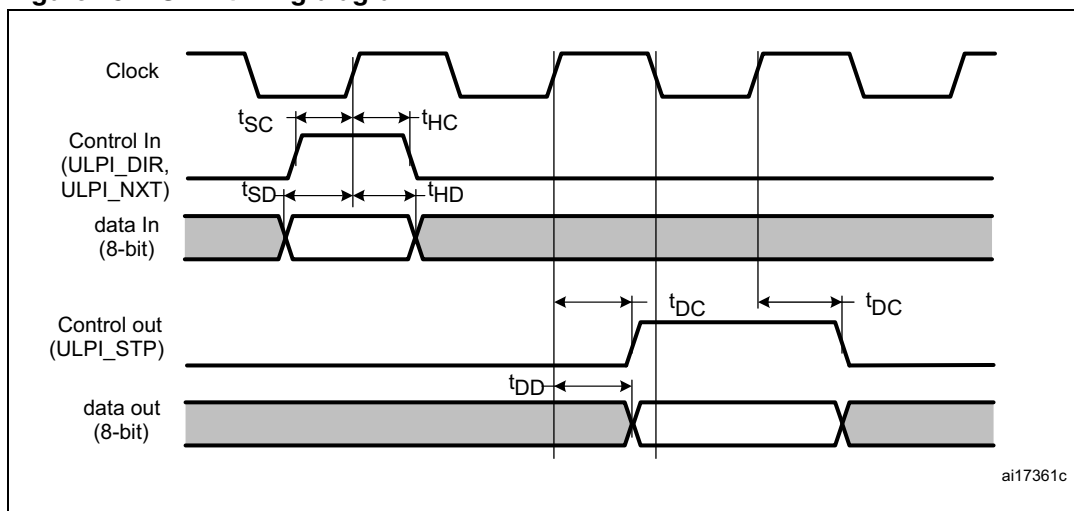


Table 59. ULPI timing

| Symbol | Parameter | Value ⁽¹⁾ | | Unit |
|-----------------|---|----------------------|------|------|
| | | Min. | Max. | |
| t _{SC} | Control in (ULPI_DIR) setup time | - | 2.0 | ns |
| | Control in (ULPI_NXT) setup time | - | 1.5 | |
| t _{HC} | Control in (ULPI_DIR, ULPI_NXT) hold time | 0 | - | |
| t _{SD} | Data in setup time | - | 2.0 | |
| t _{HD} | Data in hold time | 0 | - | |
| t _{DC} | Control out (ULPI_STP) setup time and hold time | - | 9.2 | |
| t _{DD} | Data out available from clock rising edge | - | 10.7 | |

1. V_{DD} = 2.7 V to 3.6 V and T_A = -40 to 85 °C.

Ethernet characteristics

Table 60 shows the Ethernet operating voltage.

Table 60. Ethernet DC electrical characteristics

| Symbol | Parameter | Min. ⁽¹⁾ | Max. ⁽¹⁾ | Unit |
|-------------|-----------------|---------------------|---------------------|------|
| Input level | V _{DD} | 2.7 | 3.6 | V |

1. All the voltages are measured from the local ground potential.

Table 61 gives the list of Ethernet MAC signals for the SMI (station management interface) and Figure 46 shows the corresponding timing diagram.

Figure 46. Ethernet SMI timing diagram

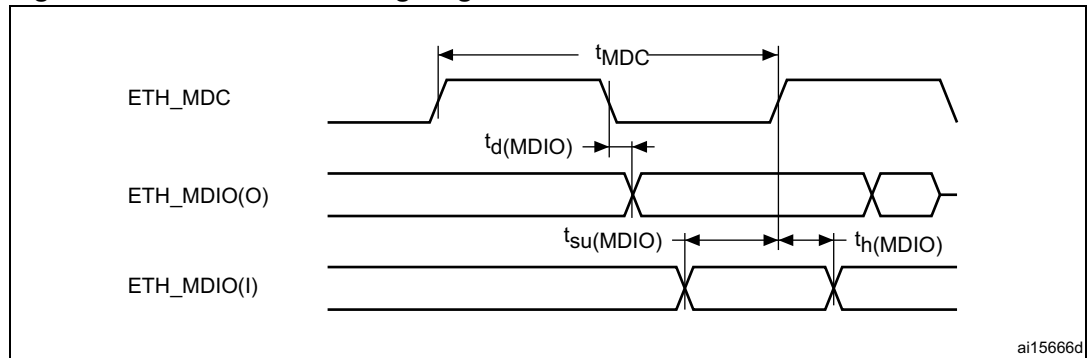


Table 61. Dynamics characteristics: Ethernet MAC signals for SMI

| Symbol | Rating | Min | Typ | Max | Unit |
|----------------|----------------------------|-----|-----|-----|------|
| t_{MDC} | MDC cycle time (2.38 MHz) | 411 | 420 | 425 | ns |
| $t_d(MDIO)$ | MDIO write data valid time | 6 | 10 | 13 | ns |
| $t_{su}(MDIO)$ | Read data setup time | 12 | - | - | ns |
| $t_h(MDIO)$ | Read data hold time | 0 | - | - | ns |

Table 62 gives the list of Ethernet MAC signals for the RMII and Figure 47 shows the corresponding timing diagram.

Figure 47. Ethernet RMII timing diagram

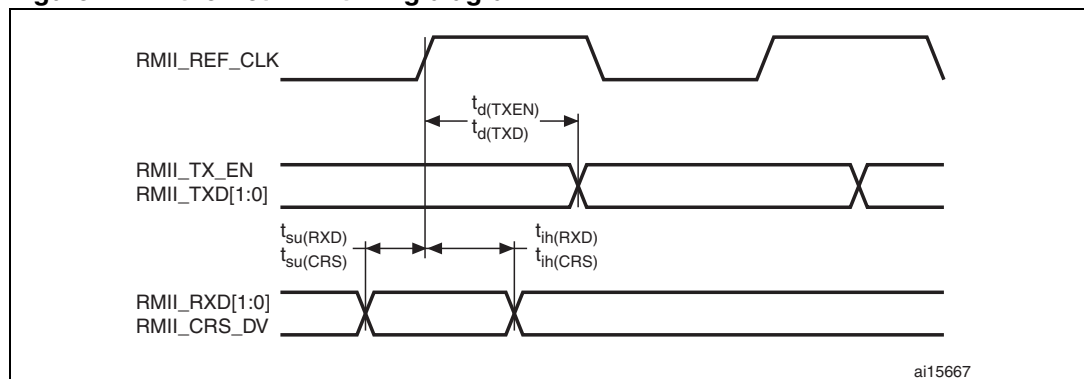


Table 62. Dynamics characteristics: Ethernet MAC signals for RMII

| Symbol | Rating | Min | Typ | Max | Unit |
|---------------|----------------------------------|-----|------|-----|------|
| $t_{su}(RXD)$ | Receive data setup time | 1 | - | - | ns |
| $t_h(RXD)$ | Receive data hold time | 1.5 | - | - | |
| $t_{su}(CRS)$ | Carrier sense set-up time | 0 | - | - | |
| $t_h(CRS)$ | Carrier sense hold time | 2 | - | - | |
| $t_d(TXEN)$ | Transmit enable valid delay time | 9 | 11 | 13 | |
| $t_d(TXD)$ | Transmit data valid delay time | 9 | 11.5 | 14 | |

Table 63 gives the list of Ethernet MAC signals for MII and Figure 47 shows the corresponding timing diagram.

Figure 48. Ethernet MII timing diagram

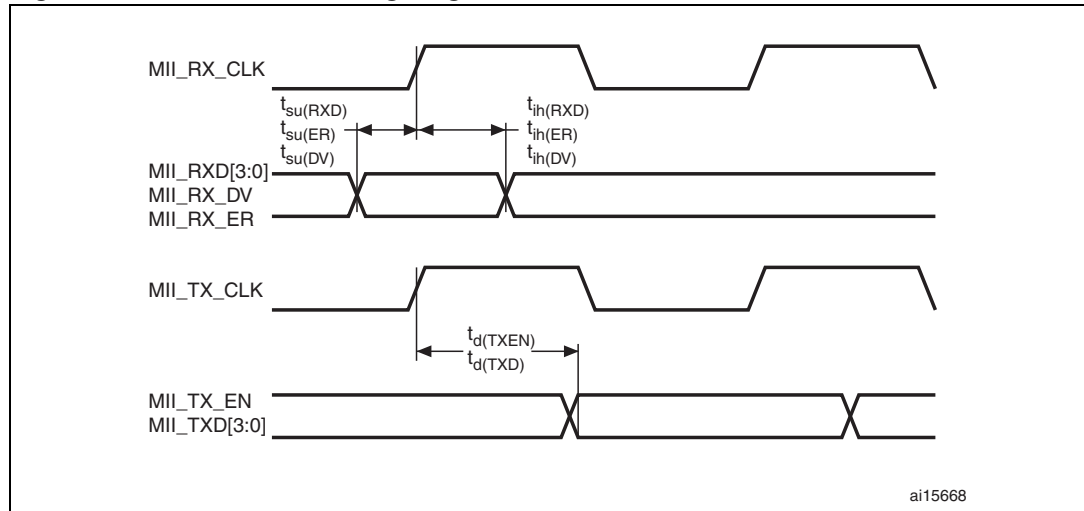


Table 63. Dynamics characteristics: Ethernet MAC signals for MII

| Symbol | Rating | Min | Typ | Max | Unit |
|---------------|----------------------------------|-----|-----|-----|------|
| $t_{su}(RXD)$ | Receive data setup time | 7.5 | - | - | ns |
| $t_{oh}(RXD)$ | Receive data hold time | 1 | - | - | ns |
| $t_{su}(DV)$ | Data valid setup time | 4 | - | - | ns |
| $t_{oh}(DV)$ | Data valid hold time | 0 | - | - | ns |
| $t_{su}(ER)$ | Error setup time | 3.5 | - | - | ns |
| $t_{oh}(ER)$ | Error hold time | 0 | - | - | ns |
| $t_d(TXEN)$ | Transmit enable valid delay time | - | 11 | 14 | ns |
| $t_d(TXD)$ | Transmit data valid delay time | - | 11 | 14 | ns |

CAN (controller area network) interface

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 64](#) are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 12](#).

Table 64. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|---|---|---|-----|------------------|--------------|
| V_{DDA} | Power supply | | 1.8 ⁽¹⁾ | - | 3.6 | V |
| V_{REF+} | Positive reference voltage | | 1.8 ⁽¹⁾⁽²⁾ | - | V_{DDA} | V |
| f_{ADC} | ADC clock frequency | $V_{DDA} = 1.8^{(1)}$ to 2.4 V | 0.6 | - | 15 | MHz |
| | | $V_{DDA} = 2.4$ to 3.6 V | 0.6 | - | 30 | MHz |
| $f_{TRIG}^{(3)}$ | External trigger frequency | $f_{ADC} = 30$ MHz with 12-bit resolution | - | - | 1764 | kHz |
| | | | - | - | 17 | 1/ f_{ADC} |
| V_{AIN} | Conversion voltage range ⁽⁴⁾ | | 0 (V_{SSA} or V_{REF-} tied to ground) | - | V_{REF+} | V |
| $R_{AIN}^{(3)}$ | External input impedance | See Equation 1 for details | - | - | 50 | k Ω |
| $R_{ADC}^{(3)(5)}$ | Sampling switch resistance | | 1.5 | - | 6 | k Ω |
| $C_{ADC}^{(3)}$ | Internal sample and hold capacitor | | - | 4 | - | pF |
| $t_{lat}^{(3)}$ | Injection trigger conversion latency | $f_{ADC} = 30$ MHz | - | - | 0.100 | μ s |
| | | | - | - | 3 ⁽⁶⁾ | 1/ f_{ADC} |
| $t_{latr}^{(3)}$ | Regular trigger conversion latency | $f_{ADC} = 30$ MHz | - | - | 0.067 | μ s |
| | | | - | - | 2 ⁽⁶⁾ | 1/ f_{ADC} |
| $t_S^{(3)}$ | Sampling time | $f_{ADC} = 30$ MHz | 0.100 | - | 16 | μ s |
| | | | 3 | - | 480 | 1/ f_{ADC} |
| $t_{STAB}^{(3)}$ | Power-up time | | - | 2 | 3 | μ s |
| $t_{CONV}^{(3)}$ | Total conversion time (including sampling time) | $f_{ADC} = 30$ MHz 12-bit resolution | 0.5 | - | 16.40 | μ s |
| | | $f_{ADC} = 30$ MHz 10-bit resolution | 0.43 | - | 16.34 | μ s |
| | | $f_{ADC} = 30$ MHz 8-bit resolution | 0.37 | - | 16.27 | μ s |
| | | $f_{ADC} = 30$ MHz 6-bit resolution | 0.3 | - | 16.20 | μ s |
| | | 9 to 492 (t_S for sampling +n-bit resolution for successive approximation) | | | | |

Table 64. ADC characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|---|--|-----|-----|------|---------------|
| $f_S^{(3)}$ | Sampling rate ($f_{ADC} = 30 \text{ MHz}$) | 12-bit resolution Single ADC | - | - | 2 | Msp/s |
| | | 12-bit resolution Interleave Dual ADC mode | - | - | 3.75 | Msp/s |
| | | 12-bit resolution Interleave Triple ADC mode | - | - | 6 | Msp/s |
| $I_{VREF+}^{(3)}$ | ADC V_{REF} DC current consumption in conversion mode | $f_{ADC} = 30 \text{ MHz}$ 3 sampling time 12-bit resolution | - | 300 | 500 | μA |
| | | $f_{ADC} = 30 \text{ MHz}$ 480 sampling time 12-bit resolution | - | - | 16 | μA |
| $I_{VDDA}^{(3)}$ | ADC V_{DDA} DC current consumption in conversion mode | $f_{ADC} = 30 \text{ MHz}$ 3 sampling time 12-bit resolution | - | 1.6 | 1.8 | mA |
| | | $f_{ADC} = 30 \text{ MHz}$ 480 sampling time 12-bit resolution | - | - | 60 | μA |

1. If IRROFF is set to V_{DD} , this value can be lowered to 1.7 V when the device operates in the 0 to 70 °C temperature range.
2. It is recommended to maintain the voltage difference between V_{REF+} and V_{DDA} below 1.8 V.
3. Based on characterization, not tested in production.
4. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA} .
5. R_{ADC} maximum value is given for $V_{DD}=1.8 \text{ V}$, and minimum value for $V_{DD}=3.3 \text{ V}$.
6. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 64](#).

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. $N = 12$ (from 12-bit resolution) and k is the number of sampling periods defined in the `ADC_SMPR1` register.

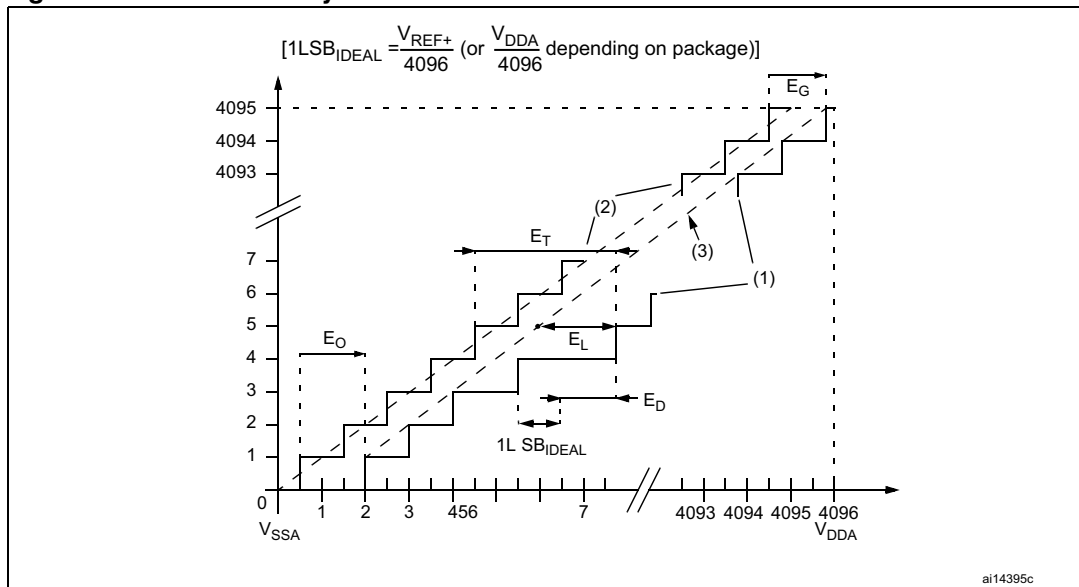
Table 65. ADC accuracy (1)

| Symbol | Parameter | Test conditions | Typ | Max ⁽²⁾ | Unit |
|--------|------------------------------|---|-----------|--------------------|------|
| ET | Total unadjusted error | $f_{PCLK2} = 60 \text{ MHz}$, $f_{ADC} = 30 \text{ MHz}$, $R_{AIN} < 10 \text{ k}\Omega$, $V_{DDA} = 1.8^{(3)}$ to 3.6 V | ± 2 | ± 5 | LSB |
| EO | Offset error | | ± 1.5 | ± 2.5 | |
| EG | Gain error | | ± 1.5 | ± 3 | |
| ED | Differential linearity error | | ± 1 | ± 2 | |
| EL | Integral linearity error | | ± 1.5 | ± 3 | |

1. Better performance could be achieved in restricted V_{DD} , frequency and temperature ranges.
2. Based on characterization, not tested in production.
3. If IRROFF is set to V_{DD} , this value can be lowered to 1.7 V when the device operates in the 0 to 70 °C temperature range.

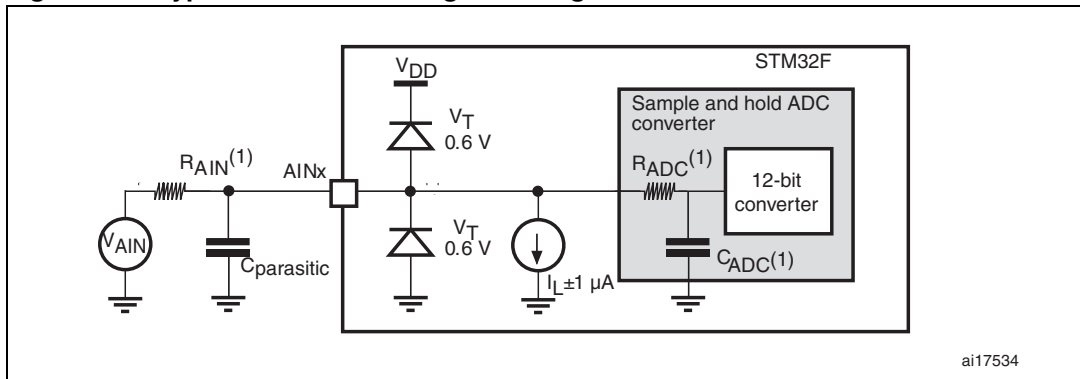
Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 5.3.16](#) does not affect the ADC accuracy.

Figure 49. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
 E_O = Offset Error: deviation between the first actual transition and the first ideal one.
 E_G = Gain Error: deviation between the last ideal transition and the last actual one.
 E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
 E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 50. Typical connection diagram using the ADC

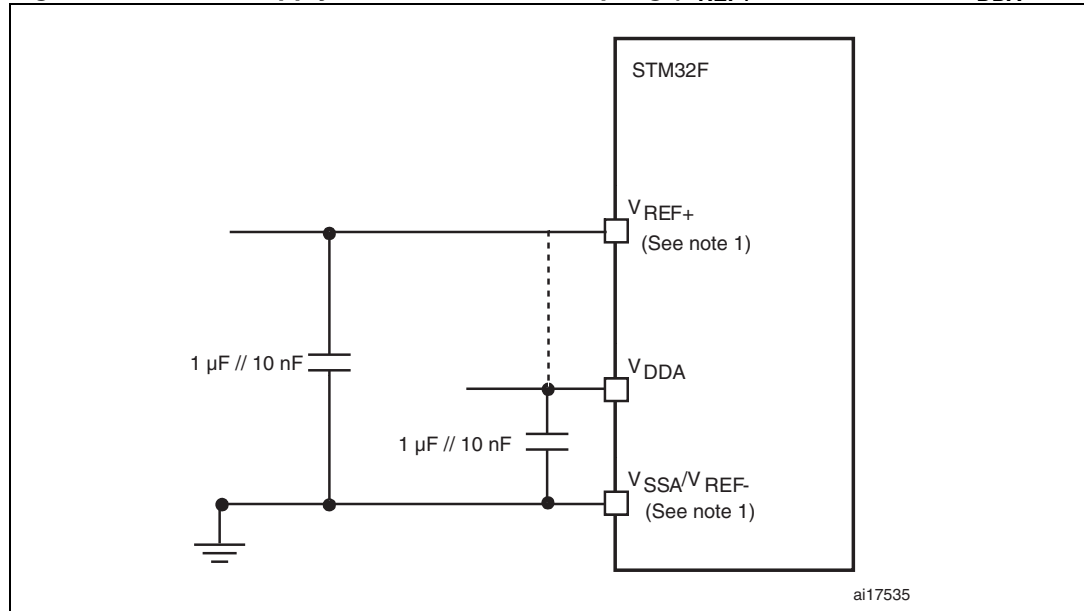


1. Refer to [Table 64](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

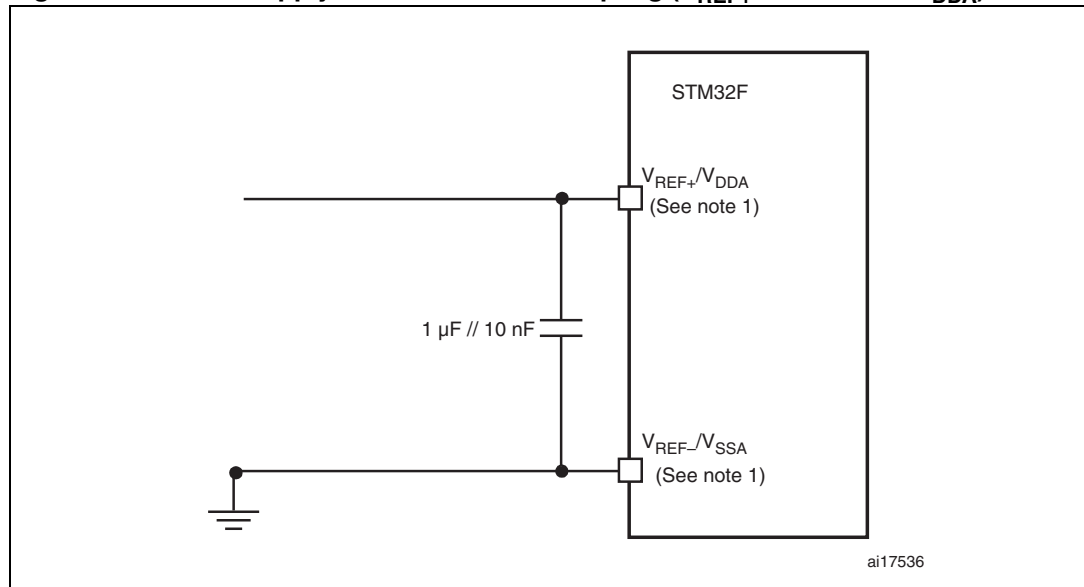
Power supply decoupling should be performed as shown in *Figure 51* or *Figure 52*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 51. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176 package. V_{REF+} is also available on all packages except for LQFP64. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

5.3.21 DAC electrical characteristics

Table 66. DAC characteristics

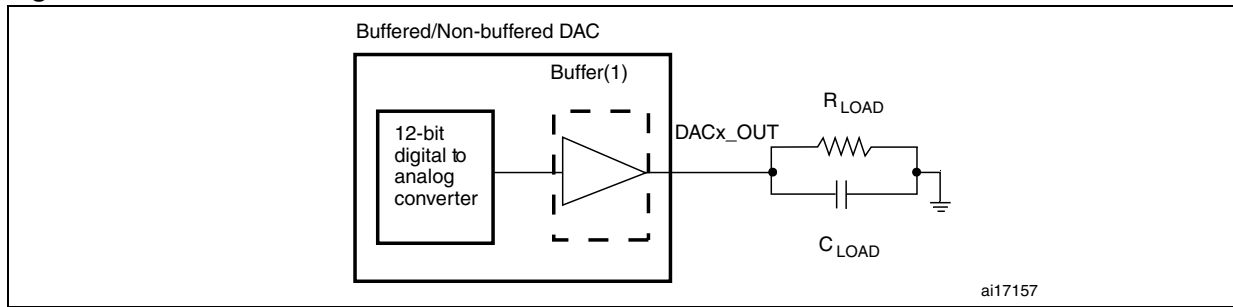
| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|----------------------------|---|--------------------|-----|-------------------|------------|--|
| V_{DDA} | Analog supply voltage | 1.8 ⁽¹⁾ | - | 3.6 | V | |
| V_{REF+} | Reference supply voltage | 1.8 ⁽¹⁾ | - | 3.6 | V | $V_{REF+} \leq V_{DDA}$ |
| V_{SSA} | Ground | 0 | - | 0 | V | |
| $R_{LOAD}^{(2)}$ | Resistive load with buffer ON | 5 | - | - | k Ω | |
| $R_O^{(2)}$ | Impedance output with buffer OFF | - | - | 15 | k Ω | When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω |
| $C_{LOAD}^{(2)}$ | Capacitive load | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min ⁽²⁾ | Lower DAC_OUT voltage with buffer ON | 0.2 | - | - | V | It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x1C7) to (0xE38) at $V_{REF+} = 1.8$ V |
| DAC_OUT max ⁽²⁾ | Higher DAC_OUT voltage with buffer ON | - | - | $V_{DDA} - 0.2$ | V | |
| DAC_OUT min ⁽²⁾ | Lower DAC_OUT voltage with buffer OFF | - | 0.5 | - | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max ⁽²⁾ | Higher DAC_OUT voltage with buffer OFF | - | - | $V_{REF+} - 1LSB$ | V | |
| $I_{VREF+}^{(4)}$ | DAC DC V_{REF} current consumption in quiescent mode (Standby mode) | - | 170 | 240 | μ A | With no load, worst code (0x800) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs |
| | | - | 50 | 75 | | With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs |
| $I_{DDA}^{(4)}$ | DAC DC V_{DDA} current consumption in quiescent mode ⁽³⁾ | - | 280 | 380 | μ A | With no load, middle code (0x800) on the inputs |
| | | - | 475 | 625 | μ A | With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs |
| DNL ⁽⁴⁾ | Differential non linearity Difference between two consecutive code-1LSB) | - | - | ± 0.5 | LSB | Given for the DAC in 10-bit configuration. |
| | | - | - | ± 2 | LSB | Given for the DAC in 12-bit configuration. |

Table 66. DAC characteristics (continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|--------------------------------------|--|-----|-----|------|------|---|
| INL ⁽⁴⁾ | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | - | - | ±1 | LSB | Given for the DAC in 10-bit configuration. |
| | | - | - | ±4 | LSB | Given for the DAC in 12-bit configuration. |
| Offset ⁽⁴⁾ | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$) | - | - | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | - | - | ±3 | LSB | Given for the DAC in 10-bit at $V_{REF+} = 3.6$ V |
| | | - | - | ±12 | LSB | Given for the DAC in 12-bit at $V_{REF+} = 3.6$ V |
| Gain error ⁽⁴⁾ | Gain error | - | - | ±0.5 | % | Given for the DAC in 12-bit configuration |
| t _{SETTLING} ⁽⁴⁾ | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB) | - | 3 | 6 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| THD ⁽⁴⁾ | Total Harmonic Distortion Buffer ON | - | - | - | dB | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| Update rate ⁽²⁾ | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| t _{WAKEUP} ⁽⁴⁾ | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. |
| PSRR ⁺ ⁽²⁾ | Power supply rejection ratio (to V _{DDA}) (static DC measurement) | - | -67 | -40 | dB | No R _{LOAD} , C _{LOAD} = 50 pF |

1. If IRROFF is set to V_{DD}, this value can be lowered to 1.7 V when the device operates in the 0 to 70 °C temperature range.
2. Guaranteed by design, not tested in production.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization, not tested in production.

Figure 53. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.22 Temperature sensor characteristics

Table 67. TS characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|--|-----|---------|---------|-----------------|
| $T_L^{(1)}$ | V_{SENSE} linearity with temperature | - | ± 1 | ± 2 | $^{\circ}C$ |
| Avg_Slope ⁽¹⁾ | Average slope | - | 2.5 | | mV/ $^{\circ}C$ |
| $V_{25}^{(1)}$ | Voltage at 25 $^{\circ}C$ | - | 0.76 | | V |
| $t_{START}^{(2)}$ | Startup time | - | 6 | 10 | μs |
| $T_{S_temp}^{(3)(2)}$ | ADC sampling time when reading the temperature 1 $^{\circ}C$ accuracy | 10 | - | - | μs |

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

5.3.23 V_{BAT} monitoring characteristics

Table 68. V_{BAT} monitoring characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------------|--|-----|-----|-----|------------|
| R | Resistor bridge for V_{BAT} | - | 50 | - | K Ω |
| Q | Ratio on V_{BAT} measurement | - | 2 | - | |
| $E_r^{(1)}$ | Error on Q | -1 | - | +1 | % |
| $T_{S_vbat}^{(2)(2)}$ | ADC sampling time when reading the V_{BAT} 1mV accuracy | 5 | - | - | μs |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.24 Embedded reference voltage

The parameters given in [Table 69](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 12](#).

Table 69. Embedded internal reference voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|--|------|------|------|-------------------------|
| V_{REFINT} | Internal reference voltage | $-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$ | 1.18 | 1.21 | 1.24 | V |
| $T_{S_vrefint}^{(1)}$ | ADC sampling time when reading the internal reference voltage | | 10 | - | - | μs |
| $V_{REFINT_s}^{(2)}$ | Internal reference voltage spread over the temperature range | $V_{DD} = 3\text{ V}$ | - | 3 | 5 | mV |
| $T_{Coeff}^{(2)}$ | Temperature coefficient | | - | 30 | 50 | ppm/ $^{\circ}\text{C}$ |
| $t_{START}^{(2)}$ | Startup time | | - | 6 | 10 | μs |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.25 FSMC characteristics

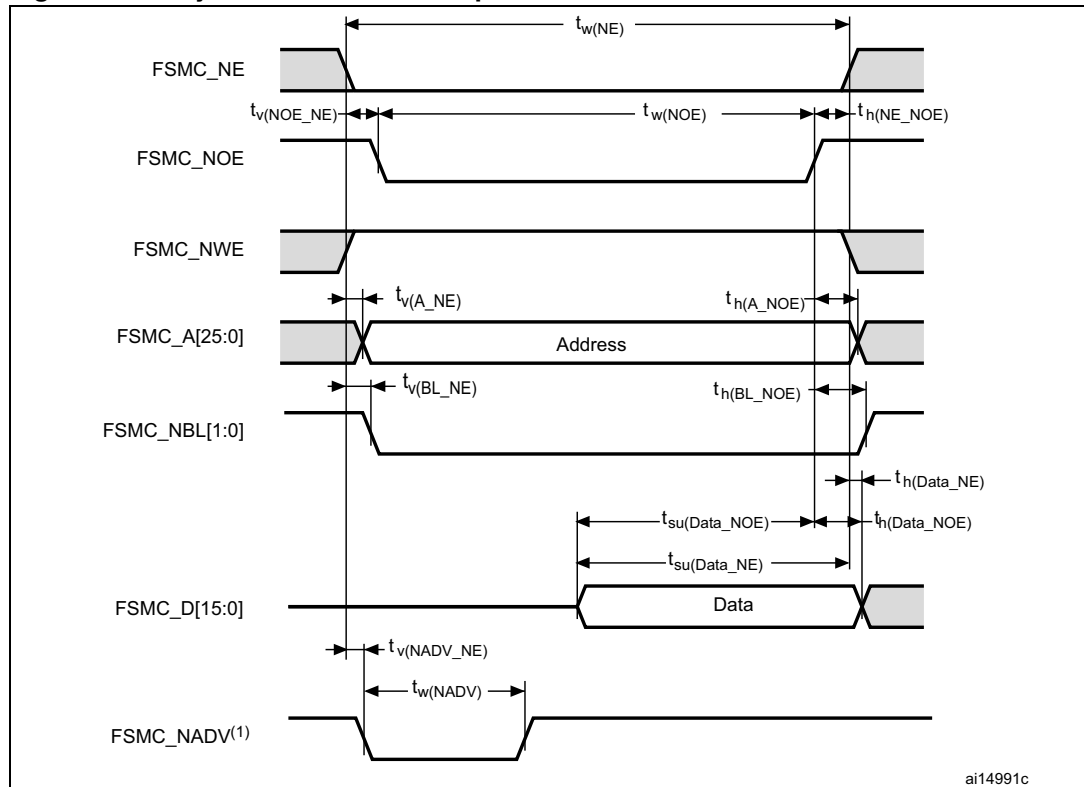
Asynchronous waveforms and timings

[Figure 54](#) through [Figure 57](#) represent asynchronous waveforms and [Table 70](#) through [Table 73](#) provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 1
- DataSetupTime = 1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 54. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

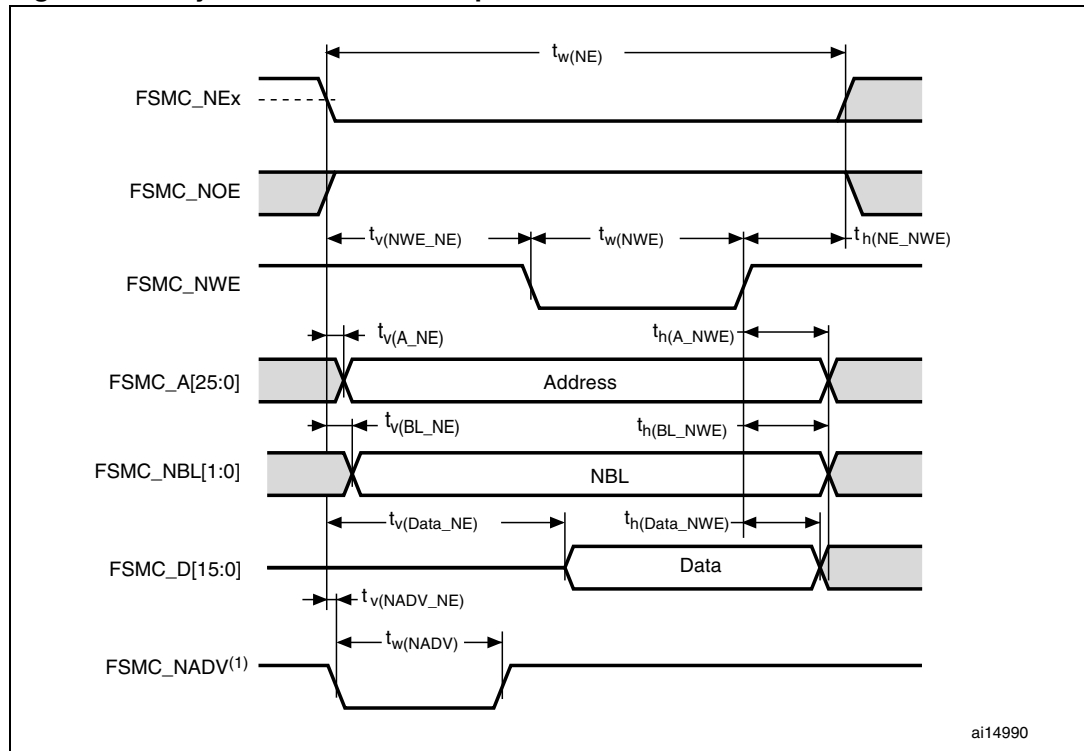
Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|---------------------|---|-------------------|-------------------|------|
| $t_{w(NE)}$ | FSMC_NE low time | $2T_{HCLK} - 0.5$ | $2T_{HCLK} + 0.5$ | ns |
| $t_{v(NOE_NE)}$ | FSMC_NEx low to FSMC_NOE low | 0.5 | 2.5 | ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | $2T_{HCLK} - 1$ | $2T_{HCLK} + 0.5$ | ns |
| $t_{h(NE_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | 0 | - | ns |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 4 | ns |
| $t_{h(A_NOE)}$ | Address hold time after FSMC_NOE high | 0 | - | ns |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | ns |
| $t_{h(BL_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | 0 | - | ns |
| $t_{su(Data_NE)}$ | Data to FSMC_NEx high setup time | $T_{HCLK} + 0.5$ | - | ns |
| $t_{su(Data_NOE)}$ | Data to FSMC_NOEx high setup time | $T_{HCLK} + 2.5$ | - | ns |
| $t_{h(Data_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | ns |
| $t_{h(Data_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | ns |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | - | 2.5 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | - | $T_{HCLK} - 0.5$ | ns |

1. $C_L = 30$ pF.

2. Based on characterization, not tested in production.

Figure 55. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|--------------------|--|------------------|------------------|------|
| $t_{w(NE)}$ | FSMC_NEx low time | $3T_{HCLK}$ | $3T_{HCLK} + 4$ | ns |
| $t_{v(NWE_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK} - 0.5$ | $T_{HCLK} + 0.5$ | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | $T_{HCLK} - 0.5$ | $T_{HCLK} + 3$ | ns |
| $t_{h(NE_NWE)}$ | FSMC_NWE high to FSMC_NEx high hold time | T_{HCLK} | - | ns |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | ns |
| $t_{h(A_NWE)}$ | Address hold time after FSMC_NWE high | $T_{HCLK} - 3$ | - | ns |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_NBL valid | - | 0.5 | ns |
| $t_{h(BL_NWE)}$ | FSMC_NBL hold time after FSMC_NWE high | $T_{HCLK} - 1$ | - | ns |
| $t_{v(Data_NE)}$ | Data to FSMC_NEx low to Data valid | - | $T_{HCLK} + 5$ | ns |
| $t_{h(Data_NWE)}$ | Data hold time after FSMC_NWE high | $T_{HCLK} + 0.5$ | - | ns |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | - | 2 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | - | $T_{HCLK} + 1.5$ | ns |

1. $C_L = 30$ pF.

2. Based on characterization, not tested in production.

Figure 56. Asynchronous multiplexed PSRAM/NOR read waveforms

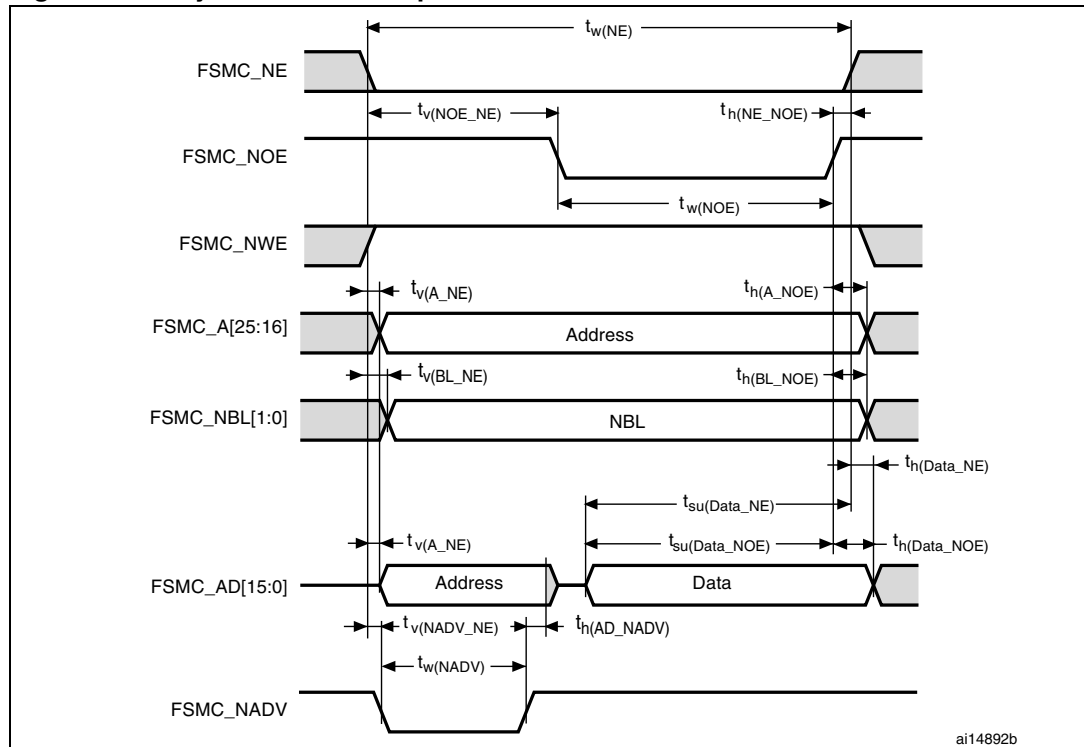
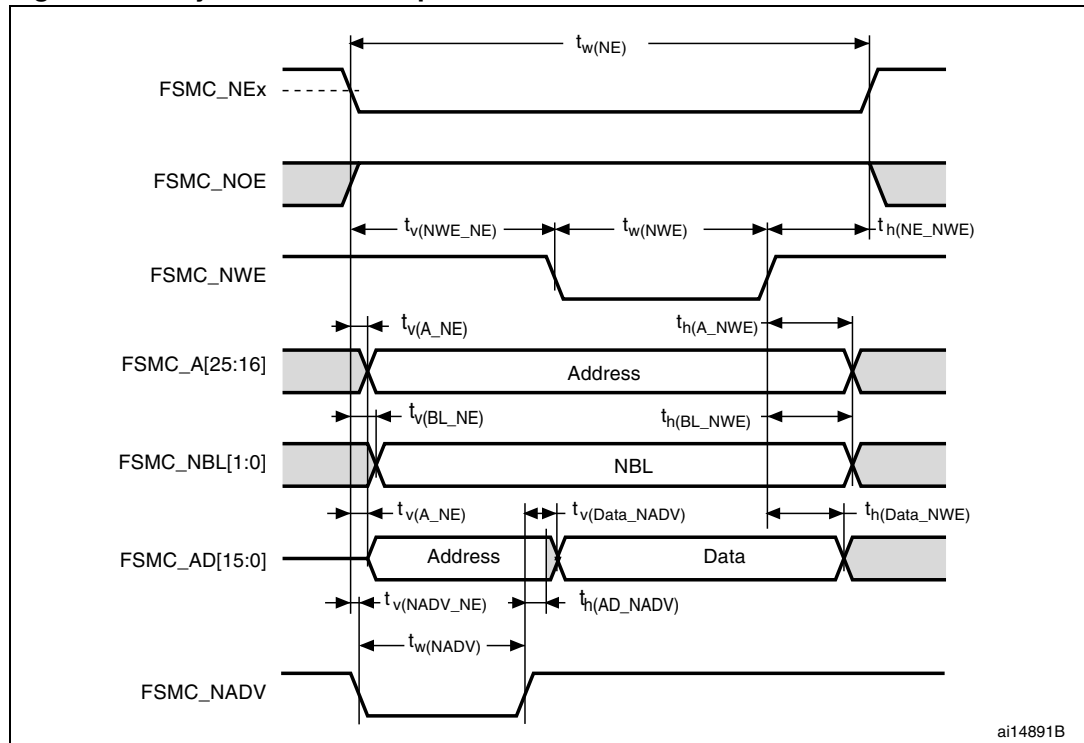


Table 72. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|---------------------|---|----------------|-----------------|------|
| $t_{w(NE)}$ | FSMC_NE low time | $3T_{HCLK}-1$ | $3T_{HCLK}+1$ | ns |
| $t_{v(NOE_NE)}$ | FSMC_NEx low to FSMC_NOE low | $2T_{HCLK}$ | $2T_{HCLK}+0.5$ | ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | $T_{HCLK}-1$ | $T_{HCLK}+1$ | ns |
| $t_{h(NE_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | 0 | - | ns |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 2 | ns |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | 1 | 2.5 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK}-1.5$ | T_{HCLK} | ns |
| $t_{h(AD_NADV)}$ | FSMC_AD(address) valid hold time after FSMC_NADV high | T_{HCLK} | - | ns |
| $t_{h(A_NOE)}$ | Address hold time after FSMC_NOE high | T_{HCLK} | - | ns |
| $t_{h(BL_NOE)}$ | FSMC_BL time after FSMC_NOE high | 0 | - | ns |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 1 | ns |
| $t_{su(Data_NE)}$ | Data to FSMC_NEx high setup time | $T_{HCLK}+2$ | - | ns |
| $t_{su(Data_NOE)}$ | Data to FSMC_NOE high setup time | $T_{HCLK}+3$ | - | ns |
| $t_{h(Data_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | ns |
| $t_{h(Data_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | ns |

1. $C_L = 30$ pF.
2. Based on characterization, not tested in production.

Figure 57. Asynchronous multiplexed PSRAM/NOR write waveforms



ai14891B

Table 73. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|---------------------|---|----------------|---------------|------|
| $t_{w(NE)}$ | FSMC_NE low time | $4T_{HCLK}-1$ | $4T_{HCLK}+1$ | ns |
| $t_{v(NWE_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK}-1$ | T_{HCLK} | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | $2T_{HCLK}$ | $2T_{HCLK}+1$ | ns |
| $t_{h(NE_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $T_{HCLK}-1$ | - | ns |
| $t_{v(A_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | ns |
| $t_{v(NADV_NE)}$ | FSMC_NEx low to FSMC_NADV low | 1 | 2 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK}-2$ | $T_{HCLK}+2$ | ns |
| $t_{h(AD_NADV)}$ | FSMC_AD(address) valid hold time after FSMC_NADV high | T_{HCLK} | - | ns |
| $t_{h(A_NWE)}$ | Address hold time after FSMC_NWE high | $T_{HCLK}-0.5$ | - | ns |
| $t_{h(BL_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $T_{HCLK}-1$ | - | ns |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | ns |
| $t_{v(Data_NADV)}$ | FSMC_NADV high to Data valid | - | $T_{HCLK}+2$ | ns |
| $t_{h(Data_NWE)}$ | Data hold time after FSMC_NWE high | $T_{HCLK}-0.5$ | - | ns |

1. $C_L = 30$ pF.
2. Based on characterization, not tested in production.

Synchronous waveforms and timings

Figure 58 through Figure 61 represent synchronous waveforms and Table 75 through Table 77 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F20xxx/21xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 58. Synchronous multiplexed NOR/PSRAM read timings

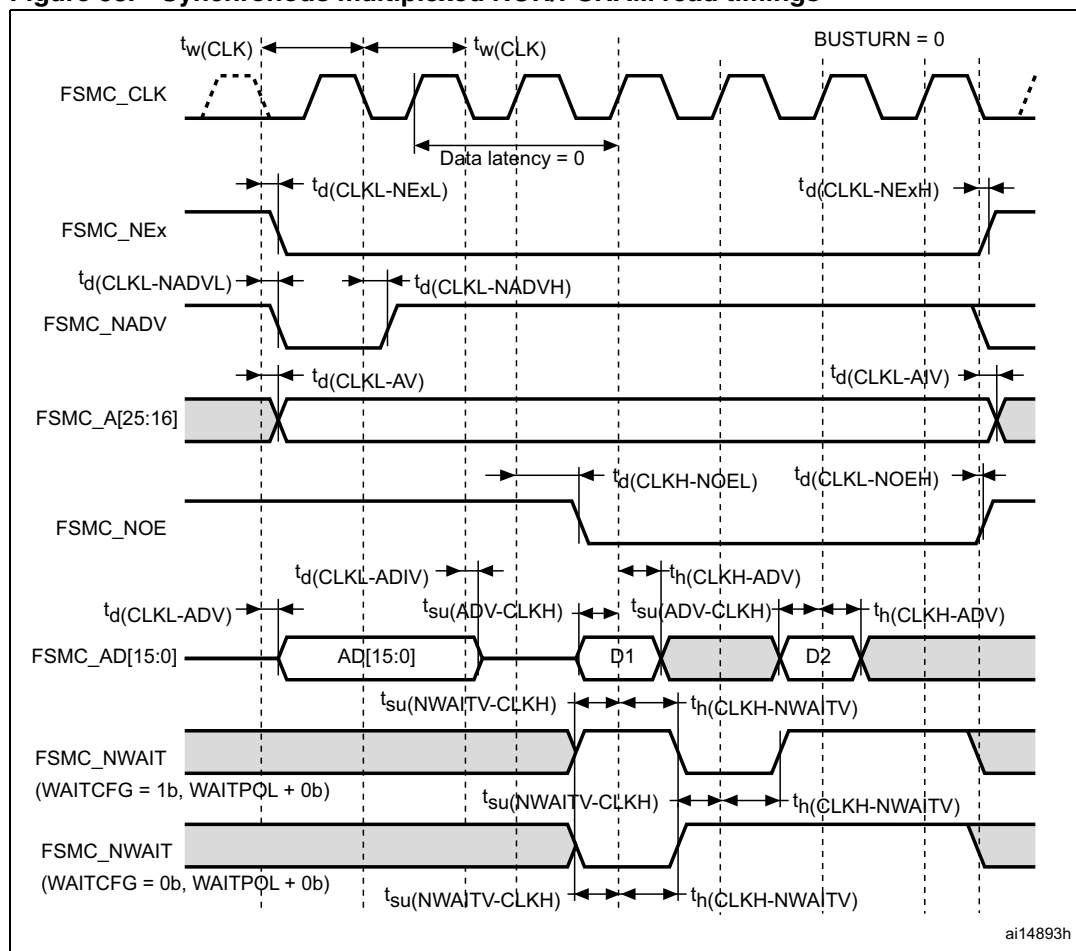


Table 74. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|----------------------------------|--|--------------------|-----|------|
| $t_w(\text{CLK})$ | FSMC_CLK period | $2T_{\text{HCLK}}$ | - | ns |
| $t_d(\text{CLKL-NExL})$ | FSMC_CLK low to FSMC_NEx low (x=0..2) | - | 0 | ns |
| $t_d(\text{CLKL-NExH})$ | FSMC_CLK low to FSMC_NEx high (x= 0...2) | 1 | - | ns |
| $t_d(\text{CLKL-NADVl})$ | FSMC_CLK low to FSMC_NADV low | - | 1.5 | ns |
| $t_d(\text{CLKL-NADVh})$ | FSMC_CLK low to FSMC_NADV high | 2.5 | - | ns |
| $t_d(\text{CLKL-AV})$ | FSMC_CLK low to FSMC_Ax valid (x=16...25) | - | 0 | ns |
| $t_d(\text{CLKL-AIV})$ | FSMC_CLK low to FSMC_Ax invalid (x=16...25) | 0 | - | ns |
| $t_d(\text{CLKH-NOEL})$ | FSMC_CLK high to FSMC_NOE low | - | 1 | ns |
| $t_d(\text{CLKL-NOEH})$ | FSMC_CLK low to FSMC_NOE high | 1 | - | ns |
| $t_d(\text{CLKL-ADV})$ | FSMC_CLK low to FSMC_AD[15:0] valid | - | 3 | ns |
| $t_d(\text{CLKL-ADIV})$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 0 | - | ns |
| $t_{\text{su}}(\text{ADV-CLKH})$ | FSMC_A/D[15:0] valid data before FSMC_CLK high | 5 | - | ns |
| $t_h(\text{CLKH-ADV})$ | FSMC_A/D[15:0] valid data after FSMC_CLK high | 0 | - | ns |

1. $C_L = 30 \text{ pF}$.
2. Based on characterization, not tested in production.

Figure 59. Synchronous multiplexed PSRAM write timings

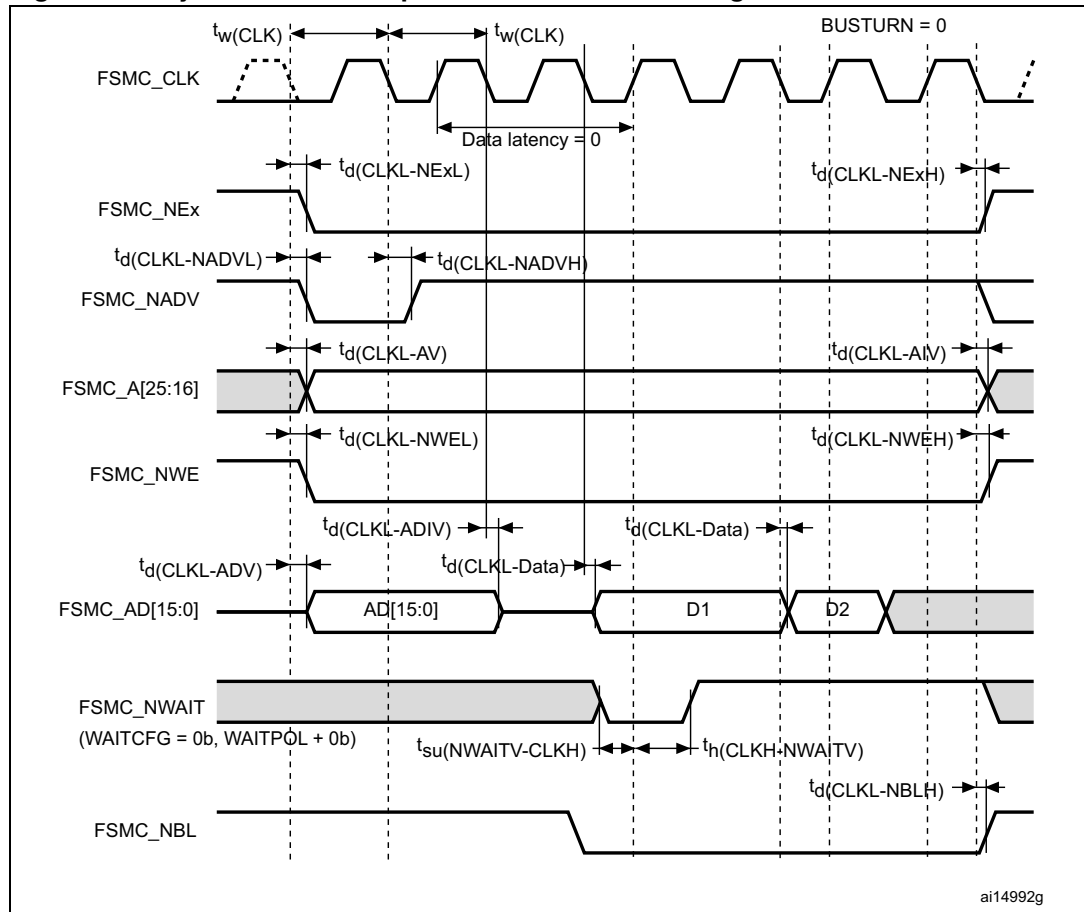


Table 75. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|--------------------------|--|------------------------|-----|------|
| $t_w(\text{CLK})$ | FSMC_CLK period | $2T_{\text{HCLK}} - 1$ | - | ns |
| $t_d(\text{CLKL-NExL})$ | FSMC_CLK low to FSMC_NEx low (x=0..2) | - | 0 | ns |
| $t_d(\text{CLKL-NExH})$ | FSMC_CLK low to FSMC_NEx high (x= 0...2) | 2 | - | ns |
| $t_d(\text{CLKL-NADVl})$ | FSMC_CLK low to FSMC_NADV low | - | 2 | ns |
| $t_d(\text{CLKL-NADVh})$ | FSMC_CLK low to FSMC_NADV high | 3 | - | ns |
| $t_d(\text{CLKL-AV})$ | FSMC_CLK low to FSMC_Ax valid (x=16...25) | - | 0 | ns |
| $t_d(\text{CLKL-AIV})$ | FSMC_CLK low to FSMC_Ax invalid (x=16...25) | 7 | - | ns |
| $t_d(\text{CLKL-NWEL})$ | FSMC_CLK low to FSMC_NWE low | - | 1 | ns |
| $t_d(\text{CLKL-NWEH})$ | FSMC_CLK low to FSMC_NWE high | 0 | - | ns |
| $t_d(\text{CLKL-ADIV})$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 0 | - | ns |
| $t_d(\text{CLKL-DATA})$ | FSMC_A/D[15:0] valid data after FSMC_CLK low | - | 2 | ns |
| $t_d(\text{CLKL-NBLH})$ | FSMC_CLK low to FSMC_NBL high | 0.5 | - | ns |

1. $C_L = 30 \text{ pF}$.
2. Based on characterization, not tested in production.

Figure 60. Synchronous non-multiplexed NOR/PSRAM read timings

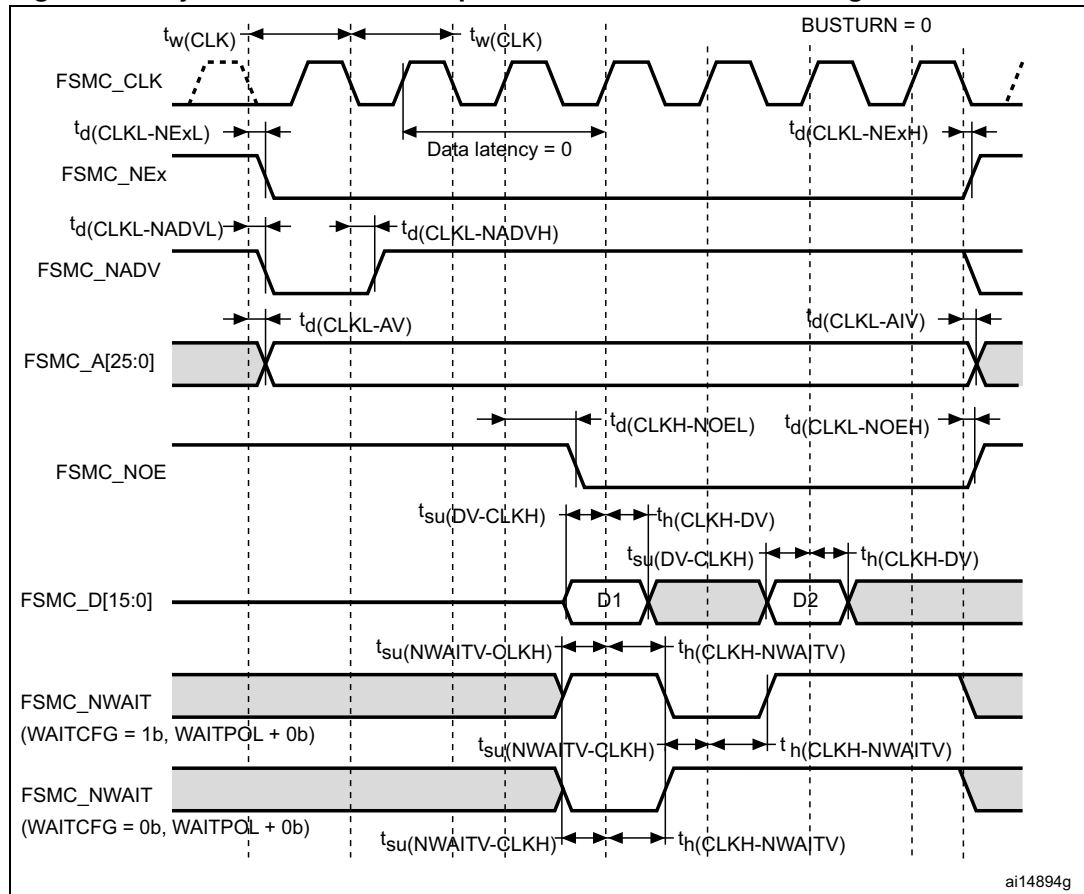


Table 76. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|--------------------------|--|--------------------|-----|------|
| $t_w(\text{CLK})$ | FSMC_CLK period | $2T_{\text{HCLK}}$ | - | ns |
| $t_d(\text{CLKL-NExL})$ | FSMC_CLK low to FSMC_NEx low (x=0..2) | - | 0 | ns |
| $t_d(\text{CLKL-NExH})$ | FSMC_CLK low to FSMC_NEx high (x= 0...2) | 1 | - | ns |
| $t_d(\text{CLKL-NADVl})$ | FSMC_CLK low to FSMC_NADV low | - | 2.5 | ns |
| $t_d(\text{CLKL-NADVh})$ | FSMC_CLK low to FSMC_NADV high | 4 | - | ns |
| $t_d(\text{CLKL-AV})$ | FSMC_CLK low to FSMC_Ax valid (x=16...25) | - | 0 | ns |
| $t_d(\text{CLKL-AiV})$ | FSMC_CLK low to FSMC_Ax invalid (x=16...25) | 3 | - | ns |
| $t_d(\text{CLKH-NOEL})$ | FSMC_CLK high to FSMC_NOE low | - | 1 | ns |
| $t_d(\text{CLKL-NOEH})$ | FSMC_CLK low to FSMC_NOE high | 1.5 | - | ns |
| $t_{su}(\text{DV-CLKH})$ | FSMC_D[15:0] valid data before FSMC_CLK high | 8 | - | ns |
| $t_h(\text{CLKH-DV})$ | FSMC_D[15:0] valid data after FSMC_CLK high | 3.5 | - | ns |

1. $C_L = 30 \text{ pF}$.
2. Based on characterization, not tested in production.

Figure 61. Synchronous non-multiplexed PSRAM write timings

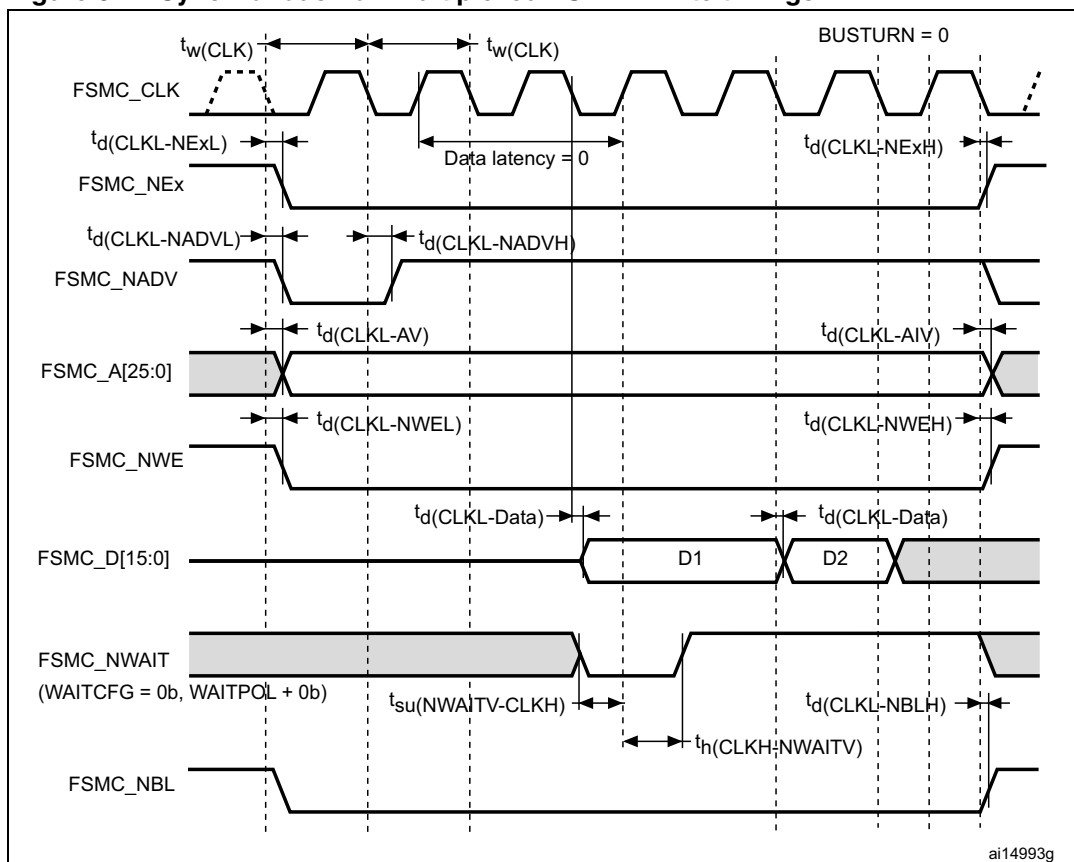


Table 77. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|--------------------------|---|------------------------|-----|------|
| $t_w(\text{CLK})$ | FSMC_CLK period | $2T_{\text{HCLK}} - 1$ | - | ns |
| $t_d(\text{CLKL-NExL})$ | FSMC_CLK low to FSMC_NEx low (x=0..2) | - | 1 | ns |
| $t_d(\text{CLKL-NExH})$ | FSMC_CLK low to FSMC_NEx high (x=0..2) | 1 | - | ns |
| $t_d(\text{CLKL-NADV})$ | FSMC_CLK low to FSMC_NADV low | - | 5 | ns |
| $t_d(\text{CLKL-NADVH})$ | FSMC_CLK low to FSMC_NADV high | 6 | - | ns |
| $t_d(\text{CLKL-AV})$ | FSMC_CLK low to FSMC_Ax valid (x=16...25) | - | 0 | ns |
| $t_d(\text{CLKL-AIV})$ | FSMC_CLK low to FSMC_Ax invalid (x=16...25) | 8 | - | ns |
| $t_d(\text{CLKL-NWEL})$ | FSMC_CLK low to FSMC_NWE low | - | 1 | ns |
| $t_d(\text{CLKL-NWEH})$ | FSMC_CLK low to FSMC_NWE high | 1 | - | ns |
| $t_d(\text{CLKL-Data})$ | FSMC_D[15:0] valid data after FSMC_CLK low | - | 2 | ns |
| $t_d(\text{CLKL-NBLH})$ | FSMC_CLK low to FSMC_NBL high | 2 | - | ns |

1. $C_L = 30$ pF.

2. Based on characterization, not tested in production.

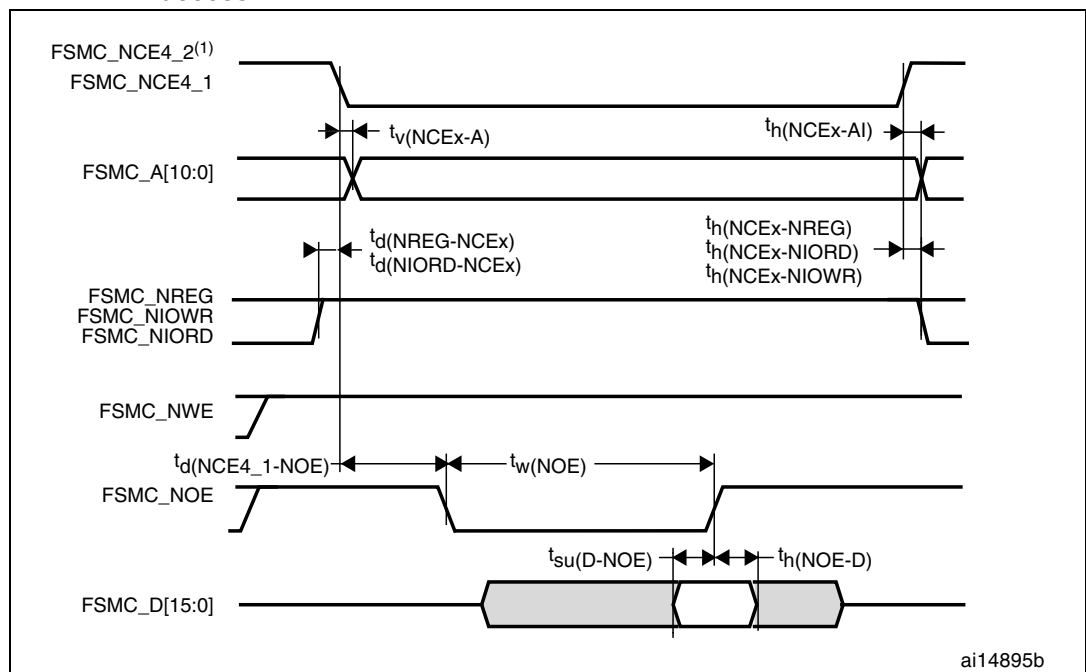
PC Card/CompactFlash controller waveforms and timings

Figure 62 through Figure 67 represent synchronous waveforms together with Table 78 and Table 79 provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 62. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access).

Figure 63. PC Card/CompactFlash controller waveforms for common memory write access

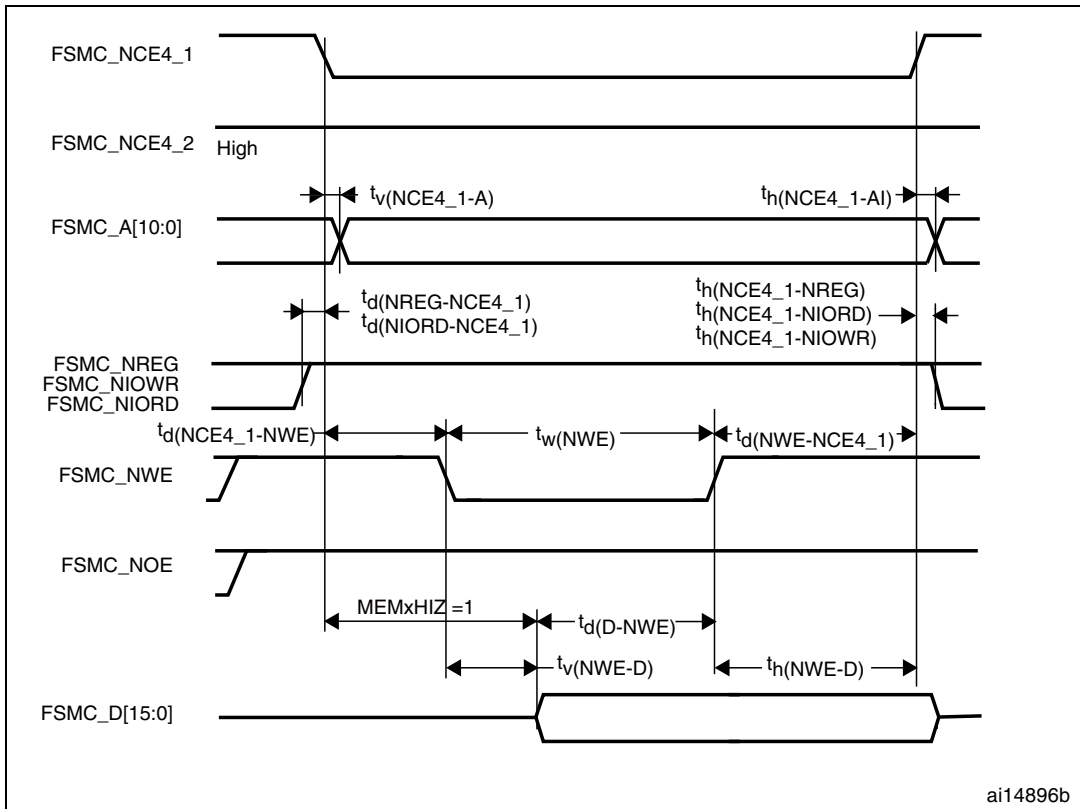
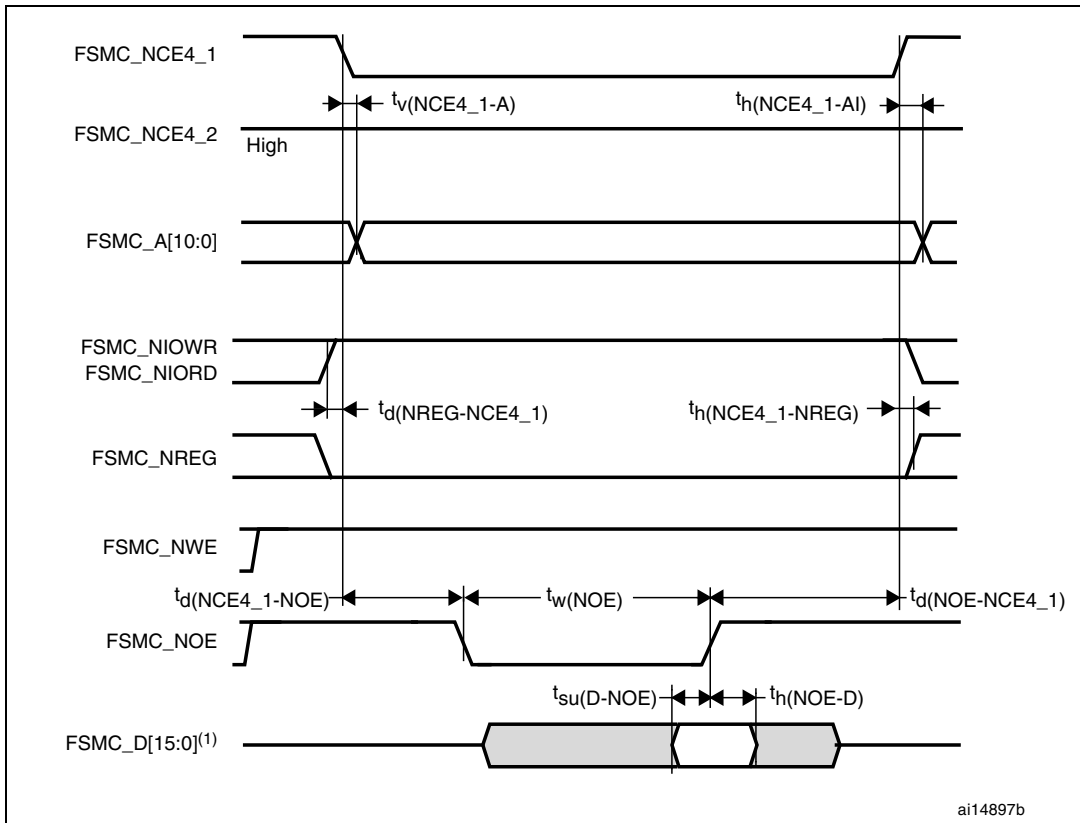
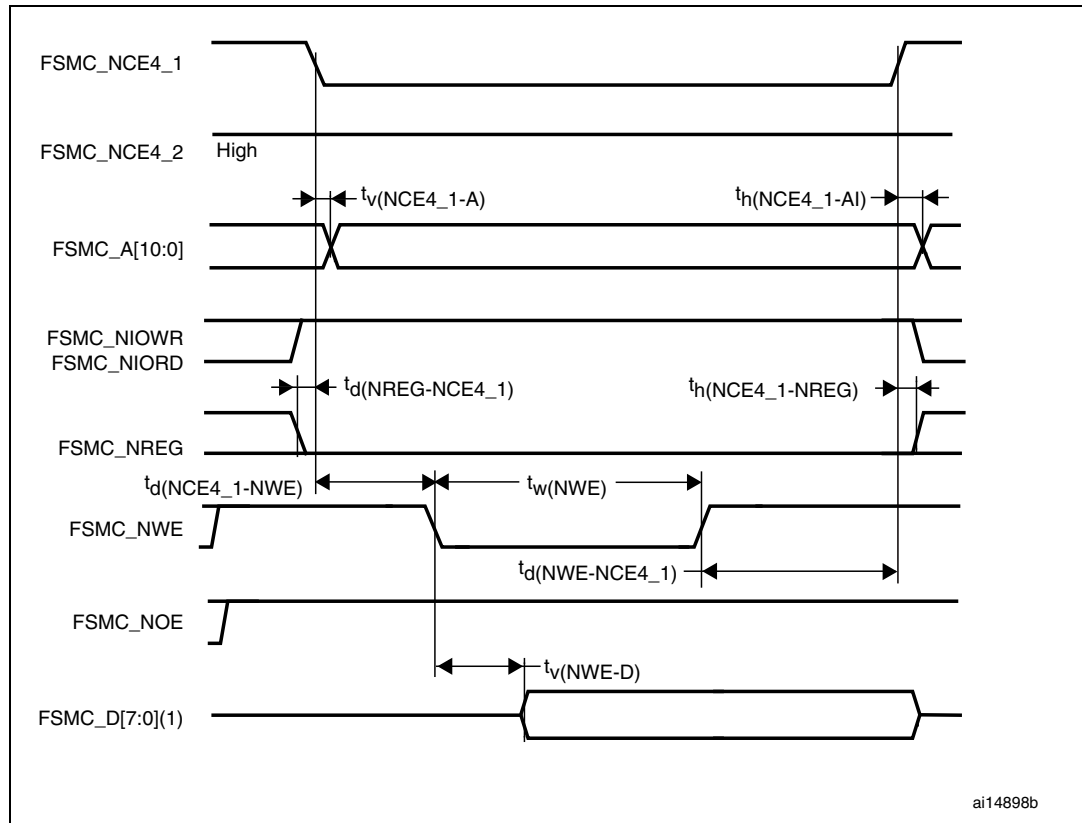


Figure 64. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 65. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Figure 66. PC Card/CompactFlash controller waveforms for I/O space read access

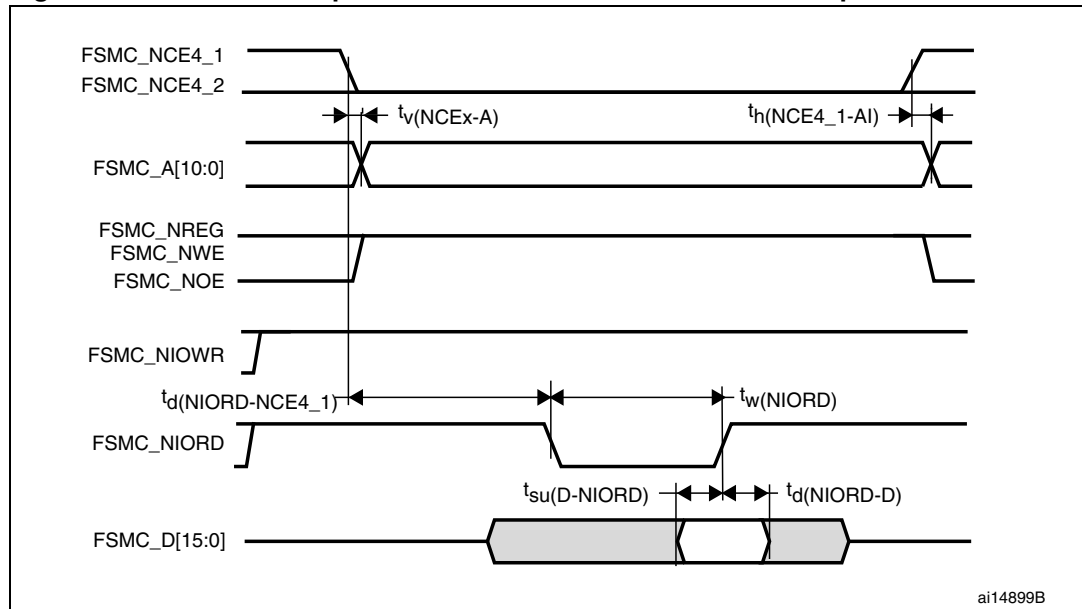


Figure 67. PC Card/CompactFlash controller waveforms for I/O space write access

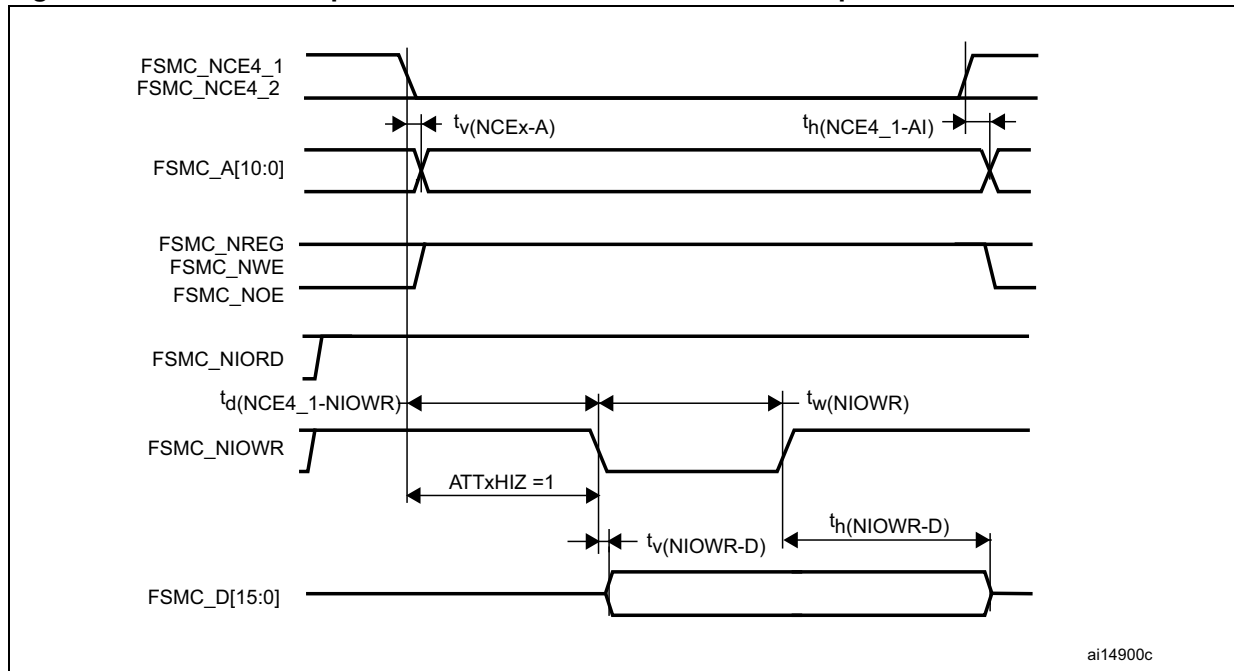


Table 78. Switching characteristics for PC Card/CF read and write cycles in attribute/common space⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|--------------------|--|-------------------|-----------------|------|
| $t_{v(NCEx-A)}$ | FSMC_Ncex low to FSMC_Ay valid | - | 0 | ns |
| $t_{h(NCEx-AI)}$ | FSMC_NCEx high to FSMC_Ax invalid | 4 | - | ns |
| $t_{d(NREG-NCEx)}$ | FSMC_NCEx low to FSMC_NREG valid | - | 3.5 | ns |
| $t_{h(NCEx-NREG)}$ | FSMC_NCEx high to FSMC_NREG invalid | $T_{HCLK} + 4$ | - | ns |
| $t_{d(NCEx-NWE)}$ | FSMC_NCEx low to FSMC_NWE low | - | $5T_{HCLK} + 1$ | ns |
| $t_{d(NCEx-NOE)}$ | FSMC_NCEx low to FSMC_NOE low | - | $5T_{HCLK}$ | ns |
| $t_{w(NOE)}$ | FSMC_NOE low width | $8T_{HCLK} - 0.5$ | $8T_{HCLK} + 1$ | ns |
| $t_{d(NOE-NCEx)}$ | FSMC_NOE high to FSMC_NCEx high | $5T_{HCLK} + 2.5$ | - | ns |
| $t_{su(D-NOE)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | 4 | - | ns |
| $t_{h(NOE-D)}$ | FSMC_NOE high to FSMC_D[15:0] invalid | 2 | - | ns |
| $t_{w(NWE)}$ | FSMC_NWE low width | $8T_{HCLK} - 1$ | $8T_{HCLK} + 4$ | ns |
| $t_{d(NWE-NCEx)}$ | FSMC_NWE high to FSMC_NCEx high | $5T_{HCLK} + 1.5$ | - | ns |
| $t_{d(NCEx-NWE)}$ | FSMC_NCEx low to FSMC_NWE low | - | $5HCLK + 1$ | ns |
| $t_{v(NWE-D)}$ | FSMC_NWE low to FSMC_D[15:0] valid | - | 0 | ns |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[15:0] invalid | $8 T_{HCLK}$ | - | ns |
| $t_{d(D-NWE)}$ | FSMC_D[15:0] valid before FSMC_NWE high | $13T_{HCLK}$ | - | ns |

1. $C_L = 30$ pF.
2. Based on characterization, not tested in production.

Table 79. Switching characteristics for PC Card/CF read and write cycles in I/O space⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|------------------------|---|-------------------|-------------------|------|
| $t_{w(NIOWR)}$ | FSMC_NIOWR low width | $8T_{HCLK} - 0.5$ | - | ns |
| $t_{v(NIOWR-D)}$ | FSMC_NIOWR low to FSMC_D[15:0] valid | - | $5T_{HCLK} - 1$ | ns |
| $t_{h(NIOWR-D)}$ | FSMC_NIOWR high to FSMC_D[15:0] invalid | $8T_{HCLK} - 3$ | - | ns |
| $t_{d(NCE4_1-NIOWR)}$ | FSMC_NCE4_1 low to FSMC_NIOWR valid | - | $5T_{HCLK} + 1.5$ | ns |
| $t_{h(NCEx-NIOWR)}$ | FSMC_NCEx high to FSMC_NIOWR invalid | $5T_{HCLK}$ | - | ns |
| $t_{d(NIORD-NCEx)}$ | FSMC_NCEx low to FSMC_NIORD valid | - | $5T_{HCLK} + 1$ | ns |
| $t_{h(NCEx-NIORD)}$ | FSMC_NCEx high to FSMC_NIORD valid | $5T_{HCLK} - 0.5$ | - | ns |
| $t_{w(NIORD)}$ | FSMC_NIORD low width | $8T_{HCLK} + 1$ | - | ns |
| $t_{su(D-NIORD)}$ | FSMC_D[15:0] valid before FSMC_NIORD high | 9.5 | | ns |
| $t_{d(NIORD-D)}$ | FSMC_D[15:0] valid after FSMC_NIORD high | 0 | | ns |

1. $C_L = 30$ pF.
2. Based on characterization, not tested in production.

NAND controller waveforms and timings

Figure 68 through Figure 71 represent synchronous waveforms, together with Table 80 and Table 81 provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 68. NAND controller waveforms for read access

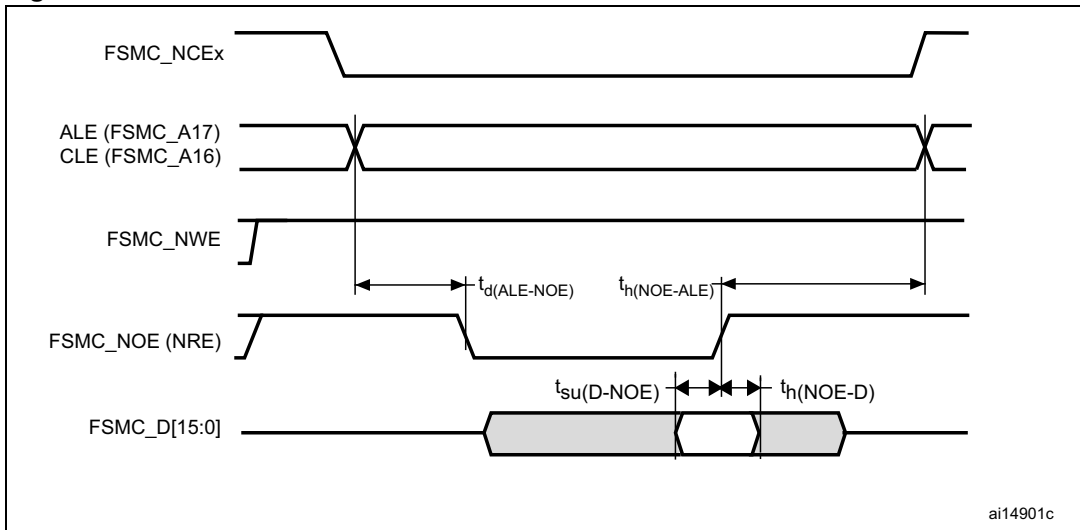


Figure 69. NAND controller waveforms for write access

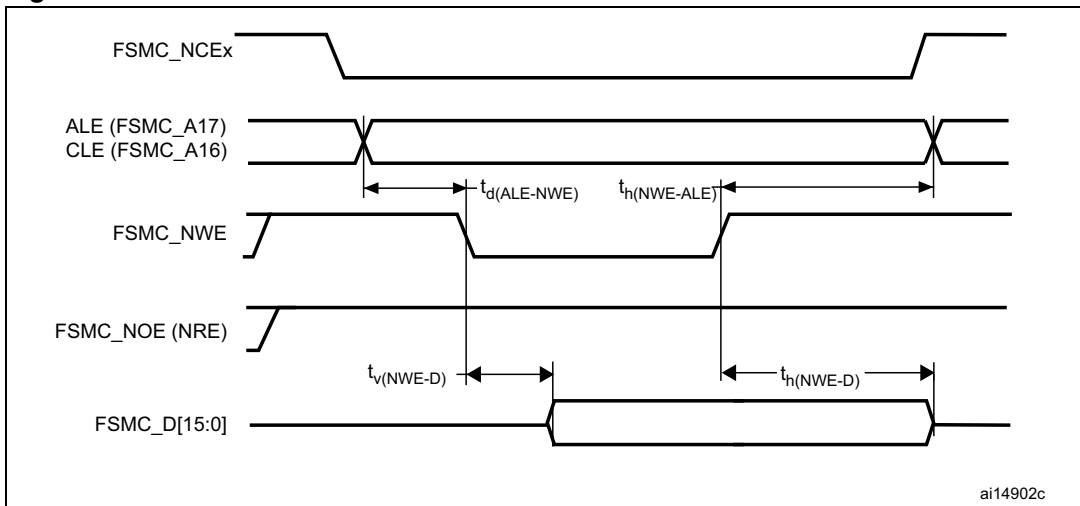


Figure 70. NAND controller waveforms for common memory read access

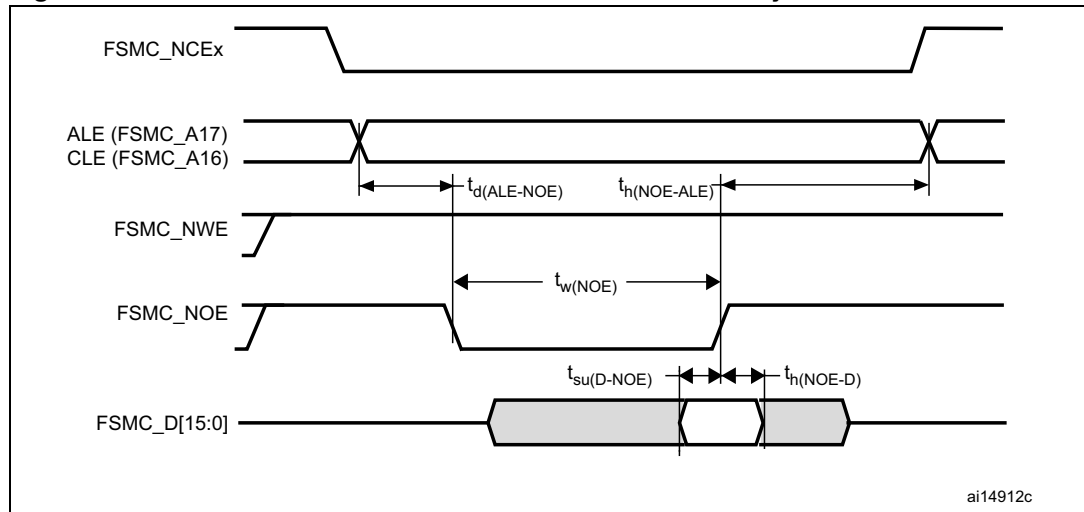


Figure 71. NAND controller waveforms for common memory write access

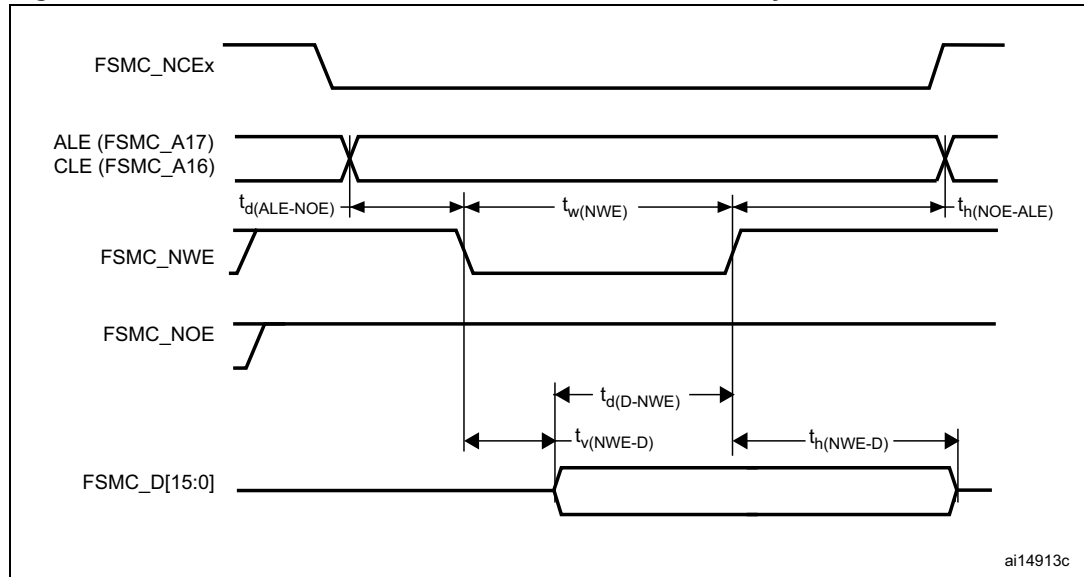


Table 80. Switching characteristics for NAND Flash read cycles⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|------------------|--|-----------------|-----------------|------|
| $t_{w(NOE)}$ | FSMC_NOE low width | $4T_{HCLK} - 1$ | $4T_{HCLK} + 2$ | ns |
| $t_{su(D-NOE)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | 9 | - | ns |
| $t_{h(NOE-D)}$ | FSMC_D[15:0] valid data after FSMC_NOE high | 3 | - | ns |
| $t_{d(ALE-NOE)}$ | FSMC_ALE valid before FSMC_NOE low | - | $3T_{HCLK}$ | ns |
| $t_{h(NOE-ALE)}$ | FSMC_NWE high to FSMC_ALE invalid | $3T_{HCLK} + 2$ | - | ns |

1. $C_L = 30$ pF.

2. Based on characterization, not tested in production.

Table 81. Switching characteristics for NAND Flash write cycles⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Unit |
|------------------|---|-----------------|-----------------|------|
| $t_{w(NWE)}$ | FSMC_NWE low width | $4T_{HCLK} - 1$ | $4T_{HCLK} + 3$ | ns |
| $t_{v(NWE-D)}$ | FSMC_NWE low to FSMC_D[15-0] valid | - | 0 | ns |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[15-0] invalid | $3T_{HCLK}$ | - | ns |
| $t_{d(D-NWE)}$ | FSMC_D[15-0] valid before FSMC_NWE high | $5T_{HCLK}$ | - | ns |
| $t_{d(ALE-NWE)}$ | FSMC_ALE valid before FSMC_NWE low | - | $3T_{HCLK} + 2$ | ns |
| $t_{h(NWE-ALE)}$ | FSMC_NWE high to FSMC_ALE invalid | $3T_{HCLK} - 2$ | - | ns |

1. $C_L = 30$ pF.
2. Based on characterization, not tested in production.

5.3.26 Camera interface (DCMI) timing specifications

Table 82. DCMI characteristics

| Symbol | Parameter | Conditions | Min | Max |
|--------|--|-------------------------|-----|-----|
| | Frequency ratio $DCMI_PIXCLK/f_{HCLK}$ | $DCMI_PIXCLK = 48$ MHz | | 0.4 |

5.3.27 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 83](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 12](#).

Refer to [Section 5.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 72. SDIO high-speed mode

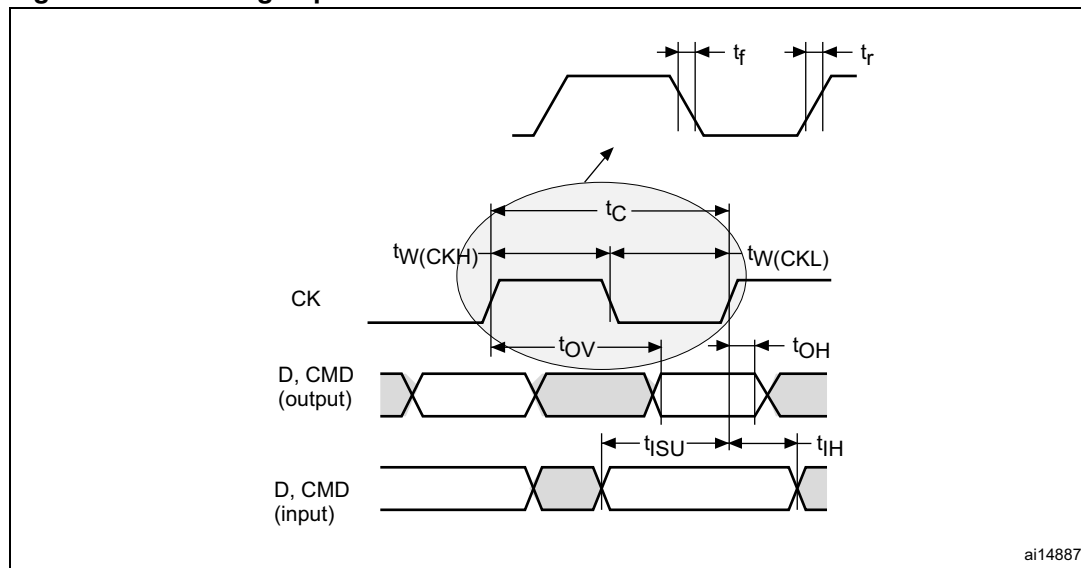
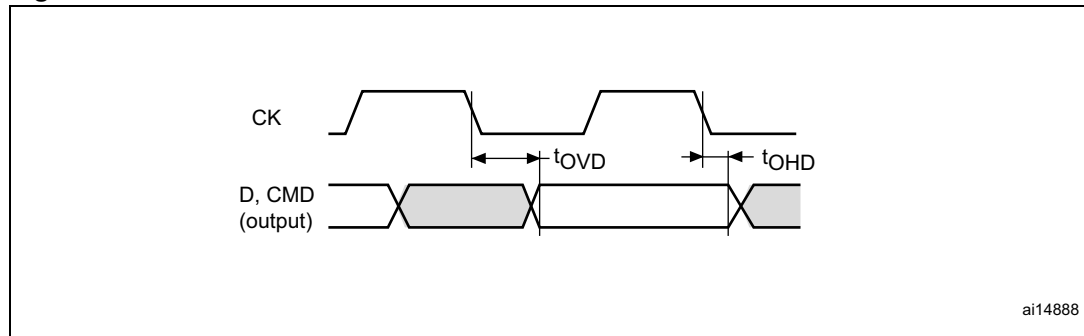


Figure 73. SD default mode



ai14888

Table 83. SD / MMC characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|--|------------------------|-----|-----|------|
| f _{PP} | Clock frequency in data transfer mode | C _L ≤ 30 pF | 0 | 48 | MHz |
| - | SDIO_CK/f _{PCLK2} frequency ratio | - | - | 8/3 | - |
| t _{W(CKL)} | Clock low time, f _{PP} = 16 MHz | C _L ≤ 30 pF | 32 | | ns |
| t _{W(CKH)} | Clock high time, f _{PP} = 16 MHz | C _L ≤ 30 pF | 31 | | |
| t _r | Clock rise time | C _L ≤ 30 pF | | 3.5 | |
| t _f | Clock fall time | C _L ≤ 30 pF | | 5 | |
| CMD, D inputs (referenced to CK) | | | | | |
| t _{SU} | Input setup time | C _L ≤ 30 pF | 2 | | ns |
| t _{IH} | Input hold time | C _L ≤ 30 pF | 0 | | |
| CMD, D outputs (referenced to CK) in MMC and SD HS mode | | | | | |
| t _{OV} | Output valid time | C _L ≤ 30 pF | | 6 | ns |
| t _{OH} | Output hold time | C _L ≤ 30 pF | 0.3 | | |
| CMD, D outputs (referenced to CK) in SD default mode⁽¹⁾ | | | | | |
| t _{OVD} | Output valid default time | C _L ≤ 30 pF | | 7 | ns |
| t _{OHD} | Output hold default time | C _L ≤ 30 pF | 0.5 | | |

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

5.3.28 RTC characteristics

Table 84. RTC characteristics

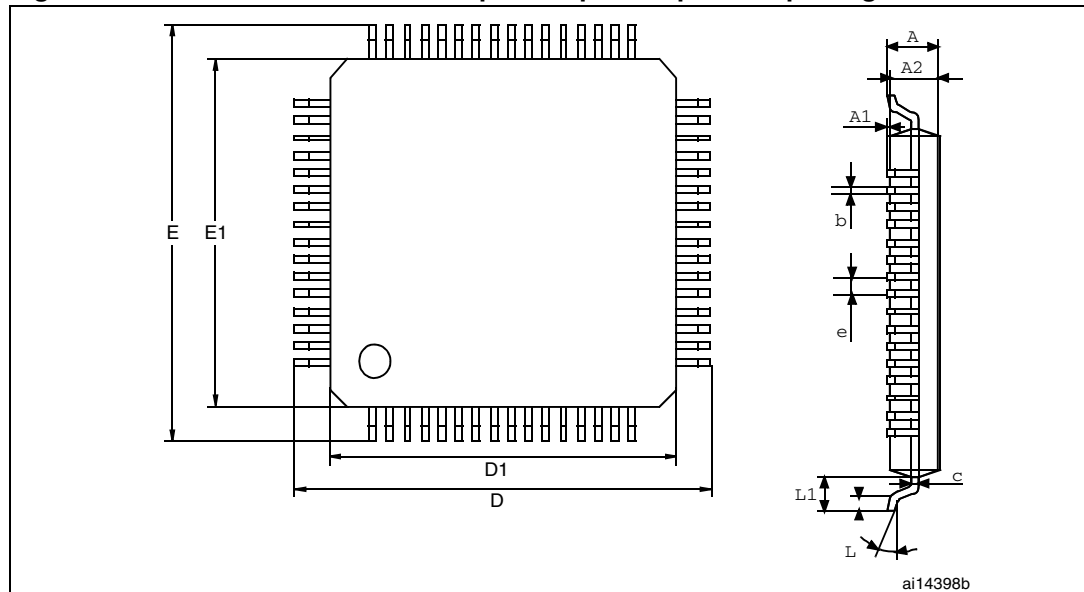
| Symbol | Parameter | Conditions | Min | Max |
|--------|--|--|-----|-----|
| - | f _{PCLK1} /RTCCLK frequency ratio | Any read/write operation from/to an RTC register | 4 | - |

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 74. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



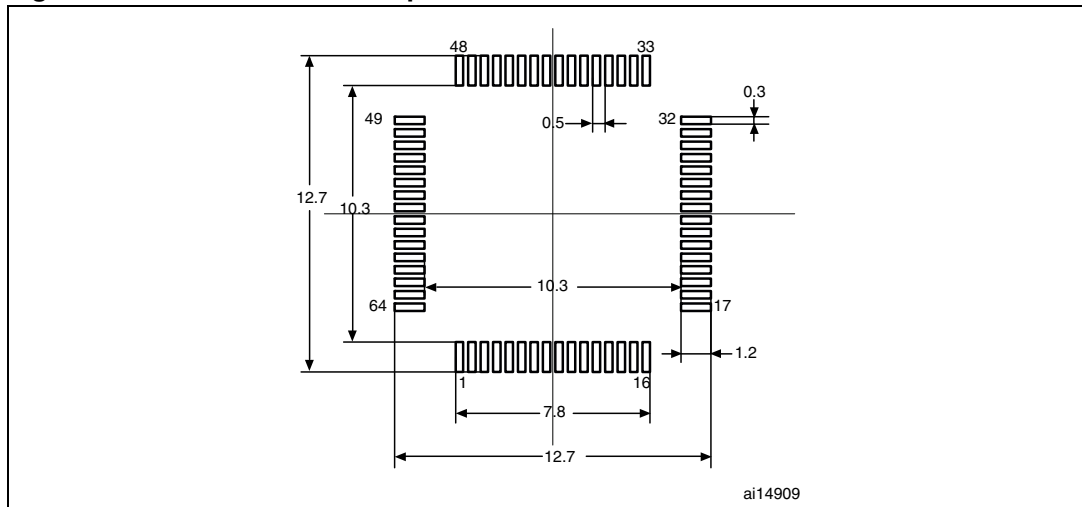
1. Drawing is not to scale.

Table 85. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-----------------------|--------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | | 12.000 | | | 0.4724 | |
| D1 | | 10.000 | | | 0.3937 | |
| E | | 12.000 | | | 0.4724 | |
| E1 | | 10.000 | | | 0.3937 | |
| e | | 0.500 | | | 0.0197 | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| N | Number of pins | | | | | |
| | 64 | | | | | |

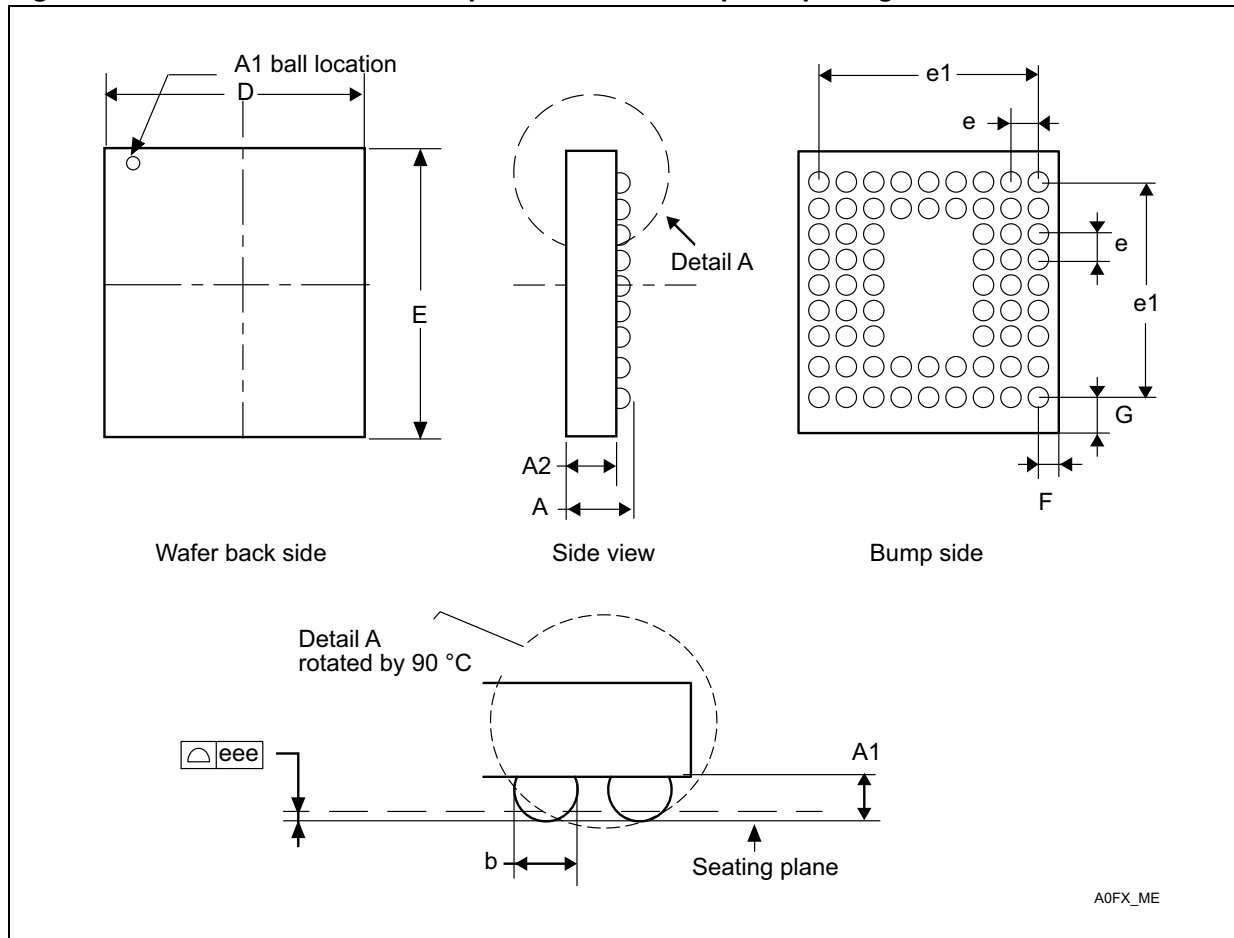
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 75. Recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 76. WLCSP64+2 - 0.400 mm pitch wafer level chip size package outline

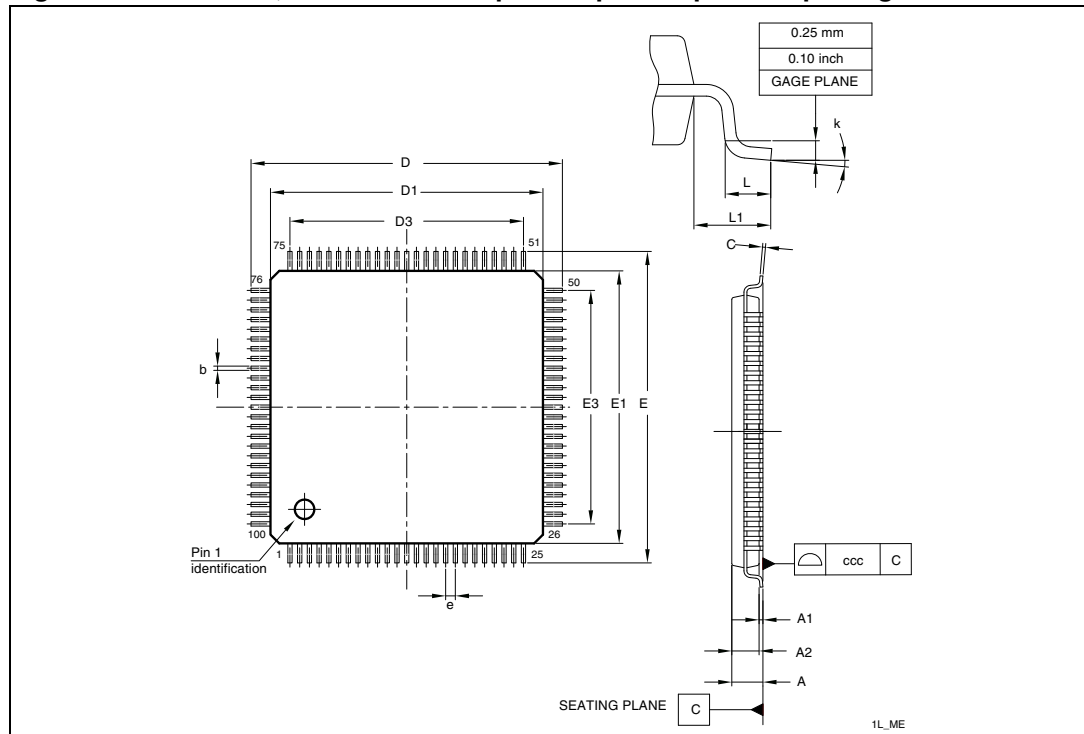


1. Drawing is not to scale.

Table 86. WLCSP64+2 - 0.400 mm pitch wafer level chip size package mechanical data

| Symbol | millimeters | | | inches | | |
|--------|-------------|-------|-------|--------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.520 | 0.570 | 0.600 | 0.0205 | 0.0224 | 0.0236 |
| A1 | 0.170 | 0.190 | 0.210 | 0.0067 | 0.0075 | 0.0083 |
| A2 | 0.350 | 0.380 | 0.410 | 0.0138 | 0.0150 | 0.0161 |
| b | 0.245 | 0.270 | 0.295 | 0.0096 | 0.0106 | 0.0116 |
| D | 3.619 | 3.639 | 3.659 | 0.1425 | 0.1433 | 0.1441 |
| E | 3.951 | 3.971 | 3.991 | 0.1556 | 0.1563 | 0.1571 |
| e | | 0.400 | | | 0.0157 | |
| e1 | | 3.218 | | | 0.1267 | |
| F | | 0.220 | | | 0.0087 | |
| G | | 0.386 | | | 0.0152 | |
| eee | | | 0.050 | | | 0.0020 |

Figure 77. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



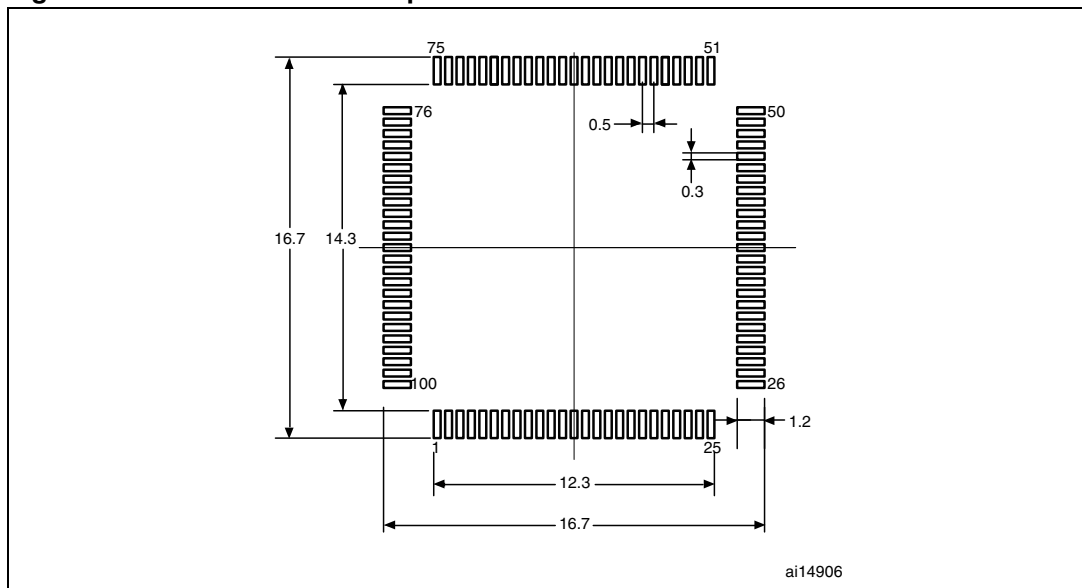
1. Drawing is not to scale.

Table 87. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | | 12.000 | | | 0.4724 | |
| E | 15.80v | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | | 12.000 | | | 0.4724 | |
| e | | 0.500 | | | 0.0197 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | | | 0.080 | | | 0.0031 |

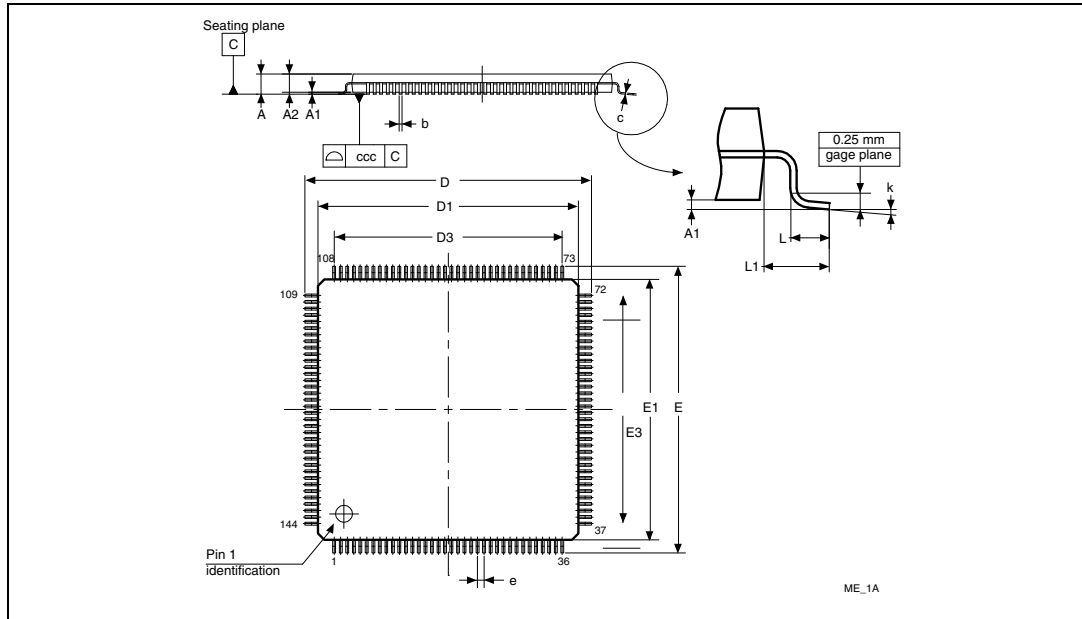
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 78. Recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 79. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



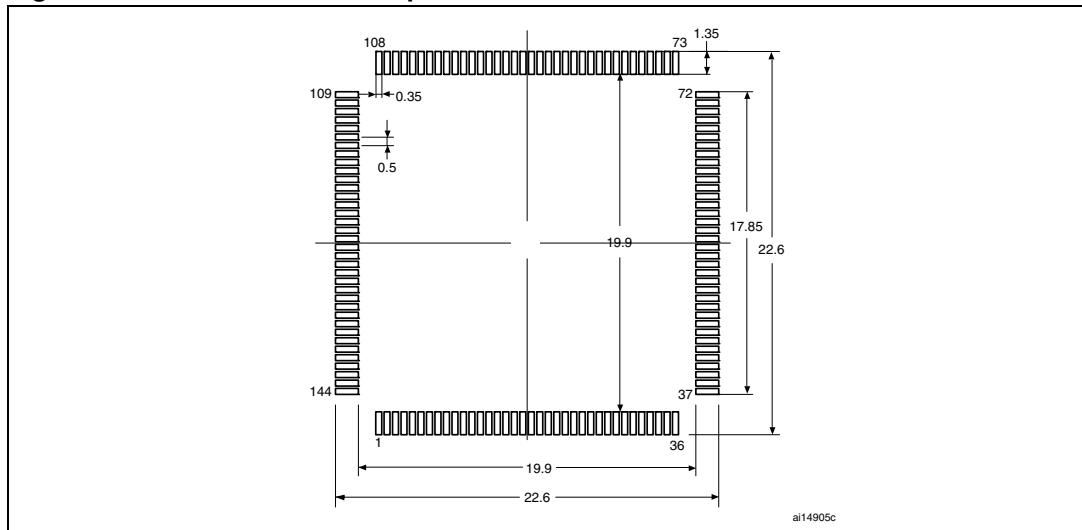
1. Drawing is not to scale.

Table 88. LQFP144 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.874 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | | 17.500 | | | 0.689 | |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | | 17.500 | | | 0.6890 | |
| e | | 0.500 | | | 0.0197 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | | | 0.080 | | | 0.0031 |

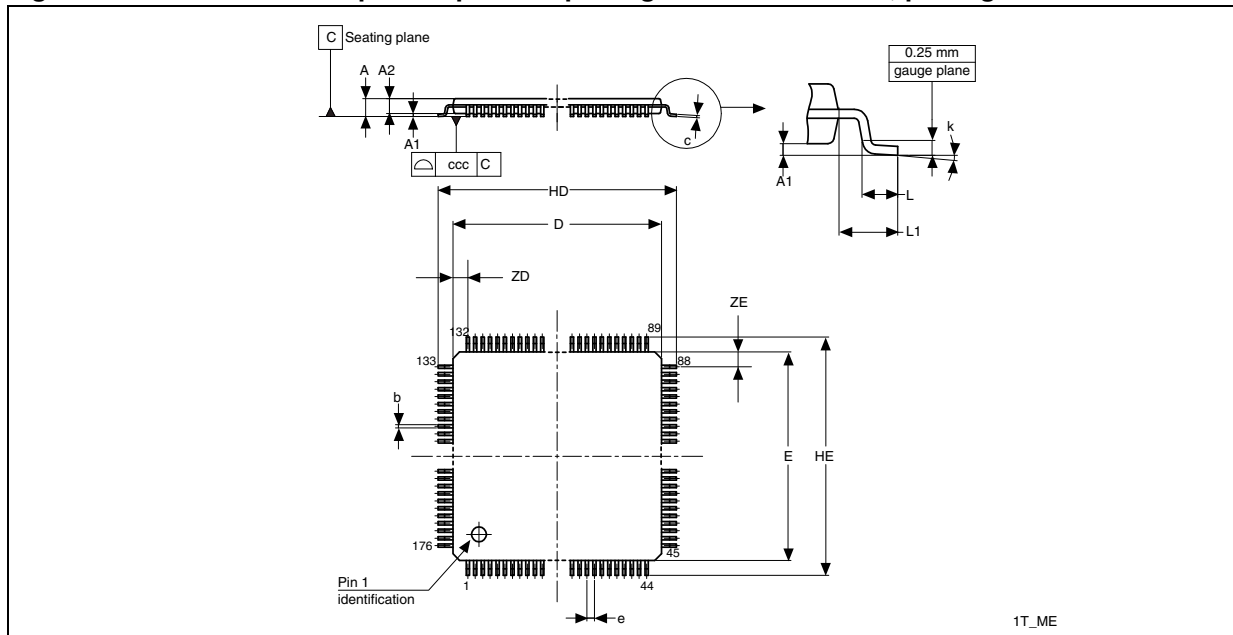
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 80. Recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 81. LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline



1. Drawing is not to scale.

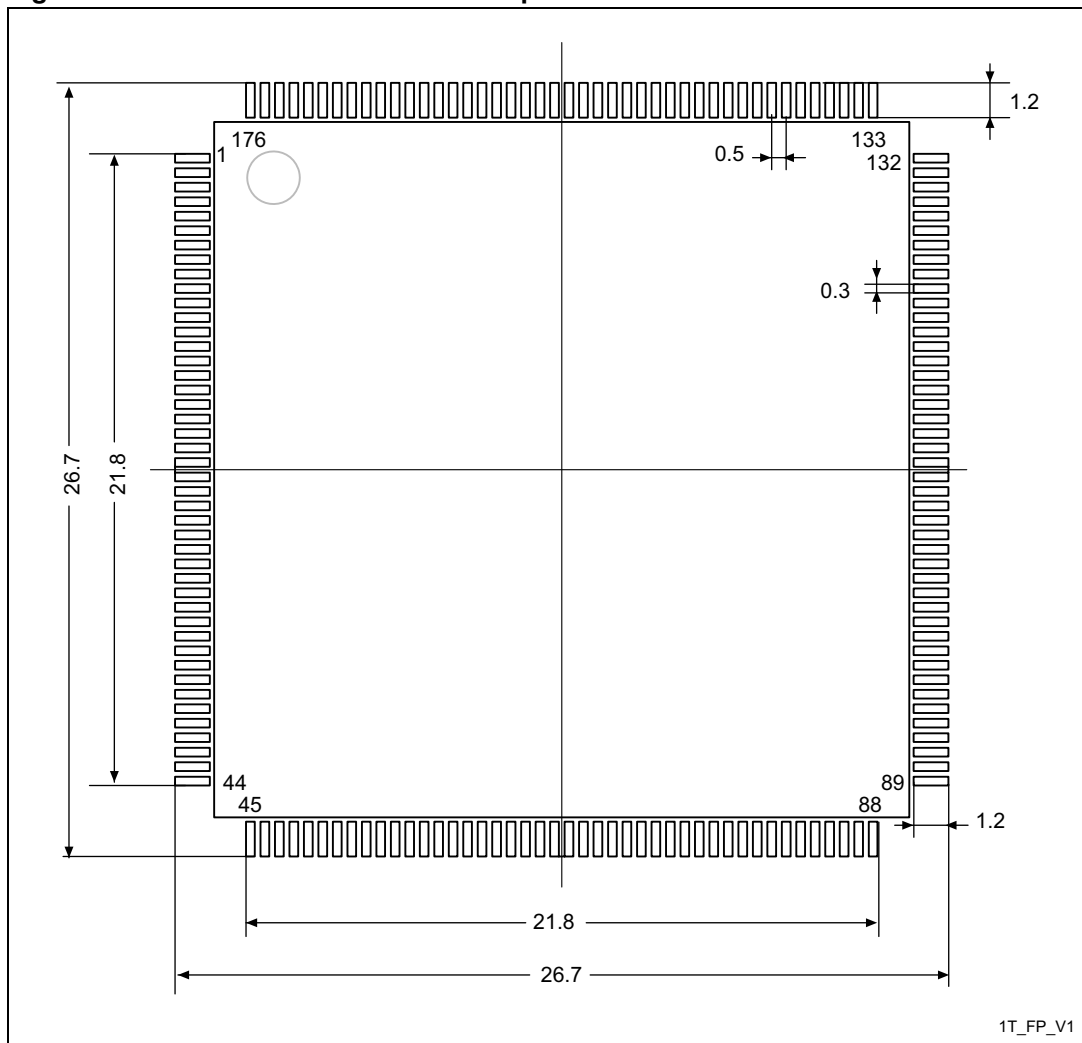
Table 89. LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|------------------|-------------|-------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | | 1.450 | 0.0531 | | 0.0571 |
| b | 0.170 | | 0.270 | 0.0067 | | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 23.900 | | 24.100 | 0.9409 | | 0.9488 |
| E | 23.900 | | 24.100 | 0.9409 | | 0.9488 |
| e | | 0.500 | | | 0.0197 | |
| HD | 25.900 | | 26.100 | 1.0197 | | 1.0276 |
| HE | 25.900 | | 26.100 | 1.0197 | | 1.0276 |
| L ⁽²⁾ | 0.450 | | 0.750 | 0.0177 | | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| ZD | | 1.250 | | | 0.0492 | |
| ZE | | 1.250 | | | 0.0492 | |
| k | 0° | | 7° | 0° | | 7° |
| ccc | | | 0.080 | | | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

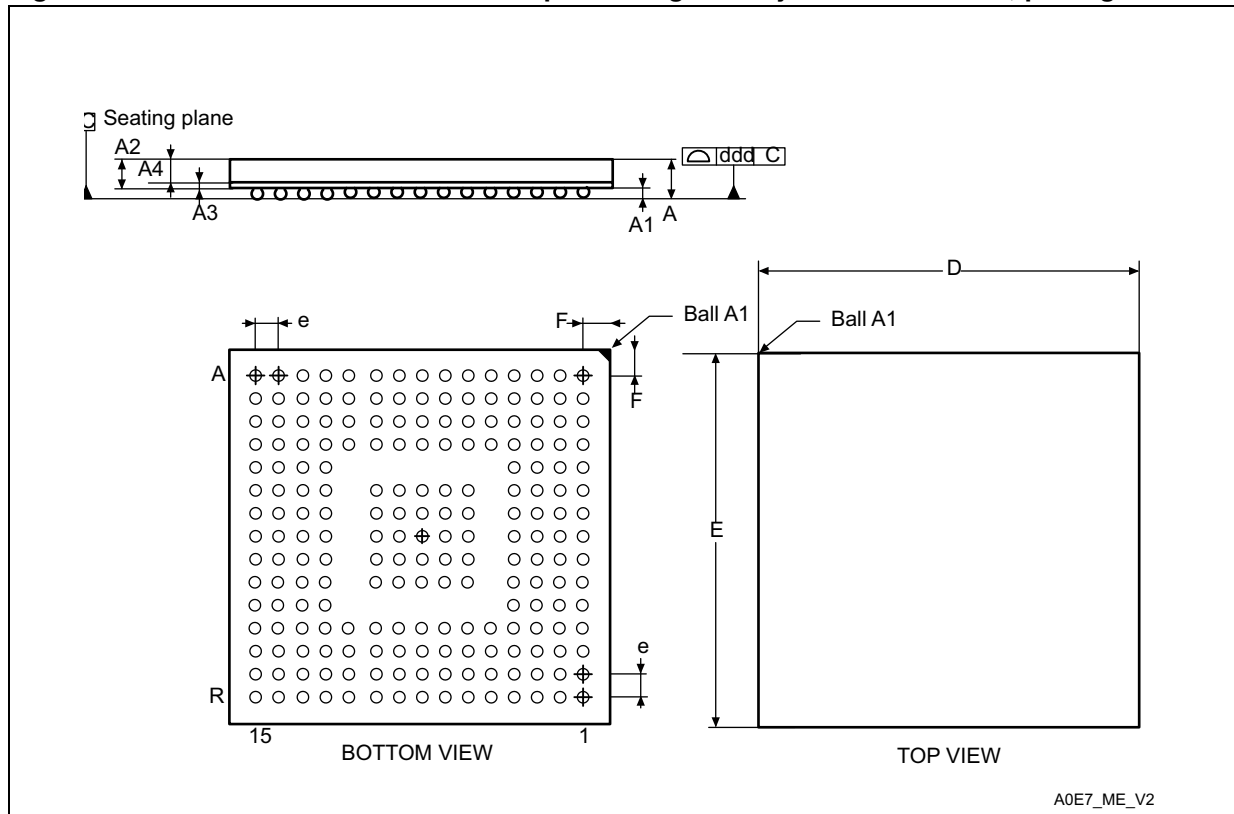
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

Figure 82. LQFP176 recommended footprint



1. Dimensions are expressed in millimeters.

Figure 83. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline



1. Drawing is not to scale.

Table 90. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.002 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | 0.130 | | | 0.0051 | | |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |
| b | 0.230 | 0.280 | 0.330 | 0.0091 | 0.0110 | 0.0130 |
| D | 9.950 | 10.000 | 10.050 | 0.3740 | 0.3937 | 0.3957 |
| E | 9.950 | 10.000 | 10.050 | 0.3740 | 0.3937 | 0.3957 |
| e | 0.600 | 0.650 | 0.700 | 0.0236 | 0.0256 | 0.0276 |
| F | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| ddd | | | 0.080 | | | 0.0031 |
| eee | | | 0.150 | | | 0.0059 |
| fff | | | 0.080 | | | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 91. Package thermal characteristics

| Symbol | Parameter | Value | Unit |
|---------------|--|-------|------|
| Θ_{JA} | Thermal resistance junction-ambient LQFP 64 - 10 × 10 mm / 0.5 mm pitch | 45 | °C/W |
| | Thermal resistance junction-ambient WLCSP64+2 - 0.400 mm pitch | 51 | |
| | Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch | 46 | |
| | Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch | 40 | |
| | Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch | 38 | |
| | Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch | 39 | |

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7 Part numbering

Table 92. Ordering information scheme

| | | | | | | | | | |
|---|-------|---|-----|---|---|---|---|---|-----|
| Example: | STM32 | F | 205 | R | E | T | 6 | V | xxx |
| Device family STM32 = ARM-based 32-bit microcontroller | | | | | | | | | |
| Product type F = general-purpose | | | | | | | | | |
| Device subfamily 205 = STM32F20x, connectivity, 207= STM32F20x, connectivity, camera interface, Ethernet | | | | | | | | | |
| Pin count R = 64 pins or 66 pins ⁽¹⁾ V = 100 pins Z = 144 pins I = 176 pins | | | | | | | | | |
| Flash memory size B = 128 Kbytes of Flash memory C = 256 Kbytes of Flash memory E = 512 Kbytes of Flash memory F = 768 Kbytes of Flash memory G = 1024 Kbytes of Flash memory | | | | | | | | | |
| Package T = LQFP H = UFBGA Y = WLCSP | | | | | | | | | |
| Temperature range 6 = Industrial temperature range, -40 to 85 °C. 7 = Industrial temperature range, -40 to 105 °C. | | | | | | | | | |
| Software option Internal code or Blank | | | | | | | | | |
| Options xxx = programmed parts TR = tape and reel | | | | | | | | | |

1. The 66 pins is available on WLCSP package only.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Application block diagrams

A.1 Main applications versus package

Table 93 gives examples of configurations for each package.

Table 93. Main applications versus package for STM32F2xxx microcontrollers

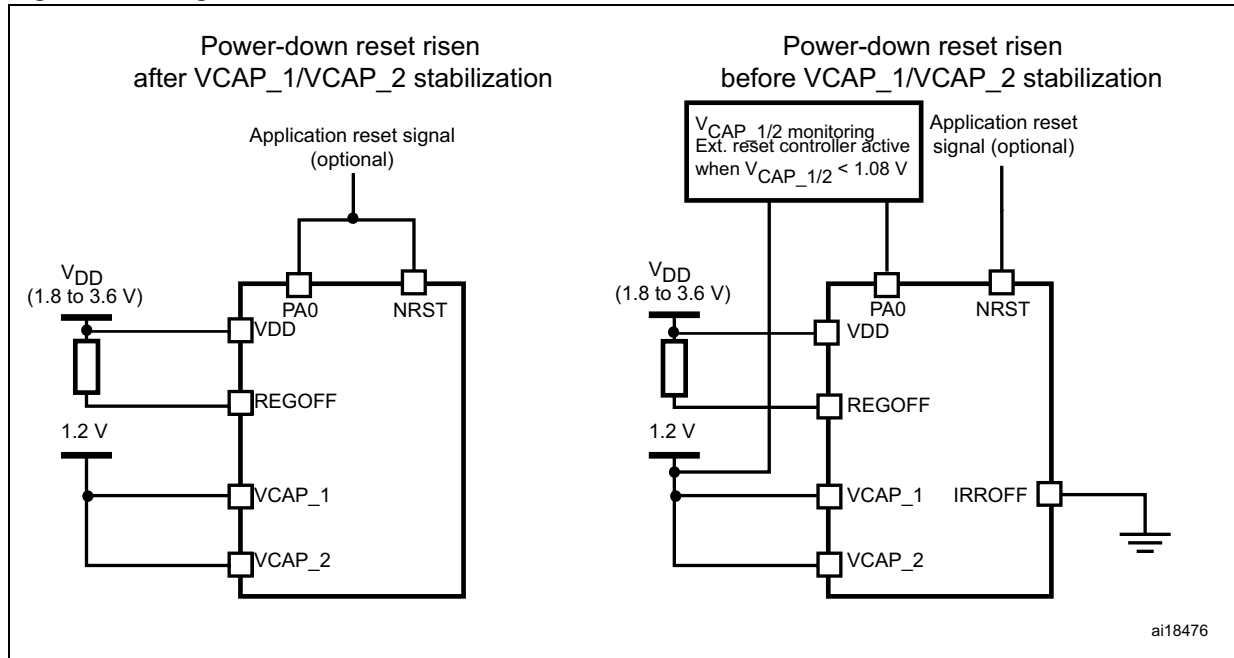
| | | 64 pins ⁽¹⁾ | | | 100 pins | | | | 144 pins | | | | 176 pins | |
|-------------------------|---------------|------------------------|----------|----------|--------------|--------------|--------------|----------|--------------|----------|--------------|----------|----------|----------|
| | | Config 1 | Config 2 | Config 3 | Config 1 | Config 2 | Config 3 | Config 4 | Config 1 | Config 2 | Config 3 | Config 4 | Config 1 | Config 2 |
| USB OTG FS | OTG FS | - | - | - | X | X | X | - | X | - | X | - | X | - |
| | FS | - | - | - | X | X | X | X | X | X | X | X | X | - |
| USB OTG HS | HS ULPI | X | - | X | X | - | - | - | X | X | - | - | X | X |
| | OTG FS | X | X | X | X | - | - | - | X | X | - | - | X | X |
| | FS | X | X | X | X | X | X | X | X | X | X | X | X | X |
| Ethernet ⁽²⁾ | MII | - | - | - | - | - | X | X | - | - | X | X | X | X |
| | RMII | - | - | - | - | X | X | X | X | X | X | X | X | X |
| SPI/I2S2 SPI/I2S3 | | - | X | - | - | X | X | X | X | X | X | X | X | X |
| SDIO | SDIO | X | X | - | | | | X | | X | | X | X | X |
| DCMI ⁽²⁾ | 8-bit Data | - | - | - | SDIO or DCMI | SDIO or DCMI | SDIO or DCMI | X | SDIO or DCMI | X | SDIO or DCMI | X | X | X |
| | 10-bit Data | - | - | - | | | | X | | X | | X | | |
| | 12-bit Data | - | - | - | | | | X | | X | | X | | |
| | 14-bit Data | - | - | - | | | | - | | - | | - | X | - |
| FSMC | NOR/RAM Muxed | - | - | - | X | X | X | X | X | X | X | X | X | X |
| | NOR/RAM | - | - | - | | | | | X | X | X | X | X | X |
| | NAND | - | - | - | X | X | X | X | X | X | X | X | X | X |
| | CF | - | - | - | - | - | - | - | X | X | X | X | X | X |
| CAN | | - | X | X | - | X | X | X | - | - | X | X | - | X |

1. Not available on STM32F2x7xx.

2. Not available on STM32F2x5xx.

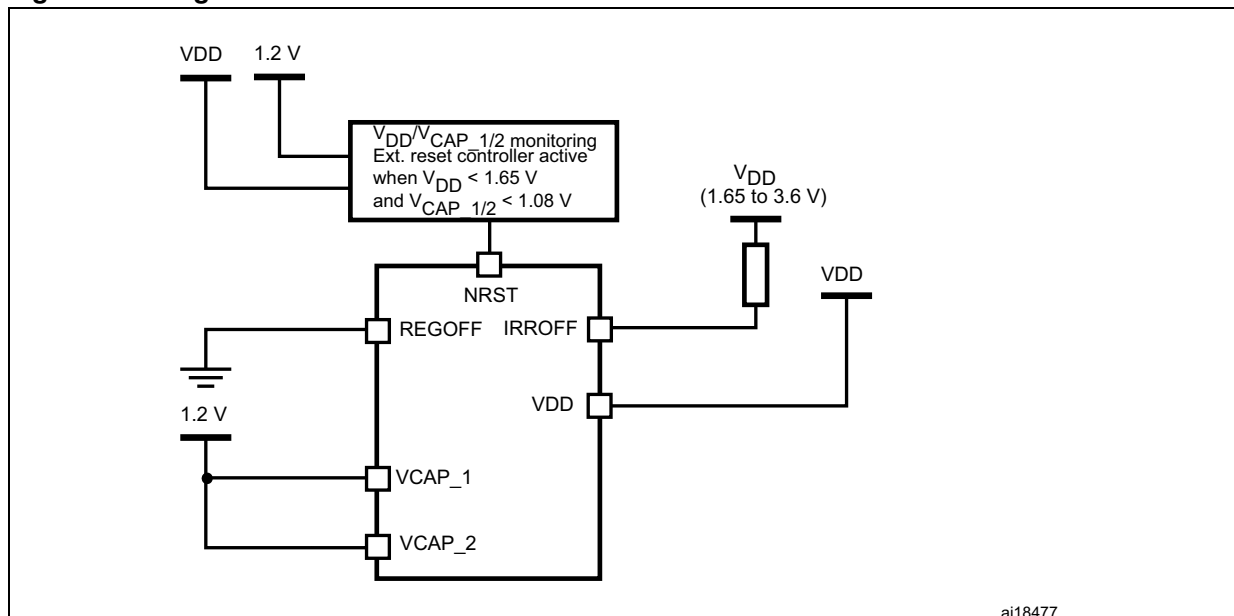
A.2 Application example with regulator OFF

Figure 84. Regulator OFF/internal reset ON



1. This mode is available only on UFBGA176 and WLCSP64+2 packages.
2. In regulator bypass mode, PA0 is used as power-on reset. The connection between PA0 and NRST can consequently prevent debug connection. If the debug connection under reset or pre-reset is required, the user must manage the reset and the power-on reset separately.

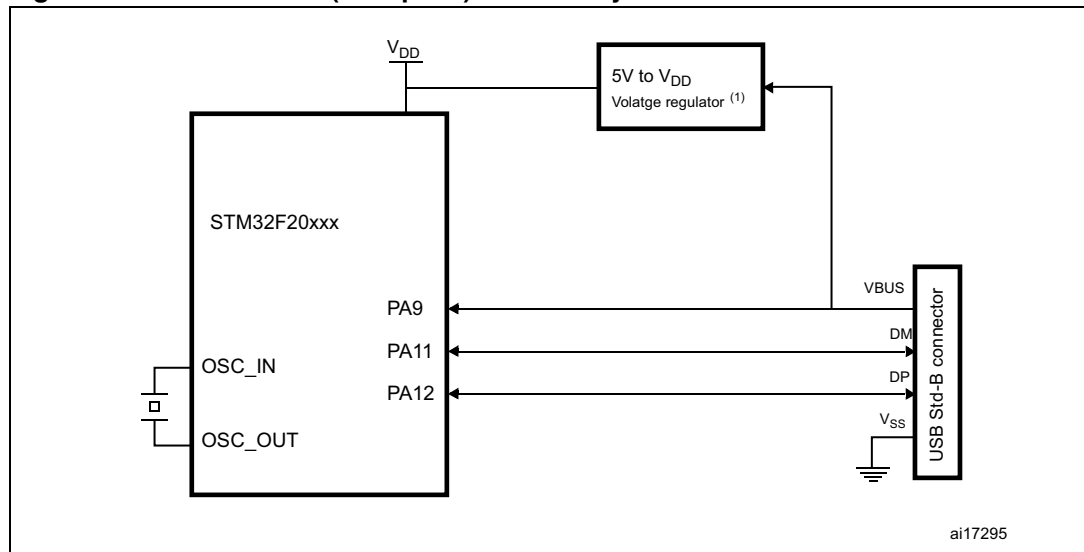
Figure 85. Regulator OFF/ internal reset OFF



1. This mode is available only on WLCSP64+2 package.

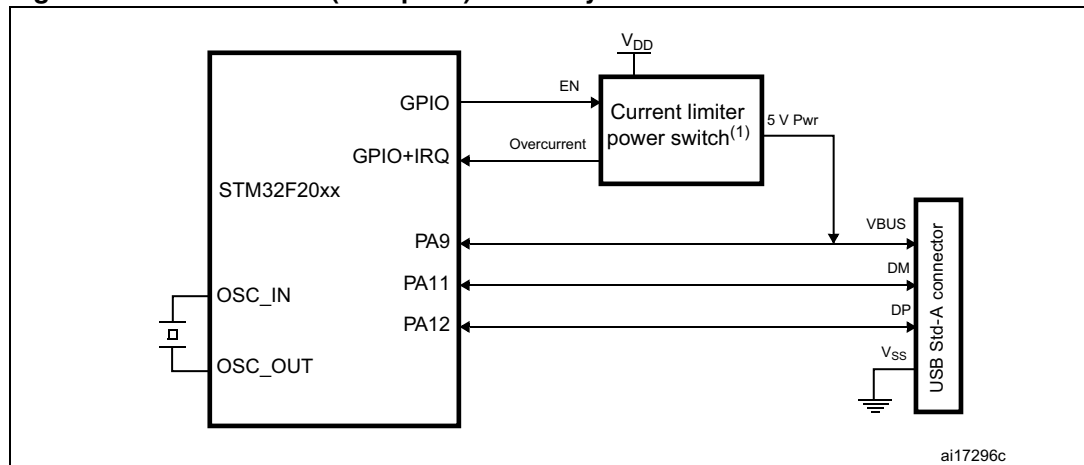
A.3 USB OTG full speed (FS) interface solutions

Figure 86. USB OTG FS (full speed) device-only connection



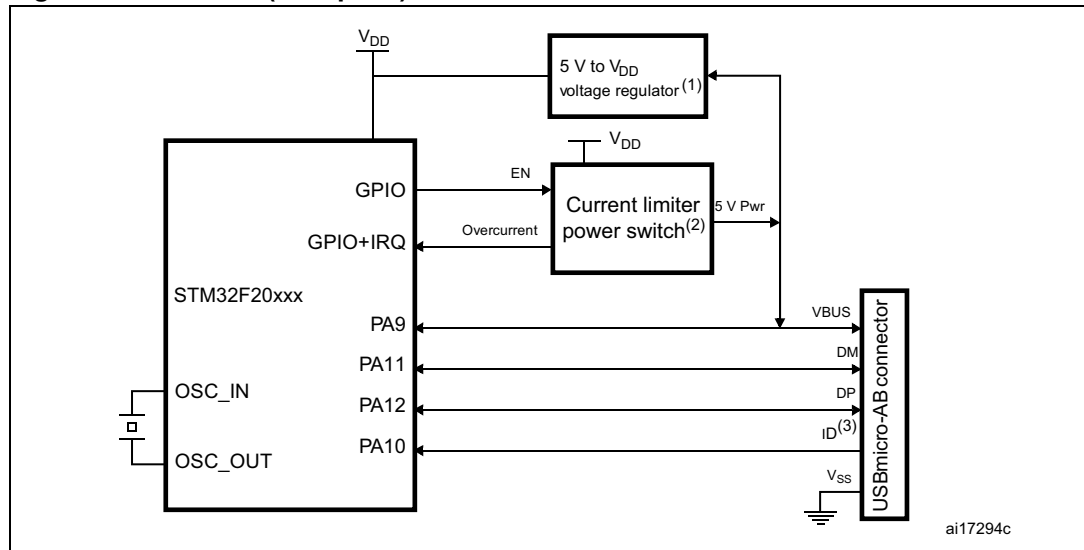
1. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

Figure 87. USB OTG FS (full speed) host-only connection



1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

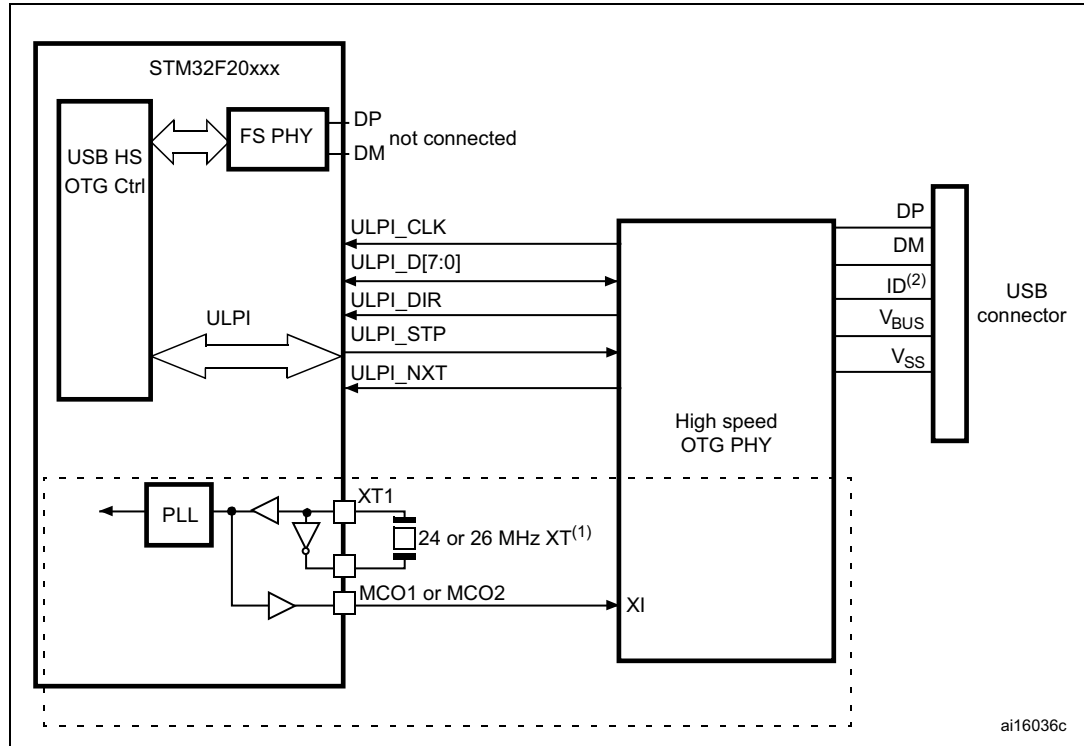
Figure 88. OTG FS (full speed) connection dual-role with internal PHY



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

A.4 USB OTG high speed (HS) interface solutions

Figure 89. OTG HS (high speed) device connection, host and dual-role in high-speed mode with external PHY



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F20x with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.

A.5 Complete audio player solutions

Two solutions are offered, illustrated in *Figure 90* and *Figure 91*.

Figure 90 shows storage media to audio DAC/amplifier streaming using a software Codec. This solution implements an audio crystal to provide audio class I²S accuracy on the master clock (0.5% error maximum, see the Serial peripheral interface section in the reference manual for details).

Figure 90. Complete audio player solution 1

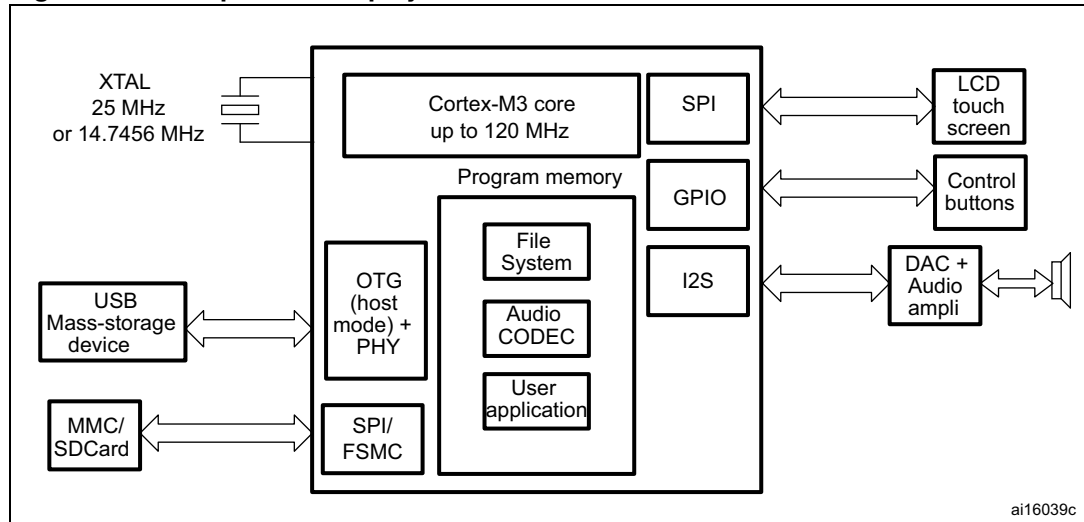
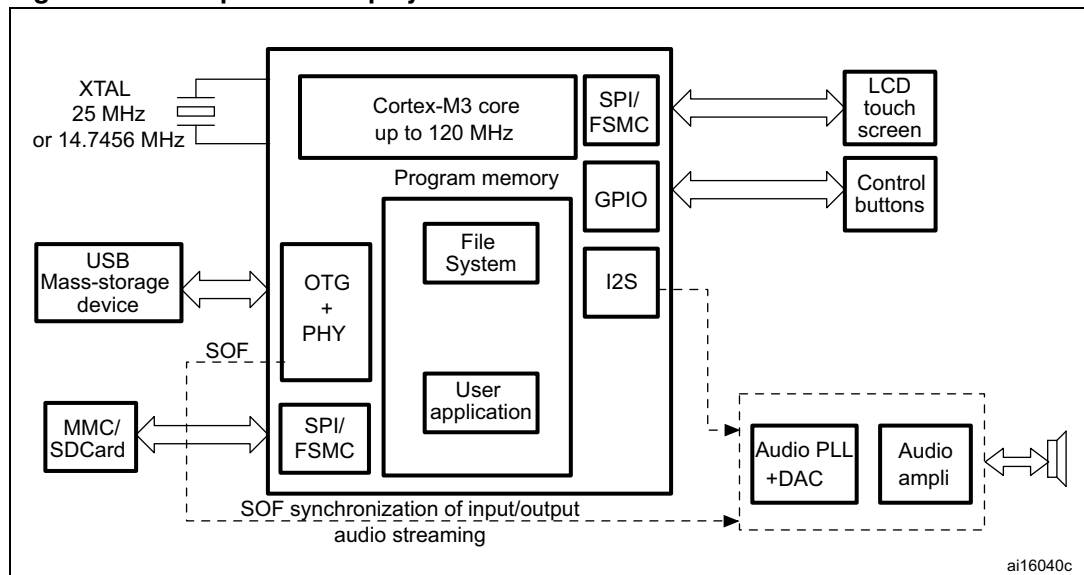


Figure 91 shows storage media to audio Codec/amplifier streaming with SOF synchronization of input/output audio streaming using a hardware Codec.

Figure 91. Complete audio player solution 2



1. SOF = start of frame.

Figure 92. Audio player solution using PLL, PLLI2S, USB and 1 crystal

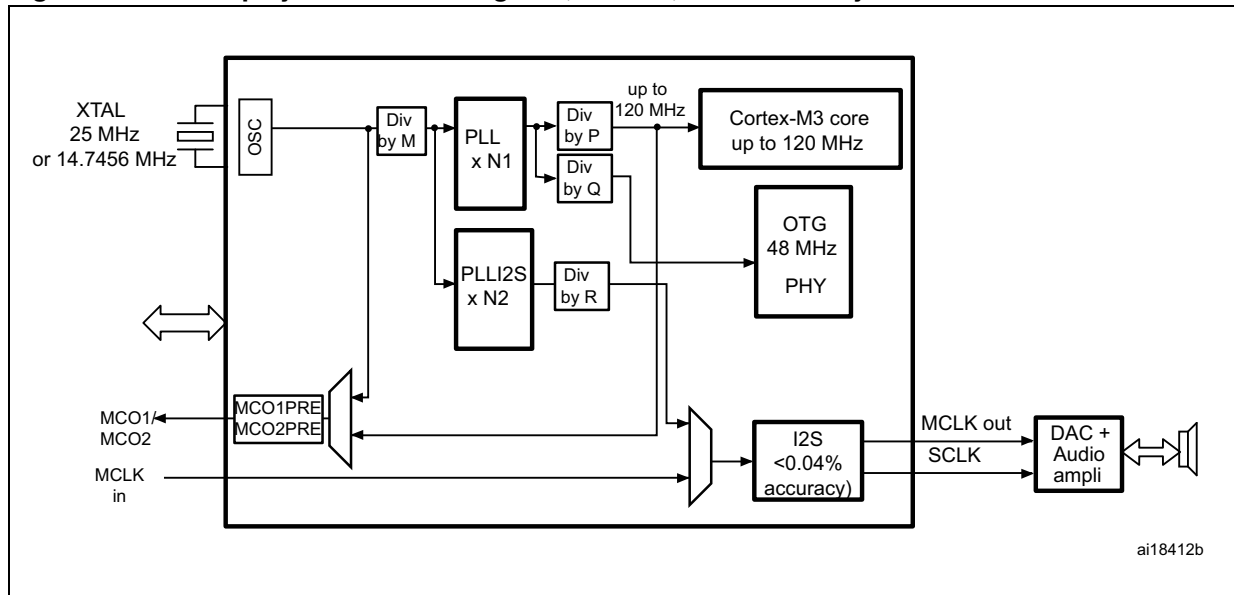


Figure 93. Audio PLL (PLLI2S) providing accurate I2S clock

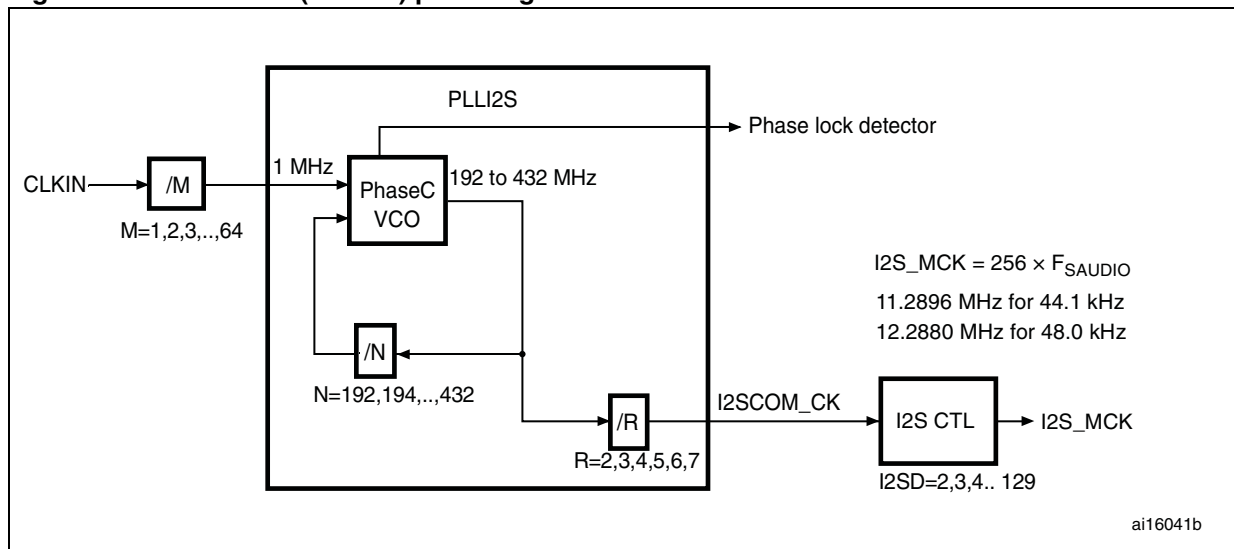
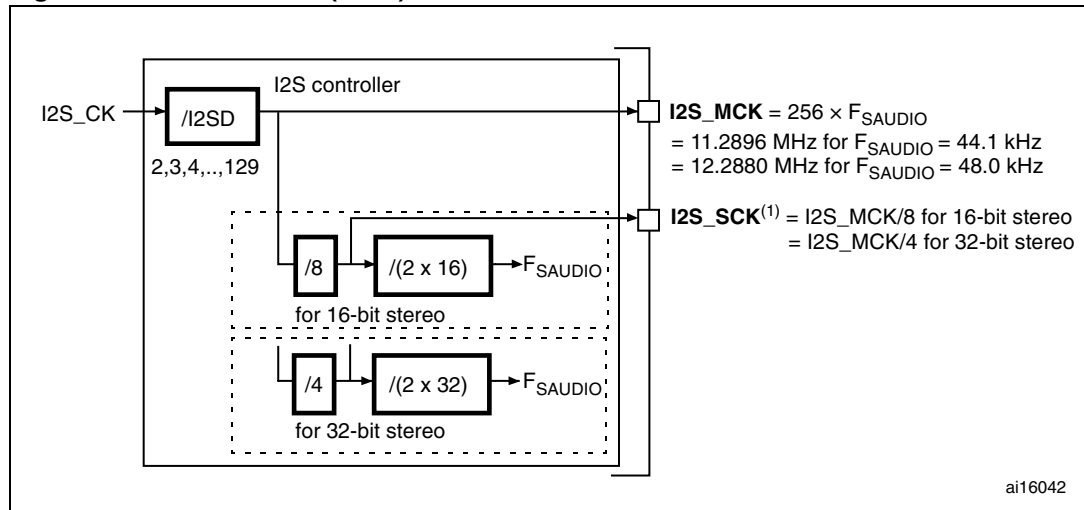
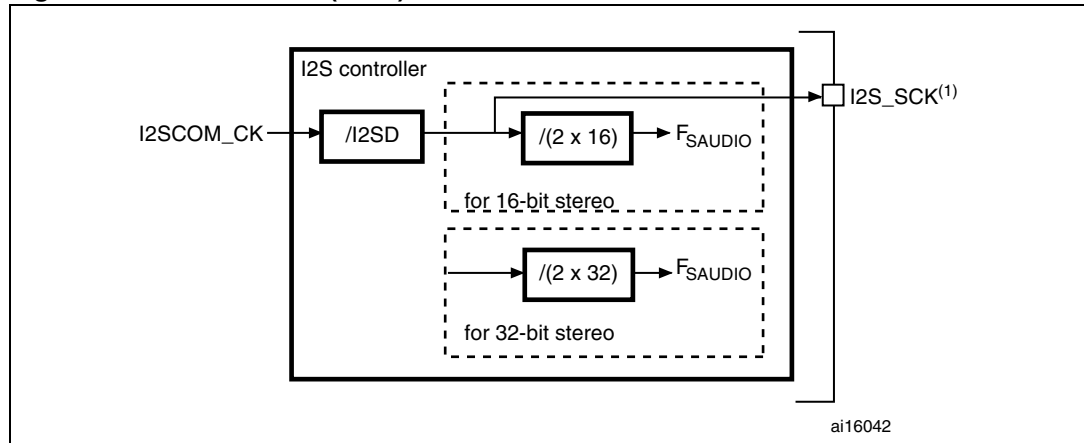


Figure 94. Master clock (MCK) used to drive the external audio DAC



1. $I2S_SCK$ is the I2S serial clock to the external audio DAC (not to be confused with $I2S_CK$).

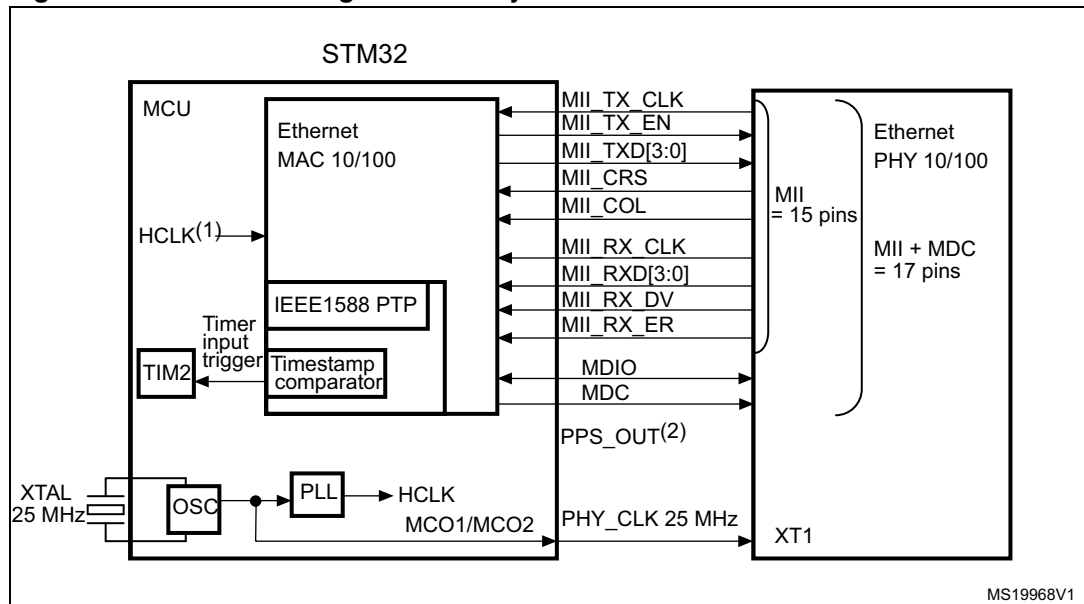
Figure 95. Master clock (MCK) not used to drive the external audio DAC



1. $I2S_SCK$ is the I2S serial clock to the external audio DAC (not to be confused with $I2S_CK$).

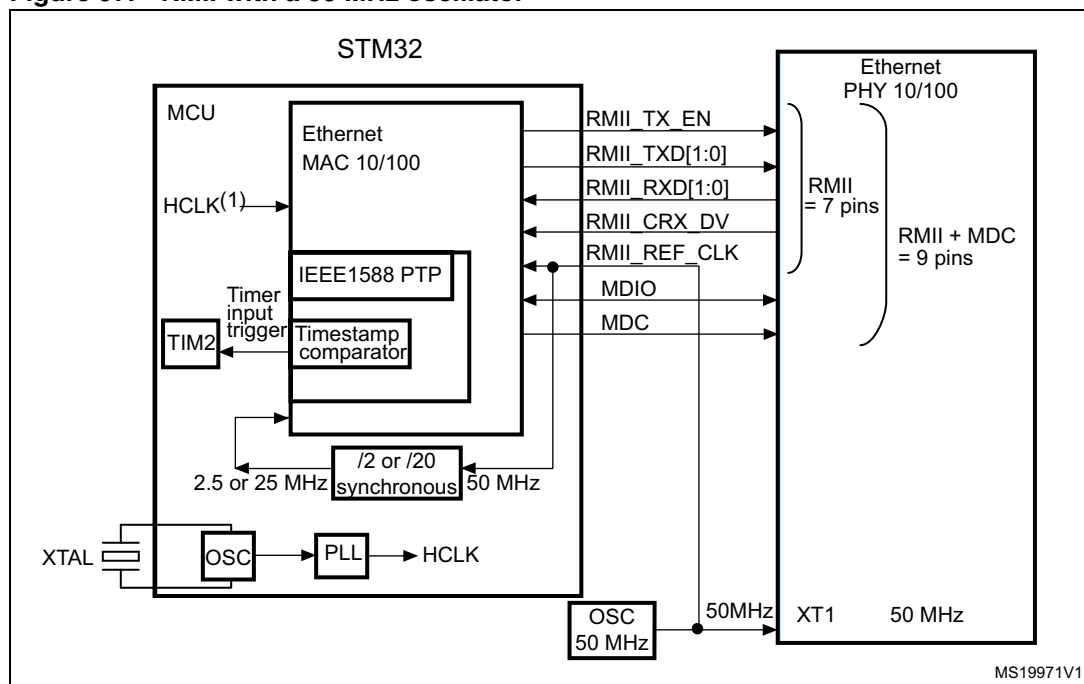
A.6 Ethernet interface solutions

Figure 96. MII mode using a 25 MHz crystal



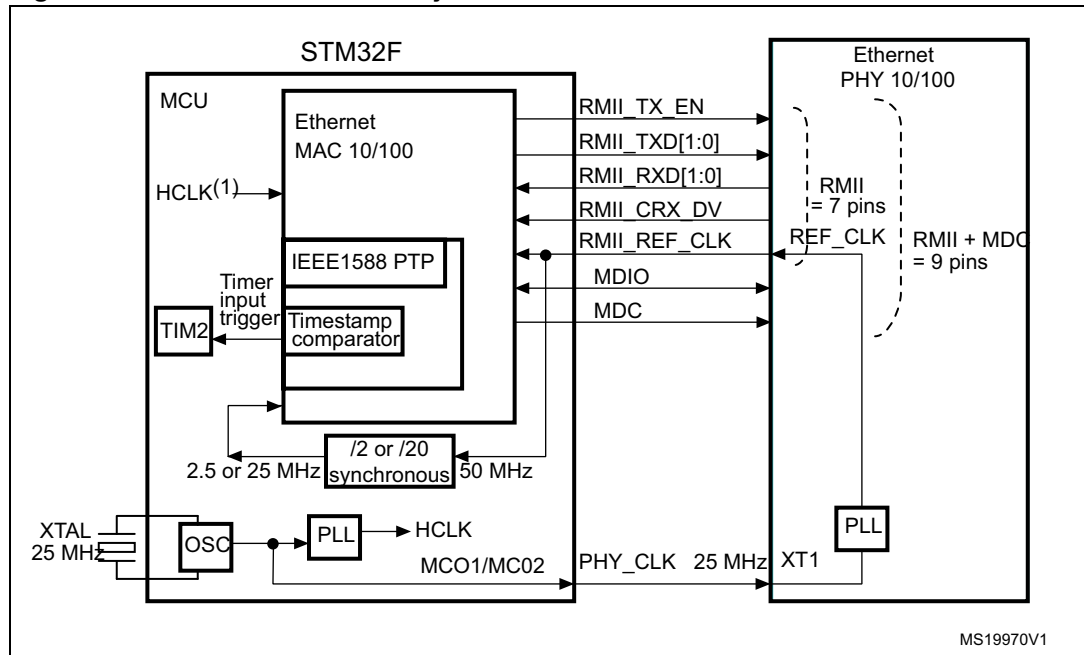
1. f_{HCLK} must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP optional signal.

Figure 97. RMIi with a 50 MHz oscillator



1. f_{HCLK} must be greater than 25 MHz.

Figure 98. RMIi with a 25 MHz crystal and PHY with PLL



1. f_{HCLK} must be greater than 25 MHz.
2. The 25 MHz (PHY_CLK) must be derived directly from the HSE oscillator, before the PLL block.

8 Revision history

Table 94. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 05-Jun-2009 | 1 | Initial release. |
| 09-Oct-2009 | 2 | Document status promoted from Target specification to Preliminary data. In Table 6: STM32F20x pin and ball definitions : – Note 4 updated – V _{DD_SA} and V _{DD_3} pins inverted (Figure 10: STM32F20x LQFP100 pinout , Figure 11: STM32F20x LQFP144 pinout and Figure 12: STM32F20x LQFP176 pinout corrected accordingly). Section 6.1: Package mechanical data changed to LQFP with no exposed pad. |
| 01-Feb-2010 | 3 | LFBGA144 package removed. STM32F203xx part numbers removed. Part numbers with 128 and 256 Kbyte Flash densities added. Encryption features removed. PC13-TAMPER-RTC renamed to PC13-RTC_AF1 and PI8-TAMPER-RTC renamed to PI8-RTC_AF2. |
| 13-Jul-2010 | 4 | Renamed high-speed SRAM, system SRAM. Removed combination: 128 KBytes Flash memory in LQFP144. Added UFBGA176 package. Added note 1 related to LQFP176 package in Table 2 , Figure 12 , and Table 92 . Added information on ART accelerator and audio PLL (PLLI2S). Added Table 5: USART feature comparison . Several updates on Table 6: STM32F20x pin and ball definitions and Table 8: Alternate function mapping . ADC, DAC, oscillator, RTC_AF, WKUP and VBUS signals removed from alternate functions and moved to the “other functions” column in Table 6: STM32F20x pin and ball definitions . TRACESWO added in Figure 4: STM32F20x block diagram , Table 6: STM32F20x pin and ball definitions , and Table 8: Alternate function mapping . XTAL oscillator frequency updated on cover page, in Figure 4: STM32F20x block diagram and in Section 2.2.11: External interrupt/event controller (EXTI) . Updated list of peripherals used for boot mode in Section 2.2.13: Boot modes . Added Regulator bypass mode in Section 2.2.16: Voltage regulator , and Section 5.3.4: Operating conditions at power-up / power-down (regulator OFF) . Updated Section 2.2.17: Real-time clock (RTC), backup SRAM and backup registers . Added Note Note : in Section 2.2.18: Low-power modes . Added SPI TI protocol in Section 2.2.23: Serial peripheral interface (SPI) . |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|------------------|---|
| 13-Jul-2010 | 4 (continued) | <p>Added USB OTG_FS features in Section 2.2.28: Universal serial bus on-the-go full-speed (OTG_FS).</p> <p>Updated V_{CAP_1} and V_{CAP_2} capacitor value to 2.2 µF in Figure 17: Power supply scheme.</p> <p>Removed DAC, modified ADC limitations, and updated I/O compensation for 1.8 to 2.1 V range in Table 13: Limitations depending on the operating power supply range.</p> <p>Added V_{BORL}, V_{BORM}, V_{BORH} and I_{RUSH} in Table 17: Embedded reset and power control block characteristics.</p> <p>Removed table Typical current consumption in Sleep mode with Flash memory in Deep power down mode. Merged typical and maximum current consumption sections and added Table 18: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled), Table 19: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM, Table 20: Typical and maximum current consumption in Sleep mode, Table 21: Typical and maximum current consumptions in Stop mode, Table 22: Typical and maximum current consumptions in Standby mode, and Table 23: Typical and maximum current consumptions in VBAT mode.</p> <p>Update Table 32: Main PLL characteristics and added Section 5.3.11: PLL spread spectrum clock generation (SSCG) characteristics.</p> <p>Added Note 8 for CIO in Table 44: I/O static characteristics.</p> <p>Updated Section 5.3.18: TIM timer characteristics.</p> <p>Added T_{NRST_OUT} in Table 47: NRST pin characteristics.</p> <p>Updated Table 50: I2C characteristics.</p> <p>Removed 8-bit data in and data out waveforms from Figure 45: ULPI timing diagram.</p> <p>Removed note related to ADC calibration in Table 65. Section 5.3.20: 12-bit ADC characteristics: ADC characteristics tables merged into one single table; tables ADC conversion time and ADC accuracy removed.</p> <p>Updated Table 66: DAC characteristics.</p> <p>Updated Section 5.3.22: Temperature sensor characteristics and Section 5.3.23: VBAT monitoring characteristics.</p> <p>Update Section 5.3.26: Camera interface (DCMI) timing specifications.</p> <p>Added Section 5.3.27: SD/SDIO MMC card host interface (SDIO) characteristics, and Section 5.3.28: RTC characteristics.</p> <p>Added Section 6.2: Thermal characteristics. Updated Table 89: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm package mechanical data and Figure 81: LQFP176 - Low profile quad flat package 24 × 24 × 1.4 mm, package outline.</p> <p>Changed tape and reel code to TX in Table 92: Ordering information scheme.</p> <p>Added Table 93: Main applications versus package for STM32F2xxx microcontrollers. Updated figures in Appendix A.3: USB OTG full speed (FS) interface solutions and A.4: USB OTG high speed (HS) interface solutions. Updated Figure 92: Audio player solution using PLL, PLLI2S, USB and 1 crystal and Figure 93: Audio PLL (PLLI2S) providing accurate I2S clock.</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 25-Nov-2010 | 5 | <p>Update I/Os in Section : Features.</p> <p>Added WLCSP66(64+2) package. Added note 1 related to LQFP176 on cover page.</p> <p>Added trademark for ART accelerator. Updated Section 2.2.2: Adaptive real-time memory accelerator (ART Accelerator™).</p> <p>Updated Figure 5: Multi-AHB matrix.</p> <p>Added case of BOR inactivation using IRROFF on WLCSP devices in Section 2.2.15: Power supply supervisor.</p> <p>Reworked Section 2.2.16: Voltage regulator to clarify regulator off modes. Renamed PDROFF, IRROFF in the whole document.</p> <p>Added Section 2.2.19: VBAT operation.</p> <p>Updated LIN and IrDA features for UART4/5 in Table 5: USART feature comparison.</p> <p>Table 6: STM32F20x pin and ball definitions: Modified V_{DD_3} pin, and added note related to the FSMC_NL pin; renamed BYPASS-REG REGOFF, and add IRROFF pin; renamed USART4/5 UART4/5. USART4 pins renamed UART4.</p> <p>Changed V_{SS_SA} to V_{SS}, and V_{DD_SA} pin reserved for future use.</p> <p>Updated maximum HSE crystal frequency to 26 MHz.</p> <p>Section 5.2: Absolute maximum ratings: Updated V_{IN} minimum and maximum values and note related to five-volt tolerant inputs in Table 9: Voltage characteristics. Updated I_{INJ(PIN)} maximum values and related notes in Table 10: Current characteristics.</p> <p>Updated V_{DDA} minimum value in Table 12: General operating conditions.</p> <p>Added Note 2 and updated Maximum CPU frequency in Table 13: Limitations depending on the operating power supply range, and added Figure 19: Number of wait states versus fCPU and VDD range.</p> <p>Added brownout level 1, 2, and 3 thresholds in Table 17: Embedded reset and power control block characteristics.</p> <p>Changed f_{OSC_IN} maximum value in Table 28: HSE 4-26 MHz oscillator characteristics.</p> <p>Changed f_{PLL_IN} maximum value in Table 32: Main PLL characteristics, and updated jitter parameters in Table 33: PLLI2S (audio PLL) characteristics.</p> <p>Section 5.3.16: I/O port characteristics: updated V_{IH} and V_{IL} in Table 44: I/O static characteristics.</p> <p>Added Note 1 below Table 45: Output voltage characteristics.</p> <p>Updated R_{PD} and R_{PU} parameter description in Table 55: USB OTG FS DC electrical characteristics.</p> <p>Updated V_{REF+} minimum value in Table 64: ADC characteristics.</p> <p>Updated Table 69: Embedded internal reference voltage.</p> <p>Removed Ethernet and USB2 for 64-pin devices in Table 93: Main applications versus package for STM32F2xxx microcontrollers.</p> <p>Added A.2: Application example with regulator OFF, removed “OTG FS connection with external PHY” figure, updated Figure 87, Figure 88, and Figure 90 to add STULPI01B.</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 22-Apr-2011 | 6 | <p>Changed datasheet status to “Full Datasheet”.</p> <p>Introduced concept of SRAM1 and SRAM2.</p> <p>LQFP176 package now in production and offered only for 256 Kbyte and 1 Mbyte devices. Availability of WLCSP64+2 package limited to 512 Kbyte and 1 Mbyte devices.</p> <p>Updated Figure 3: Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package and Figure 2: Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package.</p> <p>Added camera interface for STM32F207Vx devices in Table 2: STM32F205xx features and peripheral counts.</p> <p>Removed 16 MHz internal RC oscillator accuracy in Section 2.2.12: Clocks and startup.</p> <p>Updated Section 2.2.16: Voltage regulator.</p> <p>Modified I²S sampling frequency range in Section 2.2.12: Clocks and startup, Section 2.2.24: Inter-integrated sound (I2S), and Section 2.2.30: Audio PLL (PLL12S).</p> <p>Updated Section 2.2.17: Real-time clock (RTC), backup SRAM and backup registers and description of TIM2 and TIM5 in Section : General-purpose timers (TIMx).</p> <p>Modified maximum baud rate (oversampling by 16) for USART1 in Table 5: USART feature comparison.</p> <p>Updated note related to RFU pin below Figure 10: STM32F20x LQFP100 pinout, Figure 11: STM32F20x LQFP144 pinout, Figure 12: STM32F20x LQFP176 pinout, Figure 13: STM32F20x UFBGA176 ballout, and Table 6: STM32F20x pin and ball definitions.</p> <p>In Table 6: STM32F20x pin and ball definitions,:changed I2S2_CK and I2S3_CK to I2S2_SCK and I2S3_SCK, respectively; added PA15 and TT (3.6 V tolerant I/O).</p> <p>Added RTC_50Hz as PB15 alternate function in Table 6: STM32F20x pin and ball definitions and Table 8: Alternate function mapping.</p> <p>Removed ETH_RMII_TX_CLK for PC3/AF11 in Table 8: Alternate function mapping.</p> <p>Updated Table 9: Voltage characteristics and Table 10: Current characteristics.</p> <p>T_{STG} updated to -65 to +150 in Table 11: Thermal characteristics.</p> <p>Added CEXT, ESL, and ESR in Table 12: General operating conditions as well as Section 5.3.2: VCAP1/VCAP2 external capacitor.</p> <p>Modified Note 4 in Table 13: Limitations depending on the operating power supply range.</p> <p>Updated Table 15: Operating conditions at power-up / power-down (regulator ON), and Table 16: Operating conditions at power-up / power-down (regulator OFF).</p> <p>Added OSC_OUT pin in Figure 15: Pin loading conditions. and Figure 16: Pin input voltage.</p> <p>Updated Figure 17: Power supply scheme to add IRROFF and REGOFF pins and modified notes.</p> <p>Updated V_{PVD}, V_{BOR1}, V_{BOR2}, V_{BOR3}, T_{RSTTEMPO} typical value, and I_{RUSH}, added E_{RUSH} and Note 3 in Table 17: Embedded reset and power control block characteristics.</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|------------------|--|
| 22-Apr-2011 | 6 (continued) | <p>Updated <i>Typical and maximum current consumption</i> conditions, as well as <i>Table 18: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)</i> and <i>Table 19: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM</i>. Added <i>Figure 21</i>, <i>Figure 22</i>, <i>Figure 23</i>, and <i>Figure 24</i>.</p> <p>Updated <i>Table 20: Typical and maximum current consumption in Sleep mode</i>, and added <i>Figure 25</i> and <i>Figure 26</i>.</p> <p>Updated <i>Table 21: Typical and maximum current consumptions in Stop mode</i>. Added <i>Figure 27: Typical current consumption vs temperature in Stop mode</i>.</p> <p>Updated <i>Table 22: Typical and maximum current consumptions in Standby mode</i> and <i>Table 23: Typical and maximum current consumptions in VBAT mode</i>.</p> <p>Updated <i>On-chip peripheral current consumption</i> conditions and <i>Table 24: Peripheral current consumption</i>.</p> <p>Updated $t_{WUSTDBY}$ and t_{WUSTOP} and added <i>Note 3</i> in <i>Table 25: Low-power mode wakeup timings</i>.</p> <p>Maximum f_{HSE_ext} and minimum $t_{w(HSE)}$ values updated in <i>Table 26: High-speed external user clock characteristics</i>.</p> <p>Updated C and g_m in <i>Table 28: HSE 4-26 MHz oscillator characteristics</i>. Updated R_F, I_2, g_m, and $t_{su(LSE)}$ in <i>Table 29: LSE oscillator characteristics (fLSE = 32.768 kHz)</i>.</p> <p>Added <i>Note 1</i> and updated ACC_{HSI}, $IDD_{(HSI)}$, and $t_{su(HSI)}$ in <i>Table 30: HSI oscillator characteristics</i>. Added <i>Figure 32: ACCHSI versus temperature</i>.</p> <p>Updated f_{LSI}, $t_{su(LSI)}$ and $IDD_{(LSI)}$ in <i>Table 31: LSI oscillator characteristics</i>. Added <i>Figure 33: ACCLSI versus temperature</i></p> <p><i>Table 32: Main PLL characteristics</i>: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLL)}$ and $IDD_{A(PLL)}$, added <i>Note 2</i> for f_{PLL_IN} minimum and maximum values.</p> <p><i>Table 33: PLLI2S (audio PLL) characteristics</i>: removed note 1, updated t_{LOCK}, jitter, $IDD_{(PLLI2S)}$ and $IDD_{A(PLLI2S)}$, added <i>Note 2</i> for f_{PLLI2S_IN} minimum and maximum values.</p> <p>Added <i>Note 1</i> in <i>Table 34: SSCG parameters constraint</i>.</p> <p>Updated <i>Table 35: Flash memory characteristics</i>. Modified <i>Table 36: Flash memory programming</i> and added <i>Note 2</i> for t_{prog}. Updated t_{prog} and added <i>Note 1</i> in <i>Table 37: Flash memory programming with VPP</i>. Modified <i>Figure 37: Recommended NRST pin protection</i>.</p> <p>Updated <i>Table 40: EMI characteristics</i> and EMI monitoring conditions in <i>Section : Electromagnetic Interference (EMI)</i>. Added <i>Note 2</i> related to $V_{ESD(HBM)}$ in <i>Table 41: ESD absolute maximum ratings</i>.</p> <p>Updated <i>Table 44: I/O static characteristics</i>.</p> <p>Added <i>Section 5.3.15: I/O current injection characteristics</i>.</p> <p>Modified maximum frequency values and conditions in <i>Table 46: I/O AC characteristics</i>.</p> <p>Updated $t_{res(TIM)}$ in <i>Table 48: Characteristics of TIMx connected to the APB1 domain</i>. Modified $t_{res(TIM)}$ and f_{EXT} <i>Table 49: Characteristics of TIMx connected to the APB2 domain</i>.</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|------------------|--|
| 22-Apr-2011 | 6 (continued) | <p>Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, and $t_{f(SCK)}$ to $t_{f(SCL)}$ in Table 50: I2C characteristics and in Figure 38: I2C bus AC waveforms and measurement circuit.</p> <p>Added Table 55: USB OTG FS DC electrical characteristics and updated Table 56: USB OTG FS electrical characteristics.</p> <p>Updated V_{DD} minimum value in Table 60: Ethernet DC electrical characteristics.</p> <p>Updated Table 64: ADC characteristics and R_{AIN} equation.</p> <p>Updated R_{AIN} equation. Updated Table 66: DAC characteristics.</p> <p>Updated t_{START} in Table 67: TS characteristics.</p> <p>Updated R typical value in Table 68: VBAT monitoring characteristics.</p> <p>Updated Table 69: Embedded internal reference voltage.</p> <p>Modified FSMC_NOE waveform in Figure 54: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms. Shifted end of FSMC_NEx/NADV/addresses/NWE/NOE/NWAIT of a half FSMC_CLK period, changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, and $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and updated data latency from 1 to 0 in Figure 58: Synchronous multiplexed NOR/PSRAM read timings, Figure 59: Synchronous multiplexed PSRAM write timings, Figure 60: Synchronous non-multiplexed NOR/PSRAM read timings, and Figure 61: Synchronous non-multiplexed PSRAM write timings,</p> <p>Changed $t_{d(CLKH-NExH)}$ to $t_{d(CLKL-NExH)}$, $t_{d(CLKH-AIV)}$ to $t_{d(CLKL-AIV)}$, $t_{d(CLKH-NOEH)}$ to $t_{d(CLKL-NOEH)}$, $t_{d(CLKH-NWEH)}$ to $t_{d(CLKL-NWEH)}$, and modified $t_{w(CLK)}$ minimum value in Table 74, Table 75, Table 76, and Table 77.</p> <p>Updated note 2 in Table 70, Table 71, Table 72, Table 73, Table 74, Table 75, Table 76, and Table 77.</p> <p>Modified $t_{h(NIOWR-D)}$ in Figure 67: PC Card/CompactFlash controller waveforms for I/O space write access.</p> <p>Modified FSMC_NCEx signal in Figure 68: NAND controller waveforms for read access, Figure 69: NAND controller waveforms for write access, Figure 70: NAND controller waveforms for common memory read access, and Figure 71: NAND controller waveforms for common memory write access</p> <p>Specified Full speed (FS) mode for Figure 89: USB OTG HS peripheral-only connection in FS mode and Figure 90: USB OTG HS host-only connection in FS mode.</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 14-Jun-2011 | 7 | <p>Added SDIO in Table 2: STM32F205xx features and peripheral counts. Updated V_{IN} for 5V tolerant pins in Table 9: Voltage characteristics. Updated jitter parameters description in Table 32: Main PLL characteristics. Remove jitter values for system clock in Table 33: PLLI2S (audio PLL) characteristics. Updated Table 40: EMI characteristics. Update Note 2 in Table 50: I2C characteristics. Updated Avg_Slope typical value and T_{S_temp} minimum value in Table 67: TS characteristics. Updated T_{S_vbat} minimum value in Table 68: VBAT monitoring characteristics. Updated $T_{S_vrefint}$ minimum value in Table 69: Embedded internal reference voltage. Added Software option in Section 7: Part numbering. In Table 93: Main applications versus package for STM32F2xxx microcontrollers, renamed USB1 and USB2, USB OTG FS and USB OTG HS, respectively; and removed USB OTG FS and camera interface for 64-pin package; added USB OTG HS on 64-pin package; added Note 1 and Note 2.</p> |
| 20-Dec-2011 | 8 | <p>Updated SDIO register addresses in Figure 14: Memory map. Updated Figure 3: Compatible board design between STM32F10xx and STM32F2xx for LQFP144 package, Figure 2: Compatible board design between STM32F10xx and STM32F2xx for LQFP100 package, Figure 1: Compatible board design between STM32F10xx and STM32F2xx for LQFP64 package, and added Figure 4: Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package. Updated Section 2.2.3: Memory protection unit. Updated Section 2.2.6: Embedded SRAM. Updated Section 2.2.28: Universal serial bus on-the-go full-speed (OTG_FS) to remove external FS OTG PHY support. In Table 6: STM32F20x pin and ball definitions: changed SPI2_MCK and SPI3_MCK to I2S2_MCK and I2S3_MCK, respectively. Added ETH_RMII_TX_EN alternate function to PG11. Added EVENTOUT in the list of alternate functions for I/O pin/balls. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions. In Table 8: Alternate function mapping: changed I2S3_SCK to I2S3_MCK for PC7/AF6, added FSMC_NCE3 for PG9, FSMC_NE3 for PG10, and FSMC_NCE2 for PD7. Removed OTG_FS_SDA, OTG_FS_SCL and OTG_FS_INTN alternate functions. Changed I2S3_SCK into I2S3_MCK for PC7/AF6. Updated peripherals corresponding to AF12. Removed CEXT and ESR from Table 12: General operating conditions.</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|------------------|--|
| 20-Dec-2011 | 8 (continued) | <p>Added maximum power consumption at $T_A=25\text{ }^\circ\text{C}$ in Table 21: Typical and maximum current consumptions in Stop mode.</p> <p>Updated md minimum value in Table 34: SSCG parameters constraint.</p> <p>Added examples in Section 5.3.11: PLL spread spectrum clock generation (SSCG) characteristics.</p> <p>Updated Table 52: SPI characteristics and Table 53: I2S characteristics.</p> <p>Updated Figure 45: ULPI timing diagram and Table 59: ULPI timing.</p> <p>Updated Table 61: Dynamics characteristics: Ethernet MAC signals for SMI, Table 62: Dynamics characteristics: Ethernet MAC signals for RMII, and Table 63: Dynamics characteristics: Ethernet MAC signals for MII.</p> <p>Section 5.3.25: FSMC characteristics: updated Table 70 to Table 81, changed C_L value to 30 pF, and modified FSMC configuration for asynchronous timings and waveforms. Updated Figure 59: Synchronous multiplexed PSRAM write timings.</p> <p>Updated Table 82: DCMI characteristics.</p> <p>Updated Table 90: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm mechanical data.</p> <p>Updated Table 92: Ordering information scheme.</p> <p>Appendix A.3: USB OTG full speed (FS) interface solutions: updated Figure 87: USB OTG FS (full speed) host-only connection and added Note 2, updated Figure 88: OTG FS (full speed) connection dual-role with internal PHY and added Note 3 and Note 4, modified Figure 89: OTG HS (high speed) device connection, host and dual-role in high-speed mode with external PHY and added Note 2.</p> <p>Appendix A.4: USB OTG high speed (HS) interface solutions: removed figures USB OTG HS device-only connection in FS mode and USB OTG HS host-only connection in FS mode, updated Figure 89: OTG HS (high speed) device connection, host and dual-role in high-speed mode with external PHY.</p> <p>Added Appendix A.6: Ethernet interface solutions.</p> <p>Updated disclaimer on last page.</p> |
| 24-Apr-2012 | 9 | <p>Updated V_{DD} minimum value in Section 2: Description.</p> <p>Updated number of USB OTG HS and FS, modified packages for STM32F2071x part numbers, added Note 1 related to FSMC and Note 2 related to SPI/I2S, and updated Note 3 in Table 2: STM32F205xx features and peripheral counts and Table 3: STM32F207xx features and peripheral counts.</p> <p>Added Note 2 and update TIM5 in Figure 4: STM32F20x block diagram.</p> <p>Updated maximum number of maskable interrupts in Section 2.2.10: Nested vectored interrupt controller (NVIC).</p> <p>Updated V_{DD} minimum value in Section 2.2.14: Power supply schemes.</p> <p>Updated Note a in Section : Regulator ON.</p> <p>Removed STM32F205xx in Section 2.2.28: Universal serial bus on-the-go full-speed (OTG_FS).</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|------------------|---|
| 24-Apr-2012 | 9 (continued) | <p>Removed support of I2C for OTG PHY in Section 2.2.29: Universal serial bus on-the-go high-speed (OTG_HS).</p> <p>Removed OTG_HS_SCL, OTG_HS_SDA, OTG_FS_INTN in Table 6: STM32F20x pin and ball definitions and Table 8: Alternate function mapping.</p> <p>Renamed PH10 alternate function into TIM5_CH1 in Table 8: Alternate function mapping.</p> <p>Added Table 7: FSMC pin definition.</p> <p>Updated Note 1 in Table 12: General operating conditions, Note 2 in Table 13: Limitations depending on the operating power supply range, and Note 1 below Figure 19: Number of wait states versus fCPU and VDD range.</p> <p>Updated V_{POR/PDR} in Table 17: Embedded reset and power control block characteristics.</p> <p>Updated typical values in Table 22: Typical and maximum current consumptions in Standby mode and Table 23: Typical and maximum current consumptions in VBAT mode.</p> <p>Updated Table 28: HSE 4-26 MHz oscillator characteristics and Table 29: LSE oscillator characteristics (fLSE = 32.768 kHz).</p> <p>Updated Table 35: Flash memory characteristics, Table 36: Flash memory programming, and Table 37: Flash memory programming with VPP.</p> <p>Updated Section : Output driving current.</p> <p>Updated Note 3 and removed note related to minimum hold time value in Table 50: I2C characteristics.</p> <p>Updated Table 62: Dynamics characteristics: Ethernet MAC signals for RMII.</p> <p>Updated Note 1, C_{ADC}, I_{VREF+}, and I_{VDDA} in Table 64: ADC characteristics.</p> <p>Updated Note 3 and note concerning ADC accuracy vs. negative injection current in Table 65: ADC accuracy.</p> <p>Updated Note 1 in Table 66: DAC characteristics.</p> <p>Updated Section Figure 83.: UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline.</p> <p>Appendix A.1: Main applications versus package: removed number of address lines for FSMC/NAND in Table 93: Main applications versus package for STM32F2xxx microcontrollers.</p> <p>Appendix A.5: Complete audio player solutions: updated Figure 90: Complete audio player solution 1 and Figure 91: Complete audio player solution 2.</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 29-Oct-2012 | 10 | <p>Changed minimum supply voltage from 1.65 to 1.8 V.</p> <p>Updated number of AHB buses in Section 2: Description and Section 2.2.12: Clocks and startup.</p> <p>Removed Figure 4. Compatible board design between STM32F10xx and STM32F2xx for LQFP176 package.</p> <p>Updated Note 2 below Figure 4: STM32F20x block diagram.</p> <p>Changed System memory to System memory + OTP in Figure 14: Memory map.</p> <p>Added Note 1 below Table 14: VCAP1/VCAP2 operating conditions.</p> <p>Updated V_{DDA} and V_{REF+} decoupling capacitor in Figure 17: Power supply scheme and updated Note 3.</p> <p>Changed simplex mode into half-duplex mode in Section 2.2.24: Inter-integrated sound (I2S).</p> <p>Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively. Changed TIM2_CH1/TIM2_ETR into TIM2_CH1_ETR for PA0 and PA5 in Table 8: Alternate function mapping.</p> <p>Updated note applying to I_{DD} (external clock and all peripheral disabled) in Table 18: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled). Updated Note 3 below Table 20: Typical and maximum current consumption in Sleep mode.</p> <p>Removed f_{HSE_ext} typical value in Table 26: High-speed external user clock characteristics.</p> <p>Updated master I2S clock jitter conditions and values in Table 33: PLLI2S (audio PLL) characteristics.</p> <p>Updated equations in Section 5.3.11: PLL spread spectrum clock generation (SSCG) characteristics.</p> <p>Swapped TTL and CMOS port conditions for V_{OL} and V_{OH} in Table 45: Output voltage characteristics.</p> <p>Updated $V_{IL(NRST)}$ and $V_{IH(NRST)}$ in Table 47: NRST pin characteristics.</p> <p>Updated Table 52: SPI characteristics and Table 53: I2S characteristics. Removed note 1 related to measurement points below Figure 40: SPI timing diagram - slave mode and CPHA = 1, Figure 41: SPI timing diagram - master mode, and Figure 42: I2S slave timing diagram (Philips protocol)(1).</p> <p>Updated t_{HC} in Table 59: ULPI timing.</p> <p>Updated Figure 46: Ethernet SMI timing diagram, Table 61: Dynamics characteristics: Ethernet MAC signals for SMI and Table 63: Dynamics characteristics: Ethernet MAC signals for MII.</p> <p>Update f_{TRIG} in Table 64: ADC characteristics.</p> <p>Updated I_{DDA} description in Table 66: DAC characteristics.</p> <p>Updated note below Figure 51: Power supply and reference decoupling (VREF+ not connected to VDDA) and Figure 52: Power supply and reference decoupling (VREF+ connected to VDDA).</p> |

Table 94. Document revision history (continued)

| Date | Revision | Changes |
|-------------|-------------------|--|
| 29-Oct-2012 | 10 (continued) | <p>Replaced $t_{d(CLKL-NOEL)}$ by $t_{d(CLKH-NOEL)}$ in Table 74: Synchronous multiplexed NOR/PSRAM read timings, Table 76: Synchronous non-multiplexed NOR/PSRAM read timings, Figure 58: Synchronous multiplexed NOR/PSRAM read timings and Figure 60: Synchronous non-multiplexed NOR/PSRAM read timings.</p> <p>Added Figure 82: LQFP176 recommended footprint.</p> <p>Added Note 2 below Figure 84: Regulator OFF/internal reset ON.</p> <p>Updated device subfamily in Table 92: Ordering information scheme.</p> <p>Remove reference to note 2 for USB IOTG FS in Table 93: Main applications versus package for STM32F2xxx microcontrollers.</p> |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

