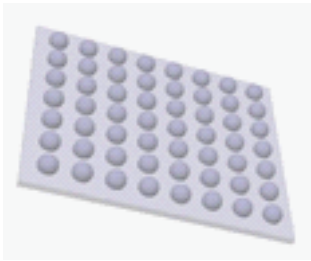
STLED524

Intelligent matrix LED display driver

Datasheet - preliminary data



CSP 56 bumps 0.4 mm pitch 3.4x3.0 mm

Features

- Operating input voltage range from 2.7 V to 5.5 V
- 5x24 LED matrix driver
- Adjustable luminance separately for each LED thanks to internal registers in 255 steps
- Internal registers store 2 patterns
- 4-way scroll function with the possibility to lock column data
- PWM dimming in 255 steps
- Adjustable blanking time
- Automatic slope function
- Cycle time and slope time adjustable for each dot separately
- SPI interface
- Integrated step-up converter with adjustable output voltage
- Integrated LDO with 3.1 V output @ 80 mA
- Boost efficiency 92% at 350 mA
- 2.4 MHz switching frequency
- CSP 56 bumps 0.4 mm pitch 3.4x3.0 mm

Applications

- Appliance user interfaces
- Display driver for handheld units

Description

The STLED524 is a 5x24 dot matrix LED display driver. It can drive each dot with a current up to 20 mA. Rows of the matrix are multiplexed. Each LED in a row is driven by a separate low-side current mirror. Current regulators are supplied by an integrated boost DC-DC converter. Its output voltage can be adjusted by the internal register to optimize efficiency according to the type of LEDs (their forward voltage). This reduces current mirror power dissipation and improves overall efficiency. The STLED524 also includes an internal LDO regulator, which can provide a supply voltage for an additional circuitry. Maximum current, provided by each current mirror, is adjusted by R_{SET} resistor. Current of each LED (dot) can be dimmed in 255 steps due to settings of internal registers.

The STLED524 features PWM dimming in 255 steps. Automatic slope function is also supported. Cycle time and slope time can be adjusted for each LED (dot) separately.

Two patterns can be stored in internal registers. The automatic scrolling of the display content is possible in 4 ways.

Table 1. Device summary

Order code	Package	Packaging
STLED524	CSP	Tape and reel

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1 Application schematic

Figure 1. Application schematic

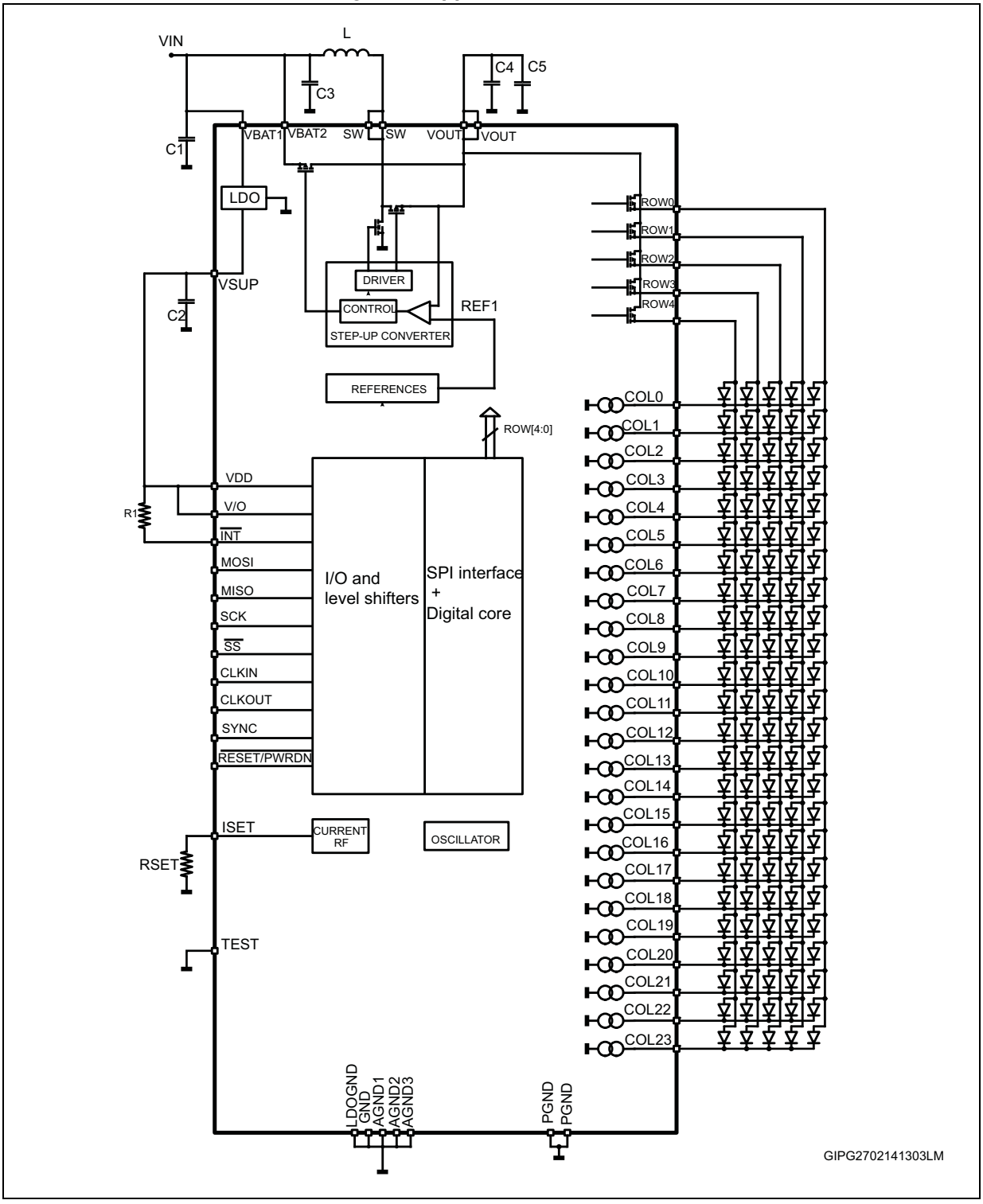


Table 2. Typical external components

Component	Manufacturer	Part number	Value	Size
C1	Murata	GRM188R60J106ME84D	10 µF	0603
C2	Murata	GRM188R60J106ME84D	10 µF	0603
C3	Murata	GRM188R60J106ME84D	10 µF	0603
C4	Murata	GRM21AR60J226ME47L	22 µF	0805
C5	Murata	GRM21AR60J226ME47L	22 µF	0805
L	Murata	LQM2HPN1R0MJC	1.0 µH	2.0x1.6x0.9 mm
R_{SET}			25 k	0402
R1			15 k	0402

Note: All above components refer to a typical application. The device operation is not limited to the choice of these external components.

Figure 2. Pin configuration (top view)

	1	2	3	4	5	6	7
A	GND	VDD	RESET	VSUP	VBAT1	PGND	PGND
B	CLKOUT	CLKIN	SCK	ISET	LDOGND	SW	SW
C	MISO	MOSI	INT	TEST	VBAT2	VOUT	VOUT
D	VIO	SYNC	SS	COL23	COL0	AGND1	ROW0
E	COL21	COL20	COL19	COL22	COL8	COL1	ROW1
F	COL18	COL17	COL15	COL9	COL3	COL2	ROW2
G	COL16	COL13	COL11	AGND2	COL6	COL4	ROW3
H	COL14	COL12	COL10	AGND2	COL7	COL5	ROW4

GIPG2702141312LM

Table 3. Pin description

Name	Pin	Description
VBAT1	A5	LDO supply voltage connection(1)
VBAT2	C5	Supply voltage connection(1)
SW	B6, B7	Coil connection
VOUT	C6, C7	Step-up converter output voltage
VSUP	A4	LDO output voltage
ROW 0-4	D7, E7, F7, G7, H7	Matrix row connections
COL 0-23	D4,D5 E1-E6, F1-F6, G1-G3, G5-G6, H1-H3, H5-H6	Matrix column connections
PGND	A6, A7	Power ground
AGND1	D6	Analog ground 1
AGND2	G4, H4	Analog ground 2
GND	A1	Ground
VDD	A2	Logic supply voltage
VIO	D1	I/O pin supply voltage
RESET/PWRDN	A3	Reset input, active low. When low, the device is in shutdown mode
MISO	C1	Master IN slave OUT (SPI bus)
MOSI	C2	Master OUT slave IN (SPI bus)
SS	D3	Slave select (SPI bus)
SCK	B3	SPU bus clock
CLKIN	B2	Clock input
CLKOUT	B1	Clock output
SYNC	D2	Synchronization input
INT	C3	Interrupt open drain output
LDOGND	B5	Boost output voltage setup resistor connection
ISET	B4	Reference current adjustment resistor connection
TEST	C4	Test input. It has to be connected to GND

1. Both VBAT1 and VBAT2 have to be supplied, even though LDO is not used to supply other devices.

2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VBAT1, VBAT2	Supply voltage	-0.3 to +6	V
SW	Switching node	-0.3 to +6	V
VOUT	Output voltage	-0.3 to +6	V
VSUP	LDO output voltage	-0.3 to 3.6	V
VDD	Logic supply voltage	-0.3 to 3.6	V
VIO	I/O pin supply voltage	-0.3 to 3.6	V
ROW 0-4	Row switches	-0.3 to VOUT +0.3	V
COL 0-23	Column current mirrors	-0.3 to +6	V
MISO, MOSI, SCK, SS, INT, THA, CLKIN, CLKOUT, SYNC, RESET	Signal pins	-0.3 to +6	V
ISET	Current setting	-0.3 to 2	V
ESD	Machine model	±200	V
	Human body model	±2000	
	Charged device model	±250	
T_{AMB}	Operating ambient temperature	-30 to 85	°C
T_J	Maximum operating junction temperature	+125	°C
T_{STG}	Storage temperature	-40 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	62	°C/W

Note: This parameter corresponds to the PCB board, 8 layers with 1 inch^2 of cooling area.

3 Electrical characteristics

- 30 °C < T_A < 85 °C, V_{IN} = 2.7 V; V_{OUT} = 4.0 V; typical values are at T_A = 25 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN}	Operating power input voltage range		2.7	3.7	5.5	V
V_{IO}	Supply voltage of I/O pins		1.8		3.6	V
V_{DD}	Digital supply voltage(1)			3.1		V
I_{SHDN}	Shutdown mode			2	10	µA
V_{UVLO}	Undervoltage lockout threshold (when reset is high)	V_{UVLOR} (V_{IN} rising)		2.5	2.6	V
		V_{UVLOF} (V_{IN} falling)	2.3	2.4		
Boost						
f_{SW}	Switching frequency		2.16	2.4	2.64	MHz
I_{OUT}	Continuous output current	V_{IN} = 3.5 V		480		mA
V_{OUT}	Boost output voltage	V_{IN} = 3.0 V	2.8		4.6	V
I_{PK}	Inductor peak current			1.5		A
η	Boost efficiency (V_{IN} = 3.7 V; V_{OUT} = 4.0 V)	I_{OUT} = 350 mA (PS mode)		92		%
V_{OVP}	Overvoltage protection			5.8	6	V
$V_{OVPHYST}$	Overvoltage protection hysteresis			200		mV
$V_{BSTOKHYST}$	Hysteresis of BST_OK comparator			250		mV
LDO						
V_{SUP}	LDO output voltage	V_{IN} = 3.3 V		3.1		V
ΔV_{SUP}	LDO output accuracy	V_{IN} = 3.3 V I_{OUT} = 1 mA		2	3	%
I_{LDO}	LDO output current	V_{IN} = 3.3 V		80	100	mA
I_Q	LDO quiescent current	V_{IN} = 3.3 V I_{OUT} = 80 mA		1.4		µA
Thermal protection						

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{SHDN1}	Thermal shutdown (boost and CM)			150		°C
$T_{SHDN1HYST}$	Hysteresis			20		
T_{SHDN2}	Thermal shutdown (LDO)			170		
$T_{SHDN2HYST}$	Hysteresis			20		
LED current						
$I_{LED0-LED23}$	Current matching	I_{COLx} = 20 mA, V_{OUT} > $V_{LED}+V_{CSH}$			5	%
ΔI_{LEDx}	Absolute channel accuracy	I_{COLx} = 20 mA, V_{OUT} > $V_{LED}+V_{CSH}$	-7.5		+7.5	%
V_{SET}	Voltage reference	R_{SET} = 25 k	1.225	1.25	1.275	V
	Current mirror ratio	I_{LED}/ I_{SET}		400		A/A
V_{CSH}	Current source headroom voltage (COLx to GND)		200			mV
I_{RIPPLE}	LED peak-to-peak current ripple(2)	V_{IN} = 3.0 V; I_{LED} = 20 mA in all channels	-15		+15	%
I_{LED_MAX}	Current mirror max. current	R_{SET} = 20 kΩ	22	25		mA
t_{SET}	LED current settling time (current reaches 90% of the target value)	I_{COLx} = 20 mA		1		µs
		I_{COLx} = 1 mA		10		
Logic inputs: MOSI, SCK, SS						
V_{IL}	Low-level input voltage	V_{IO} = 1.8 V to 3.6 V			0.3 V_{IO}	V
V_{IH}	High-level input voltage	V_{IO} = 1.8 V to 3.6 V	0.7 V_{IO}			V
I_{LK-H}	Input leakage current in high-level	V_{IO} = 3.6 V			2	µA
I_{LK-L}	Input leakage current in low-level	V_{IO} = 3.6 V			2	µA
Logic inputs: CLKIN, SYNK, RESET						
V_{IL}	Low-level input voltage	V_{IO} = 1.8 V to 3.6 V			0.3 V_{IO}	V
V_{IH}	High-level input voltage	V_{IO} = 1.8 V to 3.6 V	0.7 V_{IO}			V
I_{LK-H}	Input leakage current in high-level	V_{IO} = 3.6 V			2	µA
I_{LK-L}	Input leakage current in low-level	V_{IO} = 3.6 V			2	µA
Logic outputs						
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
V_{OH}	High-level output voltage	I_{OH} = 2 mA, V_{IO} = 3.0 V	V_{IO} -0.4			V
Clocks						
f_{OSC}	Internal oscillator frequency	V_{IN} = 2.7 V to 5.5 V	540	600	660	kHz

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
d_{CLKOUT}	Duty cycle of the clock out signal			60		
f_{EXT_MAX}	Maximum frequency of the external clock signal	V_{IN} = 2.7 V to 5.5 V			1.25	MHz
d_{CLKIN}	Duty cycle of the external clock signal	V_{IN} = 2.7 V to 5.5 V	30		70	%
$T_{INTTOEXTCLK}$	Transition time from internal to external clock		10			T_{CLKEX}
Power switches						
$R_{DS(on)}$	P-channel on-resistance (boost)			230		mΩ
	N-channel on-resistance (boost)			130		mΩ
$R_{DS(on)}$	P-channel on-resistance (ROW 0 to ROW 4)			500		mΩ
	N-channel on-resistance (ROW 0 to ROW 4)			200		mΩ
$R_{DS(on)}$	Bypass switch on-resistance					mΩ
I_{LKG-LX}	Coil leakage current	$V_{IN} = V_{SW2}$ = 4.0 V			1	µA
Time and delay						
T_{CLK}	Clock period			1.667		µs
T_{RTCR}	Delay between row rising edge and column rising edge		1		8	T_{CLK}
T_{RTCF}	Delay between column falling edge and row falling edge		1		8	
T_{ONMIN}	PWM minimum on-time			2		
T_{ONMAX}	PWM maximum on-time			510		
T_{FRAME}	Frame period			2560		
T_{ROW}	Row duration			512		
Reset						
T_{RST}	Minimum pulse width on RESET pin		100			µs

1. It is strongly recommended to connect VDD pin to VSUP pin directly.
2. It is valid only if LED matrix is not farther than 10 cm from the driver, otherwise ceramic capacitors should be connected between COLx pin and ground to improve ripple.

4 Detailed description

The STLED524 is a 5x24 LED dot matrix display driver. It includes 24 low-side current mirrors (for each LED in a row). Rows are multiplexed by 5 internal PMOS transistors. Current mirrors are supplied by the integrated boost converter. Its output voltage is adjustable so it can be adapted to the forward voltage of LEDs. It reduces power dissipation and improves efficiency.

4.1 Boost converter

The step-up bridge with current mode control regulation provides output voltage according to the value of VOUT[3:0] register. This voltage should be adjusted to be high enough to provide sufficient headroom to regulate current sources connected to COL 0-23 pins. On the other hand, keeping boost output voltage unnecessarily high, increases power dissipation and degrades efficiency.

Boost incorporates a zero current comparator. When the input voltage is close to the output voltage, pulse-skipping is applied to keep the output voltage regulated.

If the input voltage is higher than desired output voltage, boost switches to bypass mode automatically. In this mode, the output voltage is equal to the input voltage lowered by voltage drop on the PMOS transistor.

Boost converter is enabled only when BSTEN bit in the boost control register is set to 1. VOUT setting shouldn't be changed when boost is on (BSTEN=1).

Table 7. Boost control register bits

Boost control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 16h	BSTEN	-	-	-	VOUT3	VOUT2	VOUT1	VOUT0
Default	0	0	0	0	1	0	1	0

BSTEN = 0, boost is disabled

BSTEN = 1, boost is enabled

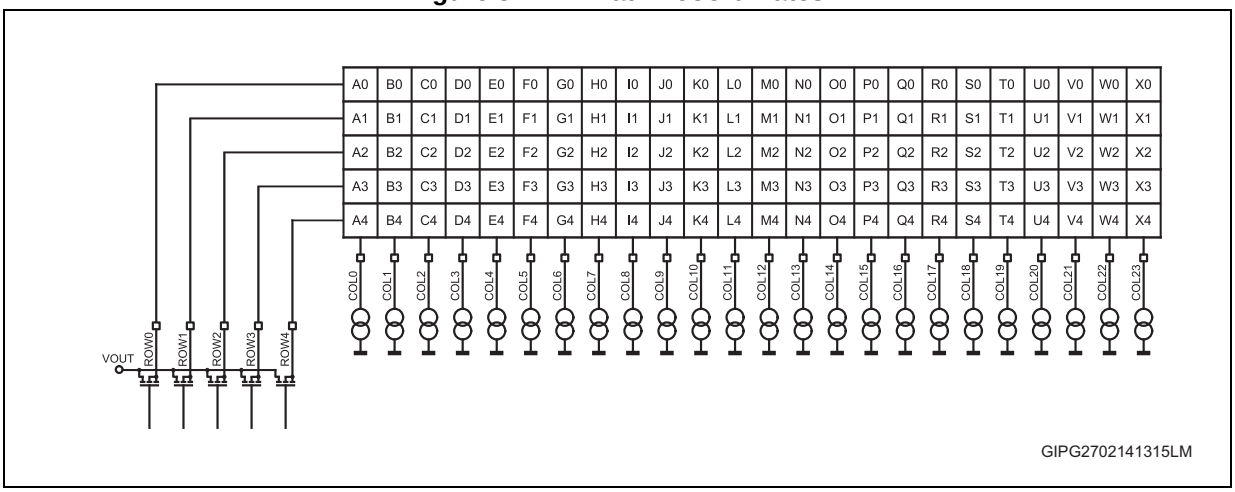
Table 8. Boost output voltage

VOUT[3:0]	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
V_{OUT}[V]	2.80	2.92	3.04	3.16	3.28	3.40	3.52	3.64	3.76	3.88	4.00	4.12	4.24	4.36	4.48	4.60

One step = 120 mV

4.2 LED matrix

Figure 3. LED matrix coordinates

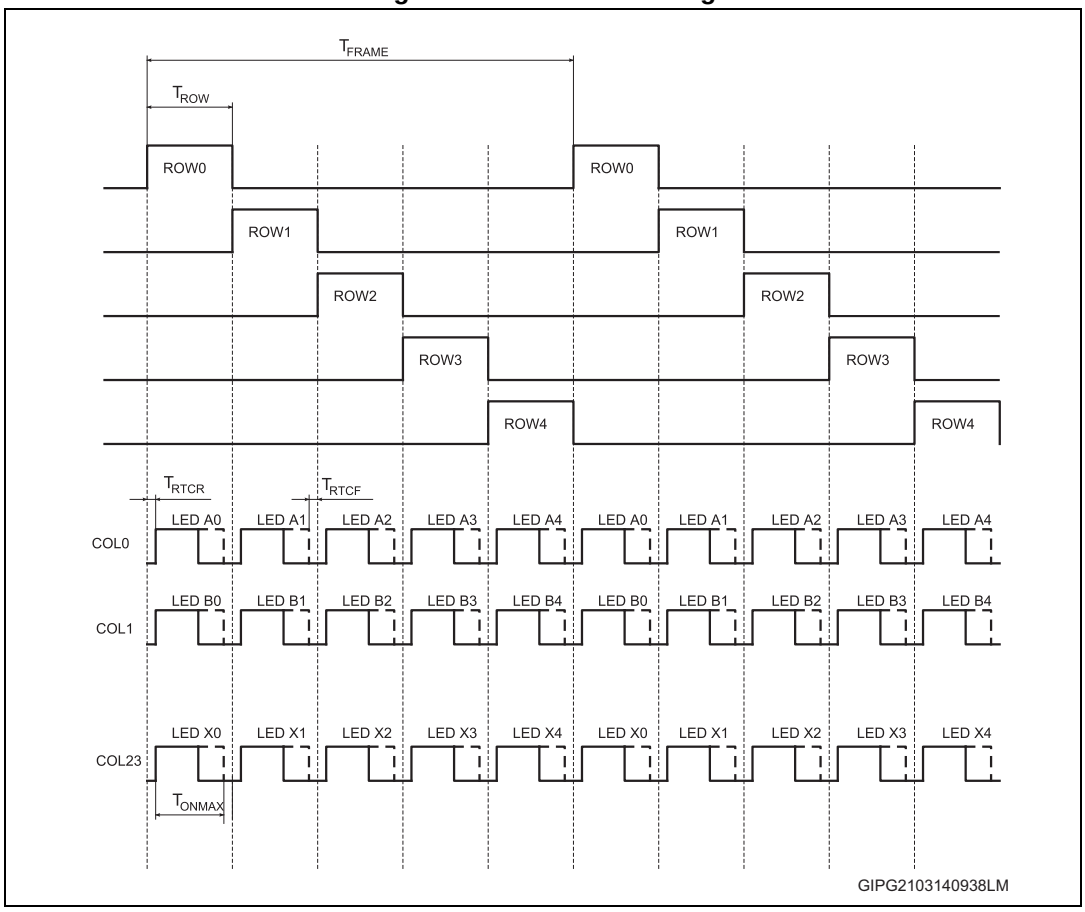


LED matrix rows are connected to ROW 0-4 pins. Columns are connected to COL 0-23 pins.

4.2.1 Blanking time

Rows are multiplexed by T_{ROW} period according to *Figure 4*. The duration of one row is given by $T_{ROW} = T_{FRAME} / 5$, but the maximum dot on-time is $T_{ONMAX} = T_{ROW} - (T_{RTCR} + T_{RTCF})$ only.

Figure 4. LED matrix timing



T_{RTCR} and T_{RTCF} are adjustable due to the blanking time register. If a blanking time is set longer than 2 T_{CLK}, maximum PWM duty cycle is limited according to *Table 10*.

Table 9. Blanking time register

Blanking time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 15h	-	-	-	-	-	BLK[2:0]		
Default	-	-	-	-	-	0	0	0

Table 10. Impact of blanking time on the maximum PWM duty cycle

Blanking time register value	Blanking time [T_{CLK}]	T_{RTCR} [T_{CLK}]	T_{RTCF} [T_{CLK}]	Max. PWM duty cycle
000	2	1	1	255/255
001	4	2	2	254/255
010	6	3	3	253/255
011	8	4	4	252/255
100	10	5	5	251/255
101	12	6	6	250/255
110	14	7	7	249/255
111	16	8	8	248/255

4.3 LED current setting

Although each current mirror can sink up to ~35 mA (that is more than test conditions), the following conditions have to be met:

- The sum of all current mirrors should not exceed 600 mA in bypass mode.
- The sum of all current mirrors should not exceed 480 mA in boost mode.
- If sum of all current mirrors exceeds test conditions, it may exceed the related specifications. The device is not guaranteed to sink current greater than test conditions.

Maximum current of all current mirrors can be adjusted by R_{SET} resistor value according to the following formula:

Equation 1

$$I_{LEDMAX} = \frac{V_{SET}}{R_{SET}} \times 400$$

where: V_{SET} = 1.25 V typically.

Current of each dot can be adjusted in its register, so each LED may have an independent setting of current.

Current can be adjusted in 255 steps; 1 step represents approximately 0.392% of I_{LEDMAX}. Current settings are carried out by Dn_xx registers, where n is the pattern number and xx are the coordinates of a dot in the matrix.

To avoid false activation of the short or open ISET pin protection, the minimum value of R_{SET} should be higher than 14 kΩ and lower than 270 kΩ.

4.4 Patterns

The STLED524 includes the memory for 2 patterns of 5x24 dots. Each dot in a pattern has 2 registers for its setting.

One 8-bit register stores dimming settings. The other one is 4-bit only and stores information about slope and delay.

Table 11. Dimming, slope and delay registers of one dot

Dimming	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = nnh	Dn_xx[7:0]							
Default value	Not defined							
Slope and delay (S&D)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = (nn+1)h	-	-	-	-	PnCYC*xx*[1:0]		PnDLY*xx*[1:0]	
Default value	-	-	-	-	Not defined		Not defined	

where:

n: is a number of pattern

xx: are coordinates of a dot in the matrix xx = {A0, A1, A2, A3, A4, B0, B1, …, B4, C0…, X0, X1, X2, X3, X4}.

Pattern 1 and pattern 2 memories are not initialized after the reset. They can contain random data. Their content should be reset by CLR1/CLR2 bits.

4.4.1 Pattern register organization

A pair of 8-bit registers is used to set properties of each dot in the matrix.

Table 12. Dimming, slope and delay registers of one dot (memory organization)

Address 0xnnh								Address 0x(nn+1)h							
Dimming register								Slope and delay register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Dn_xx[7:0]								-	-	-	-	PnCYCxx[1:0]		PnDLYxx[1:0]	

Table 13. Register addresses in pattern 1

Address	Dimming register	Address	Slope and delay register	
00h	D1_A0[7:0]	01h	P1CYCA0[1:0]	P1DLYA0[1:0]
02hh	D1_A1[7:0]	03h	P1CYCA1[1:0]	P1DLYA1[1:0]
…	…	…	…	…
EEh	D1_X4[7:0]	EFh	P1CYCX4[1:0]	P1DLYX4[1:0]

Table 14. Register addresses in pattern 2

Address	Dimming register	Address	Slope and delay register	
00h	D2_A0[7:0]	01h	P2CYCA0[1:0]	P2DLYA0[1:0]
02h	D2_A1[7:0]	03h	P2CYCA1[1:0]	P2DLYA1[1:0]
…	…	…	…	…
EEh	D2_X4[7:0]	EFh	P2CYCX4[1:0]	P2DLYX4[1:0]

4.4.2 Display size

If DISPSIZE bit is set to 1, the content of columns 20-23 is always linked to pattern 1 regardless of the value of DISP bits. Columns 0-19 can still be used as a display, while columns 20-23 can be used for other functions.

If DISPSIZE bit is set to 1, the content of pattern 2 is also limited to columns 0-19 only. Columns 20-23 are not displayed during scrolling.

The minimum number of scroll steps in horizontal direction is reduced to 20, if DISPSIZE = 1.

Table 15. Content of columns 20-23

DISP	DISPSIZE	COL 0-19	COL 20-23
00	0	Blank	Blank
01	0	Pattern 1	Pattern 1
10	0	Pattern 2	Pattern 2
00	1	Blank	Pattern 1
01	1	Pattern 1	Pattern 1
10	1	Pattern 2	Pattern 1

4.5 Description of registers

4.5.1 Software control register

Table 16. Software control register

Software control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 00h	SWRST	-	-	-	-	CLR2	CLR1	EN
Default	0	0	0	0	0	0	0	0

When CLR1 is set to 1, pattern 1 is cleared, (dimming, slope and delay of all dots are set to 0) then it is set to 0 automatically.

When CLR2 is set to 1, pattern 2 is cleared, (dimming, slope and delay of all dots are set to 0) then it is set to 0 automatically.

If SWRST bit is set to 1, content of all registers is set to default values and SWRST bit is cleared automatically.

If EN = 0, display is off

If EN = 1, display is on

4.5.2 Display control register

Table 17. Display control register

Display control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 01h	-	-	-	-	-	-	DISP2	DISP1
Default	0	0	0	0	0	0	0	0

DISP1 and DISP2 bits define which pattern is displayed, see *Table 18*.

Table 18. DISP bits

DISP2	DISP1	Displayed pattern
0	0	No pattern is displayed (blank screen)
0	1	Pattern 1 is displayed
1	0	Pattern 2 is displayed
1	1	No pattern is displayed (blank screen)

DISP bits can be written by SPI anytime, but the display change (from pattern 1 to pattern 2 or vice versa) is performed according to the following rules:

- On next frame, if the display is on and scroll features are disabled (EN=1, SCRLEN=0).
- If SCRLEN=1 and EN=1, scroll operation starts according to the scroll setup.

4.5.3 Clock register

This register is used to set up clock signals.

Table 19. Clock register

Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 10h	-	-	-	REFSEL	SYNCSEL	SYNCEN	CLKIN	CLKOUT
Default	0	0	0	0	1	0	0	0

CLKOUT = 0, CLKOUT pin does not provide any clock signal. It is permanently low

CLKOUT = 1, CLKOUT pin provides CLK signal

CLKIN = 0, clock signal from the internal oscillator is used for display timings

CLKIN = 1, clock signal from CLKIN pin is used for display timings

SYNCEN = 0, driver operation synchronization is disabled by an external signal connected to SYNC pin

SYNCEN = 1, driver operation synchronization is enabled by an external signal connected to SYNC pin

SYNCSEL = 0, driver operation is enabled when SYNC signal is low

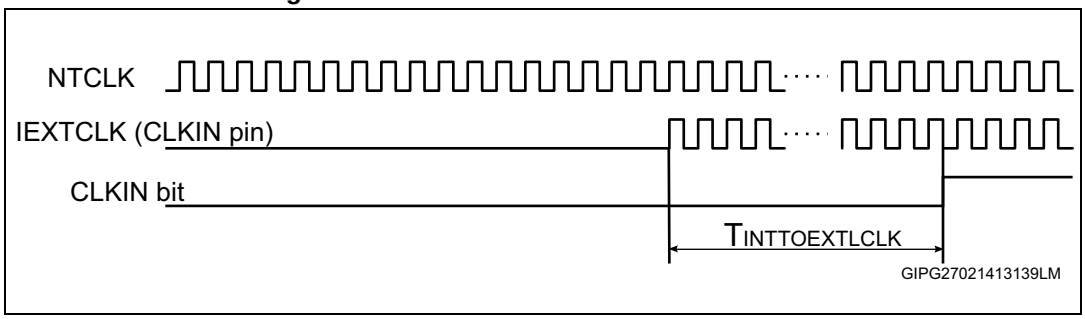
SYNCSEL = 1, driver operation is enabled when SYNC signal is high

REFSEL = 0, external reference defined by R_{SET} value is used for current mirrors

REFSEL = 1, internal reference is used for current mirrors

If the clock signal changes from internal to external, the external clock has to be provided, at least $T_{INTTOEXTCLK}$ before than CLKIN bit is set to 1.

Figure 5. Internal to external clock transition



SYNC pin behavior

If the synchronization is enabled (SYNCEN = 1), SYNC pin is in inactive state (defined by SYNCSEL bit) and the micro writes EN, DISP or SLPEN bits, but the corresponding operation is delayed, until SYNC pin gets to the active state.

If the synchronization is disabled (SYNCEN = 0), the micro writes EN, DISP or SLPEN bits, and the corresponding operation starts immediately.

Table 20. SYNC pin behavior

SYNCEN bit	SYNCSEL bit	SYNC pin	Operation
0	0	0	Not synchronized
0	0	1	Not synchronized
0	1	0	Not synchronized
0	1	1	Not synchronized
1	0	0	Synchronized, but the bit change has immediate effect
1	0	1	Synchronized, the operation is delayed, until SYNC pin is 0
1	1	0	Synchronized, the operation is delayed, until SYNC pin is 1
1	1	1	Synchronized, but bit change has immediate effect

4.5.4 Column control register

These registers are used to enable/disable columns of the matrix.

Table 21. Column control 1 register

Column control 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 11h	COL7EN	COL6EN	COL5EN	COL4EN	COL3EN	COL2EN	COL1EN	COL0EN
Default	1	1	1	1	1	1	1	1

Table 22. Column control 2 register

Column control 2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 12h	COL15EN	COL14EN	COL13EN	COL12EN	COL11EN	COL10EN	COL9EN	COL8EN
Default	1	1	1	1	1	1	1	1

Table 23. Column control 3 register

Column control 3	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 13h	COL23EN	COL22EN	COL21EN	COL20EN	COL19EN	COL18EN	COL17EN	COL16EN
Default	1	1	1	1	1	1	1	1

COL<i>EN = 0, column <i> is disabled

COL<i>EN = 1, column <i> is enabled

These bits can be read or written in any configuration, but these registers should be changed when EN=0.

4.5.5 Row control register

This register is used to enable/disable rows of the matrix.

Table 24. Row control register

Row control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 14h	-	-	-	ROW4EN	ROW3EN	ROW2EN	ROW1EN	ROW0EN
Default	0	0	0	1	1	1	1	1

ROW<i>EN = 0, row <i> is disabled

ROW<i>EN = 1, row <i> is enabled

These bits can be read or written in any configuration, but these registers should be registerd when EN=0.

4.5.6 Blanking time register

This register sets the blanking time duration.

Table 25. Blanking time duration

Blanking time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 16h	-	-	-	-	-	BLK[2:0]		
Default	0	0	0	0	0	0	0	0

BLK[2:0] - blanking time duration

000: 2 clock periods

001: 4 clock periods

010: 6 clock periods

011: 8 clock periods

100: 10 clock periods

101: 12 clock periods

110: 14 clock periods

111: 16 clock periods

These bits can be read or written in any configuration, these registers should be changed when EN=0. See *Section 4.2.1* for details.

4.5.7 Boost control register

This register is described in *Section 4.1*.

4.5.8 Display visual control register

This register enables/disables the driver visual features.

Table 26. Display visual control register

Display visual control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 20h	-	-	BRCEN	WAITEN	SLPEN	SCRLEN	PWMEN	DISPSIZE
Default	0	0	0	0	0	0	0	0

PWMEN = 0, PWM duty cycle is fixed to maximum available

PWMEN = 1, PWM duty cycle can be customized by PWM control register

SCRLEN = 0, scrolling is disabled

SCRLEN = 1, scrolling is enabled

SLPEN = 0, slope operation is disabled

SLPEN = 1, slope operation is enabled

WAITEN = 0, wait time at the end of scroll operation is disabled

WAITEN = 1, wait time at the end of scroll operation is enabled

BRCEN = 0, insertion of blank rows/columns during scroll operation is disabled

BRCEN = 1, insertion of blank rows/columns during scroll operation is enabled

DISPSIZE = 0, full number of columns is used to display content of patterns 1 and 2

DISPSIZE = 1, content of columns 20-23 is always linked to pattern 1 regardless of the value of DISP bits. If content of pattern 2 is displayed, then columns 0-19 are visible. The rest is "hidden behind" in the columns 20-23 that display content of pattern 1 permanently.

Note: Setting EN=0, the display turns off immediately.

If PWM is enabled / disabled while a slope cycle is running, new PWM settings have effect as described in PWM control register.

When SLPEN is set to 0, slope is disabled immediately, regardless of the current slope status for each dot.

When SCRLEN is set to 0, the display reverts immediately to its target pattern (given by DISP bit values), aborting any scrolling cycle.

4.5.9 PWM control register

This register is used to set PWM duty cycle.

Table 27. PWM control register

PWM control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 21h	PWM[7:0]							
Default	0	0	0	0	0	0	0	0

PWM[7:0] represents PWM duty cycle value

PWM[7:0] = 0x00h represents 0/255 duty cycle (0%)

PWM[7:0] = 0x01h represents 1/255 duty cycle (0.4%)

PWM[7:0] = 0x80h represents 128/255 duty cycle (50.2%)

PWM[7:0] = 0xFFh represents 255/255 duty cycle (100%)

PWM control register is accessible anytime, but a change of its value is evident only if PWM operation is enabled (PWMEN=1). PWM is a global setting valid for all dots.

PWM duty cycle changes next frame period.

If slope operation is active, new settings of PWM are applied according to slope cycle evolution:

- During slope phase 1 (PWM ramp-up), PWM setting change is applied only if PWM value is lower than the new value.
- During slope phase 2 (PWM at maximum), PWM setting change is ignored and it takes effect during next slope cycle.
- During 3 and 4 slope phase, new PWM settings don't have any effect and they take effect during next slope cycle.

If blanking time is longer than default, the highest values in PWM register are not valid and the maximum allowed value is applied. See *Section 4.2.1*.

4.5.10 Scroll control 1, scroll control 2 and scroll control 3 registers

These registers are described in *Section 4.7*.

4.5.11 Interrupt enable register

Table 28. Interrupt enable register

Interrupt enable	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 40h	BSTOK_M	ROWSC_M	EOSCR_M	STEP_M	SHORT_M	OPEN_M	THP_M	OVP_M
Default	0	0	0	0	0	0	0	0

OVP_M = 0, the interrupt generated by overvoltage protection is disabled

OVP_M = 1, the interrupt generated by overvoltage protection is enabled

THP_M = 0, the interrupt generated by overtemperature protection is disabled

THP_M = 1, the interrupt generated by overtemperature protection is enabled

OPEN_M = 0, the interrupt generated by open R_{SET} protection is disabled

OPEN_M = 1, the interrupt generated by open R_{SET} protection is enabled

SHORT_M = 0, the interrupt generated by short R_{SET} protection is disabled

SHORT_M = 1, the interrupt generated by short R_{SET} protection is enabled

STEP_M = 0 the interrupt generated at the beginning of a scroll step is disabled

STEP_M = 1, the interrupt generated at the beginning of a scroll step is enabled

EOSCR_M = 0, the interrupt generated at the end of scroll operation is disabled

EOSCR_M = 1, the interrupt generated at the end of scroll operation is enabled

ROWSC_M = 0, the interrupt generated by row short-circuit is disabled

ROWSC_M = 1, the interrupt generated by row short-circuit is enabled

BSTOK_M = 0, the interrupt generated is disabled, when boost output voltage reaches the target value

BSTOK_M = 1, the interrupt generated is enabled, when the boost output voltage reaches the target value

4.5.12 Latch register

Table 29. Latch register (read only)

Latch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 41h	BSTOK	ROWSC	EOSCR	STEP	SHORT	OPEN	THP	OVP
Default	0	0	0	0	0	0	0	0

Bits in this register are set when the corresponding interrupt occurs and they are latched. Those bits, which have been set, can only be cleared by reading the register through SPI.

4.5.13 Status register

Table 30. Status register (read only)

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 42h	BSTOK	-	EOSCR	-	SHORT	OPEN	THP	OVP
Default	0	0	1	0	0	0	0	0

Bits in the status register are set and reset according to the state of internal signals (overtemperature, overvoltage etc.). Reading the status register through SPI does not affect the state of bits.

BSTOK bit is set to 1 when V_{OUT} voltage has reached the target value. The bit is set to 0, if V_{OUT} is lower than V_{OUTSET} - $V_{BSTOKHYST}$. V_{OUTSET} is the target output voltage given by VOUT[3:0] register. $V_{BSTOKHYST}$ is the hysteresis of BST_OK comparator. An interrupt is generated, it is enabled and BSTOK bit in the latch register is set.

THP bit is set when thermal protection has been activated (when junction temperature exceeds T_{SHDN1}). The bit is reset if the temperature falls below $T_{SHDN1HYST}$ thermal protection hysteresis. An interrupt is generated, when THP bit is set, if it is enabled and THP bit is set in the latch register. When the thermal protection is activated, EN and BSTEN bits are set to 0. The device has to be re-enabled through SPI to restart the operation. An interrupt is also generated when THP bit is reset to 0. So the microcontroller can wait for this interrupt and then re-enable the device.

OVP bit is set when boost output voltage exceeds V_{OVP} threshold. The bit is reset, if the voltage falls below the hysteresis of OVP threshold. An interrupt is generated, when this bit is set, if it is enabled and OVP bit in the latch register is set. The boost is disabled automatically, BSTEN bit is set to 0.

R_{SET} resistance is checked when EN bit is set to 1. If R_{SET} value is too high (or it is not connected at all), OPEN bit in the status register is set. An interrupt is generated, if it is enabled and OPEN bit is set in the latch register.

If R_{SET} value is smaller than R_{SETMIN} (typically 14 kΩ), SHORT bit in the status register is set to 1. An interrupt is generated, if it is enabled. Current mirrors and boost are not stopped.

STEP bit is set at the beginning of each scroll step. An interrupt is generated, if it is enabled. It hasn't a corresponding bit in the status register.

EOSCR bit is set, when the scroll operation is over. An interrupt is generated, if it is enabled.

When a short-circuit is detected on any row connections, current mirrors are disabled by setting EN bit to 0 automatically. Boost operation is not touched. An interrupt is generated if it is enabled and ROWSC bit is set in the latch register.

Table 31. Interrupt overview

Latch register bit	Interrupt generated when set	Interrupt generated when reset
BSTOK	Yes	Yes
ROWSC	Yes	No
EOSCR	Yes	No
SHORT	Yes	No
OPEN	Yes	No
THP	Yes	Yes
OVP	Yes	No

4.5.14 Scroll step register

This register is described in *Section 4.7.1*

4.5.15 Version register

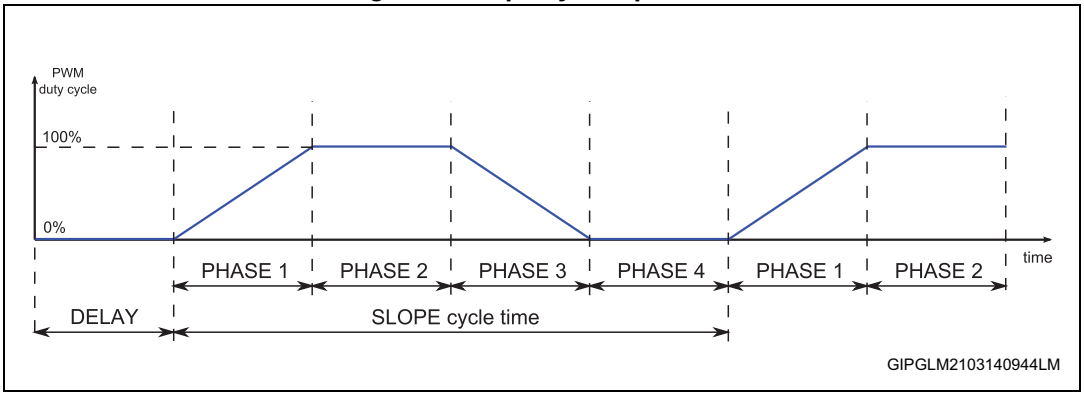
Table 32. Version register

Version	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = FFh	-	-	-	-	VER[3:0]			
Default	0	0	0	0	0	0	0	1

The version register contains information about the version of the chip.

4.6 Slope mode operation

Figure 6. Slope cycle operation



A delay and a slope cycle time can be specified for each dot of the matrix separately.

The delay is set by PnDLYxx bits, n is a pattern number (see *Section 4.4*) and xx are the coordinates of a dot.

Table 33. Delay duration

PnDLYxx	Delay time
00	No delay
01	1/4 of the slope cycle time
10	1/2 of the slope cycle time
11	3/4 of the slope cycle time

Slope cycle time is set by PnCYCxx bits, n is a pattern number (see *Section 4.4*) and xx are the coordinates of a dot.

Table 34. Slope cycle duration

PnCYCxx	Cycle time [s]	Duration of one phase [s]	Duty cycle step
00	0	0	0
01	1.456	0.364	3
10	2.184	0.546	2
11	4.367	1.092	1

PWM duty cycle is incremented / decremented during slope operation in steps stated in *Table 32*. If the final value of PWM duty cycle given by the value in PWM duty register is not a multiple of the duty cycle step, then last step in phase 1 is truncated to reach the final value of PWM duty cycle given by PWM duty register. Therefore, last step in phase 3 is truncated to reach 0 duty cycle. See *Figure 8*.

Figure 7. Duty cycle increments during phase 1 of slope operation

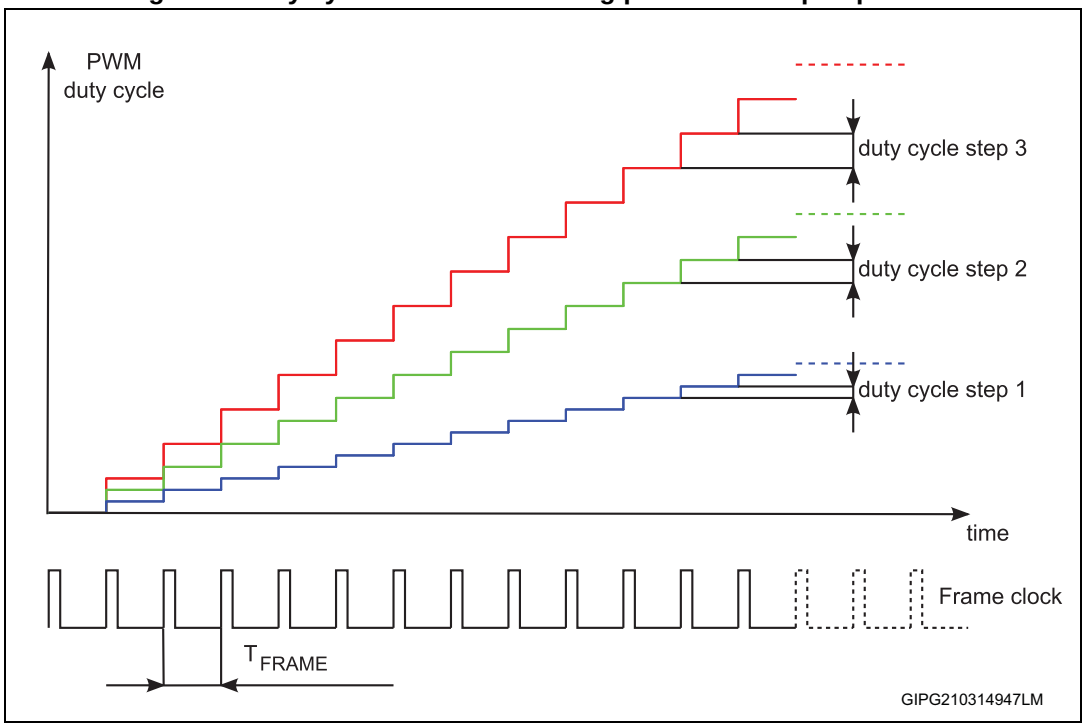
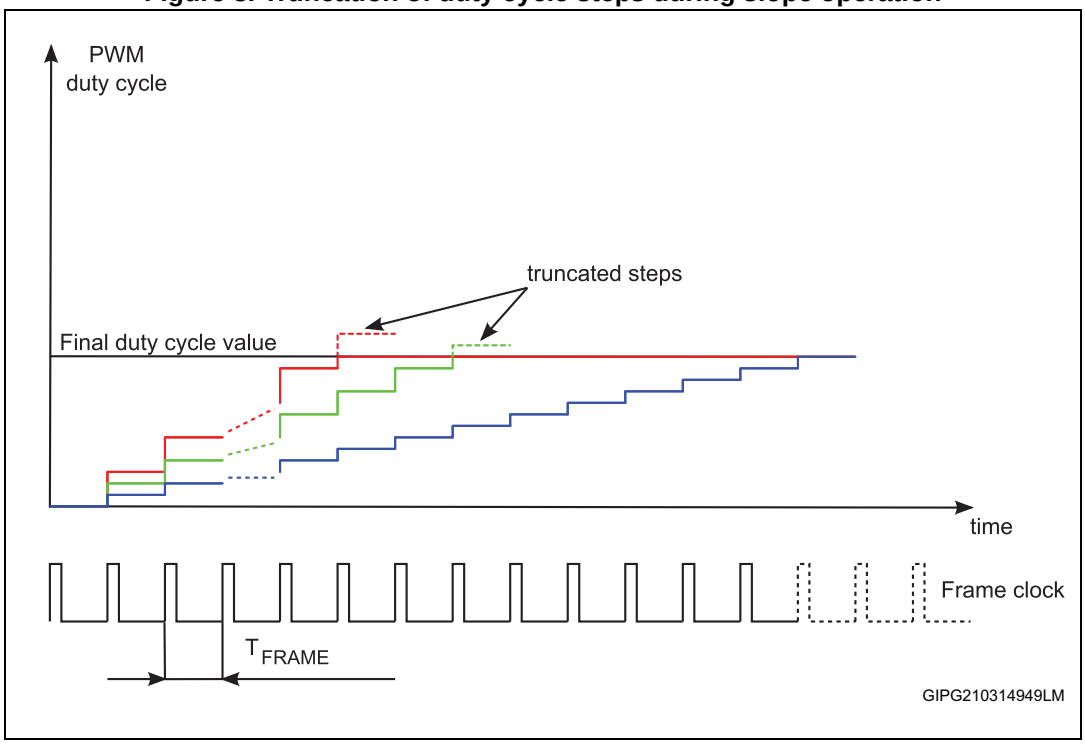


Figure 8. Truncation of duty cycle steps during slope operation



If SLPEN is set to 0 during the slope cycle, slope cycle is not finished and the display goes to the new operation mode immediately.

4.7 Scrolling

The STLED524 has built-in function of 4-way scroll of the display content. The scroll speed can be defined in 8 steps. Blank rows or columns can be added to patterns to improve readability during scrolling and a wait loop with adjustable duration can be performed at the end of scroll to let reader read the display content.

4.7.1 Scroll control registers

Table 35. Scroll control register 1

Scroll control 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 30h	SCRSPD[5:0]						DIR1	DIR0
Default	0	0	0	0	0	0	0	0

SCRSPD[5:0] scroll speed register fixes the speed according to which the content of the display is scrolled.

Table 36 shows duration of one scroll step according to SCRSPD[5:0] value.

Table 36. Scroll speed

	1 step duration	
SCLSPD[5:0]	[T_{FRAME}]	[ms](1)
0	3	12.8
1	7	29.9
2	11	46.9
…	…	…
N	N x 4 + 3	(N x 4 + 3) x 10.24/2.4
…	…	…
62	252	1075
63	255	1088

1. When the internal clock is used.

Table 37. Scroll direction

DIR1	DIR0	Direction
0	0	Left
0	1	Right
1	0	Down
1	1	Up

SCRSPD settings can be updated only when scroll is disabled.

DIR bits can be updated only when scroll is disabled.

Table 38. Scroll control register 2

Scroll control 2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 31h	BLNK_R[2:0]			BLNK_C[4:0]				
Default	0	0	0	0	0	0	0	0

BLNK_C[4:0] - blank column register. It defines the number of blank columns during horizontal direction scroll (left/right). Maximum allowed value is 24. If the value is higher than 24, 24 blank columns are inserted only. If DISPISIZE = 1, the maximum number of blank columns is limited to 20.

BLNK_R[2:0] - blank row register. It defines the number of blank rows during vertical direction scroll (up/down). Maximum allowed value is 5. If the value is higher than 5, 5 blank rows can be only inserted.

Note: This register cannot be read.

Table 39. Scroll control register 3

Scroll control 3	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 32h	-	-	WAIT[5:0]					
Default	0	0	0	0	0	0	0	0

Table 40. Wait time during scroll operation

	Wait time duration	
WAIT[5:0]	**[T_{FRAME}]**	**[ms](1)**
0	3	12.8
1	7	29.9
2	11	46.9
…	…	…
N	N x 4 + 3	(N x 4 + 3) x 2.56/0.6
…	…	…
62	252	1075
63	255	1088

1. When internal clock is used.

Scroll step register stores the number of scroll steps already fulfilled.

Table 41. Scroll step register

Scroll steps	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 43h	-	-	SCRSTP[4:0]					
Default	0	0	0	0	0	0	0	0

4.7.2 Locking columns and rows

The content of any column or row can be locked during scroll. The content of locked rows/columns does not move during scroll. Locked rows/columns always display the content of pattern 1.

Any combination of columns can be locked by corresponding bits in the column lock registers. Besides, any combination of rows can be locked by corresponding bits in the row lock register. Columns and rows can be locked at the same time.

Table 42. Column lock register 1

Column lock 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 33h	COLCK7	COLCK6	COLCK5	COLCK4	COLCK3	COLCK2	COLCK1	COLCK0
Default	0	0	0	0	0	0	0	0

Table 43. Column lock register 2

Column lock 2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 34h	COLCK15	COLCK14	COLCK13	COLCK12	COLCK11	COLCK10	COLCK9	COLCK8
Default	0	0	0	0	0	0	0	0

Table 44. Column lock register 3

Column lock 3	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 35h	COLCK23	COLCK22	COLCK21	COLCK20	COLCK19	COLCK18	COLCK17	COLCK16
Default	0	0	0	0	0	0	0	0

Table 45. Row lock register

Column lock 3	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 35h				ROWLCK4	ROWLCK3	ROWLCK2	ROWLCK1	ROWLCK0
Default	0	0	0	0	0	0	0	0

4.7.3 Scroll possibilities

The display content scroll is enabled, if SCRLEN bit in the display visual control register is set to 1. If this bit is 1 and new value of DISP bits (DISP1 and DISP2) is written through SPI, scroll operation starts. The type of scroll operation is defined by the content of scroll control registers.

Blank rows or columns can be inserted between two patterns during the scroll operation. These blank rows/columns are inserted by the logic of the driver automatically, so they are not part of patterns. The number of blank rows/columns can be set by the scroll control register 2. The insertion of blank rows/columns is enabled, when BRCEN bit in the display visual control register is set to 1.

Table 44 contains all possible types of scroll operations. X → Y expression means that the display content is X and when the scroll operation is over, it is Y. All possibilities listed below are valid for all directions. DISP (act) is the value of DISP bits. DISP (new) is the new value of these bits written through SPI.

There are two interrupts related to the scroll operation. These are EOSCR (end of scroll) and step. This interrupt is generated at the end of scroll operation (when the new pattern is visible). The end of step interrupt is generated after each scroll step. It is useful to read the scroll step register value, when this interrupt is detected. It gives the microcontroller information about the position of the pattern on the display.

If WAITEN bit in the display visual control register is set, the end of scroll interrupt is delayed by the wait time given by the value of the scroll control 3 register.

Columns from 20 to 23 can be locked during the scroll operation. These locked columns do not move during scroll operation. Their content is always stored in pattern 1 register. DISPSIZE bit, in the display visual control register, has to be set to 1 to lock columns from 20 to 23. If this bit is set to 0, columns from 20 to 23 scroll in the same way as the rest of the display. If DISPSIZE bit is set to 1, the number of scroll steps is limited to 20 in horizontal direction (if no blank column is inserted). The number of steps in vertical direction is not affected.

Table 46. List of all scroll operations

DISP (act)	DISP (new)	BRCEN	
00	00	0	B → B
00	01	0	B → P1
00	10	0	B → P2
01	00	0	P1 → B
01	01	0	P1 → P1 (rotation)
01	10	0	P1 → P2
10	00	0	P2 → B
10	01	0	P2 → P1
10	10	0	P2 → P2 (rotation)
00	00	1	B → Brc →B
00	01	1	B → Brc → P1
00	10	1	B → Brc → P2

Table 46. List of all scroll operations (continued)

DISP (act)	DISP (new)	BRCEN	
01	00	1	P1 → Brc →B
01	01	1	P1 → Brc →P1 (rotation)
01	10	1	P1 → Brc →P2
10	00	1	P2 → Brc →B
10	01	1	P2 → Brc →P1
10	10	1	P2 → Brc →P2 (rotation)

P1 = pattern 1, P2 = pattern 2, B = blank display, Brc = blank rows/columns

Figure 9 shows a scroll operation in vertical direction (5 steps). No blank column or row is inserted and wait time is disabled. As for horizontal direction, the only difference is the number of scroll steps (24 instead of 5). EOSCR bit is set to 1 in the 24th step.

Figure 9. Basic scroll operation

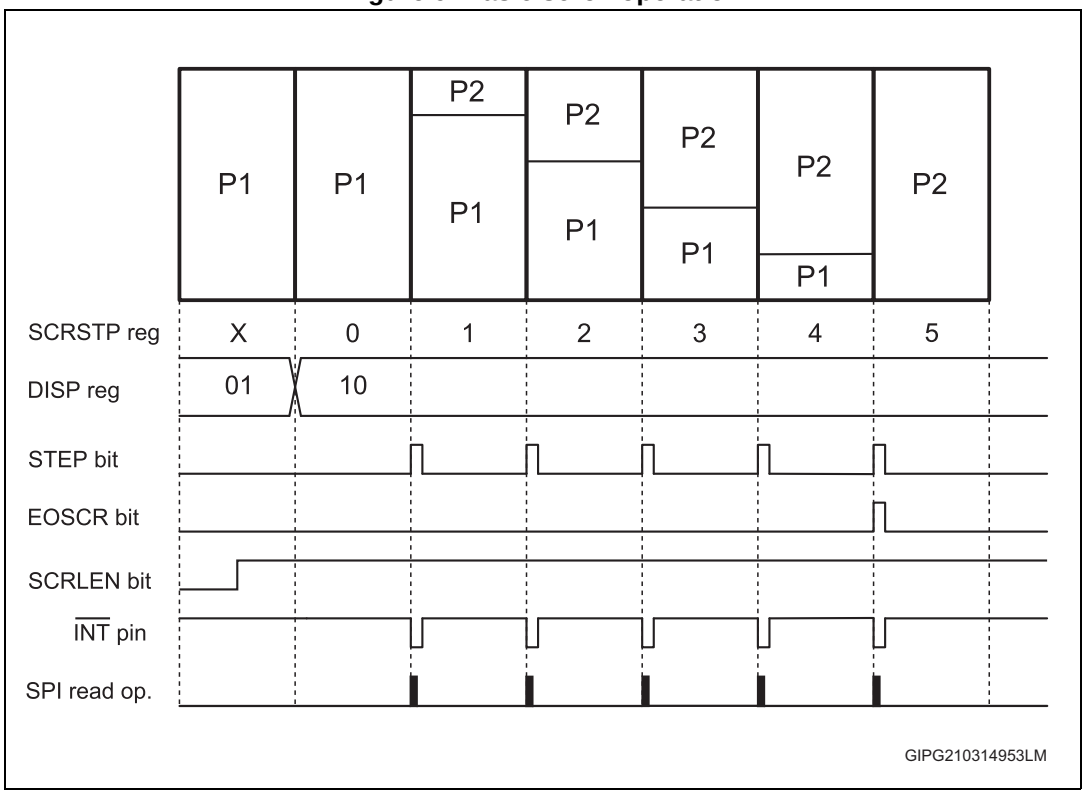


Figure 10 shows a scroll operation with blank row/column insertion enabled. S is the number of standard scroll steps (with blank row/column insertion disabled). S = 24 for horizontal direction and 5 in case of vertical direction, n is the number of blank rows/columns to be inserted.

Figure 10. Scroll operation with blank row/column insertion enabled

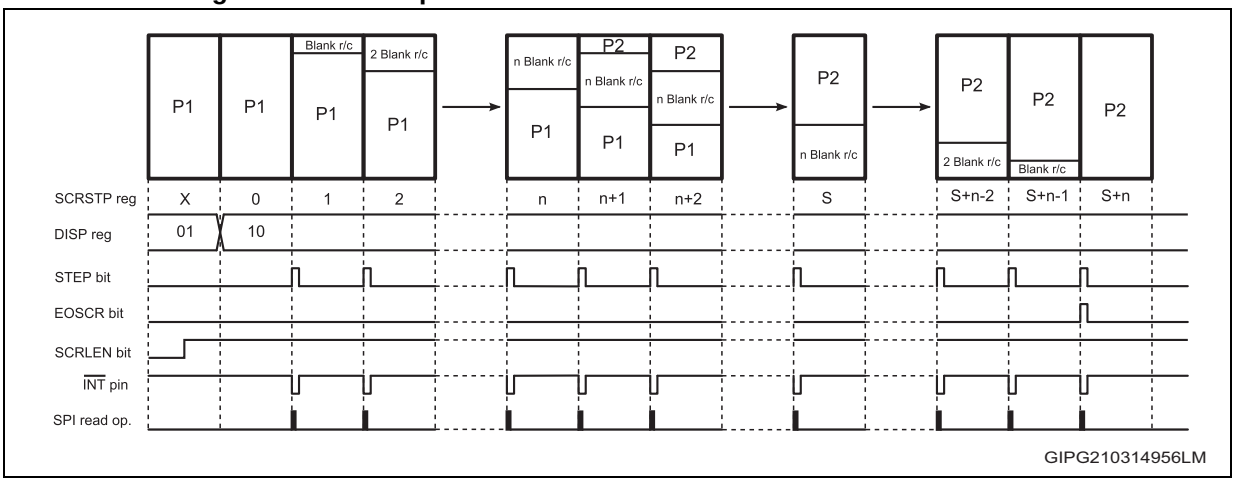
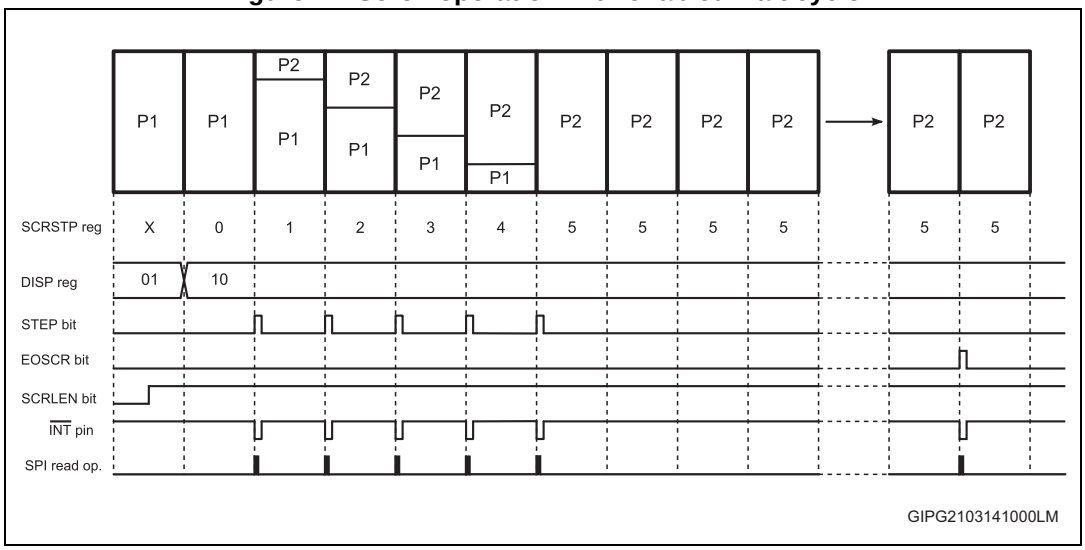


Figure 11 shows a scroll operation example when wait cycle is enabled. When P2 pattern is visible, the wait counter starts. EOSCR interrupt is generated, when the wait counter reaches the value set by scroll control register 3.

Figure 11. Scroll operation with enabled wait cycle



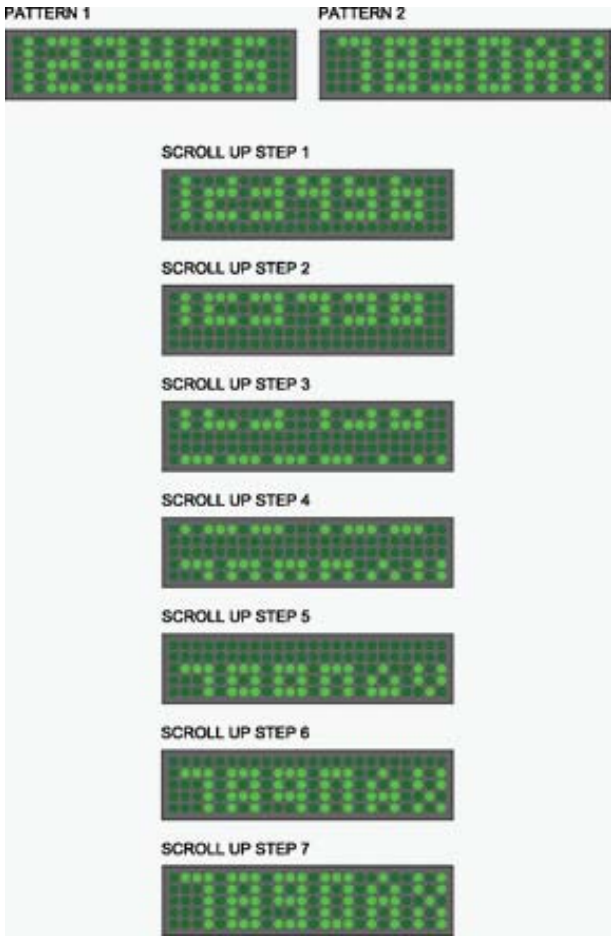
All three examples above show the scroll operation during the which P1 pattern is replaced by P2 pattern, but the behavior described in these examples is also valid for all other cases stated in *Table 44*.

4.7.4 Scroll examples

Figure 12. Examples of scroll (DISP 01→10)

Figure 13. Example of scroll when DISPSIZE = 1 (DISP 01 → 10)

Figure 14. Example of scroll with 2 inserted blank rows (BRCEN=1, DISP 01 → 10)



4.8 Combining PWM, slope and scroll

PWM and slope can be combined without any restrictions.

Figure 15. Light output in case of enabled PWM and disabled slope

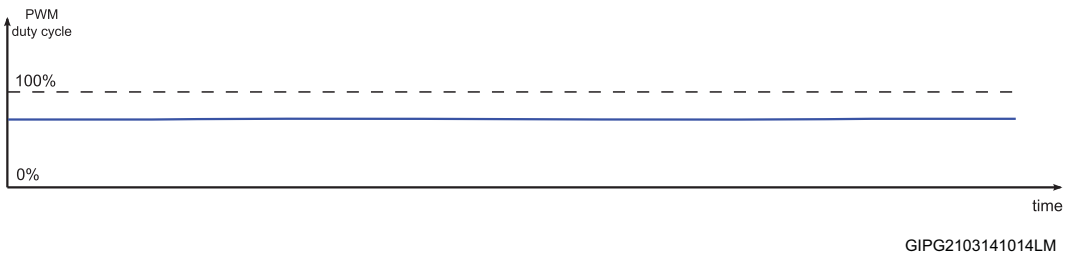


Figure 16. Light output in case of disabled PWM and enabled slope

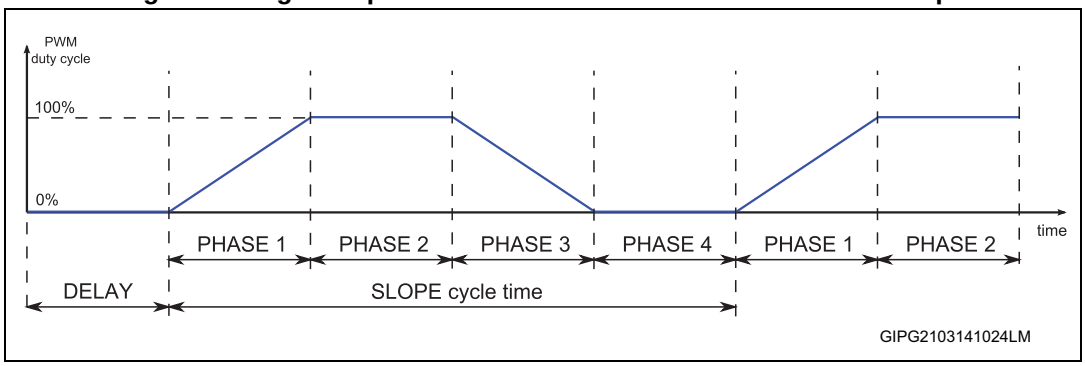


Figure 17. Light output in case of enabled PWM and enabled slope

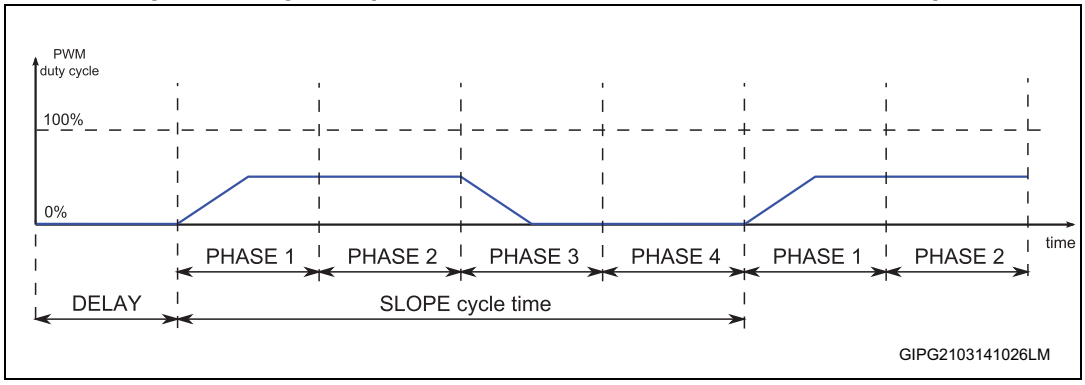
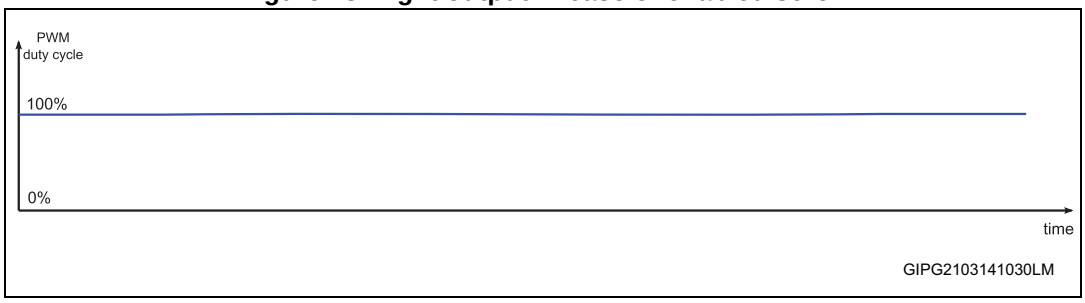


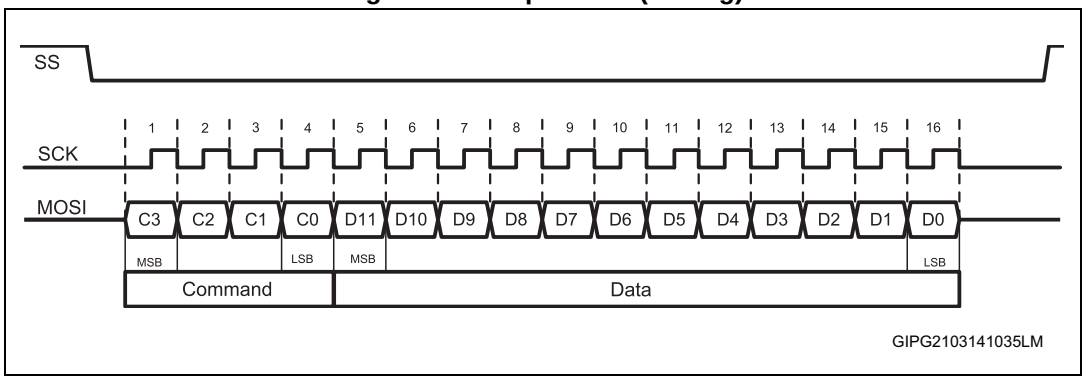
Figure 18. Light output in case of enabled scroll



4.9 SPI

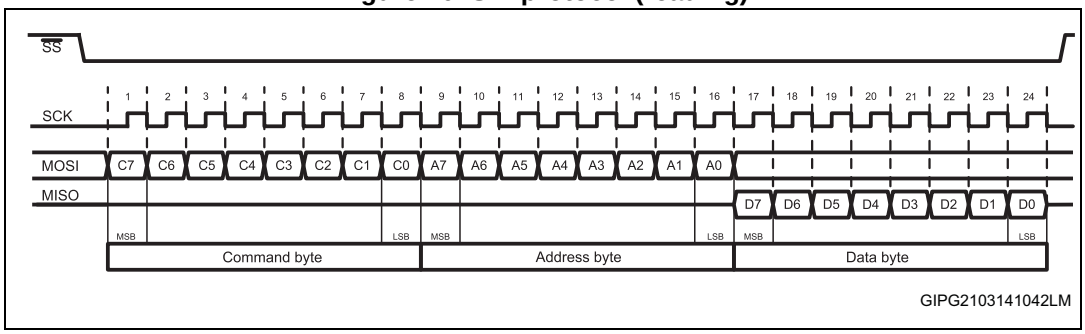
The STLED524 is fully compatible with SPI protocol. All commands, addresses and input data bytes are shifted inside the device, the most significant bit first. The first serial data input (MOSI) is sampled on the first rising edge of the serial clock (SCK) after slave select (SS) goes low. *Figure 19* shows the writing of a single byte into the device.

Figure 19. SPI protocol (writing)



All output data bytes are shifted out of the device, the most significant bit first. The serial data output (MISO) is latched on the first falling edge of the serial clock (SCK) after the command (such as the read from control registers) has been clocked into the device. *Figure 20* shows the reading of a single byte from the device.

Figure 20. SPI protocol (reading)



4.9.1 Command byte

Table 47. SPI commands

Value (hex)	Value (bin)	Meaning
00	00000000	Writing to control register memory
02	00000010	Writing to pattern 1 memory
04	00000100	Writing to pattern 2 memory
01	00000001	Reading from control register memory
03	00000011	Reading from pattern 1 memory
05	00000101	Reading from pattern 2 memory

4.9.2 Address byte

Table 48. SPI values

Value (hex)	Value (bin)	Meaning
00	00000000	Writing to control register memory
02	00000010	Writing to pattern 1 memory
04	00000100	Writing to pattern 2 memory
01	00000001	Reading from control register memory
03	00000011	Reading from pattern 1 memory
05	00000101	Reading from pattern 2 memory

Table 49. SPI addresses

Address range (hex)		Memory
from	to	
00	FF	Control registers
00	EF	Pattern 1
00	EF	Pattern 2

Writing to the address out of specified ranges is ignored.

The internal address register is incremented automatically when a byte is written or read. When the address register reaches the end of the address range, it resets to 0.

4.9.3 SPI timing

Figure 21. Serial input timing

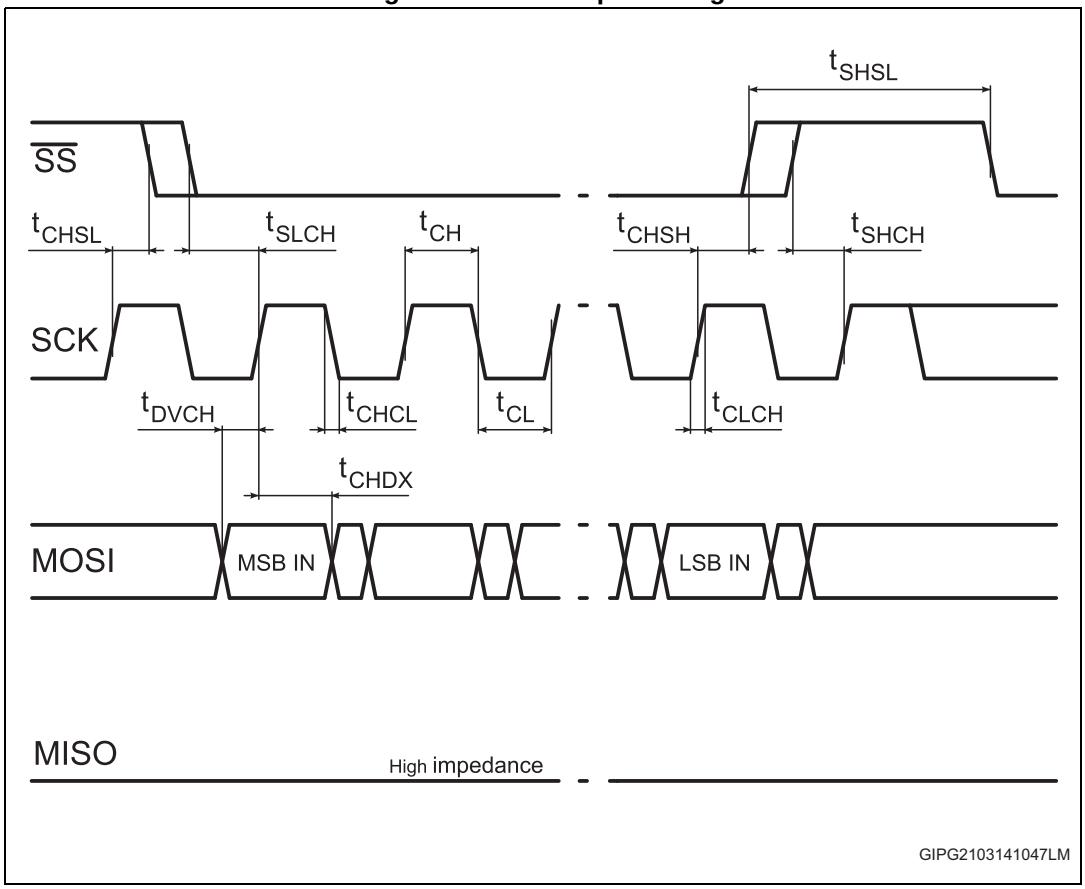
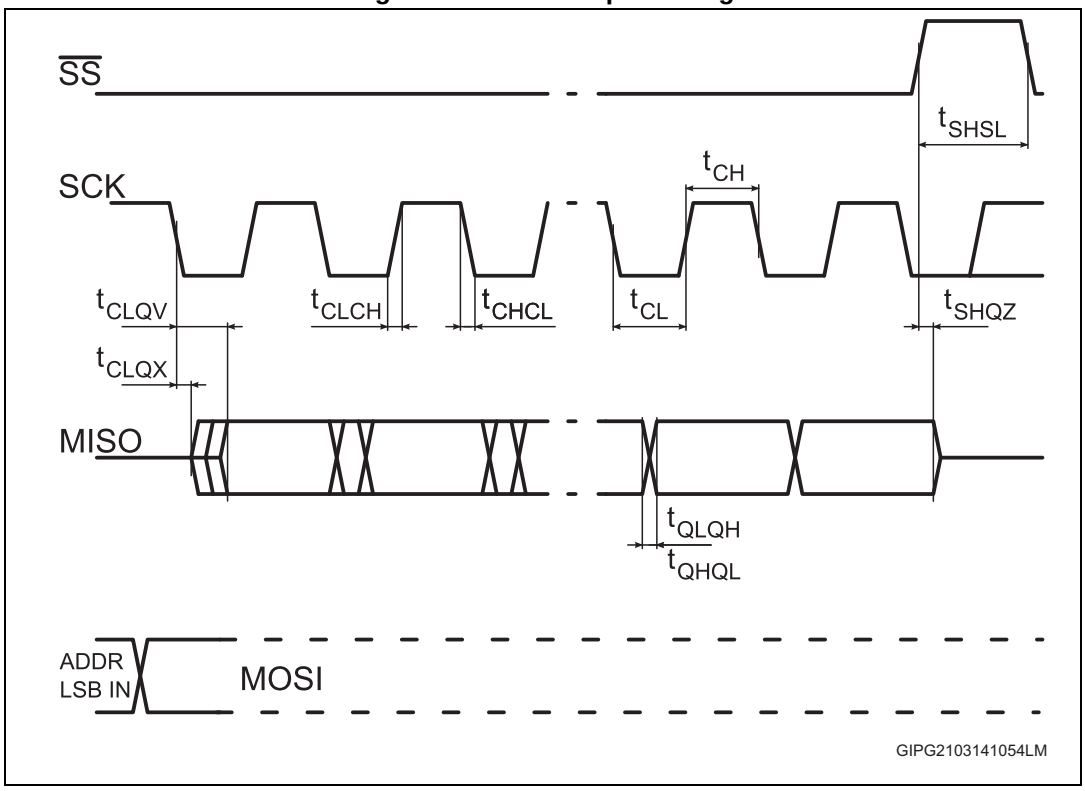


Figure 22. Serial output timing



Data are captured on SCK rising edge and are propagated to SCK falling edge.

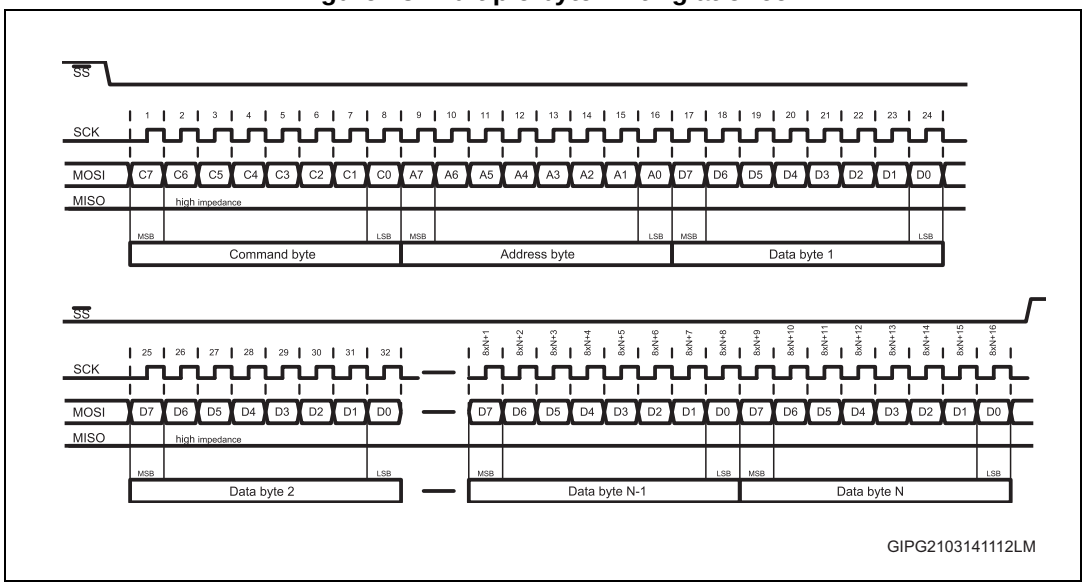
SCK is low when it is in idle mode. SPI master selects one slave at a time through 5 pF C_{max} SS signal.

Table 50. SPI timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_C	Clock frequency	DC		20	MHz
t_{SLCH}	SS active set-up time	20			ns
t_{SHCH}	SS not active set-up time	10			ns
t_{SHSL}	SS deselect time	100			ns
t_{CHSH}	SS active hold time	20			ns
t_{CHSL}	SS not active hold time	10			ns
t_{CH}	Clock high time	20			ns
t_{CL}	Clock low time	20			ns
t_{CLCH}	Clock rise time			5	ns
t_{CHCL}	Clock fall time			5	ns
t_{DVCH}	Data in set-up time	4			ns
t_{CHDX}	Data in hold time	5			ns
t_{SHQZ}	Output disable time			20	ns
t_{CLQV}	Clock low to output valid			23	ns
t_{CLQX}	Output hold time	0			ns
t_{QLQH}	Output rise time			10	ns
t_{QHQL}	Output fall time			10	ns

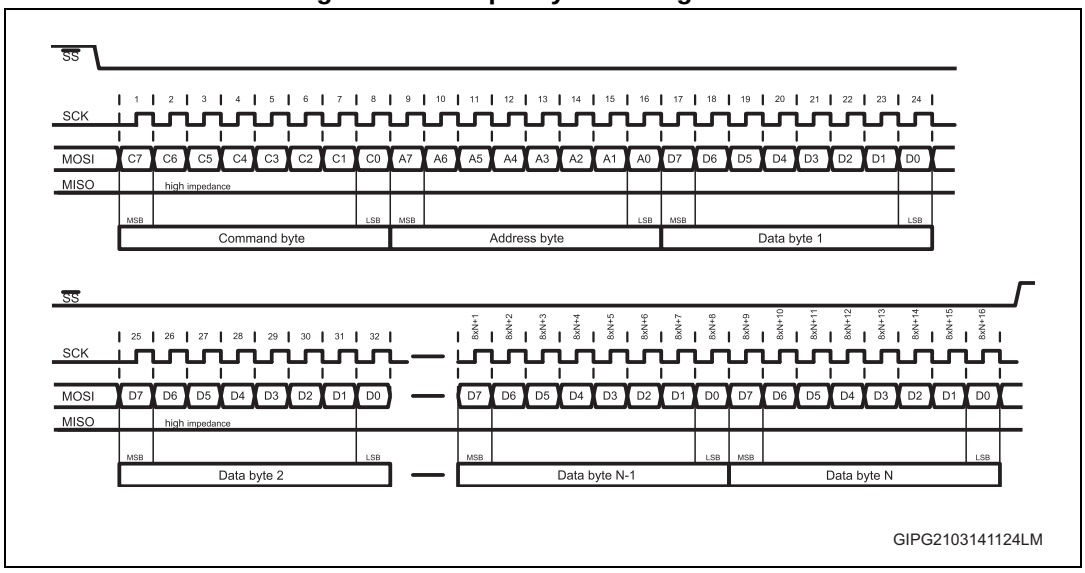
4.9.4 Writing and reading multiple bytes at once

Figure 23. Multiple byte writing at once



The STLED524 supports the writing of multiple bytes at once. When the first byte is received, the internal address counter is incremented automatically. Next byte from SPI frame is written into this new address and so on, until the n^{th} byte is received. If the address counter reaches the end of address space, it resets to 0 automatically and the writing continues. When the reading of multiple bytes is performed, the internal address register is incremented after each byte reading automatically. If the address counter reaches the end of address space, it resets to 0 automatically and the reading continues.

Figure 24. Multiple byte reading at once



4.10 Protections and interrupts

4.10.1 Registers related to protections and interrupts

There are 3 registers related to protections and interrupts. They are: status, latch and interrupt enable registers.

Table 51. Interrupt enable register

Interrupt enable	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 40h	BSTOK_M	ROWSC_M	EOSCR_M	STEP_M	SHORT_M	OPEN_M	THP_M	OVP_M
Default	0	0	0	0	0	0	0	0

OVP_M = 0, the interrupt generated by overvoltage protection is disabled

OVP_M = 1, the interrupt generated by overvoltage protection is enabled

THP_M = 0, the interrupt generated by overtemperature protection is disabled

THP_M = 1, the interrupt generated by overtemperature protection is enabled

OPEN_M = 0, the interrupt generated by open R_{SET} protection is disabled

OPEN_M = 1, the interrupt generated by open R_{SET} protection is enabled

SHORT_M = 0, the interrupt generated by short R_{SET} protection is disabled

SHORT_M = 1, the interrupt generated by short R_{SET} protection is enabled

STEP_M = 0 the interrupt generated at the beginning of a scroll step is disabled

STEP_M = 1, the interrupt generated at the beginning of a scroll step is enabled

EOSCR_M = 0, the interrupt generated at the end of scroll operation is disabled

EOSCR_M = 1, the interrupt generated at the end of scroll operation is enabled

ROWSC_M = 0, the interrupt generated by row short-circuit is disabled

ROWSC_M = 1, the interrupt generated by row short-circuit is enabled

BSTOK_M = 0, the interrupt generated, when the boost output voltage reaches the target value, is disabled

BSTOK_M = 1, the interrupt generated, when the boost output voltage reaches the target value, is enabled

Table 52. Latch register (read only)

Latch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 41h	BSTOK	ROWSC	EOSCR	STEP	SHORT	OPEN	THP	OVP
Default	0	0	0	0	0	0	0	0

Bits in this register are set when the corresponding interrupt occurs. These bits are latched and they can only be cleared by reading the register through SPI.

When an interrupt is disabled, the corresponding bit in the latch register is not set.

Table 53. Status register (read only)

Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 42h	BSTOK	-	-	-	SHORT	OPEN	THP	OVP
Default	0	0	0	0	0	0	0	0

Bits in the status register are set and reset according to the state of internal signals (overtemperature, overvoltage etc.). Reading the status register through SPI does not influence the state of bits.

4.10.2 Overvoltage protection

If the output voltage of boost is higher than the overvoltage protection threshold, the boost is stopped. OVP bit in the status register is set. The interrupt is generated, if it is enabled and OVP bit in the latch register is also set and remains latched, until it is read through SPI. If the output voltage of the boost goes below the overvoltage protection hysteresis, OVP bit in the status register is reset. The microcontroller decides, whether to start the boost again or not.

4.10.3 Thermal protection

There are two thermal sensors inside the chip. The former protects boost and current mirrors. The latter protects LDO. Boost thermal protection and current mirrors have TSHDN1 threshold (150 °C) and 20 °C hysteresis, while LDO thermal protection has TSHDN2 threshold (170 °C) and 20 °C hysteresis.

If the chip temperature reaches the first TSHDN1 threshold, boost and current mirrors are automatically disabled (EN bit and BSTEN bit are reset). An interrupt is generated, if it is enabled and THP in the latch register is set. If the chip temperature goes below thermal shutdown hysteresis, an interrupt is generated, THP bit in the status register is reset and THP bit in the latch register is set. Boost and current mirrors are not re-enabled automatically; the microcontroller can do it.

If the microcontroller tries to re-enable boost and current mirrors, when THP is active, boost and current mirrors stay off.

When LDO temperature reaches TSHDN2 threshold, it is turned off. If LDO supplies the digital part, the content of patterns and all settings in the control registers are lost. LDO is re-enabled automatically, as soon as its temperature goes below TSHDN2HYST overtemperature hysteresis.

4.10.4 Open ISET protection

When EN bit is set to 1, REFSEL bit is set to 0 and ISET pin is opened or R_{SET} resistor value is higher than 270 kΩ typically, then current mirrors are turned off. Boost operation is not touched. OPEN bit is set in the status register and an interrupt is generated, if it is enabled and OPEN bit in the latch register is set. EN bit is not touched, but current mirrors are disabled. In this situation the microcontroller has the possibility to set REFSEL bit to 1 in the clock register and run with the internal reference for the current mirrors.

4.10.5 Short ISET protection

When EN bit is set to 1, REFSEL bit is set to 0 and ISET pin is shorted or R_{SET} value is lower than 14 kΩ, then current mirrors are turned off. Boost operation is not touched. SHORT bit is set in the status register and an interrupt is generated, if it is enabled and SHORT bit in the latch register is set. EN bit is not touched, but current mirrors are disabled. In this situation the microcontroller has the possibility to set REFSEL bit to 1 in the clock register and run with the internal reference for the current mirrors.

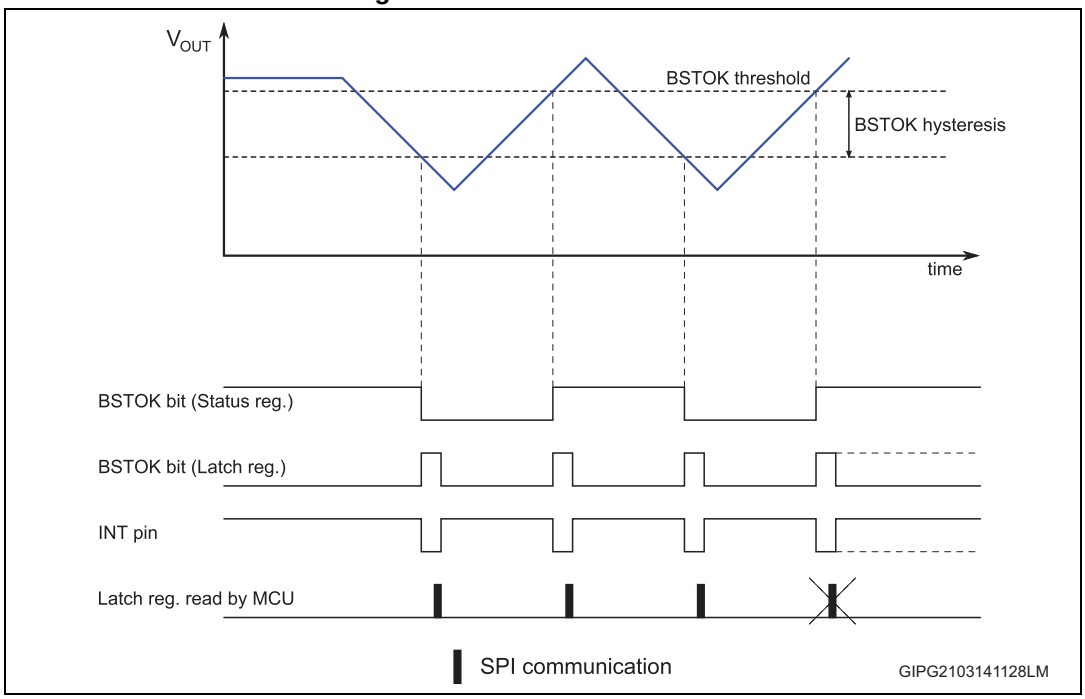
4.10.6 Row transistor protection

If any of 5-row pins is shorted to GND, current mirrors are disabled and EN bit is reset. An interrupt is generated, if it is enabled and ROWSC bit in the latch register is set.

4.10.7 Boost output voltage OK

When boost output voltage reaches the target value given by VOUT register (VOUTSET), BSTOK bit in the status register is set to 1. An interrupt is generated, if it is enabled. BSTOK bit in the latch register is set to 1. When boost output voltage falls below VOUTSET, VBSTOKHYST, BSTOK bit is reset and an interrupt is generated, if it is enabled. BSTOK bit hasn’t any impact on boost or current mirrors. The microcontroller can decide whether to stop operation of the display or not, if boost output voltage is not sufficient (BSTOK = 0).

Figure 25. BSTOK bit behavior



4.10.8 EOSCR and step interrupts

Functions of these two interrupts are described in *Section 4.7.3*.

4.11 Shutdown mode

When the device is in shutdown mode, its power consumption is minimized. It is not possible to write data to any register over SPI. RESET/PWRDN pin has to be low to keep the device in shutdown mode. LDO is always alive regardless of the level on RESET/PWRDN pin. SCK, MOSI, SS, SYNC and CLKIN logic input pins can increase power consumption, if they are left floating. These pins should be connected to either logic 0 or logic 1 in shutdown mode. Thanks to this condition, the minimum power consumption can be achieved. INT pin is pulled up typically. If this pin is not used in the application, it can be left floating in shutdown mode without any negative impact on power consumption. Do not pull this pin down in shutdown mode as it increases power consumption. MISO pin is in high Z state, when the device is in shutdown mode. So it can be left floating or it can be pulled up or down without any effect on power consumption in shutdown mode. CLKOUT pin is driven low internally in shutdown mode. So it can be left floating in shutdown mode. Do not pull this pin up in shutdown mode as it increases power consumption.

4.12 Undervoltage lockout

If the input voltage falls below VUVLOF threshold, the device enters the undervoltage lockout. Boost and drivers are turned off. LDO is not turned off. When the input voltage rises above VUVLOR, patterns have to be loaded again and the device has to be re-enabled, because it is not guaranteed that the digital section can keep data during the undervoltage lockout.

5 List of control registers

Table 54. List of control registers

Name	Add	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software control	00h	SWRST	-	-	-	-	CLR2	CLR1	EN
		0	0	0	0	0	0	0	0
		ACLR	-	-	-	-	ACLR	ACLR	R/W
Display control	01h	-	-	-	-	-	-	DISP2	DISP1
		0	0	0	0	0	0	0	0
		-	-	-	-	-	-	R/W	R/W
Section A: these settings should be applied with EN=0									
Clock	10h	-	-	-	REFSEL	SYNCSEL	SYNCEN	CLKIN	CLKOUT
		0	0	0	0	0	0	0	0
		-	-	-	R/W	R/W	R/W	R/W	R/W
Column control 1	11h	COL7EN	COL6EN	COL5EN	COL4EN	COL3EN	COL2EN	COL1EN	COL0EN
		1	1	1	1	1	1	1	1
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Column control 2	12h	COL15EN	COL14EN	COL13EN	COL12EN	COL11EN	COL10EN	COL9EN	COL8EN
		1	1	1	1	1	1	1	1
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Column control 3	13h	COL23EN	COL22EN	COL21EN	COL20EN	COL19EN	COL18EN	COL17EN	COL16EN
		1	1	1	1	1	1	1	1
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Row control	14h	-	-	-	ROW4EN	ROW3EN	ROW2EN	ROW1EN	ROW0EN
		0	0	0	1	1	1	1	1
		-	-	-	R/W	R/W	R/W	R/W	R/W

Table 54. List of control registers (continued)

Name	Add	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blanking time	15h	-	-	-	-	-	BLK[2:0]		
		0	0	0	0	0	0	0	0
		-	-	-	-	-	R/W	R/W	R/W
Boost control	16h	BSTEN	-	-	-	VOUT[3:0]			
		0	-	-	-	1	0	1	0
		R/W	-	-	-	R/W	R/W	R/W	R/W
Section B:									
Display visual control	20h	-	-	BRCEN	WAITEN	SLPEN	SCRLEN	PWMEN	DISPSIZE
		0	0	0	0	0	0	0	0
		-	-	R/W	R/W	R/W	R/W	R/W	R/W
PWM control	21h	PWM[7:0]							
		0	0	0	0	0	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Section C: these settings should be applied when scroll is not active (EOSCR = 1)									
Scroll control 1	30h	SCLSPD[5:0]						SCRL_DIR[1:0]	
		0	0	0	0	0	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Scroll control 2	31h	BLNK_R[2:0]			BLNK_C[4:0]				
		0	0	0	0	0	0	0	0
		W	W	W	W	W	W	W	W
Scroll control 3	32h	-	-	WAIT[2:0]					
		0	0	0	0	0	0	0	0
		-	-	R/W	R/W	R/W	R/W	R/W	R/W

Table 54. List of control registers (continued)

Name	Add	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Column lock 1	33h	COLCK7	COLCK6	COLCK5	COLCK4	COLCK3	COLCK2	COLCK1	COLCK0
		0	0	0	0	0	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Column lock 2	34h	COLCK15	COLCK14	COLCK13	COLCK12	COLCK11	COLCK10	COLCK9	COLCK8
		0	0	0	0	0	0	0	0
		-	-	R/W	R/W	R/W	R/W	R/W	R/W
Column lock 3	35h	COLCK23	COLCK22	COLCK21	COLCK20	COLCK19	COLCK18	COLCK17	COLCK16
		0	0	0	0	0	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Row lock	36h	-	-	-	ROWLCK4	ROWLCK3	ROWLCK2	ROWLCK1	ROWLCK0
		0	0	0	0	0	0	0	0
		-	-	-	R/W	R/W	R/W	R/W	R/W
Section D: interrupts									
Interrupt enable	40h	BST_OK_M	ROWSC_M	EOSCR_M	STEP_M	SHORT_M	OPEN_M	THP_M	OVP_M
		0	0	0	0	0	0	0	0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Latch	41h	BST_OK	ROWSC	EOSCR	STEP	SHORT	OPEN	THP	OVP
		0	0	0	0	0	0	0	0
		RCLEAR	RCLEAR	RCLEAR	RCLEAR	RCLEAR	RCLEAR	RCLEAR	RCLEAR
Status	42h	BST_OK	ROWSC	EOSCR	-	SHORT	OPEN	THP	OVP
		0	0	1	0	0	0	0	0
		R	R	R	-	R	R	R	R

Table 54. List of control registers (continued)

Name	Add	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Scroll steps	43h	-	-		SCRSTP [5:0]				
		0	0	0	0	0	0	0	0
		-	-	R	R	R	R	R	R
Version	FFh	-	-	-	-	VER[3:0]			
		0	0	0	0	0	0	0	1
		-	-	-	-	R	R	R	R

6 Application information

6.1 Pattern examples

6.1.1 Example 1 - rectangle

Dimming of all dots in the rectangle is set to 255. Slope is set to 1 and delay is set to 0.

Figure 26. Example 1

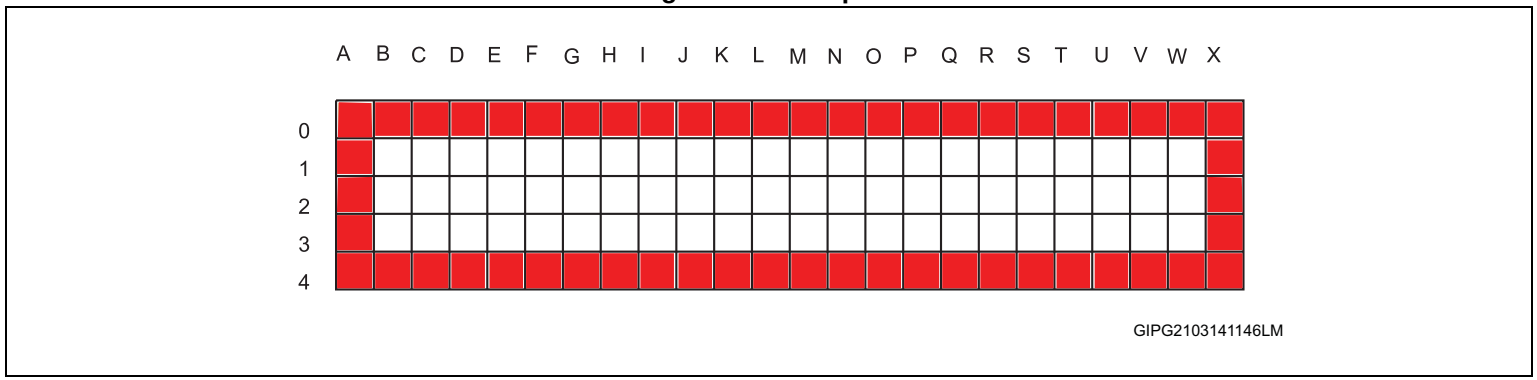


Table 55. Pattern data for example 1

Row		0			1			2			3			4	
Col.	Add	Dimm.	S&D[1]	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D
A	0x00	0xFF	0x04	0x02	0xFF	0x04	0x04	0xFF	0x04	0x06	0xFF	0x04	0x08	0xFF	0x04
B	0x0A	0xFF	0x04	0x0C	0x00	0x00	0x0E	0x00	0x00	0x10	0x00	0x00	0x12	0xFF	0x04
C	0x14	0xFF	0x04	0x16	0x00	0x00	0x18	0x00	0x00	0x1A	0x00	0x00	0x1C	0xFF	0x04
D	0x1E	0xFF	0x04	0x20	0x00	0x00	0x22	0x00	0x00	0x24	0x00	0x00	0x26	0xFF	0x04
E	0x28	0xFF	0x04	0x2A	0x00	0x00	0x2C	0x00	0x00	0x2E	0x00	0x00	0x30	0xFF	0x04
F	0x32	0xFF	0x04	0x34	0x00	0x00	0x36	0x00	0x00	0x38	0x00	0x00	0x3A	0xFF	0x04
G	0x3C	0xFF	0x04	0x3E	0x00	0x00	0x40	0x00	0x00	0x42	0x00	0x00	0x44	0xFF	0x04
H	0x46	0xFF	0x04	0x48	0x00	0x00	0x4A	0x00	0x00	0x4C	0x00	0x00	0x4E	0xFF	0x04
I	0x50	0xFF	0x04	0x52	0x00	0x00	0x54	0x00	0x00	0x56	0x00	0x00	0x58	0xFF	0x04
J	0x5A	0xFF	0x04	0x5C	0x00	0x00	0x5E	0x00	0x00	0x60	0x00	0x00	0x62	0xFF	0x04
K	0x64	0xFF	0x04	0x66	0x00	0x00	0x68	0x00	0x00	0x6A	0x00	0x00	0x6C	0xFF	0x04
L	0x6E	0xFF	0x04	0x70	0x00	0x00	0x72	0x00	0x00	0x74	0x00	0x00	0x76	0xFF	0x04
M	0x78	0xFF	0x04	0x7A	0x00	0x00	0x7C	0x00	0x00	0x7E	0x00	0x00	0x80	0xFF	0x04
N	0x82	0xFF	0x04	0x84	0x00	0x00	0x86	0x00	0x00	0x88	0x00	0x00	0x8A	0xFF	0x04
O	0x8C	0xFF	0x04	0x8E	0x00	0x00	0x90	0x00	0x00	0x92	0x00	0x00	0x94	0xFF	0x04
P	0x96	0xFF	0x04	0x98	0x00	0x00	0x9A	0x00	0x00	0x9C	0x00	0x00	0x9E	0xFF	0x04
Q	0xA0	0xFF	0x04	0xA2	0x00	0x00	0xA4	0x00	0x00	0xA6	0x00	0x00	0xA8	0xFF	0x04
R	0xAA	0xFF	0x04	0xAC	0x00	0x00	0xAE	0x00	0x00	0xB0	0x00	0x00	0xB2	0xFF	0x04
S	0xB4	0xFF	0x04	0xB6	0x00	0x00	0xB8	0x00	0x00	0xBA	0x00	0x00	0xBC	0xFF	0x04
T	0xBE	0xFF	0x04	0xC0	0x00	0x00	0xC2	0x00	0x00	0xC4	0x00	0x00	0xC6	0xFF	0x04
U	0xC8	0xFF	0x04	0xCA	0x00	0x00	0xCC	0x00	0x00	0xCE	0x00	0x00	0xD0	0xFF	0x04
V	0xD2	0xFF	0x04	0xD4	0x00	0x00	0xD6	0x00	0x00	0xD8	0x00	0x00	0xDA	0xFF	0x04

Table 55. Pattern data for example 1 (continued)

Row		0			1			2			3			4	
Col.	Add	Dimm.	S&D(1)	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D
W	0xDC	0xFF	0x04	0xDE	0x00	0x00	0xE0	0x00	0x00	0xE2	0x00	0x00	0xE4	0xFF	0x04
X	0xE6	0xFF	0x04	0xE8	0xFF	0x04	0xEA	0xFF	0x04	0xEC	0xFF	0x04	0xEE	0xFF	0x04

1. Slope and delay, please see *Table 11*.

6.1.2 Example 2 - dimming settings

Columns L and M are the brightest. Their dimming is set to 255. Columns J, K, N and O have dimming set to 240. Columns H, I, P and Q have dimming set to 225. Columns F, G, R and S have dimming set to 210. Columns D, E, T and U have dimming set to 195. Columns B, C, V and W have dimming set to 180. Slope and delay settings of all dots are 0.

Figure 27. Example 2

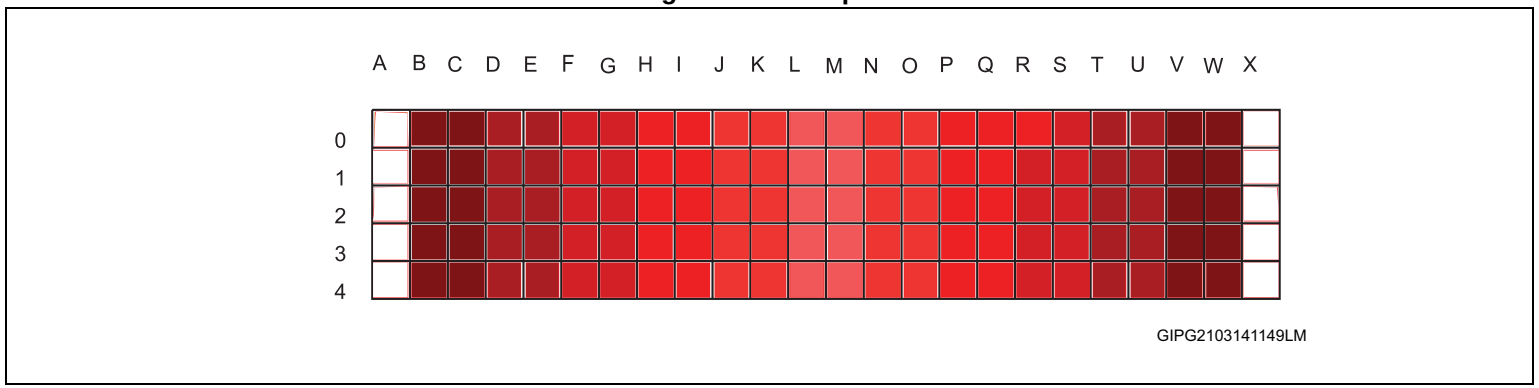


Table 56. Pattern data for example 2

Row		0			1			2			3			4	
Col.	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D
A	0x00	0x00	0x00	0x02	0x00	0x00	0x04	0x00	0x00	0x06	0x00	0x00	0x08	0x00	0x00
B	0x0A	0xAA	0x00	0x0C	0xAA	0x00	0x0E	0xAA	0x00	0x10	0xAA	0x00	0x12	0xAA	0x00
C	0x14	0xAA	0x00	0x16	0xAA	0x00	0x18	0xAA	0x00	0x1A	0xAA	0x00	0x1C	0xAA	0x00
D	0x1E	0xC3	0x00	0x20	0xC3	0x00	0x22	0xC3	0x00	0x24	0xC3	0x00	0x26	0xC3	0x00
E	0x28	0xC3	0x00	0x2A	0xC3	0x00	0x2C	0xC3	0x00	0x2E	0xC3	0x00	0x30	0xC3	0x00
F	0x32	0xD2	0x00	0x34	0xD2	0x00	0x36	0xD2	0x00	0x38	0xD2	0x00	0x3A	0xD2	0x00
G	0x3C	0xD2	0x00	0x3E	0xD2	0x00	0x40	0xD2	0x00	0x42	0xD2	0x00	0x44	0xD2	0x00
H	0x46	0xE1	0x00	0x48	0xE1	0x00	0x4A	0xE1	0x00	0x4C	0xE1	0x00	0x4E	0xE1	0x00
I	0x50	0xE1	0x00	0x52	0xE1	0x00	0x54	0xE1	0x00	0x56	0xE1	0x00	0x58	0xE1	0x00
J	0x5A	0xF0	0x00	0x5C	0xF0	0x00	0x5E	0xF0	0x00	0x60	0xF0	0x00	0x62	0xF0	0x00
K	0x64	0xF0	0x00	0x66	0xF0	0x00	0x68	0xF0	0x00	0x6A	0xF0	0x00	0x6C	0xF0	0x00
L	0x6E	0xFF	0x00	0x70	0xFF	0x00	0x72	0xFF	0x00	0x74	0xFF	0x00	0x76	0xFF	0x00
M	0x78	0xFF	0x00	0x7A	0xFF	0x00	0x7C	0xFF	0x00	0x7E	0xFF	0x00	0x80	0xFF	0x00
N	0x82	0xF0	0x00	0x84	0xF0	0x00	0x86	0xF0	0x00	0x88	0xF0	0x00	0x8A	0xF0	0x00
O	0x8C	0xF0	0x00	0x8E	0xF0	0x00	0x90	0xF0	0x00	0x92	0xF0	0x00	0x94	0xF0	0x00
P	0x96	0xE1	0x00	0x98	0xE1	0x00	0x9A	0xE1	0x00	0x9C	0xE1	0x00	0x9E	0xE1	0x00
Q	0xA0	0xE1	0x00	0xA2	0xE1	0x00	0xA4	0xE1	0x00	0xA6	0xE1	0x00	0xA8	0xE1	0x00
R	0xAA	0xD2	0x00	0xAC	0xD2	0x00	0xAE	0xD2	0x00	0xB0	0xD2	0x00	0xB2	0xD2	0x00
S	0xB4	0xD2	0x00	0xB6	0xD2	0x00	0xB8	0xD2	0x00	0xBA	0xD2	0x00	0xBC	0xD2	0x00
T	0xBE	0xC3	0x00	0xC0	0xC3	0x00	0xC2	0xC3	0x00	0xC4	0xC3	0x00	0xC6	0xC3	0x00
U	0xC8	0xC3	0x00	0xCA	0xC3	0x00	0xCC	0xC3	0x00	0xCE	0xC3	0x00	0xD0	0xC3	0x00
V	0xD2	0xAA	0x00	0xD4	0xAA	0x00	0xD6	0xAA	0x00	0xD8	0xAA	0x00	0xDA	0xAA	0x00

Table 56. Pattern data for example 2 (continued)

Row		0			1			2			3			4	
Col.	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D
W	0xDC	0xAA	0x00	0xDE	0xAA	0x00	0xE0	0xAA	0x00	0xE2	0xAA	0x00	0xE4	0xAA	0x00
X	0xE6	0x00	0x00	0xE8	0x00	0x00	0xEA	0x00	0x00	0xEC	0x00	0x00	0xEE	0x00	0x00

6.1.3 Example 3 - slope settings

Dots, creating number 1, have dimming set to 255, slope to 1 and delay to 0. Dots, creating number 2, have dimming set to 255, slope to 2 and delay to 0. Dots, creating number 3, have dimming set to 255, slope to 3 and delay to 0. When this pattern is displayed with SLPEN=1, number 1 brightness ramps up/down at the furthest speed, number 2 at medium speed and number 3 at the slowest speed.

Figure 28. Example 3

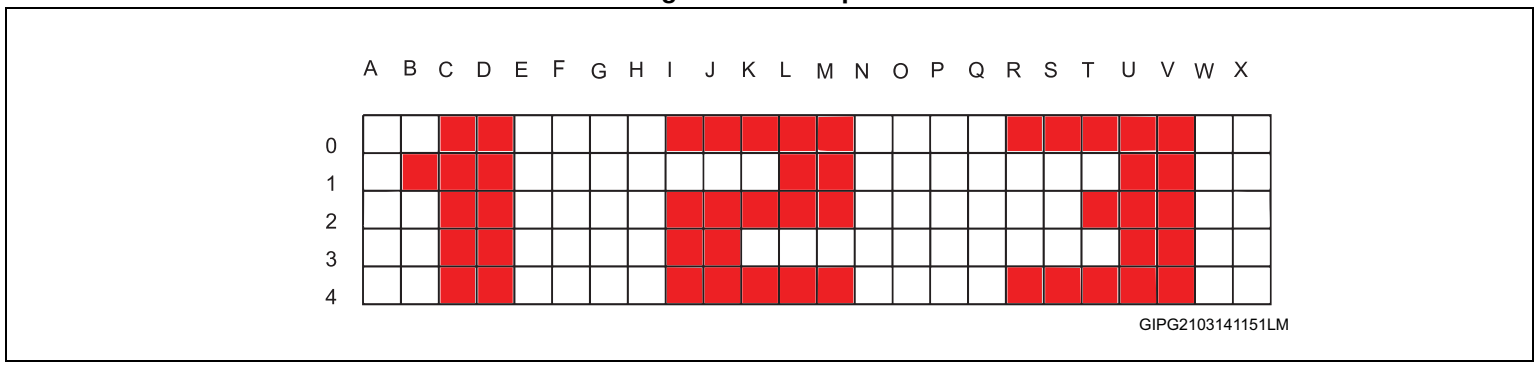


Table 57. Pattern data for example 3

Row		0			1			2			3			4	
Col.	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D
A	0x00	0x00	0x00	0x02	0x00	0x00	0x04	0x00	0x00	0x06	0x00	0x00	0x08	0x00	0x00
B	0x0A	0x00	0x00	0x0C	0xFF	0x04	0x0E	0x00	0x00	0x10	0x00	0x00	0x12	0x00	0x00
C	0x14	0xFF	0x04	0x16	0xFF	0x04	0x18	0xFF	0x04	0x1A	0xFF	0x04	0x1C	0xFF	0x04

Table 57. Pattern data for example 3 (continued)

Row		0			1			2			3			4	
Col.	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D
D	0x1E	0xFF	0x04	0x20	0xFF	0x04	0x22	0xFF	0x04	0x24	0xFF	0x04	0x26	0xFF	0x04
E	0x28	0x00	0x00	0x2A	0x00	0x00	0x2C	0x00	0x00	0x2E	0x00	0x00	0x30	0x00	0x00
F	0x32	0x00	0x00	0x34	0x00	0x00	0x36	0x00	0x00	0x38	0x00	0x00	0x3A	0x00	0x00
G	0x3C	0x00	0x00	0x3E	0x00	0x00	0x40	0x00	0x00	0x42	0x00	0x00	0x44	0x00	0x00
H	0x46	0x00	0x00	0x48	0x00	0x00	0x4A	0x00	0x00	0x4C	0x00	0x00	0x4E	0x00	0x00
I	0x50	0xFF	0x08	0x52	0x00	0x00	0x54	0xFF	0x08	0x56	0xFF	0x08	0x58	0xFF	0x08
J	0x5A	0xFF	0x08	0x5C	0x00	0x00	0x5E	0xFF	0x08	0x60	0xFF	0x08	0x62	0xFF	0x08
K	0x64	0xFF	0x08	0x66	0x00	0x00	0x68	0xFF	0x08	0x6A	0x00	0x00	0x6C	0xFF	0x08
L	0x6E	0xFF	0x08	0x70	0xFF	0x08	0x72	0xFF	0x08	0x74	0x00	0x00	0x76	0xFF	0x08
M	0x78	0xFF	0x08	0x7A	0xFF	0x08	0x7C	0xFF	0x08	0x7E	0x00	0x00	0x80	0xFF	0x08
N	0x82	0x00	0x00	0x84	0x00	0x00	0x86	0x00	0x00	0x88	0x00	0x00	0x8A	0x00	0x00
O	0x8C	0x00	0x00	0x8E	0x00	0x00	0x90	0x00	0x00	0x92	0x00	0x00	0x94	0x00	0x00
P	0x96	0x00	0x00	0x98	0x00	0x00	0x9A	0x00	0x00	0x9C	0x00	0x00	0x9E	0x00	0x00
Q	0xA0	0x00	0x00	0xA2	0x00	0x00	0xA4	0x00	0x00	0xA6	0x00	0x00	0xA8	0x00	0x00
R	0xAA	0xFF	0x0C	0xAC	0x00	0x00	0xAE	0x00	0x00	0xB0	0x00	0x00	0xB2	0xFF	0x0C
S	0xB4	0xFF	0x0C	0xB6	0x00	0x00	0xB8	0x00	0x00	0xBA	0x00	0x00	0xBC	0xFF	0x0C
T	0xBE	0xFF	0x0C	0xC0	0x00	0x00	0xC2	0xFF	0x0C	0xC4	0x00	0x00	0xC6	0xFF	0x0C
U	0xC8	0xFF	0x0C	0xCA	0xFF	0x0C	0xCC	0xFF	0x0C	0xCE	0xFF	0x0C	0xD0	0xFF	0x0C
V	0xD2	0xFF	0x0C	0xD4	0xFF	0x0C	0xD6	0xFF	0x0C	0xD8	0xFF	0x0C	0xDA	0xFF	0x0C
W	0xDC	0x00	0x00	0xDE	0x00	0x00	0xE0	0x00	0x00	0xE2	0x00	0x00	0xE4	0x00	0x00
X	0xE6	0x00	0x00	0xE8	0x00	0x00	0xEA	0x00	0x00	0xEC	0x00	0x00	0xEE	0x00	0x00

6.1.4 Example 4 - delay settings

Dots, creating number 0, have dimming set to 255, slope to 1 and delay to 0. Dots, creating number 2, have dimming set to 255, slope to 1 and delay to 1. Dots, creating number 2, have dimming set to 255, slope to 1 and delay to 2. Dots, creating number 3, have dimming set to 255, slope to 1 and delay to 3. When this pattern is displayed with SLPEN=1, brightness of all numbers ramps up/down at the same speed. Ramping of number 1 is delayed by 1 phase compared to number 0. Ramping of number 2 is delayed by 2 phases compared to number 0. Ramping of number 3 is delayed by 3 phases compared to number 0.

Figure 29. Example 4

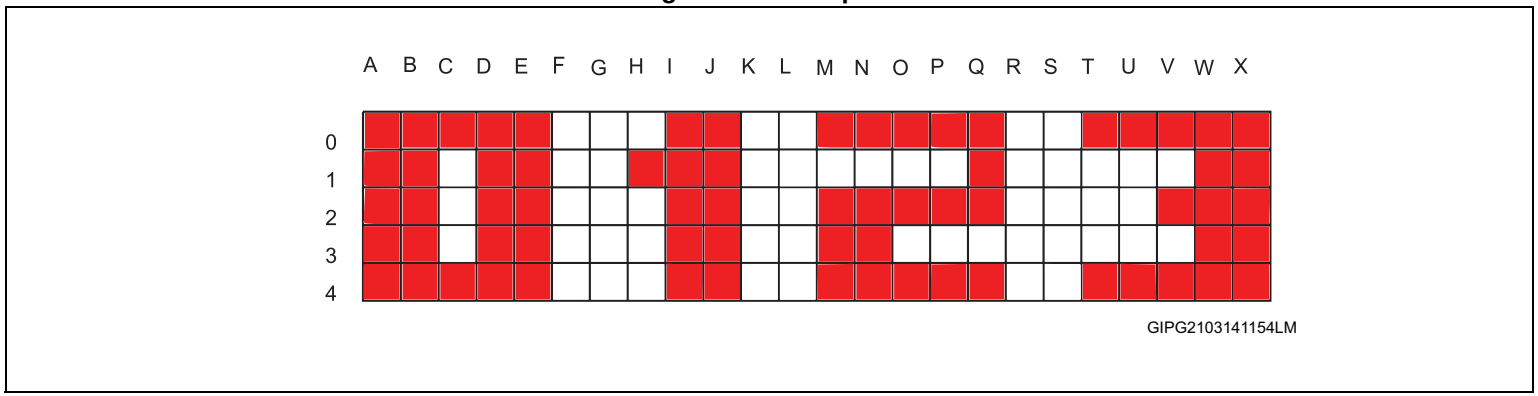


Table 58. Pattern data for example 4

Row	0			1			2			3			4		
Col.	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D
A	0x00	0x00	0x00	0x02	0x00	0x00	0x04	0x00	0x00	0x06	0x00	0x00	0x08	0x00	0x00
B	0x0A	0x00	0x00	0x0C	0xFF	0x04	0x0E	0x00	0x00	0x10	0x00	0x00	0x12	0x00	0x00
C	0x14	0xFF	0x04	0x16	0xFF	0x04	0x18	0xFF	0x04	0x1A	0xFF	0x04	0x1C	0xFF	0x04
D	0x1E	0xFF	0x04	0x20	0xFF	0x04	0x22	0xFF	0x04	0x24	0xFF	0x04	0x26	0xFF	0x04
E	0x28	0x00	0x00	0x2A	0x00	0x00	0x2C	0x00	0x00	0x2E	0x00	0x00	0x30	0x00	0x00
F	0x32	0x00	0x00	0x34	0x00	0x00	0x36	0x00	0x00	0x38	0x00	0x00	0x3A	0x00	0x00
G	0x3C	0x00	0x00	0x3E	0x00	0x00	0x40	0x00	0x00	0x42	0x00	0x00	0x44	0x00	0x00

Table 58. Pattern data for example 4 (continued)

Row	0			1			2			3			4		
Col.	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D	Add	Dimm.	S&D
H	0x46	0x00	0x00	0x48	0x00	0x00	0x4A	0x00	0x00	0x4C	0x00	0x00	0x4E	0x00	0x00
I	0x50	0xFF	0x08	0x52	0x00	0x00	0x54	0xFF	0x08	0x56	0xFF	0x08	0x58	0xFF	0x08
J	0x5A	0xFF	0x08	0x5C	0x00	0x00	0x5E	0xFF	0x08	0x60	0xFF	0x08	0x62	0xFF	0x08
K	0x64	0xFF	0x08	0x66	0x00	0x00	0x68	0xFF	0x08	0x6A	0x00	0x00	0x6C	0xFF	0x08
L	0x6E	0xFF	0x08	0x70	0xFF	0x08	0x72	0xFF	0x08	0x74	0x00	0x00	0x76	0xFF	0x08
M	0x78	0xFF	0x08	0x7A	0xFF	0x08	0x7C	0xFF	0x08	0x7E	0x00	0x00	0x80	0xFF	0x08
N	0x82	0x00	0x00	0x84	0x00	0x00	0x86	0x00	0x00	0x88	0x00	0x00	0x8A	0x00	0x00
O	0x8C	0x00	0x00	0x8E	0x00	0x00	0x90	0x00	0x00	0x92	0x00	0x00	0x94	0x00	0x00
P	0x96	0x00	0x00	0x98	0x00	0x00	0x9A	0x00	0x00	0x9C	0x00	0x00	0x9E	0x00	0x00
Q	0xA0	0x00	0x00	0xA2	0x00	0x00	0xA4	0x00	0x00	0xA6	0x00	0x00	0xA8	0x00	0x00
R	0xAA	0xFF	0x0C	0xAC	0x00	0x00	0xAE	0x00	0x00	0xB0	0x00	0x00	0xB2	0xFF	0x0C
S	0xB4	0xFF	0x0C	0xB6	0x00	0x00	0xB8	0x00	0x00	0xBA	0x00	0x00	0xBC	0xFF	0x0C
T	0xBE	0xFF	0x0C	0xC0	0x00	0x00	0xC2	0xFF	0x0C	0xC4	0x00	0x00	0xC6	0xFF	0x0C
U	0xC8	0xFF	0x0C	0xCA	0xFF	0x0C	0xCC	0xFF	0x0C	0xCE	0xFF	0x0C	0xD0	0xFF	0x0C
V	0xD2	0xFF	0x0C	0xD4	0xFF	0x0C	0xD6	0xFF	0x0C	0xD8	0xFF	0x0C	0xDA	0xFF	0x0C
W	0xDC	0x00	0x00	0xDE	0x00	0x00	0xE0	0x00	0x00	0xE2	0x00	0x00	0xE4	0x00	0x00
X	0xE6	0x00	0x00	0xE8	0x00	0x00	0xEA	0x00	0x00	0xEC	0x00	0x00	0xEE	0x00	0x00

6.1.5 Example 5 - Writing pattern data into pattern 1 memory

If pattern from example 3 is written to pattern 1 memory, the following data have to be sent through the SPI.

Table 59. SPI data for writing pattern from example 3 to pattern 1 memory

Byte index(1)	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
Data(1)	**0x02(2)**	**0x00(3)**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0xFF**	**0x04**
Byte index	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Data	0x00	0x00	0x00	0x00	0x00	0x00	0xFF	0x04	0xFF	0x04	0xFF	0x04	0xFF	0x04	0xFF	0x04
Byte index	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Data	0xFF	0x04	0xFF	0x04	0xFF	0x04	0xFF	0x04	0xFF	0x04	0x00	0x00	0x00	0x00	0x00	0x00
Byte index	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
Data	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Byte index	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
Data	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Byte index	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
Data	0x00	0x00	0xFF	0x08	0x00	0x00	0xFF	0x08	0xFF	0x08	0xFF	0x08	0xFF	0x08	0x00	0x00
Byte index	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112
Data	0xFF	0x08	0xFF	0x08	0xFF	0x08	0xFF	0x08	0x00	0x00	0xFF	0x08	0x00	0x00	0xFF	0x08
Byte index	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
Data	0xFF	0x08	0xFF	0x08	0xFF	0x08	0x00	0x00	0xFF	0x08	0xFF	0x08	0xFF	0x08	0xFF	0x08
Byte index	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144
Data	0x00	0x00	0xFF	0x08	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Byte index	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160
Data	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Byte index	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176
Data	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0xFF	0x0C	0x00	0x00
Byte index	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192
Data	0x00	0x00	0x00	0x00	0xFF	0x0C	0xFF	0x0C	0x00	0x00	0x00	0x00	0x00	0x00	0xFF	0x0C

Table 59. SPI data for writing pattern from example 3 to pattern 1 memory (continued)

Byte index(1)	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
Data(1)	**0x02(2)**	**0x00(3)**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0x00**	**0xFF**	**0x04**
Byte index	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208
Data	0xFF	0x0C	0x00	0x00	0xFF	0x0C	0x00	0x00	0xFF	0x0C	0xFF	0x0C	0xFF	0x0C	0xFF	0x0C
Byte index	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224
Data	0xFF	0x0C	0xFF	0x0C	0xFF	0x0C	0xFF	0x0C	0xFF	0x0C	0xFF	0x0C	0xFF	0x0C	0x00	0x00
Byte index	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240
Data	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Byte index	241															
Data	0x00															

1. Byte index and data represent the current data of the pattern from example 3. If the same pattern is written into pattern 2, data are the same but the byte with index 1 has to be changed to 0x04. Data can be written at once as per *Section 4.9.4*.
2. SPI command to write to pattern 1 memory.
3. Address in pattern 1 memory where the data storage begins.

6.2 Operation examples

6.2.1 Example 6 - how to display patterns

Some patterns have already been written into pattern 1 and 2 memories as described in the previous example. EN bit has to be set to 1 and DISP register value has to be set to 01 (for pattern 1) or 10 (for pattern 2). EN bit is located in the software control register whose address is 00h and DISP bits are located in the display control register whose address is 01h. As registers are located next to each other they can be written at once as it is shown in *Table 60* and *Table 61*.

Table 60. SPI data to display pattern 1

Byte index	1	2	3	4
Data	0x00	0x00	0x01	0x01

Table 61. SPI data to display pattern 2

Byte index	1	2	3	4
Data	0x00	0x00	0x01	0x02

Note: Byte 1 represents SPI command to write to the control register memory. Byte 2 is the address where the writing starts. Byte 3 contains data written to address 00h (software control register). Byte 3 contains data written to address 01h (display control register).

6.2.2 Example 7 - how to enable slope operation

When slope operation is being activated, a pattern, containing non-zero slope data, has to be used. Such patterns are in examples 1, 3 and 4. In example 2, pattern has all slope data = 0. Let's suppose that a pattern with non-zero slope data has been already written into pattern 1 memory. First of all, we enable slope operation by setting SLPEN bit to 1.

Table 62. SPI data to enable slope operation

Byte index	1	2	3
Data	0x00	0x20	0x08

Byte 1 represents SPI command to write to the control register memory.

Byte 2 is the address where the writing starts.

Byte 3 contains data written to address 20h (display visual control register).

As per example 6, we display pattern 1 by writing data to *Table 63* or pattern 2 by writing data to *Table 64* .

Table 63. SPI data to display pattern 1

Byte index	1	2	3	4
Data	0x00	0x00	0x01	0x01

Table 64. SPI data to display pattern 2

Byte index	1	2	3	4
Data	0x00	0x00	0x01	0x02

6.2.3 Example 8 - how to enable PWM operation

Pattern has already been loaded into pattern 1 memory. In this example, we display pattern 1 with 50% of brightness which is achieved by enabling PWM.

First of all, we enable PWM operation and set PWM register to 128 by using data in *Table 65*.

Table 65. SPI data to enable PWM operation (PWM control register = 128)

Byte index	1	2	3	4
Data	0x00	0x20	0x02	0x80

Byte 1 represents SPI command to write to the control register memory.

Byte 2 is the address where the writing starts.

Byte 3 contains data written to address 20h (display visual control register).

Byte 4 contains data written to address 21h (PWM control register).

As per example 6, we display pattern 1 by writing data to *Table 66*.

Table 66. SPI data to display in pattern 1

Byte index	1	2	3	4
Data	0x00	0x00	0x01	0x01

6.2.4 Example 8 - scroll operation

In this example we scroll with 2 blank rows and a speed set to 5. Pattern 2 replaces pattern 1. Both patterns, 1 and 2, have already been loaded into pattern memory according to example 5. Scroll operation should start with pattern 1, so we display pattern 1 first by writing data to *Table 67*.

Table 67. SPI data to display in pattern 1(example 5)

Byte index	1	2	3	4
Data	0x00	0x00	0x01	0x01

Scroll parameters have to be set by writing data:

Table 68. SPI data for scroll setup

Byte index	1	2	3	4
Data	0x00	0x30	0x13	0x40

Byte 1 represents SPI command to write to the control register memory.

Byte 2 is the address where writing starts.

Byte 3 contains data written to address 30h (scroll control 1 register). This sets the scroll speed to 5 and direction.

Byte 4 contains data that are written to address 31h (scroll control 2 register). This sets the number of blank rows to 2.

Scroll and insertion of blank rows/columns have to be enabled by writing to the display visual control register, in the following table:

Table 69. SPI data to enable scroll operation with blank rows/columns

Byte index	1	2	3
Data	0x00	0x20	0x24

Byte 1 represents SPI command to write to the control register memory.

Byte 2 is the address where the writing starts.

Byte 3 contains data written to address 20h (display control register). Value 24h enables insertion of blank columns/rows and enables the scroll.

Scroll operation starts by writing to the display control register. This changes DISP bit value from 01 to 10 and so the scroll operation begins. Pattern 1 is replaced by pattern 2.

Table 70. SPI data to start scroll operation

Byte index	1	2	3
Data	0x00	0x01	0x02

Byte 1 represents SPI command to write to the control register memory.

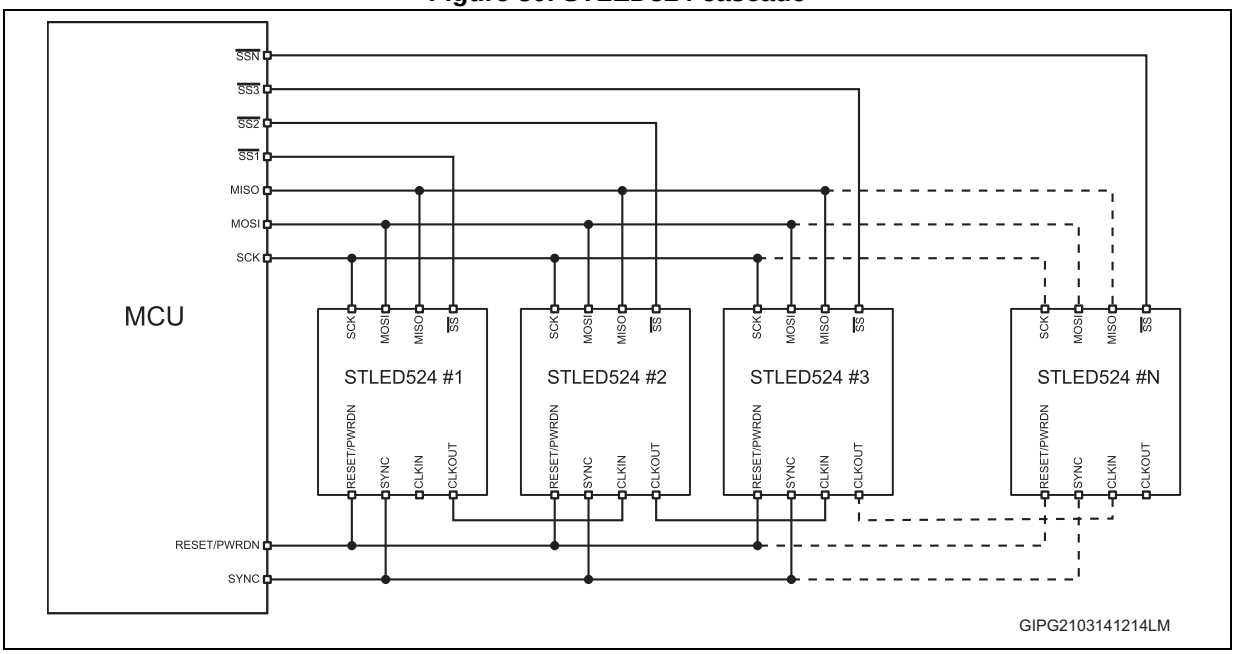
Byte 2 is the address where the writing starts.

Byte 3 contains data written to address 01h (display control register).

6.3 Multiple devices in cascade

The STLED524 multiple devices can be linked in cascade according to *Figure 30*.

Figure 30. STLED524 cascade



- Each device in cascade needs a controlled SS input separately.
- RESET/PWRDN, SYNC, SCK, MISO and MOSI pins are connected in parallel.
- CLKOUT of n^{th} device is connected to CLKIN of the $(n+1)^{th}$ device.
- CLKIN of the 1^{st} device does not have to be connected, if internal clock of the 1^{st} device is used to provide clock for the whole cascade.
- Another possibility for CLOCK signal is to connect all CLKIN pins to an external clock.

6.3.1 Register setup for the STLED524 cascade

Table 71. Cascade register setup

Position	CLKIN	CLKOUT	SYNCEN	SYNCSEL
1	0	1	1	X
2 to (n-1)	1	1	1	X
n	1	0	1	X

Position means position of the device in cascade:

CLKIN bit of the first device is set to 0, because the first device uses its internal clock.

CLKOUT bit of the last device is set to 0, because there is no other device connected.

SYNCEN bit of all devices has to be set to 1.

SYNCSEL bit can be either 0 or 1, but the value has to be the same as all devices in cascade.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 31. CSP 56 bumps (3.4x3.0 mm) drawings

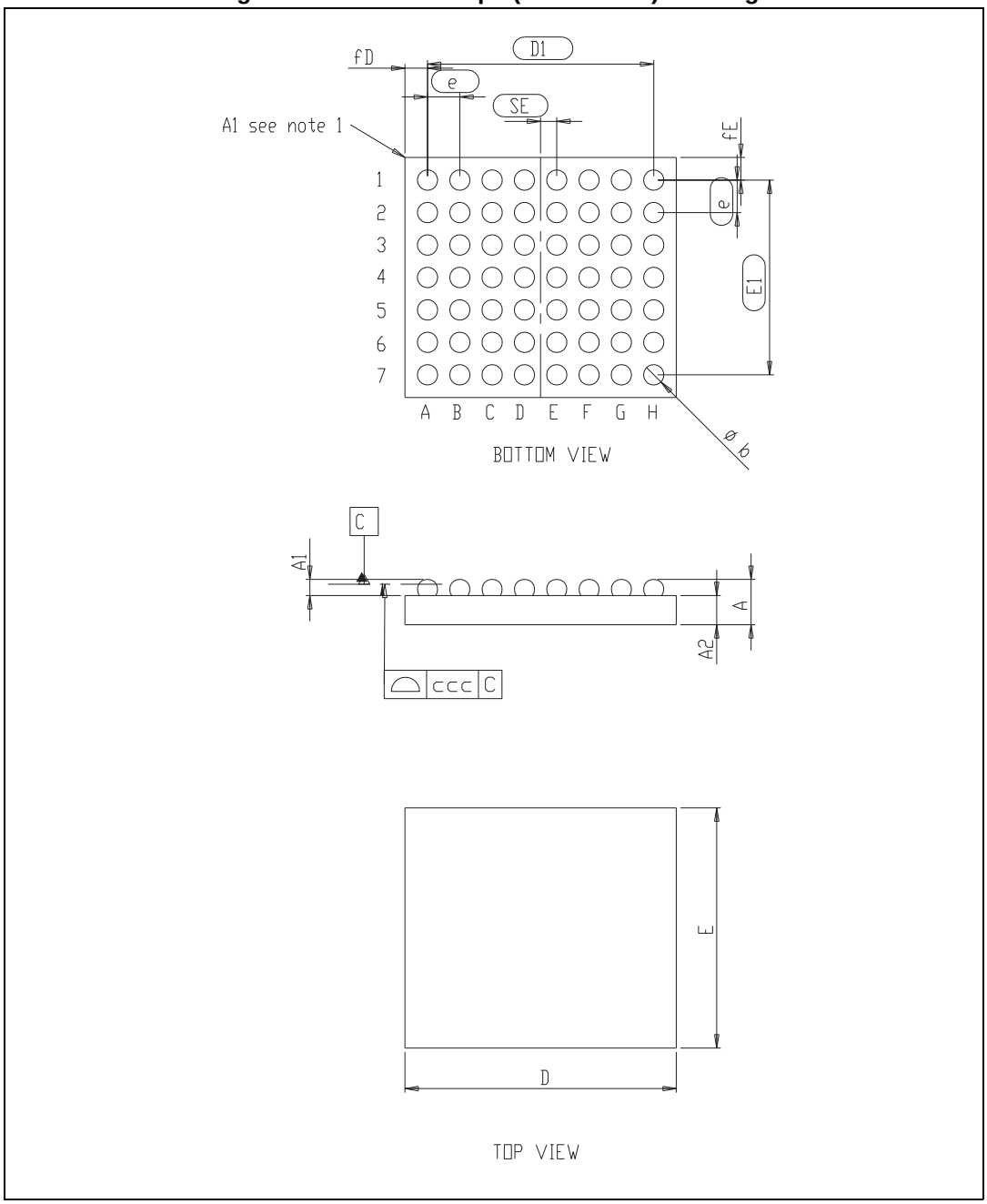


Table 72. CSP 56 bumps (3.4x3.0 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.17	0.20	0.23
A2	0.33	0.35	0.37
b	0.23	0.25	0.29
D	3.34	3.37	3.40
D1		2.8	
E	2.94	2.97	3.0
E1		2.4	
e		0.40	
SE		0.20	
fD		0.285	
fE		0.285	
ccc		0.075	

8 Revision history

Table 73. Document revision history

Date	Revision	Changes
14-Apr-2014	1	First release.

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