

P-channel -30 V, 12 mΩ typ., -9 A STripFET™ H6 Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - production data

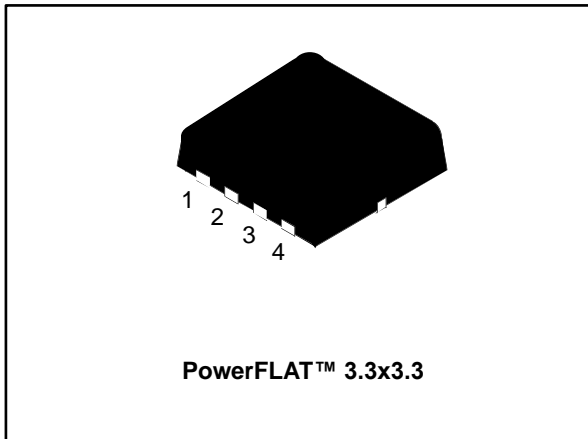
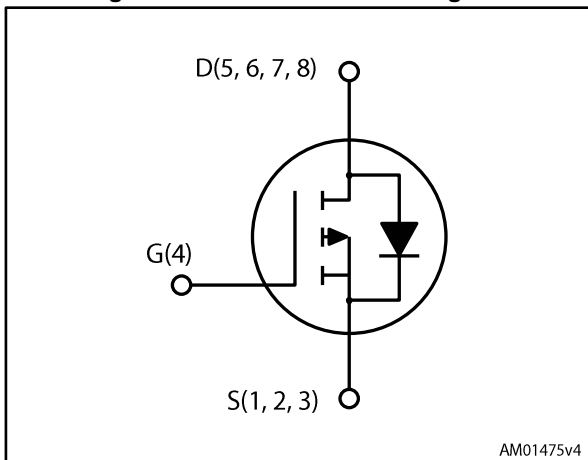


Figure 1: Internal schematic diagram



Features

| Order code | V _{DS} | R _{DS(on)} max | I _D |
|------------|-----------------|-------------------------|----------------|
| STL9P3LLH6 | -30 V | 15 mΩ | -9 A |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|------------|---------|--------------------|---------------|
| STL9P3LLH6 | 9P3L | PowerFLAT™ 3.3x3.3 | Tape and reel |

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|-------------|--------------------|
| V_{DS} | Drain-source voltage | -30 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| I_D | Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$ | -9 | A |
| I_D | Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$ | -5.9 | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | -36 | A |
| P_{TOT} | Total dissipation at $T_{pcb}=25\text{ }^{\circ}\text{C}$ | 3 | W |
| T_{stg} | Storage temperature range | - 55 to 150 | $^{\circ}\text{C}$ |
| T_j | Operating junction temperature range | | |

Notes:

⁽¹⁾Pulse width limited by safe operating area.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|----------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 2.5 | $^{\circ}\text{C/W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 42 | $^{\circ}\text{C/W}$ |

Notes:

⁽¹⁾When mounted on FR-4 board of 1inch², 2oz Cu t<10sec

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0, I_D = -1\text{ mA}$ | -30 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0, V_{DS} = -30\text{ V}$ | | | -1 | μA |
| | | $V_{GS} = 0, V_{DS} = -30\text{ V}, T_C = 125\text{ °C}$ ⁽¹⁾ | | | -10 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$ | -1 | | | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}$ | | 12 | 15 | m Ω |
| | | $V_{GS} = -4.5\text{ V}, I_D = -4.5\text{ A}$ | | 18 | 22.5 | m Ω |

Notes:

⁽¹⁾ Defined by design, not subject to production test.

Table 5: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = -25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$ | - | 2615 | - | pF |
| C_{oss} | Output capacitance | | - | 340 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 235 | - | pF |
| Q_g | Total gate charge | $V_{DD} = -15\text{ V}, I_D = -6\text{ A}, V_{GS} = -4.5\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load") | - | 24 | - | nC |
| Q_{gs} | Gate-source charge | | - | 9 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 8 | - | nC |

Table 6: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = -15\text{ V}, I_D = -4.5\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = -10\text{ V}$ | - | 13.2 | - | ns |
| t_r | Rise time | | - | 93 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 50 | - | ns |
| t_f | Fall time | | - | 18 | - | ns |

Table 7: Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|--------------------------|--|------|------|------|------|
| $V_{SD}^{(1)}$ | Forward on voltage | $I_{SD} = -9 \text{ A}$, $V_{GS} = 0$ | - | | -1.1 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = -9 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = -24 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ | - | 20 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 16 | | nC |
| I_{RRM} | Reverse recovery current | | - | -1.6 | | A |

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curves)



Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

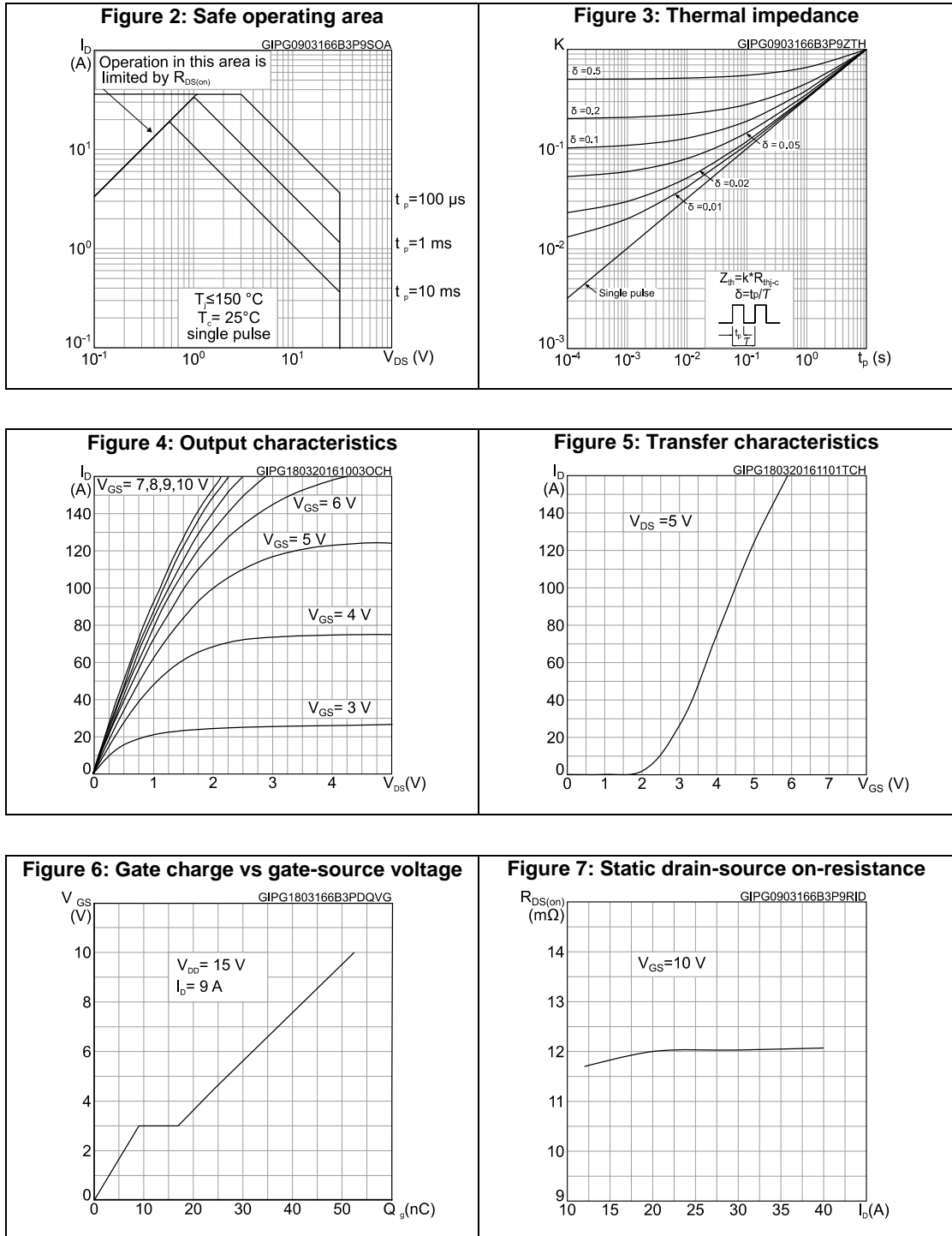


Figure 8: Capacitance variations

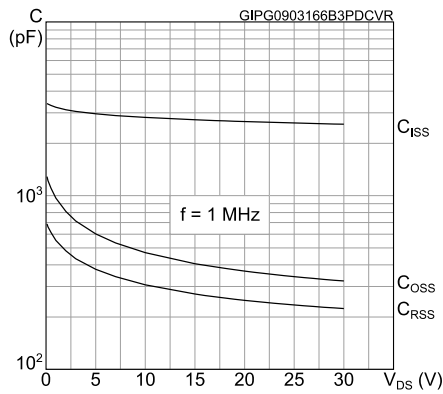


Figure 9: Normalized gate threshold voltage vs temperature

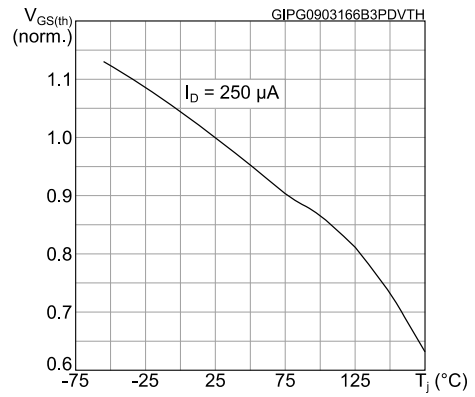


Figure 10: Normalized on-resistance vs temperature

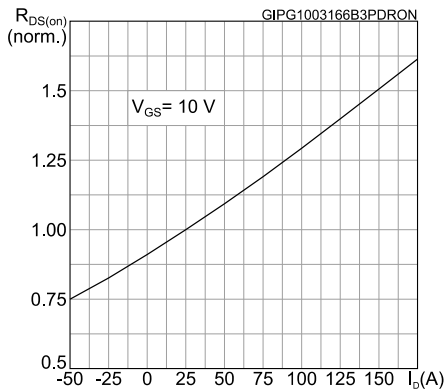


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

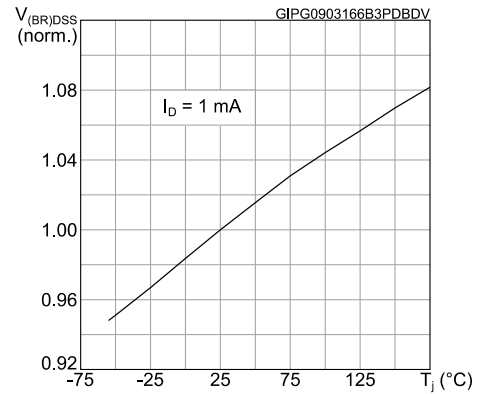
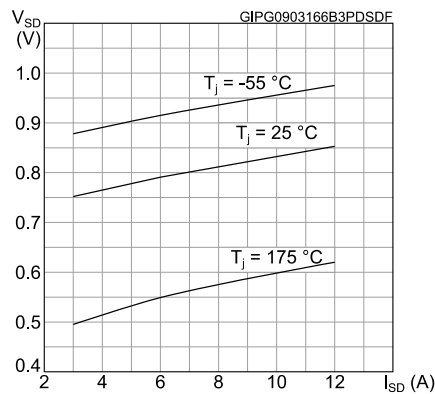


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

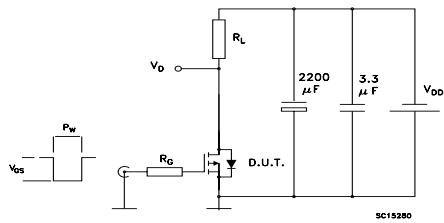


Figure 14: Gate charge test circuit

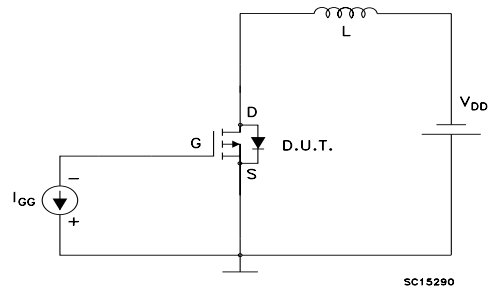
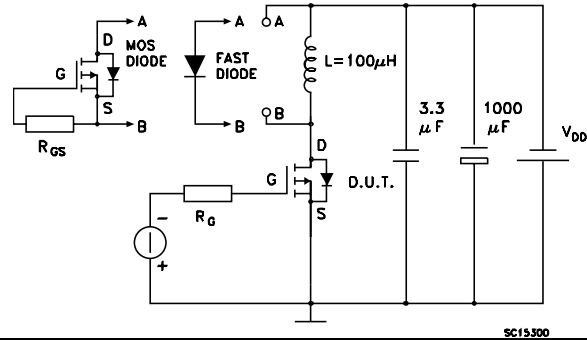


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PoweFLAT 3.3x3.3 package information

Figure 16: PowerFLAT™ 3.3x3.3 package outline

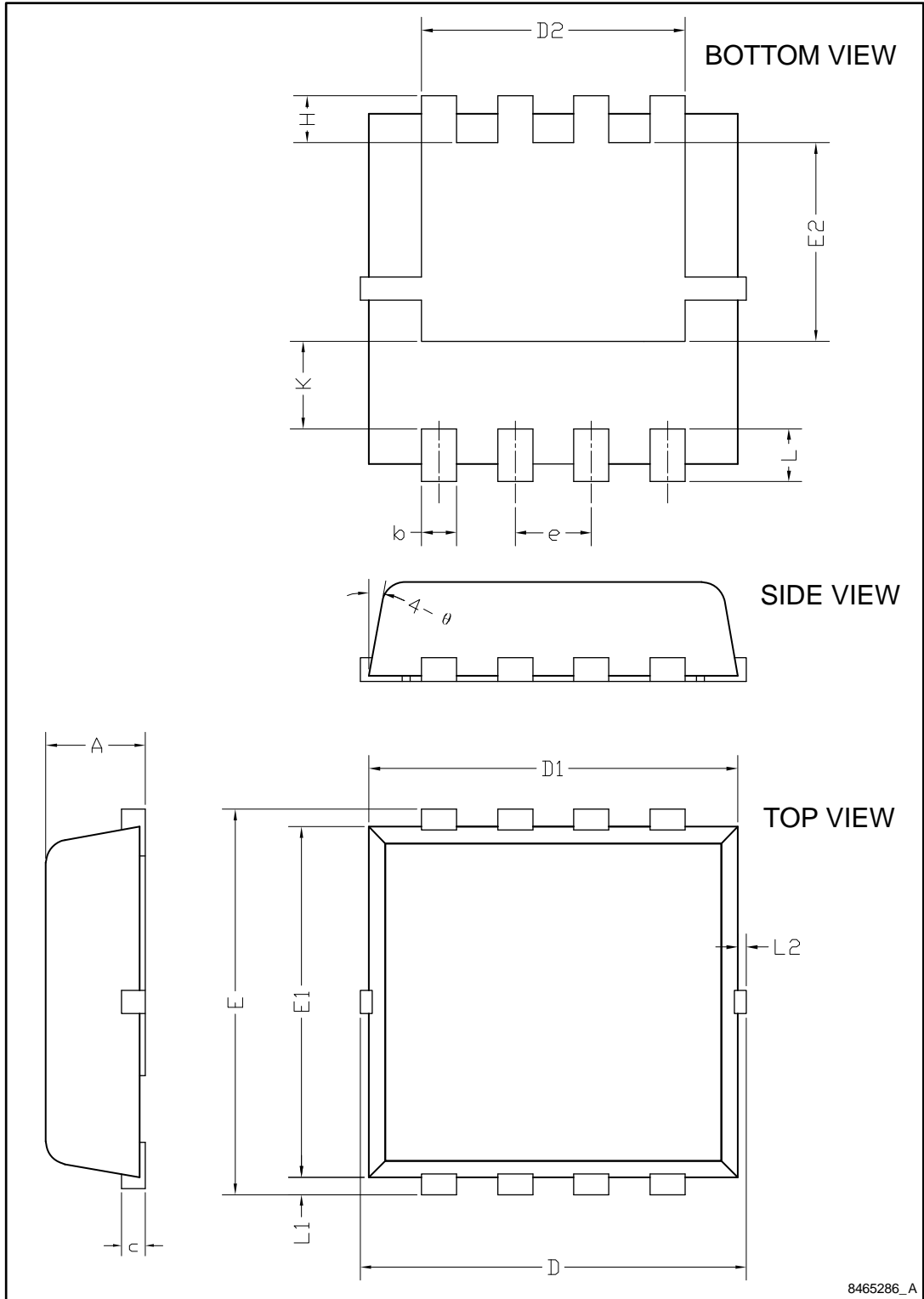
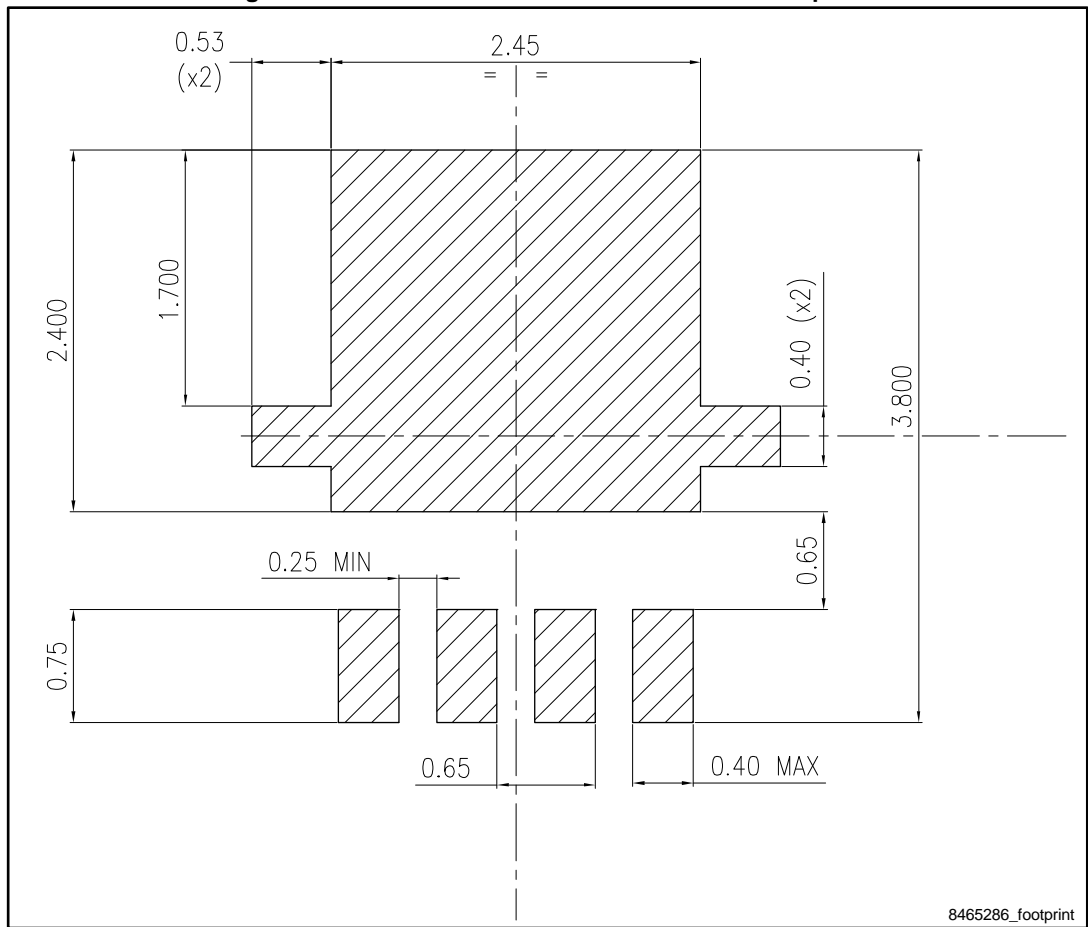


Table 8: PowerFLAT™ 3.3x3.3 package mechanical data

| Dim. | mm | | |
|----------|------|------|------|
| | Min. | Typ. | Max. |
| A | 0.70 | 0.80 | 0.90 |
| b | 0.25 | 0.30 | 0.39 |
| c | 0.14 | 0.15 | 0.20 |
| D | 3.10 | 3.30 | 3.50 |
| D1 | 3.05 | 3.15 | 3.25 |
| D2 | 2.15 | 2.25 | 2.35 |
| e | 0.55 | 0.65 | 0.75 |
| E | 3.10 | 3.30 | 3.50 |
| E1 | 2.90 | 3.00 | 3.10 |
| E2 | 1.60 | 1.70 | 1.80 |
| H | 0.25 | 0.40 | 0.55 |
| K | 0.65 | 0.75 | 0.85 |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.05 | 0.15 | 0.25 |
| L2 | | | 0.15 |
| θ | 8° | 10° | 12° |

Figure 17: PowerFLAT™ 3.3x3.3 recommended footprint



5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 23-Jan-2014 | 1 | First release. |
| 07-Mar-2016 | 2 | Modified: title and $R_{DS(on)}$ max value Modified: <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source drain diode"</i> Minor text changes. |

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