

N-channel 100 V, 0.007 Ω typ., 70 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

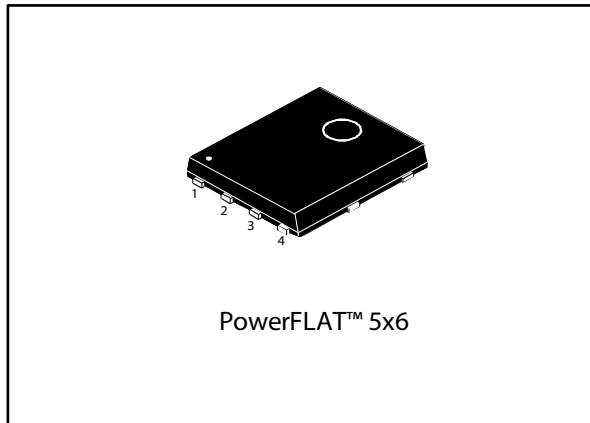
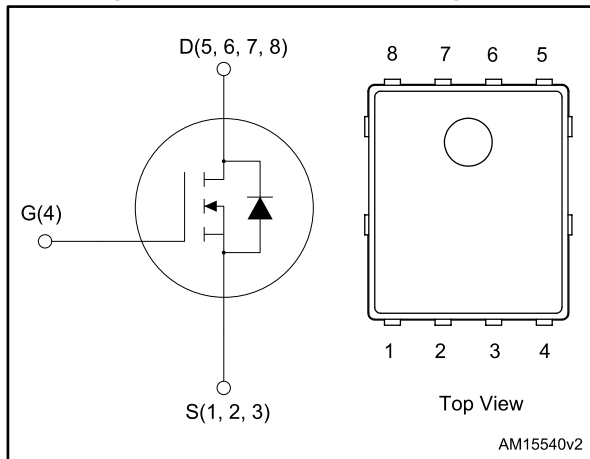


Figure 1: Internal schematic diagram



Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D | P _{TOT} |
|------------|-----------------|--------------------------|----------------|------------------|
| STL90N10F7 | 100 V | 0.008 Ω | 70 A | 100 W |

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|------------|---------|----------------|---------------|
| STL90N10F7 | 90N10F7 | PowerFLAT™ 5x6 | Tape and reel |

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-------------------|---|-------------|------------------|
| V_{DS} | Drain-source voltage | 100 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 70 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 50 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 16 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$ | 11 | A |
| $I_{DM}^{(1)(3)}$ | Drain current (pulsed) | 280 | A |
| $I_{DM}^{(2)(3)}$ | Drain current (pulsed) | 64 | A |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 100 | W |
| $P_{TOT}^{(2)}$ | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 5 | W |
| $E_{AS}^{(4)}$ | Single pulse avalanche energy | 300 | mJ |
| T_{stg} | Storage temperature | - 55 to 175 | $^\circ\text{C}$ |
| T_j | Maximum junction temperature | 175 | $^\circ\text{C}$ |

Notes:

- (1) This value is rated according to R_{thj-c} .
- (2) This value is rated according to $R_{thj-pcb}$.
- (3) Pulse width is limited by safe operating area.
- (4) Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 10\text{ A}$, $V_{DD} = 50\text{ V}$.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|--------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 1.5 | $^\circ\text{C/W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 31 | |

Notes:

- (1) When mounted on 1 inch², 2 Oz. Cu FR-4 board

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|-------|-------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | 100 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $T_C = 125\text{ °C}$ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$ | | | 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2.5 | 3.5 | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$ | | 0.007 | 0.008 | Ω |

Table 5: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 3100 | 4030 | pF |
| C_{oss} | Output capacitance | | - | 700 | 910 | pF |
| C_{rss} | Reverse transfer capacitance | | - | 45 | 58 | pF |
| Q_g | Total gate charge | $V_{DD} = 50\text{ V}$, $I_D = 16\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Gate charge test circuit") | - | 45 | 60 | nC |
| Q_{gs} | Gate-source charge | | - | 18 | | nC |
| Q_{gd} | Gate-drain charge | | - | 13 | | nC |

Table 6: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 50\text{ V}$, $I_D = 8\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load" and Figure 18: "Switching time waveform") | - | 19 | - | ns |
| t_r | Rise time | | - | 32 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 36 | - | ns |
| t_f | Fall time | | - | 13 | - | ns |

Table 7: Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|------|
| I_{SD} | Source-drain current | | - | | 16 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 64 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0 \text{ V}$, $I_{SD} = 16 \text{ A}$ | - | | 1.1 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 16 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 80 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 15: "Test circuit for inductive load switching and diode recovery times")</i>) | - | 70 | 90 | ns |
| Q_{rr} | Reverse recovery charge | | - | 125 | | nC |
| I_{RRM} | Reverse recovery current | | - | 3.6 | | A |

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

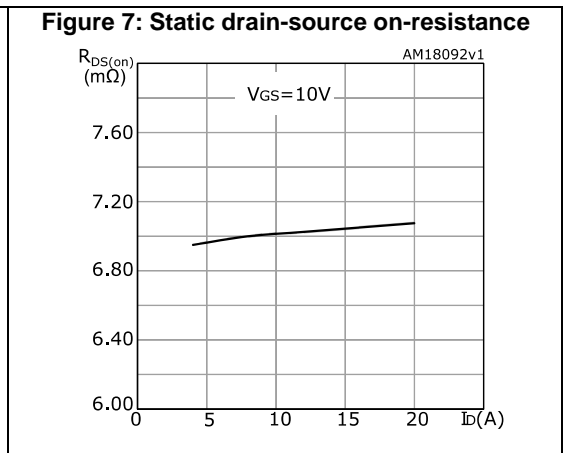
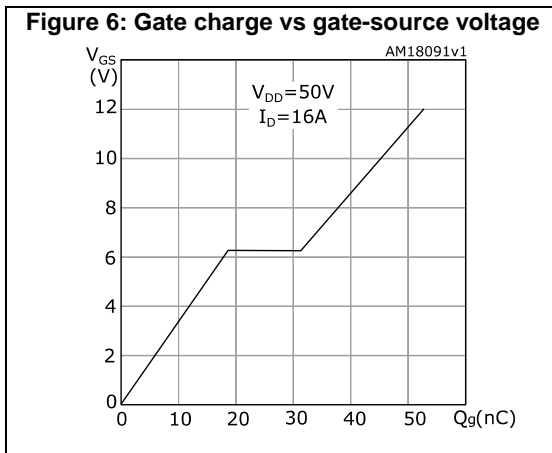
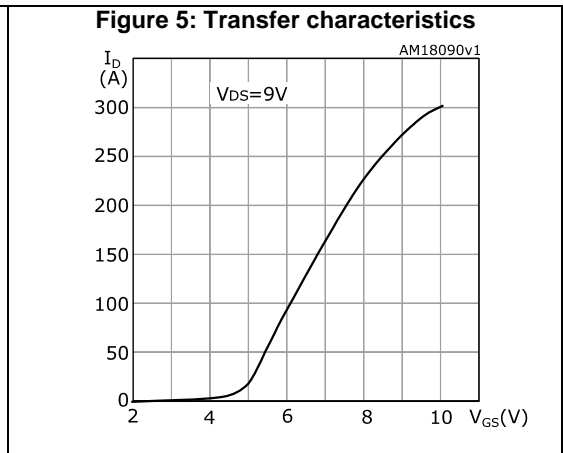
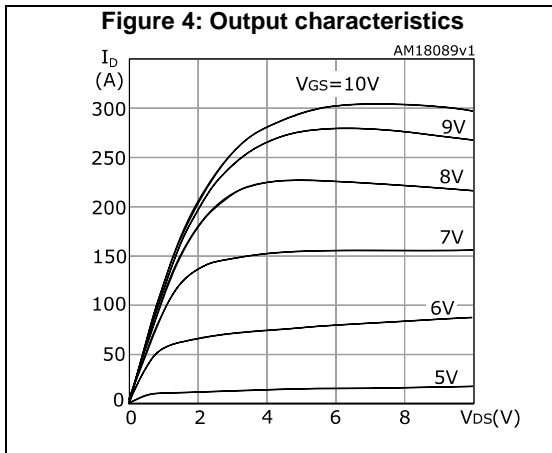
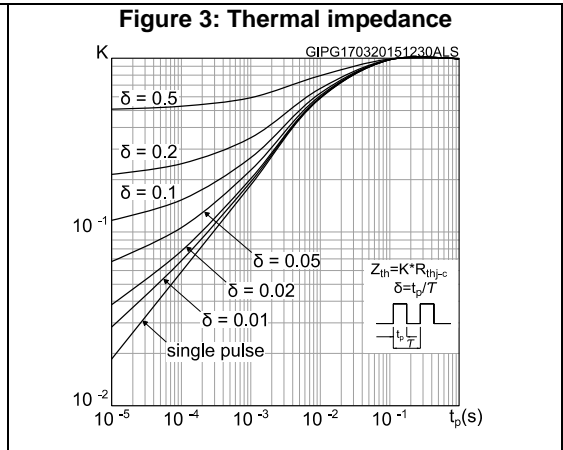
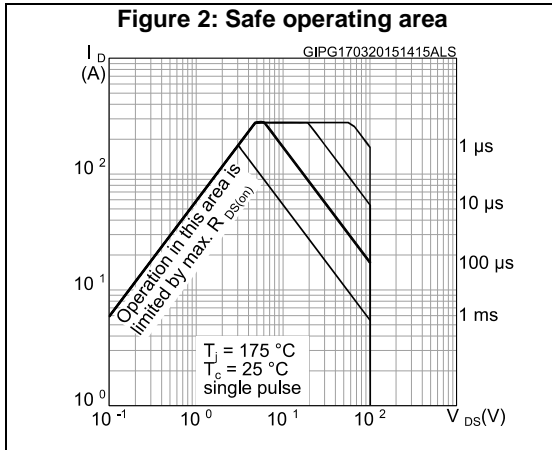


Figure 8: Capacitance variations

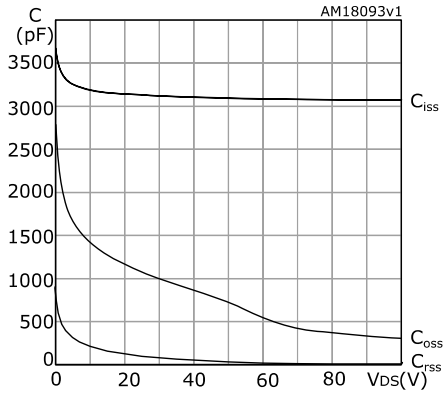


Figure 9: Normalized gate threshold voltage vs temperature

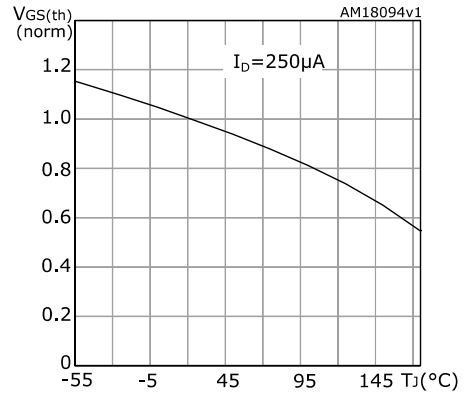


Figure 10: Normalized on-resistance vs temperature

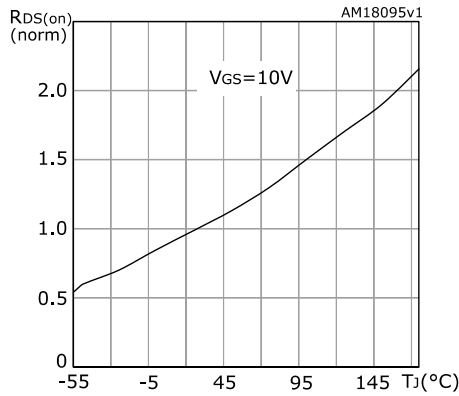


Figure 11: Normalized V(BR)DSS vs temperature

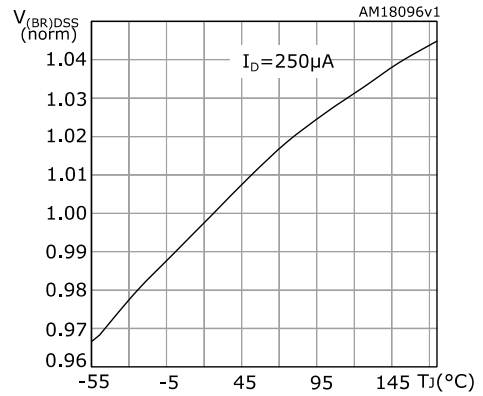
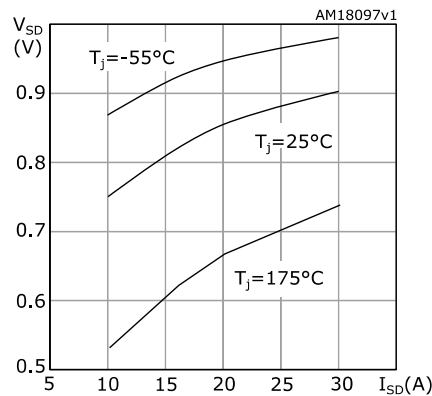
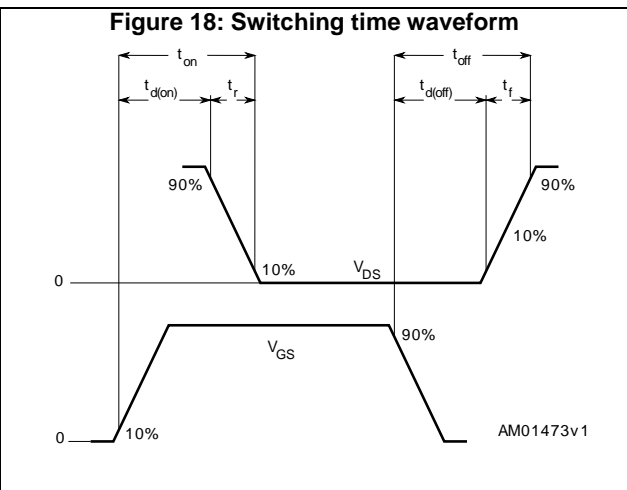
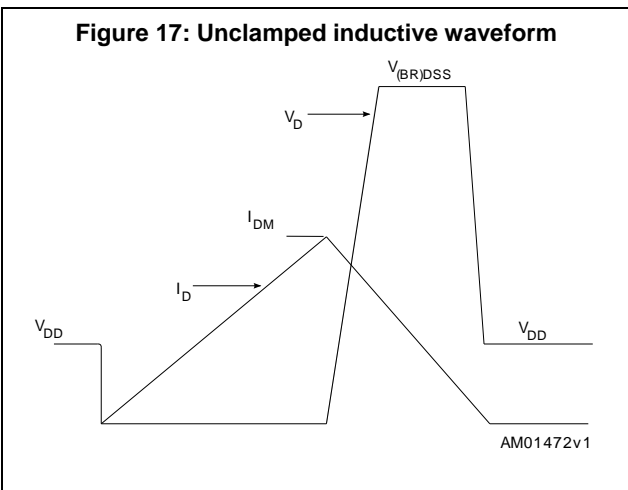
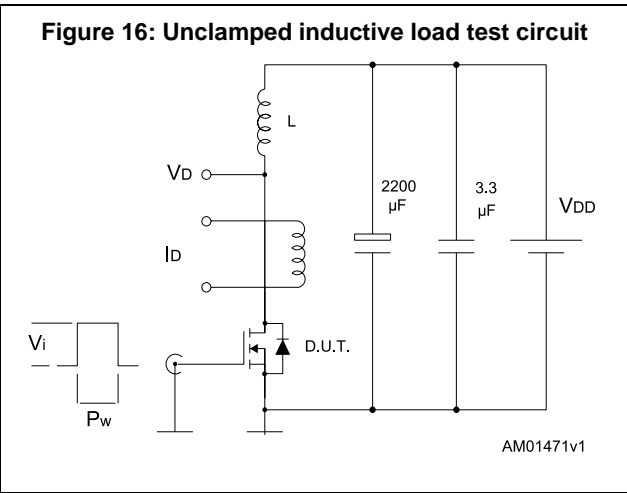
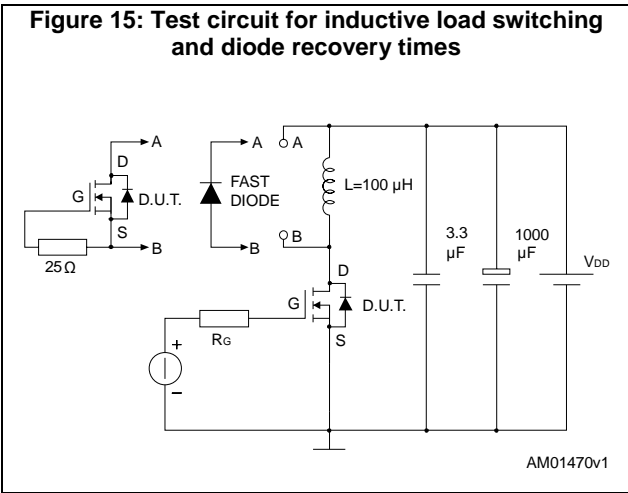
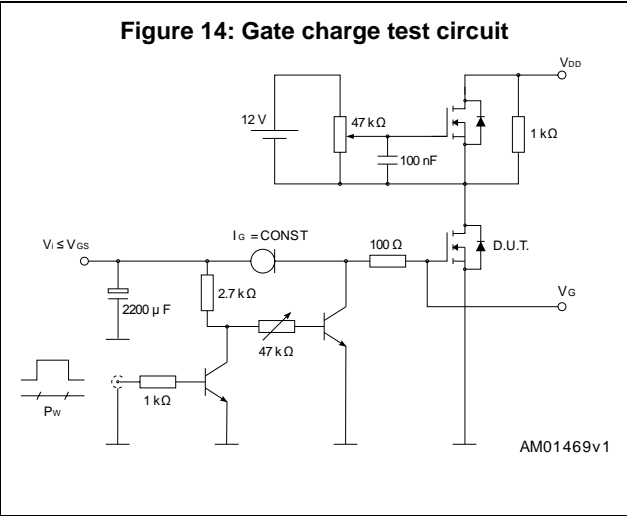
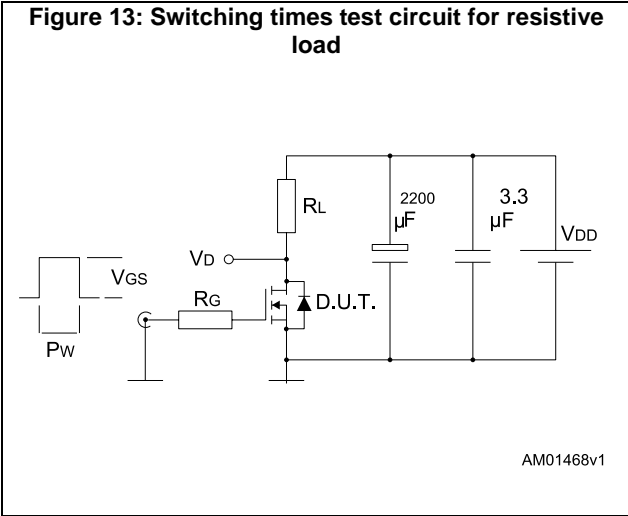


Figure 12: Source-drain diode forward characteristics



3 Test circuits



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT[™] 5x6 type R package information

Figure 19: PowerFLAT[™] 5x6 type R package outline

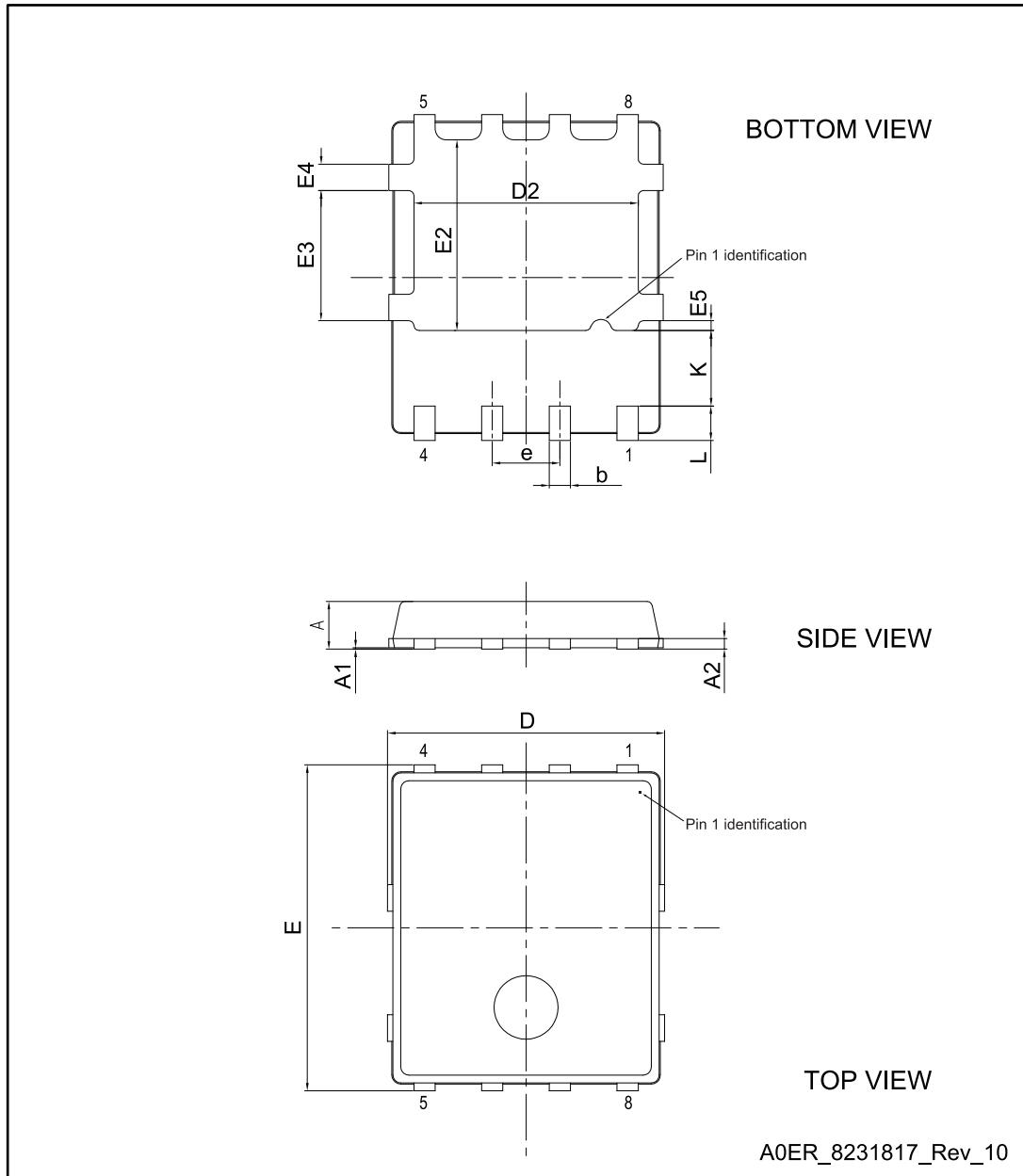
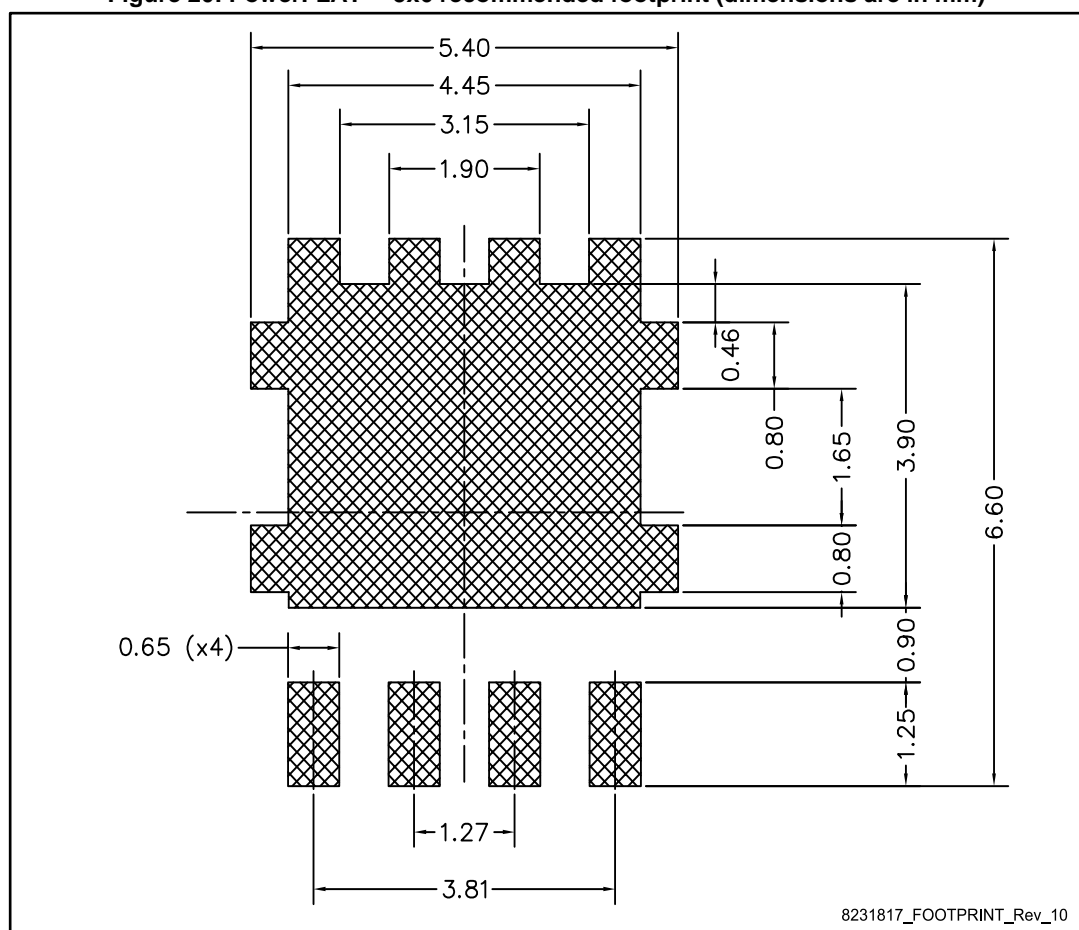


Table 8: PowerFLAT™ 5x6 type R mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | 5.00 | 5.20 | 5.40 |
| E | 5.95 | 6.15 | 6.35 |
| D2 | 4.11 | | 4.31 |
| e | | 1.27 | |
| L | 0.60 | | 0.80 |
| K | 1.275 | | 1.575 |
| E3 | 2.35 | | 2.55 |
| E4 | 0.40 | | 0.60 |
| E5 | 0.08 | | 0.28 |

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

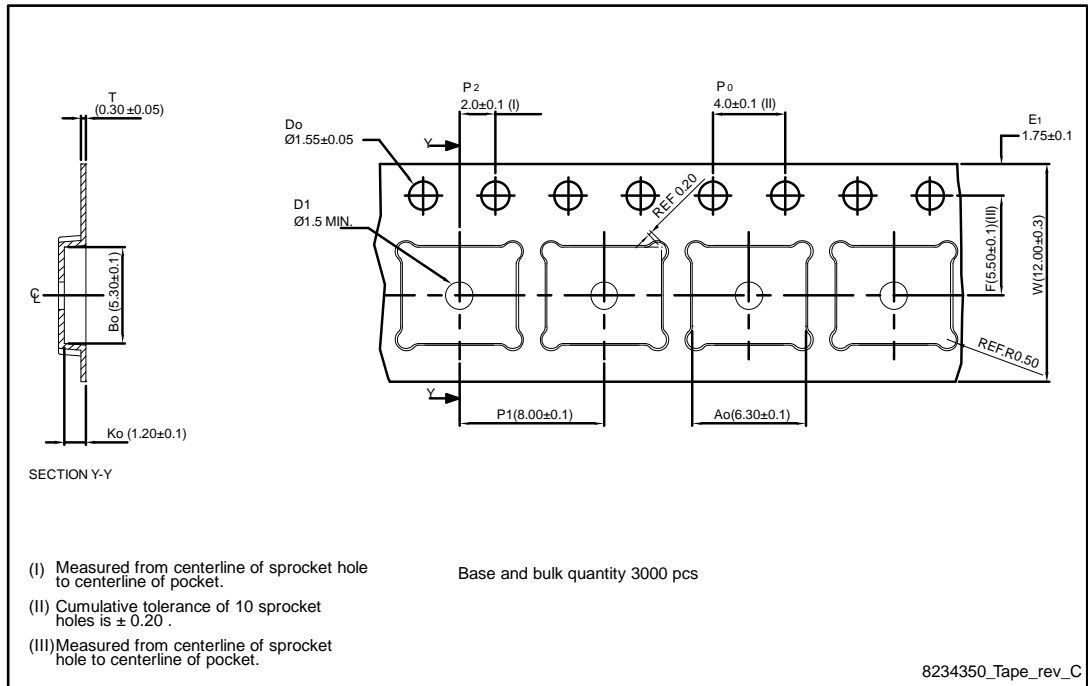


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

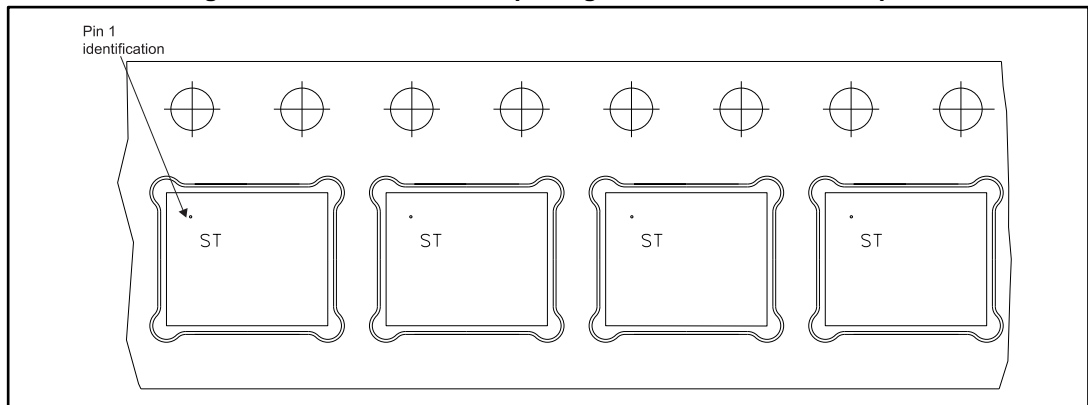
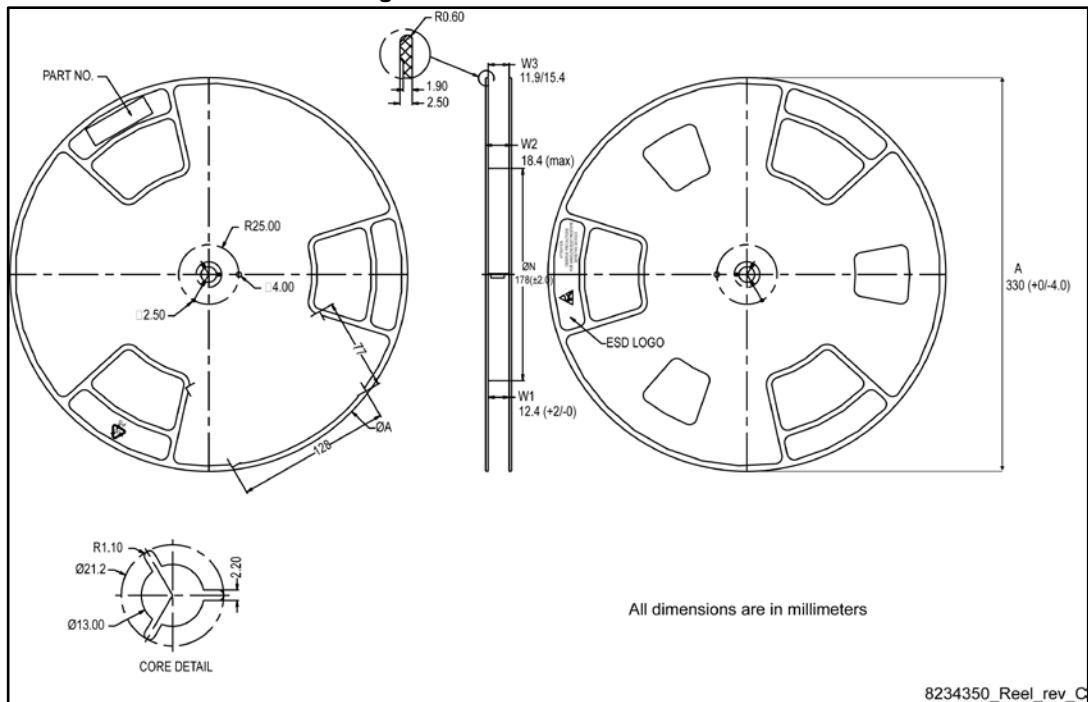


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 16-Apr-2013 | 1 | First release. |
| 06-Mar-2014 | 2 | <ul style="list-style-type: none"> – Modified: $R_{DS(on)}$ value in cover page – Modified: $V_{GS(th)}$ values in Table 4 – Modified: $R_{DS(on)}$ typ. and max values in Table 4 – Modified: typical values in Table 5, 6 and 7 – Updated: Section 4: Package mechanical data – Added: Section 2.1: Electrical characteristics (curves) – Updated: Section 4: Package mechanical data – Document status promoted from preliminary data to production data |
| 16-Dec-2014 | 3 | <ul style="list-style-type: none"> – Updated title, features and description in cover page. – Updated $R_{DS(on)}$ values and Figure 7: Static drain-source onresistance. |
| 17-Mar-2015 | 4 | <ul style="list-style-type: none"> –Text edits throughout document –Updated cover page title description –Updated cover page features table –In table 2. Absolute maximum ratings, added "E_{AS}" information and footnote 4 –In table 3. Thermal data, added footnote 1 –Renamed table 4. Static (was On/off states) –Updated table 5. Dynamic –Updated table 7. Source drain diode –In Section 2.1 Electrical characteristics (curves), updated figures 2, 3, 10 and 11 –Updated and renamed Section 4 Package information |

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