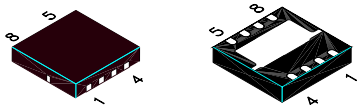
STL8NH3LL

N-channel 30V - 0.012Ω - 8A - PowerFLAT™
Ultra low gate charge STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STL8NH3LL	30V	<0.015Ω	8A (1)

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Very low gate charge
- Low threshold device
- In compliance with the 2002/95/EC Europen directive



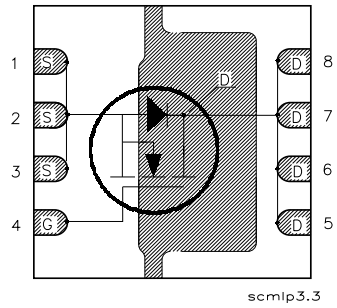
PowerFLAT™(3.3x3.3)

(Chip Scale Package)

Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique “STripFET™” technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

Internal schematic diagram



TOP VIEW

Applications

- Switching application

Order codes

Sales Type	Marking	Package	Packaging
STL8NH3LL	8NH3L	PowerFLAT™ (3.3 x 3.3)	Tape & reel

Contents:

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-Source Voltage	± 18	V
I_D (1)	Drain Current (continuous) at T_C = 25°C	8	A
I_D (1)	Drain Current (continuous) at T_C=100°C	5	A
I_{DM} (2)	Drain Current (pulsed)	32	A
P_{TOT} (3)	Total Dissipation at T_C = 25°C	50	W
P_{TOT} (1)	Total Dissipation at T_C = 25°C	2	W
	Derating Factor	0.4	W/°C
T_J T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

1. The value is rated according Rthj-pcb
2. Pulse width limited by safe operating area.
3. The vaule is rated according Rthj-c

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (Drain)	2.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	42.8	°C/W
$R_{thj\text{-}pcb}$ (2)	Thermal resistance junction-pcb	63.5	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10sec
2. Steady state

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250µA, V_{GS}= 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0) V_{DS} = Max Rating, V_{DS} = MaxRating @125°C				1 10	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±18V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 250µA	1		2.5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10V, I_D= 4A V_{GS}= 4.5V, I_D= 4A		0.012 0.0135	0.015 0.017	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} =15V, I_D = 4A		30		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		965 285 38		pF pF pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=15V, I_D = 8A V_{GS} =4.5V (see Figure 7)		9 3.7 3	12	nC nC nC
R_G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain	0.5	1.5	2.5	Ω

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD}=15V, I_D= 4A, R_G=4.7Ω, V_{GS}=4.5V (see Figure 13)		15 32 18 8.5		ns ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test Condictions	Min	Typ.	Max	Unit
I_{SD}	Source-drain Current				8	A
I_{SDM}(1)	Source-drain Current (pulsed)				32	A
V_{SD}(2)	Forward on Voltage	I_{SD}=8A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=8A, di/dt = 100A/µs, V_{DD}=20V, Tj=150°C (see Figure 15)		24 17.4 1.45		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

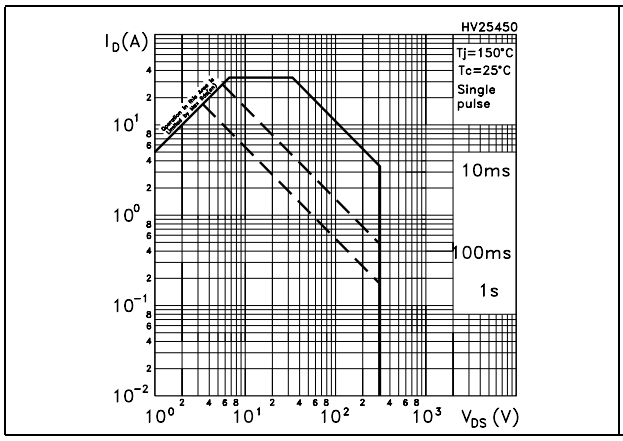


Figure 2. Thermal impedance

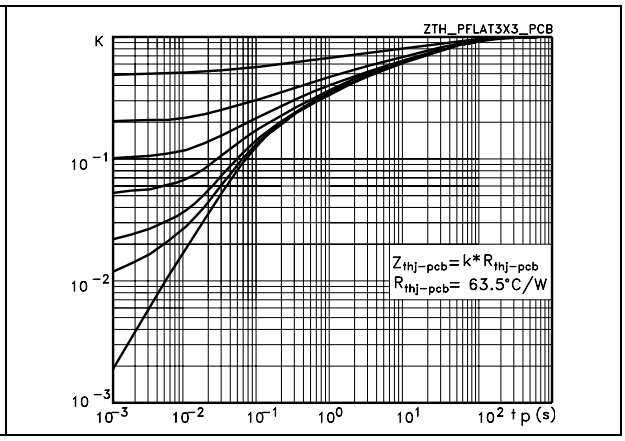


Figure 3. Output characterisics

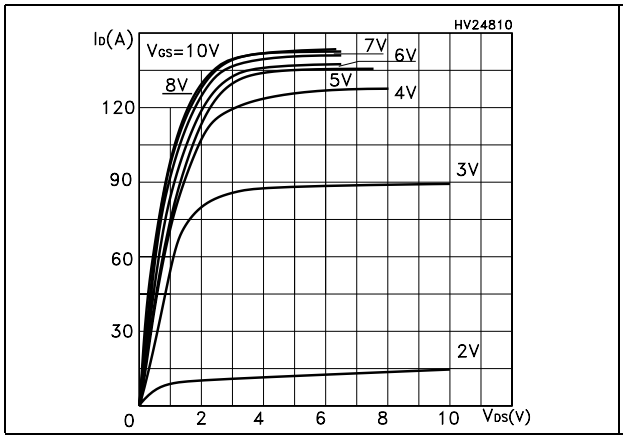


Figure 4. Transfer characteristics

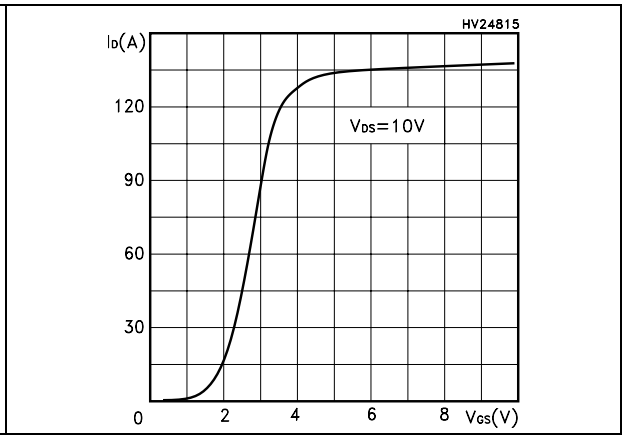


Figure 5. Transconductance

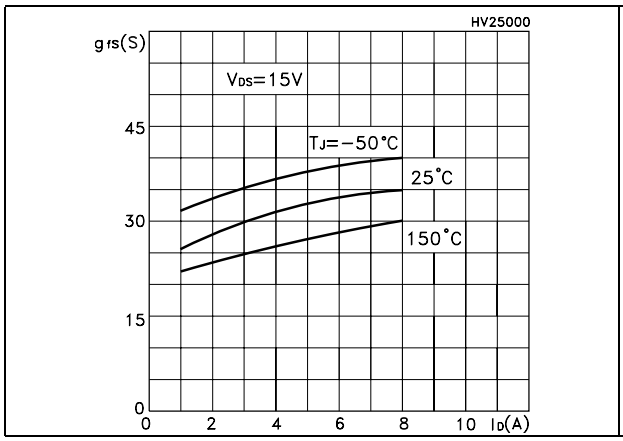


Figure 6. Static drain-source on resistance

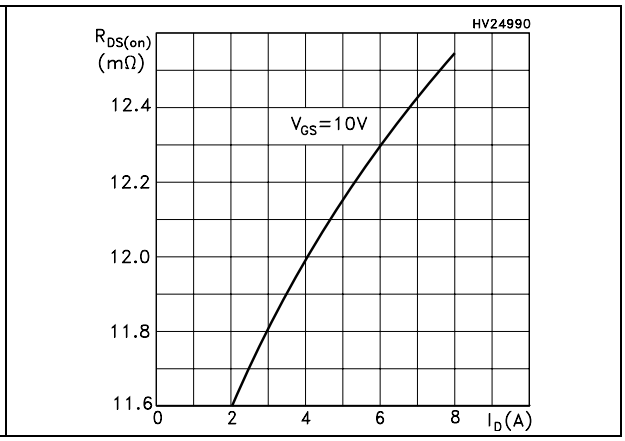


Figure 7. Gate charge vs gate-source voltage

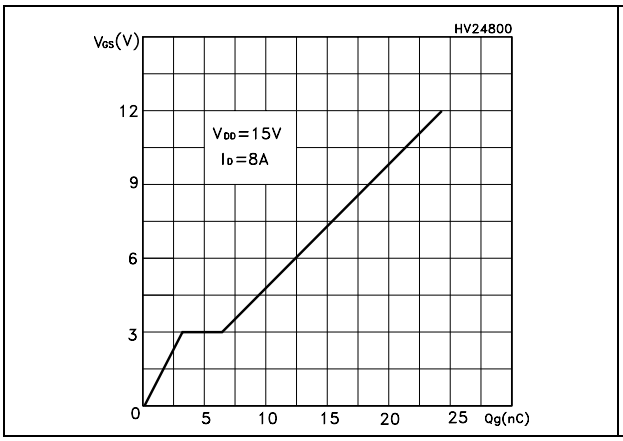


Figure 8. Capacitance variations

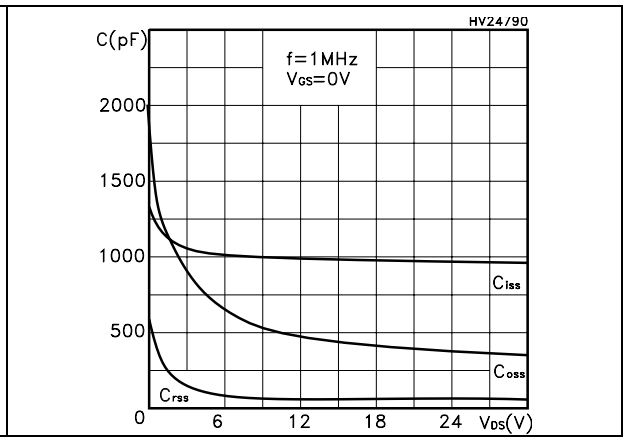


Figure 9. Normalized gate threshold voltage vs temperature

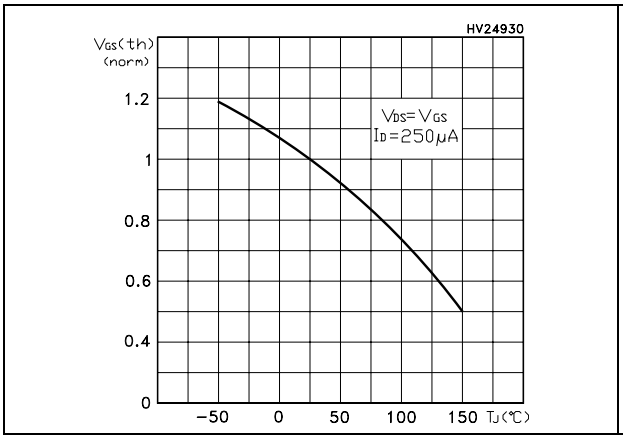


Figure 10. Normalized on resistance vs temperature

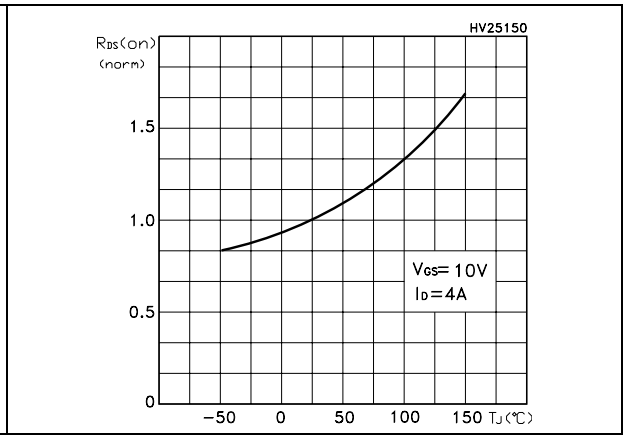


Figure 11. Source-drain diode forward characteristics

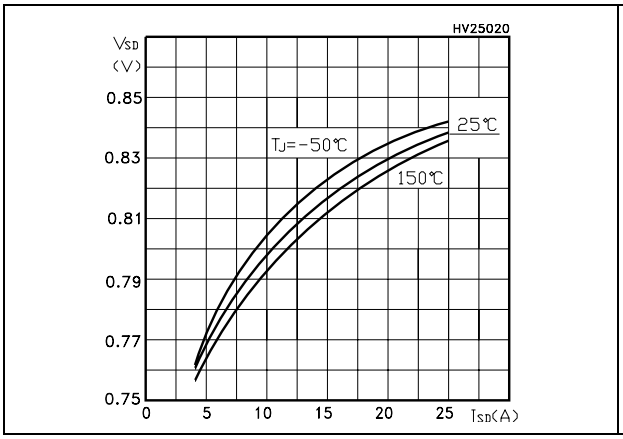
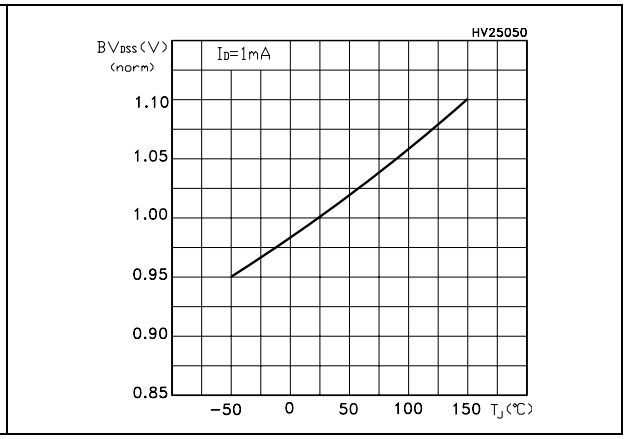


Figure 12. Normalized B_{VDSS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

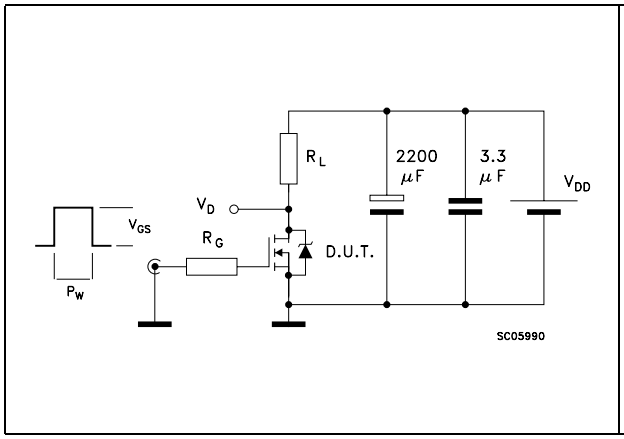


Figure 14. Gate charge test circuit

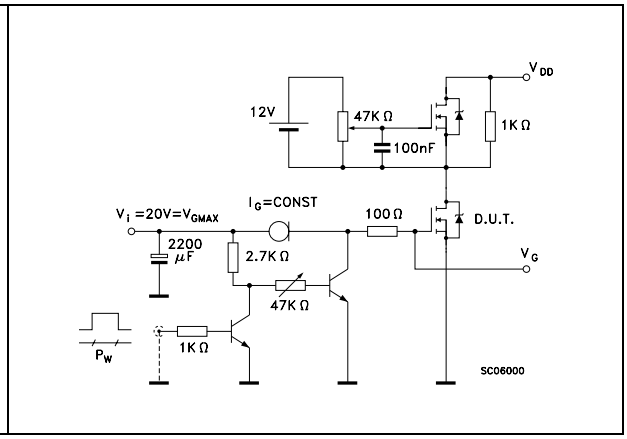


Figure 15. Test circuit for inductive load switching and diode recovery times

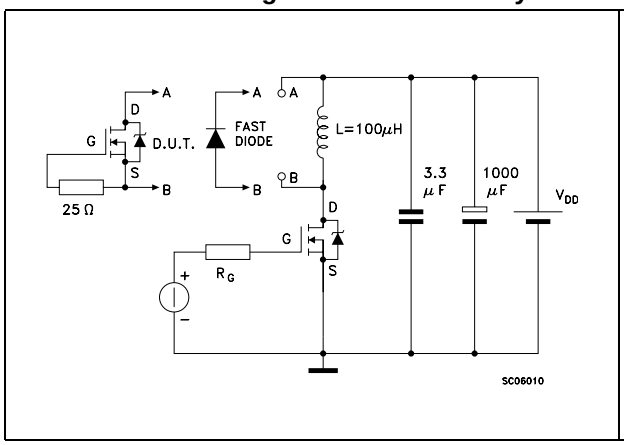


Figure 16. Unclamped inductive load test circuit

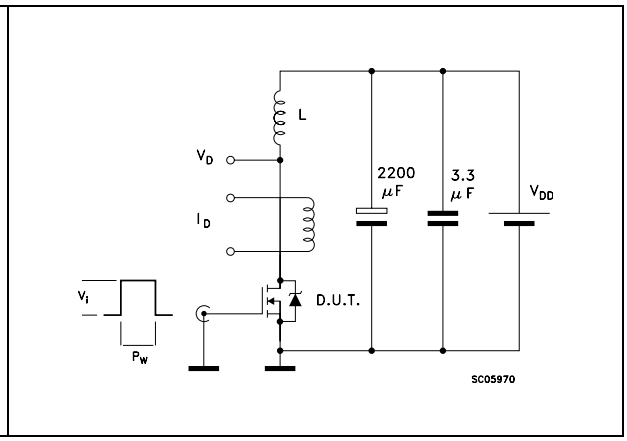


Figure 17. Unclamped inductive waveform

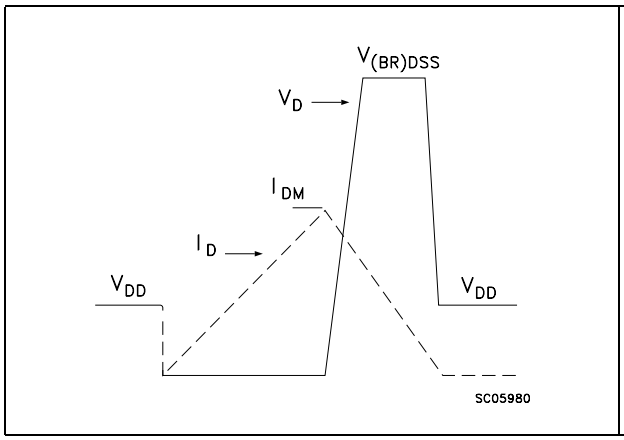
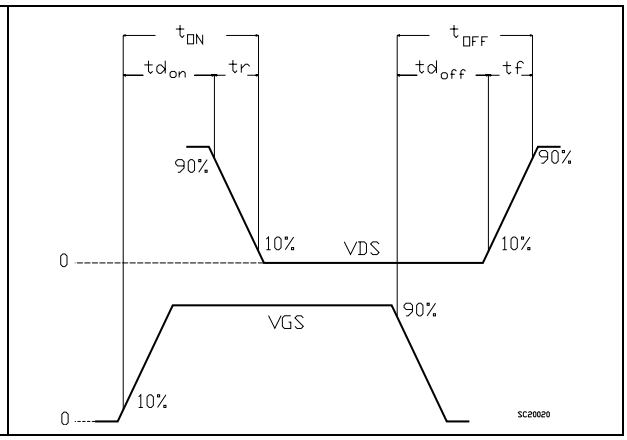


Figure 18. Switching time waveform

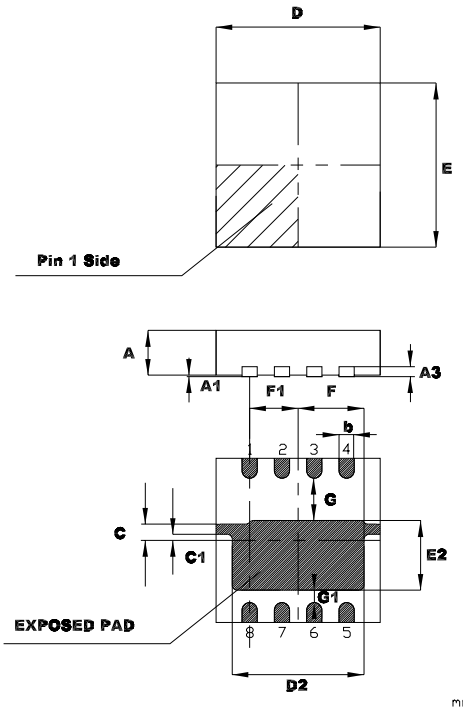


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerFLAT™ (3.3 x 3.3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.0007	
b	0.23	0.30	0.38	0.009	0.011	0.015
C		0.328			0.012	
C1		0.12			0.004	
D		3.30			0.13	
D2	2.50	2.65	2.75	0.098	0.104	0.108
E		3.30			0.13	
E2	1.25	1.40	1.50	0.049	0.055	0.059
F		1.325			0.052	
F1		0.975			0.038	
G		0.850			0.033	
G1		0.250			0.009	



5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jul-2004	1	First Release
05-Oct-2004	2	Values Changed
19-Oct-2004	3	New value inserted
22-Nov-2004	4	Document updated
21-Feb-2005	5	Final version
18-Apr-2005	6	Modified *Figure 3*, *Figure 5.*, *Figure 8.*,*Figure 9.*
14-Mar-2006	7	New template

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