

P-channel 40 V, 0.0115 Ω typ., 60 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

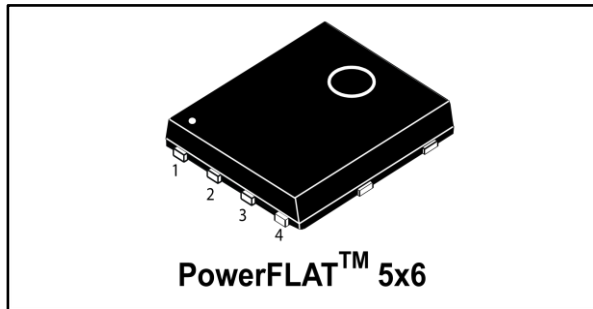
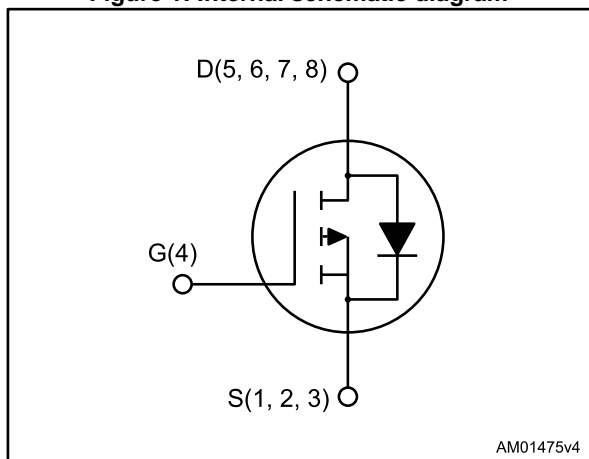


Figure 1: Internal schematic diagram



- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications


Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order codes	Marking	Package	Packaging
STL60P4LLF6	60P4LLF6	PowerFLA™ 5x6	Tape and reel

 For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Features

Order codes	V_{DS}	$R_{DS(on)max.}$	I_D
STL60P4LLF6	40 V	0.014 Ω	60

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	60	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	42	A
$I_D^{(1)(3)}$	Drain current (pulsed)	240	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	13	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	9.3	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	52	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
	Derating factor ⁽²⁾	0.03	W/ $^\circ\text{C}$
T_{stg}	Storage temperature	- 55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature	175	$^\circ\text{C}$

Notes:

- ⁽¹⁾The value is rated according to R_{thj-c}
- ⁽²⁾This value is rated according to $R_{thj-pcb}$
- ⁽³⁾Pulse width is limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	1.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb, single operation	31.3	$^\circ\text{C/W}$

Notes:

- ⁽¹⁾When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$, $I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0$, $V_{DS} = 40\text{ V}$			1	μA
		$V_{GS} = 0$, $V_{DS} = 40\text{ V}$, $T_C = 125\text{ °C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 6.5\text{ A}$		0.0115	0.014	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 6.5\text{ A}$		0.015	0.019	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	3525	-	pF
C_{OSS}	Output capacitance			344		pF
C_{RSS}	Reverse transfer capacitance			238		pF
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 13\text{ A}$, $V_{GS} = 4.5\text{ V}$	-	34	-	nC
Q_{gs}	Gate-source charge			11.3		nC
Q_{gd}	Gate-drain charge			13.8		nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 6.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	49.4	-	ns
t_r	Rise time		-	60.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	170	-	ns
t_f	Fall time		-	20	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6.5 \text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 13 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 24 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	29		ns
Q_{rr}	Reverse recovery charge		-	27.6		nC
I_{RRM}	Reverse recovery current		-	1.9		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

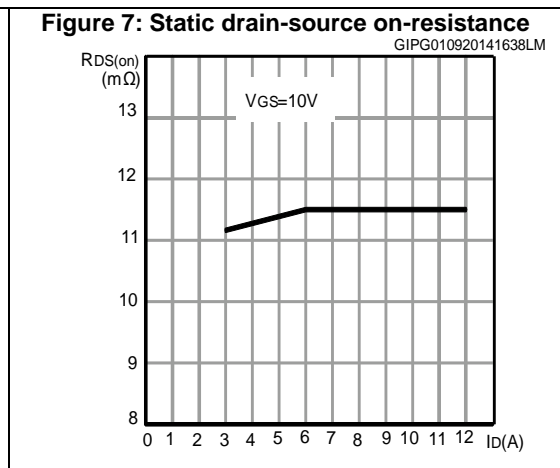
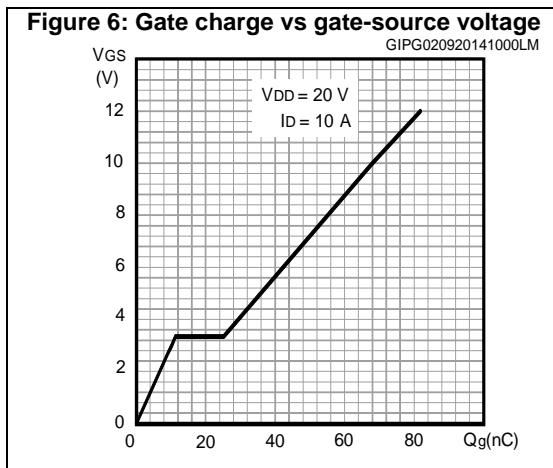
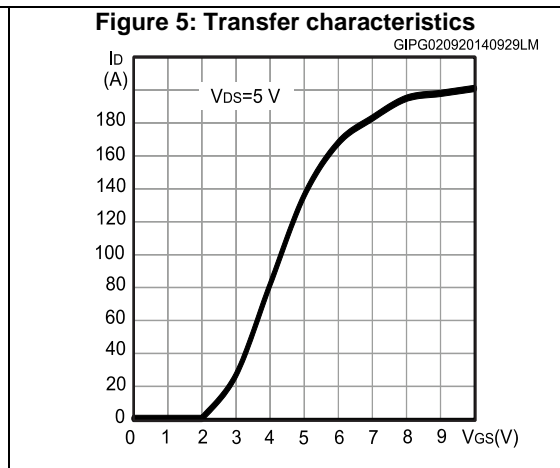
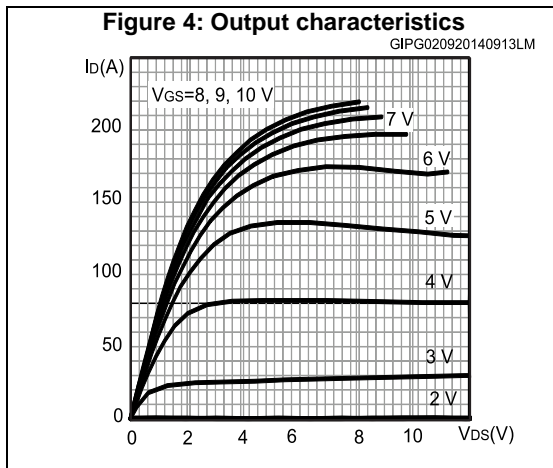
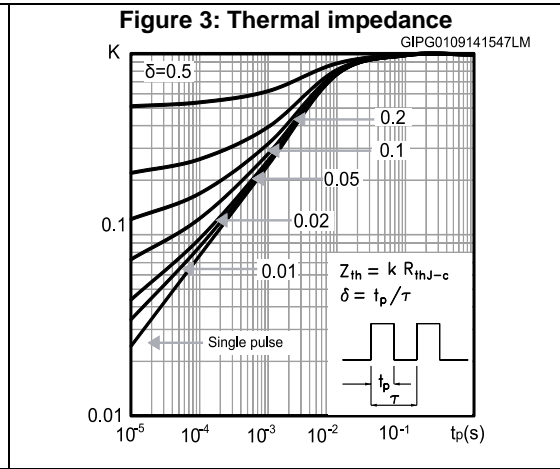
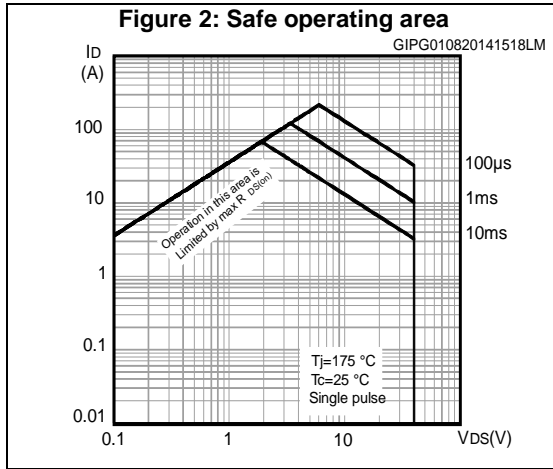


Figure 8: Capacitance variation

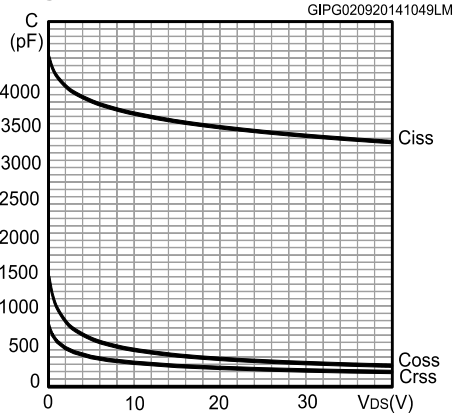


Figure 9: Normalized gate threshold voltage vs temperature

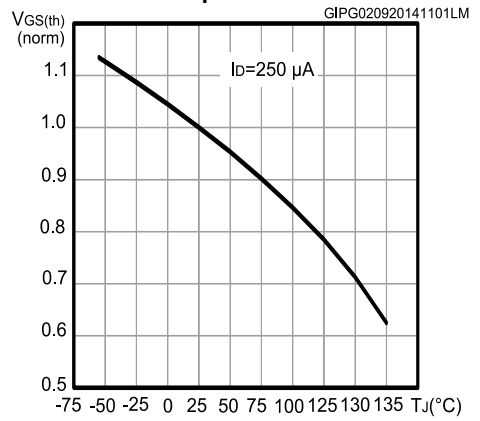


Figure 10: Normalized on-resistance vs temperature

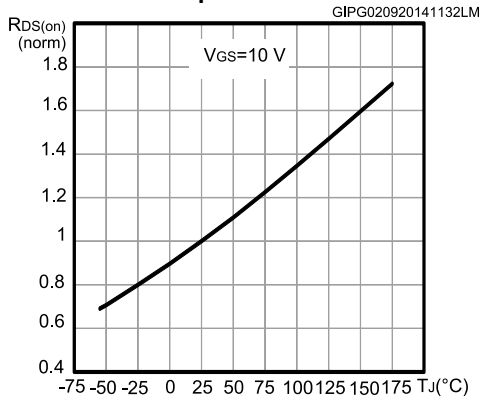


Figure 11: Normalized VBR(DSS) vs temperature

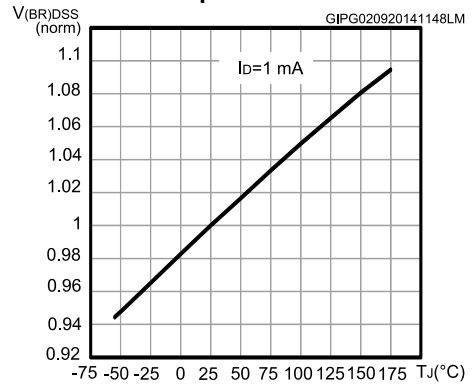
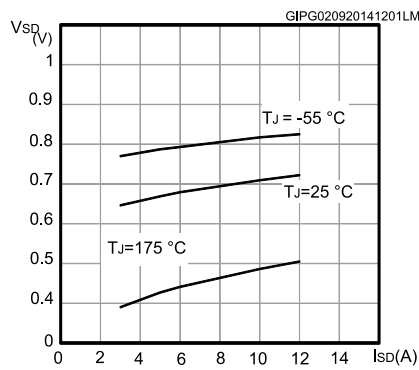
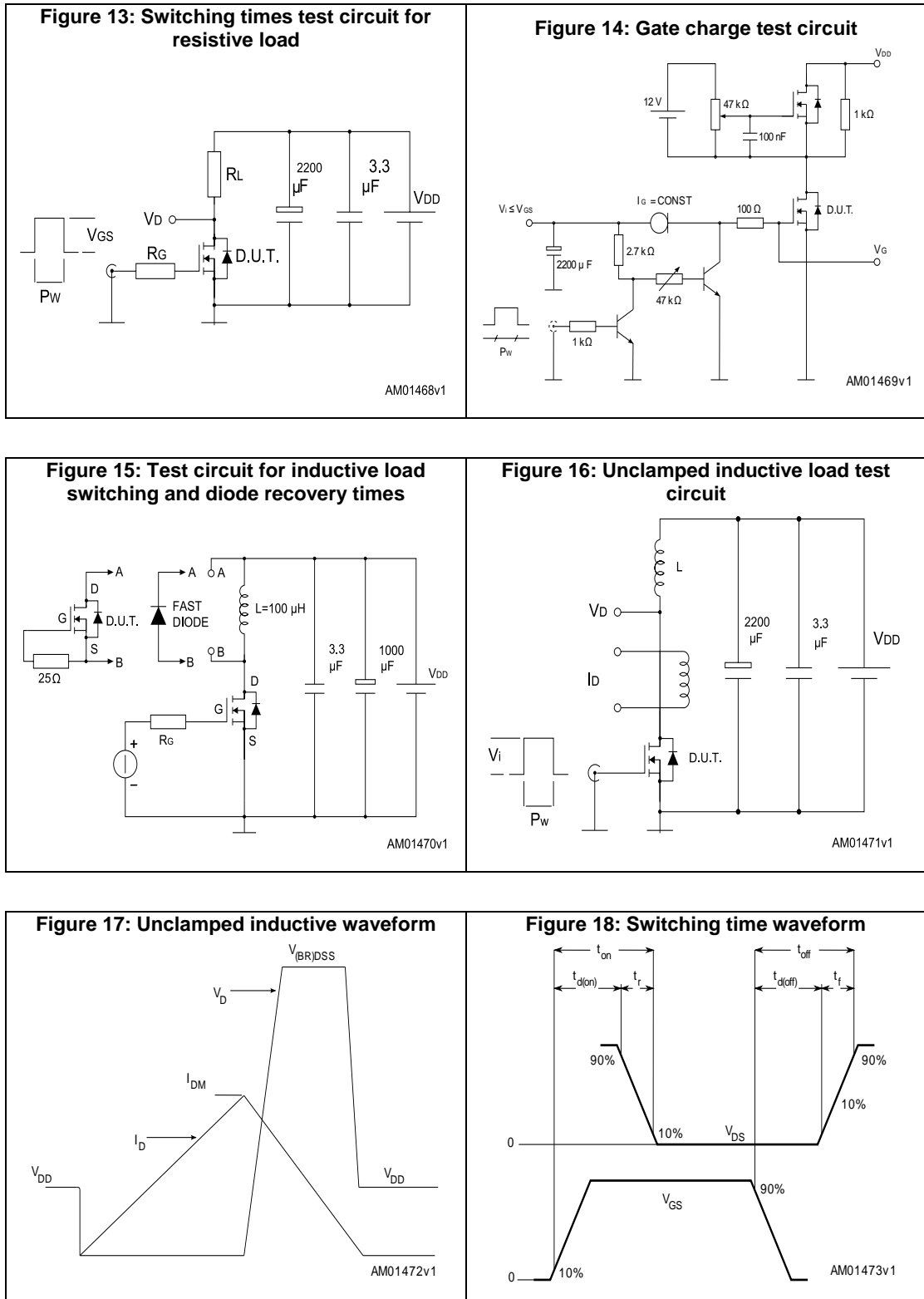


Figure 12: Source-drain diode forward characteristics



3 Test circuits



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type S-R drawings

Figure 19: PowerFLAT™ 5x6 drawings

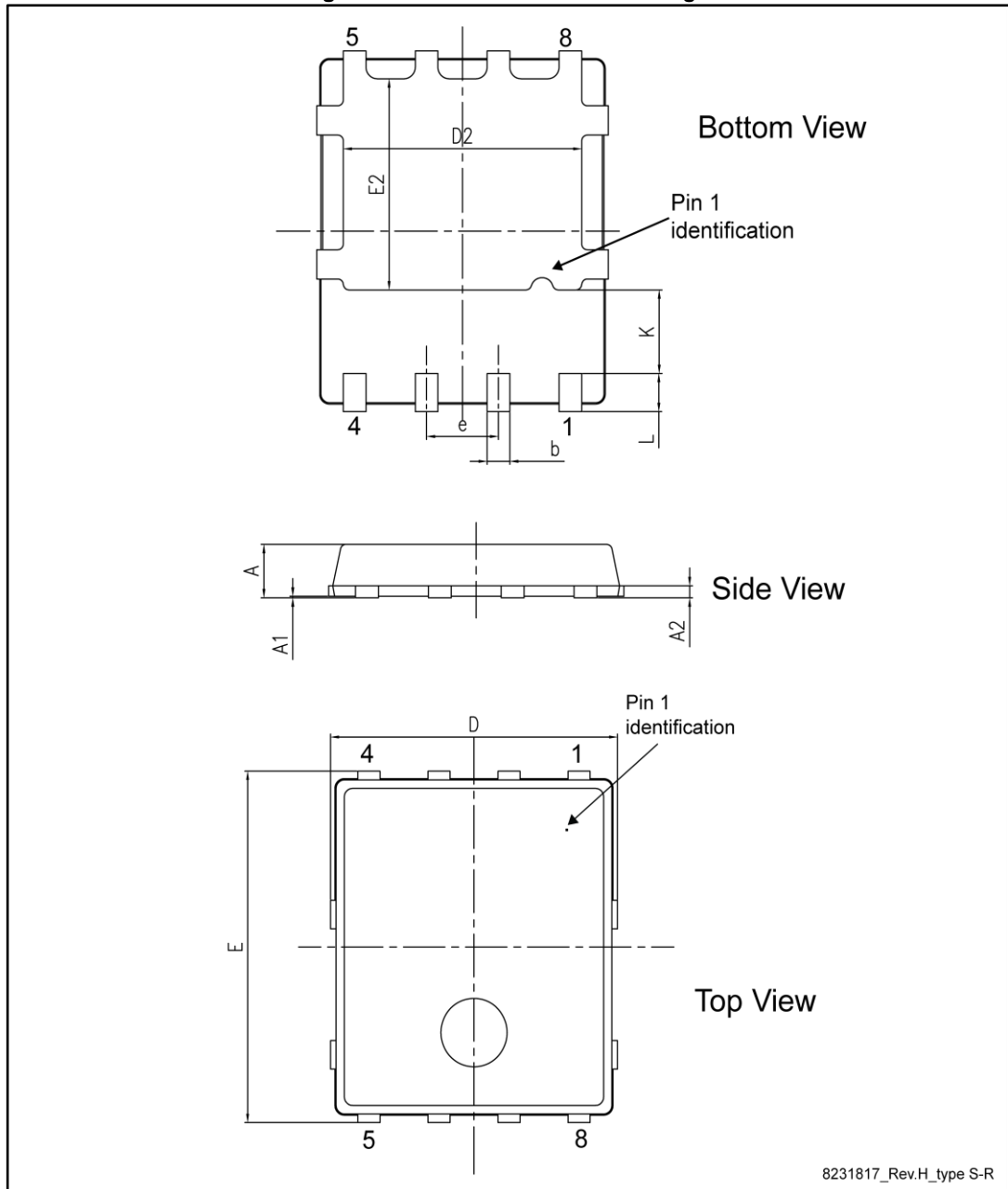
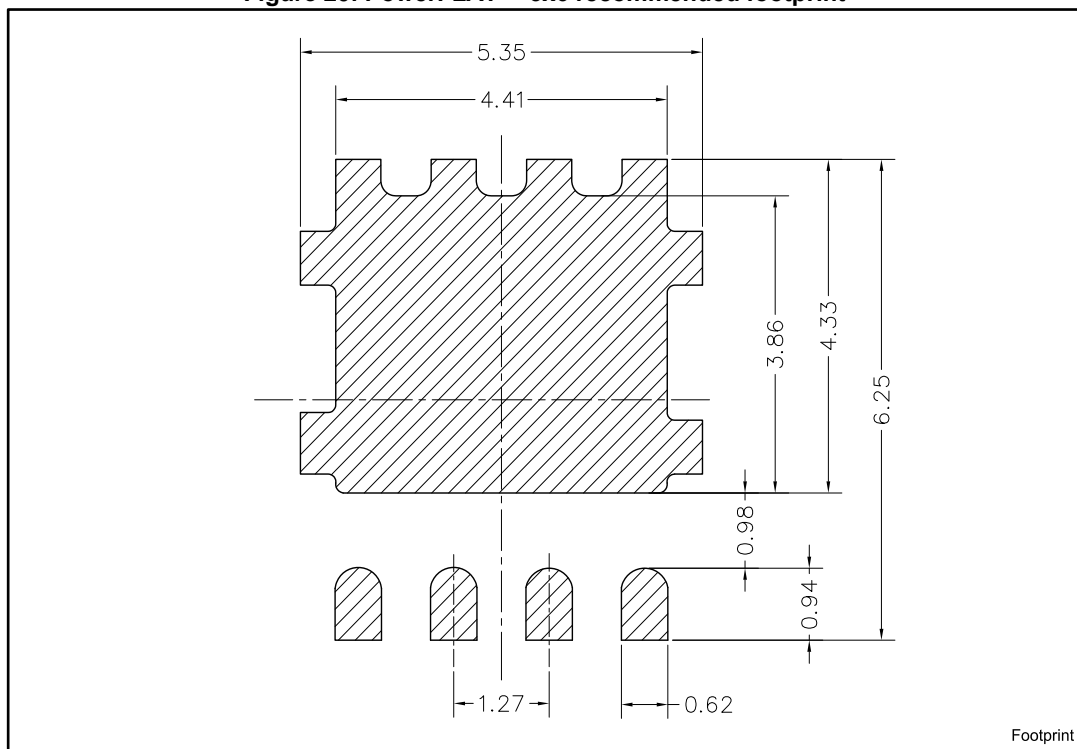


Table 8: PowerFLAT™ 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 20: PowerFLAT™ 5x6 recommended footprint



5 Packaging mechanical data

Figure 21: PowerFLAT™ 5x6 tape

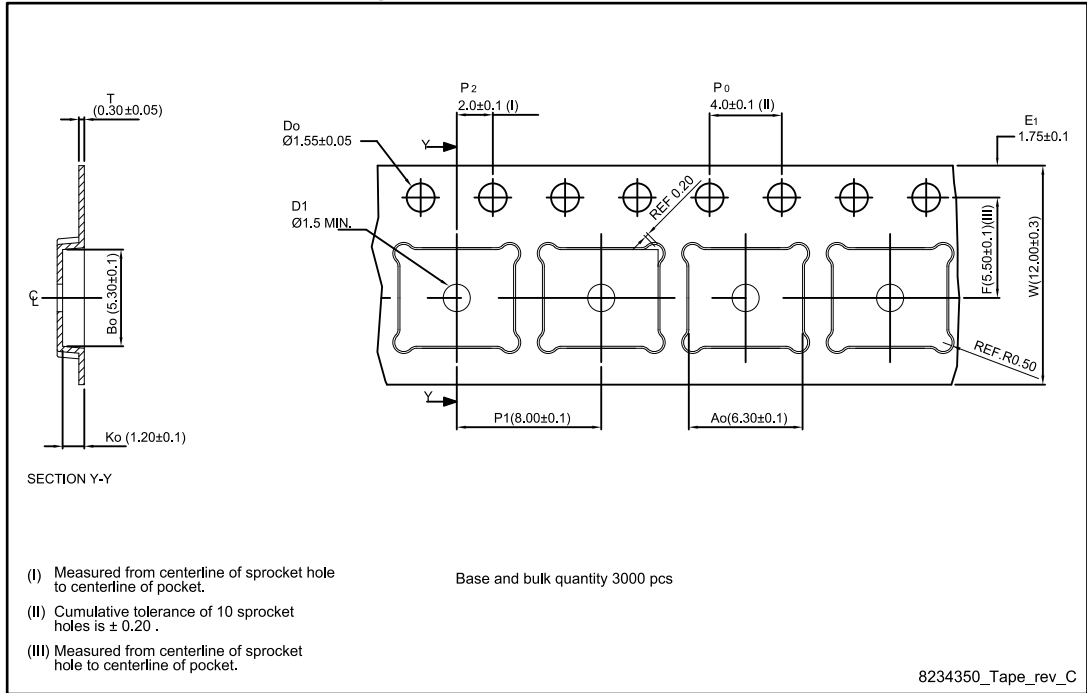


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

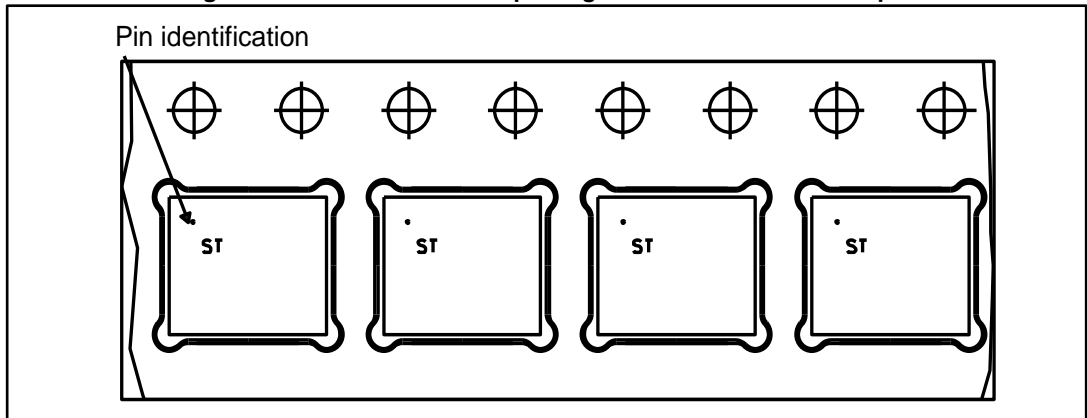
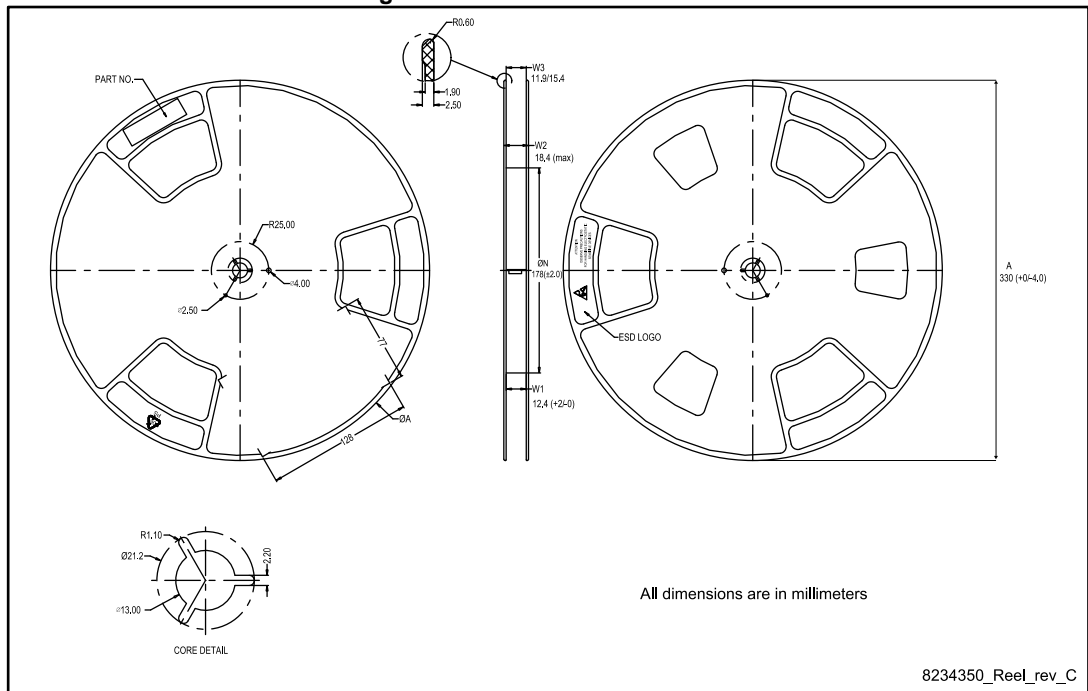


Figure 23: PowerFLAT™ 5x6 reel



6 Revision history

Table 9: Document revision history

Date	Revision	Changes
04-Sep-2014	1	Initial release.
16-Dec-2014	2	Document status promoted from preliminary data to production data. Minor text changes.

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