

## N-channel 650 V, 0.061 $\Omega$ typ., 22.5 A MDmesh™ V Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet — production data

### Features

Order code	$V_{DS}$ @ $T_{Jmax}$	$R_{DS(on)}$ max	$I_D$
STL57N65M5	710 V	0.069 $\Omega$	22.5 A <sup>(1)</sup>

1. The value is rated according to  $R_{thj-case}$  and limited by package

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

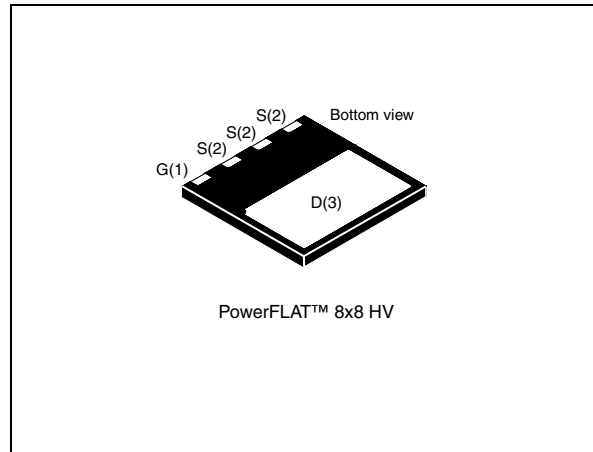


Figure 1. Internal schematic diagram

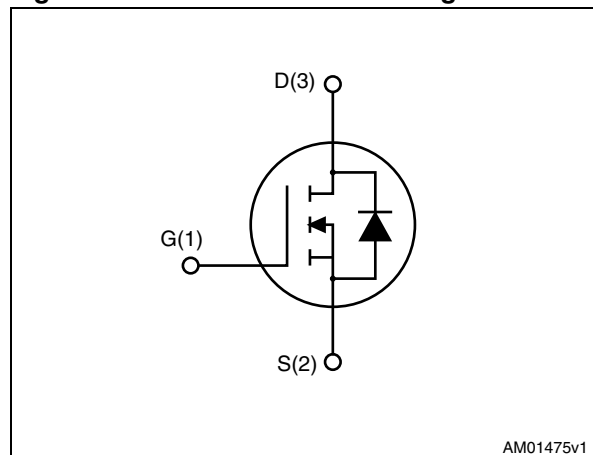


Table 1. Device summary

Order code	Marking	Package	Packaging
STL57N65M5	57N65M5	PowerFLAT™ 8x8 HV	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	22	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	90	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	4.3	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2.7	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.8	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	189	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	9	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	960	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-case}$  and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.
4.  $I_{SD} \leq 22.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$ ,  $V_{DD}=400\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.66	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$		0.061	0.069	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	4200	-	pF
$C_{oss}$	Output capacitance			100		pF
$C_{rss}$	Reverse transfer capacitance			6		pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0$ to $80\% V_{(BR)DSS}$	-	97	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related			344		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 17.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	96	-	nC
$Q_{gs}$	Gate-source charge			24		nC
$Q_{gd}$	Gate-drain charge			40		nC

1.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to  $80\% V_{DSS}$

2.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to  $80\% V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 22.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 19</a> )		84		ns
$t_r(V)$	Voltage rise time		-	10.8	-	ns
$t_{f(I)}$	Current fall time		11		ns	
$t_{c(off)}$	Crossing time		16.5		ns	

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		22.5	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		90	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 22.5\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 16</a> )	-	378		ns
$Q_{rr}$	Reverse recovery charge		7		$\mu\text{C}$	
$I_{RRM}$	Reverse recovery current		37		A	
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	454		ns
$Q_{rr}$	Reverse recovery charge		9.5		$\mu\text{C}$	
$I_{RRM}$	Reverse recovery current		42		A	

1. The value is rated according to  $R_{thj-case}$  and limited by package
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

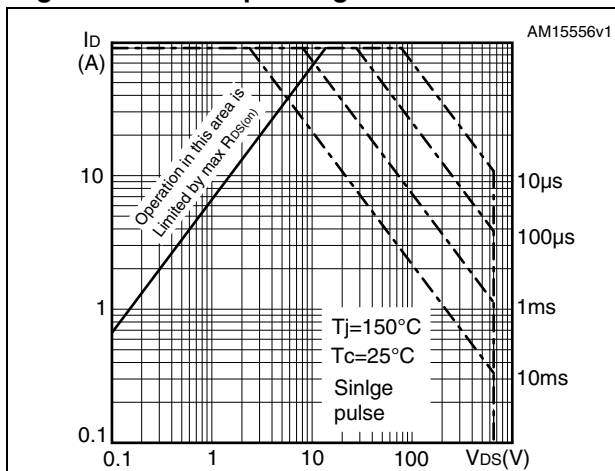


Figure 3. Thermal impedance

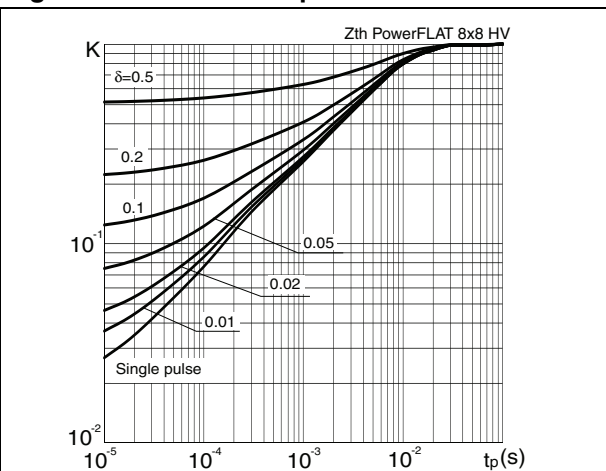


Figure 4. Output characteristics

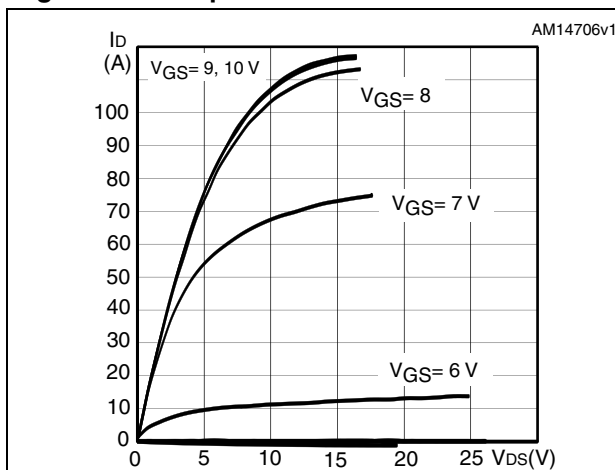


Figure 5. Transfer characteristics

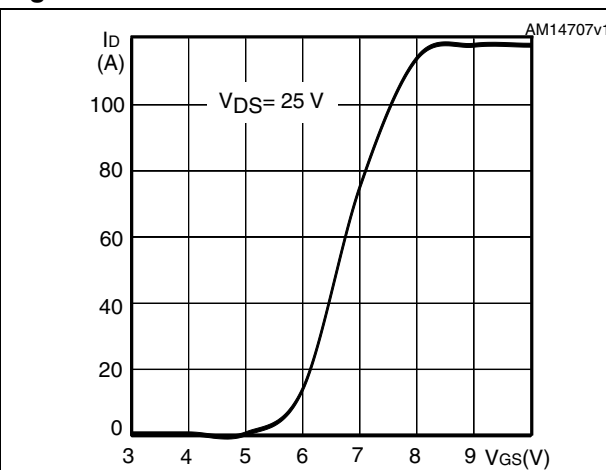


Figure 6. Gate charge vs gate-source voltage

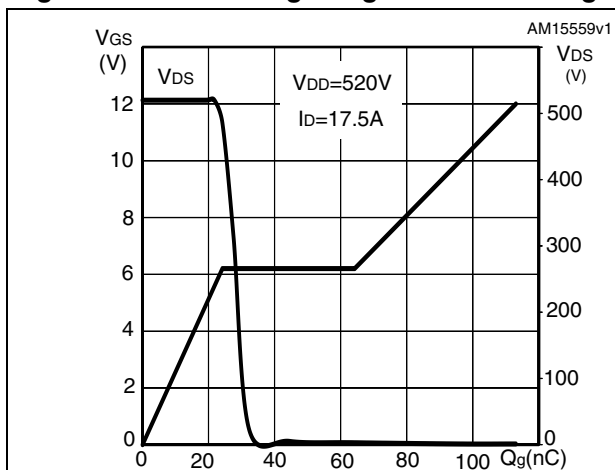


Figure 7. Static drain-source on-resistance

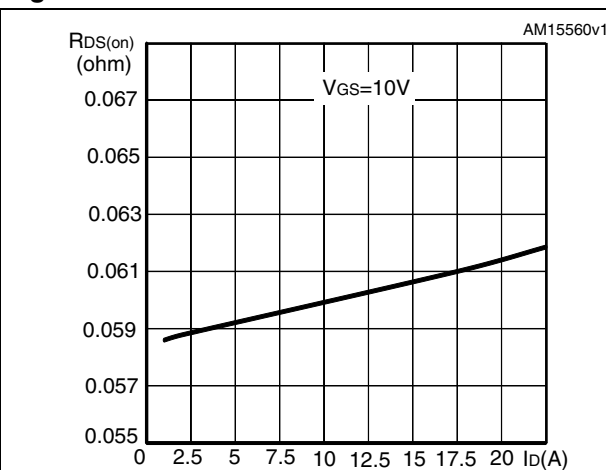


Figure 8. Capacitance variations

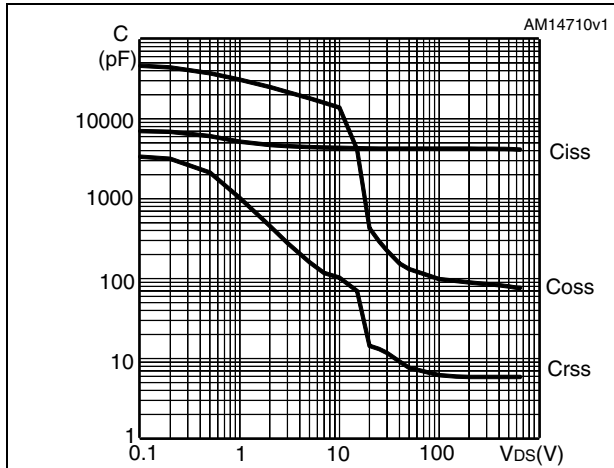


Figure 9. Output capacitance stored energy

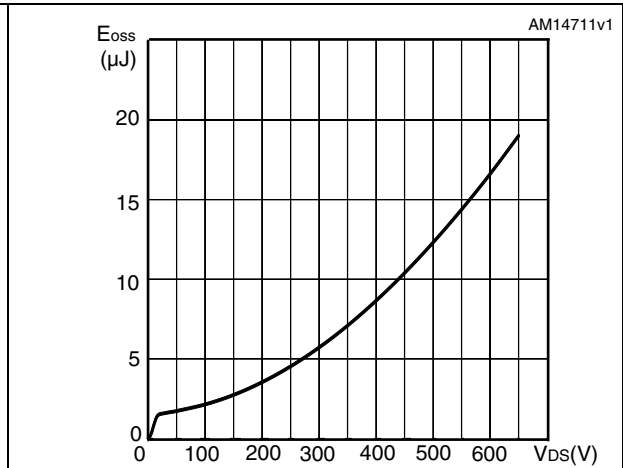


Figure 10. Normalized gate threshold voltage vs temperature

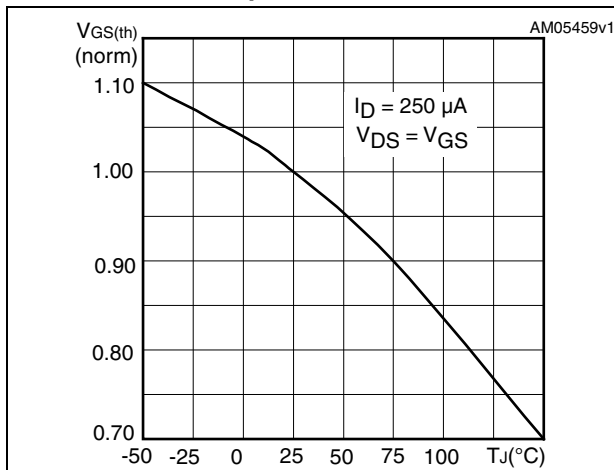


Figure 11. Normalized on-resistance vs temperature

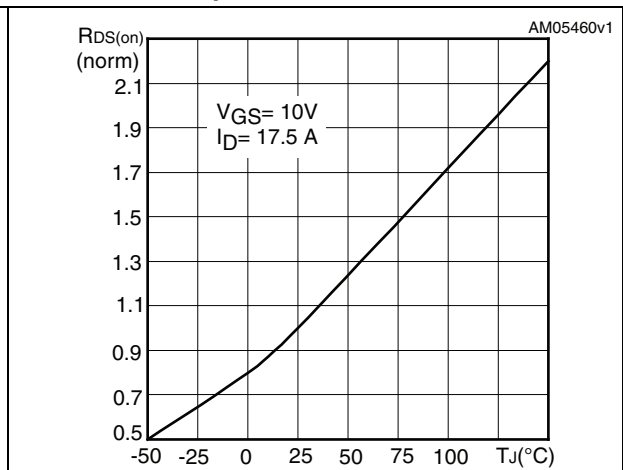


Figure 12. Normalized BVDS vs temperature

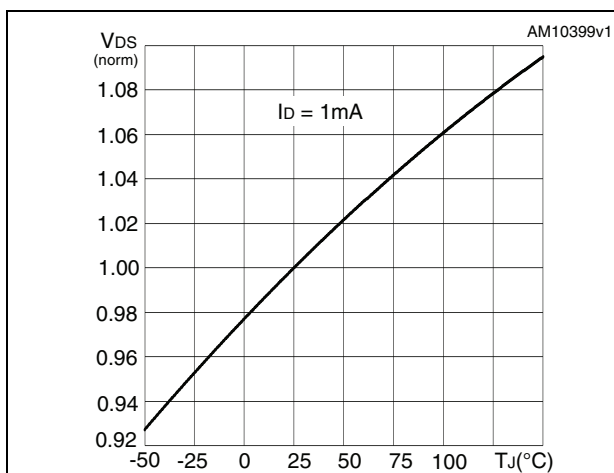
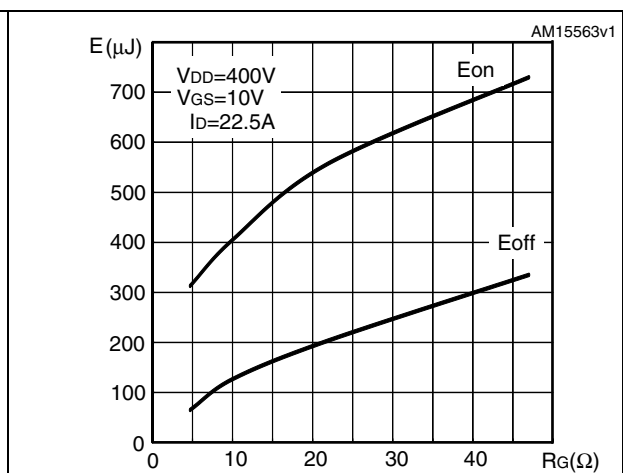


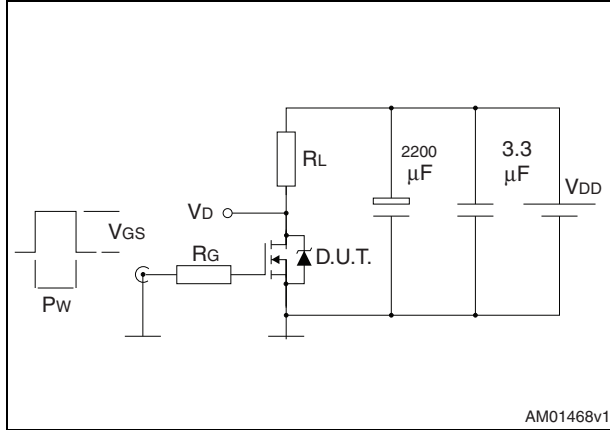
Figure 13. Switching losses vs gate resistance (1)



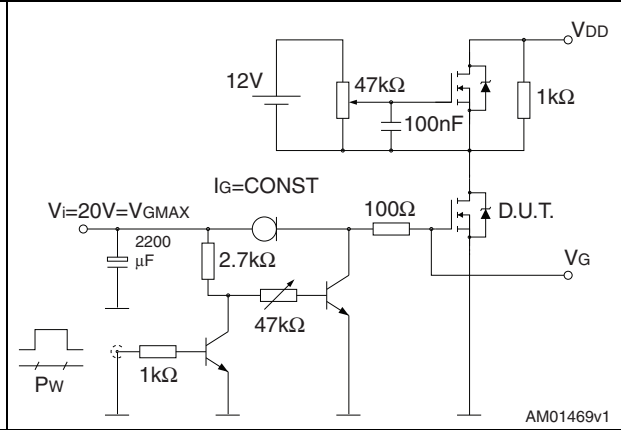
1. Eon including reverse recovery of a SiC diode

### 3 Test circuits

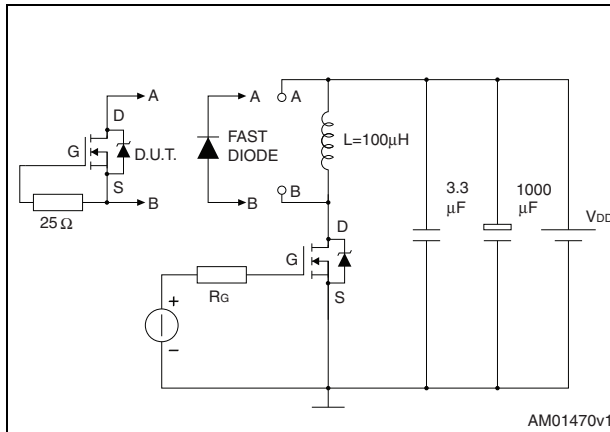
**Figure 14. Switching times test circuit for resistive load**



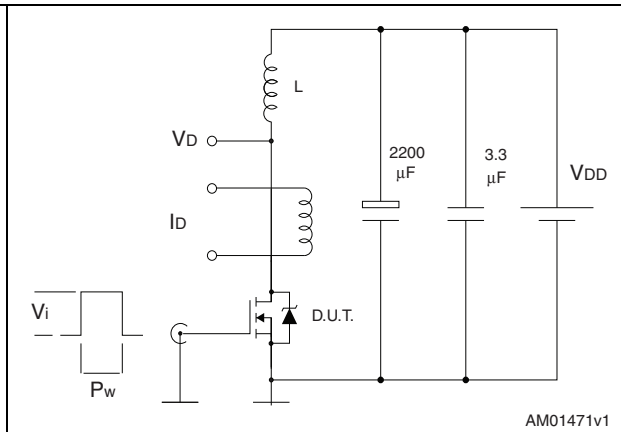
**Figure 15. Gate charge test circuit**



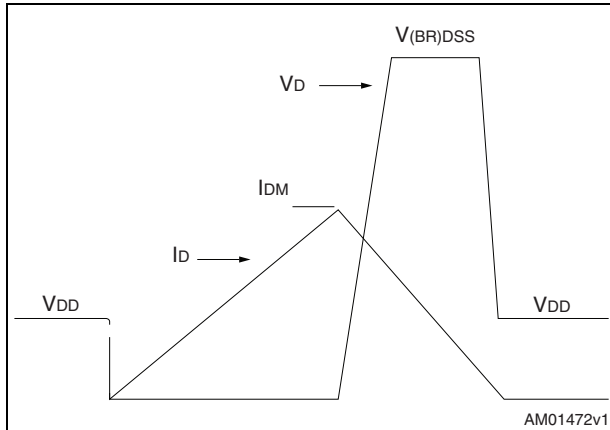
**Figure 16. Test circuit for inductive load switching and diode recovery times**



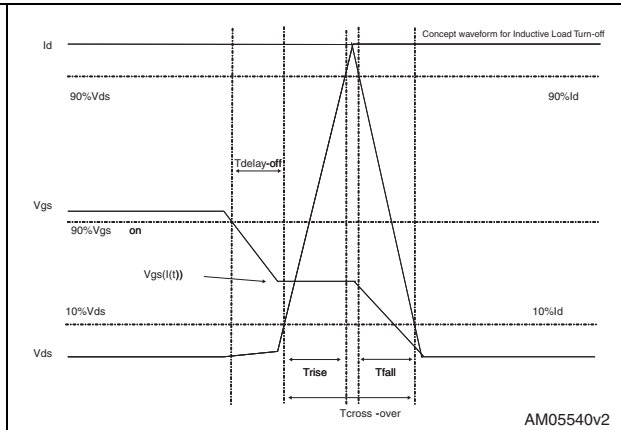
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 20. PowerFLAT™ 8x8 HV drawing mechanical data

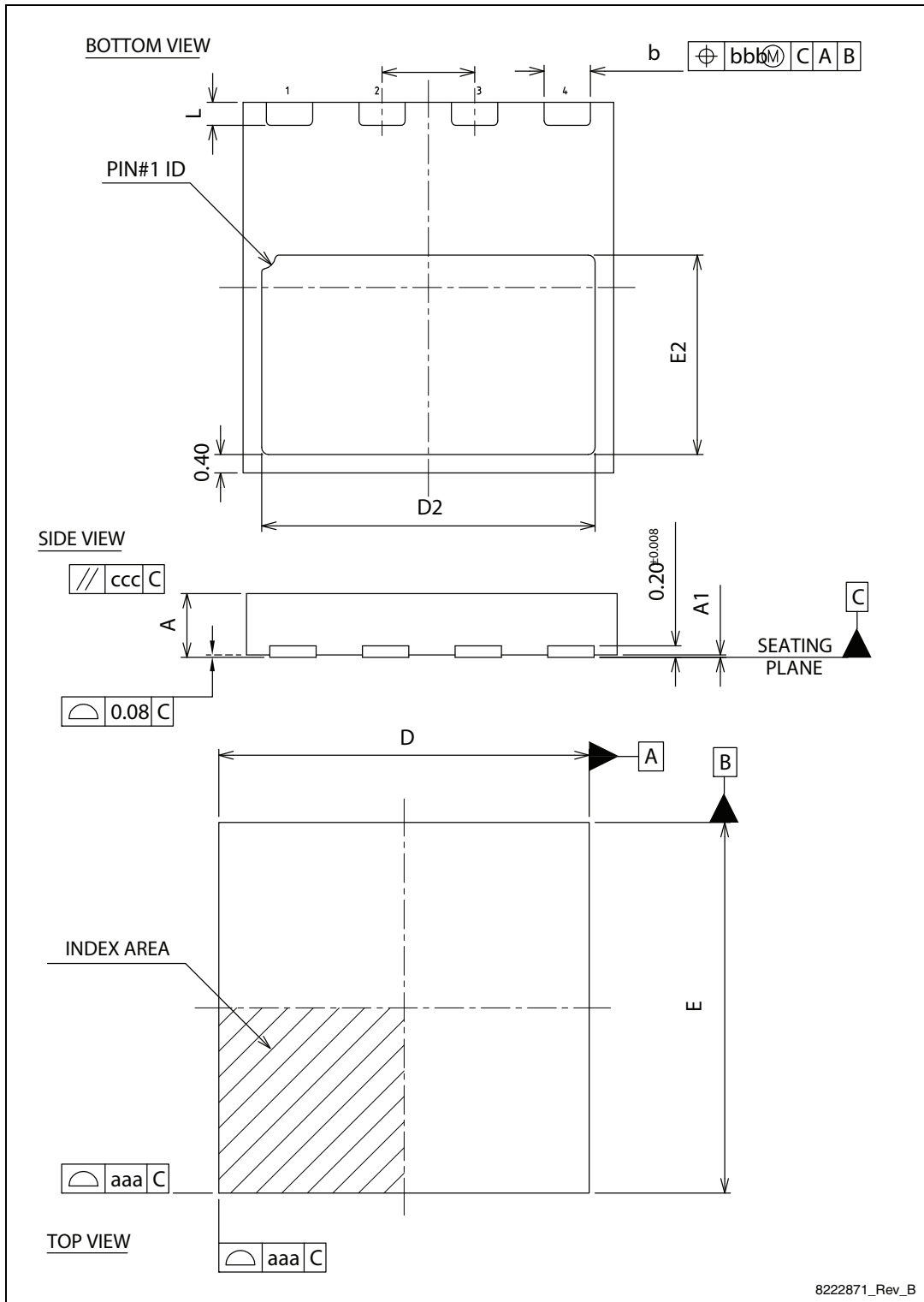
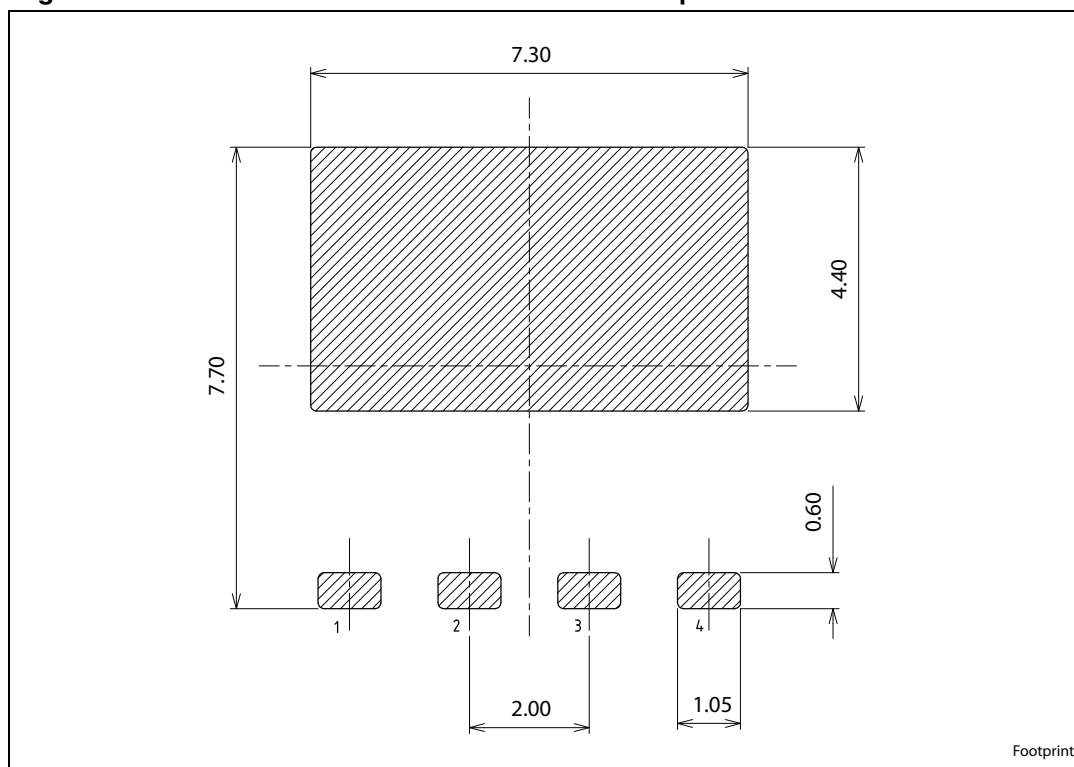


Figure 21. PowerFLAT™ 8x8 HV recommended footprint



# 5 Packaging mechanical data

Figure 22. PowerFLAT™ 8x8 HV tape

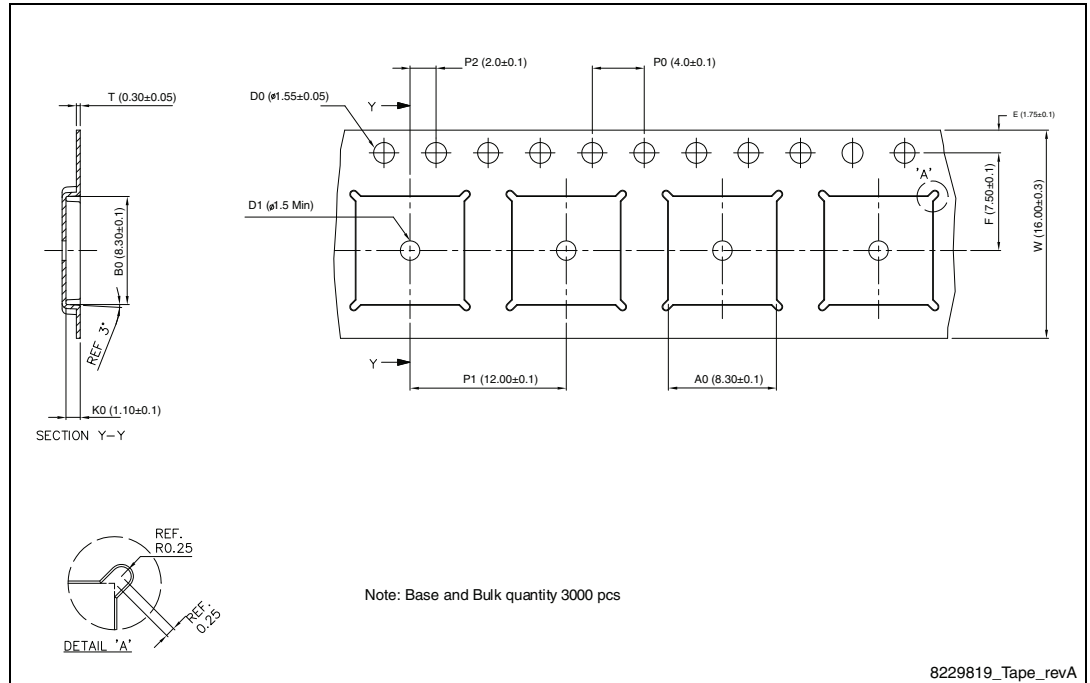
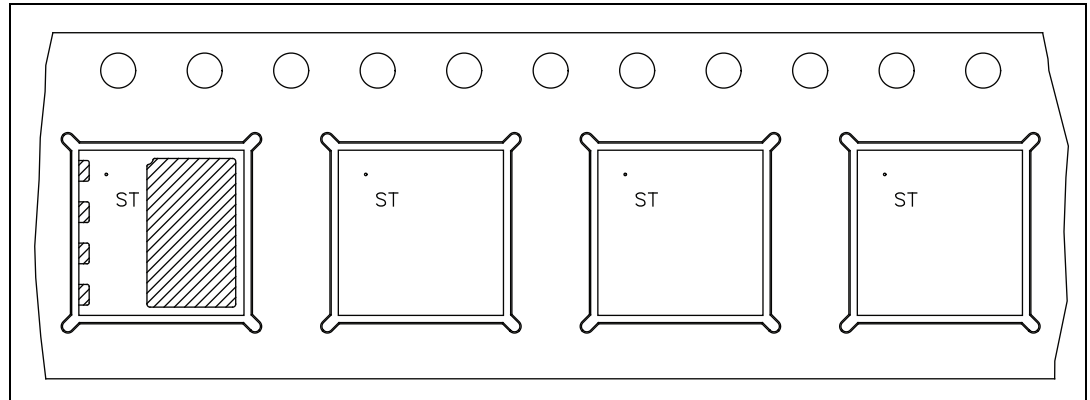


Figure 23. PowerFLAT™ 8x8 HV package orientation in carrier tape.





## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
14-May-2012	1	First release.
25-Jan-2013	2	<ul style="list-style-type: none"> <li>– Modified: <math>I_D</math> value and <a href="#">note 1</a> on first page</li> <li>– Modified: <math>I_D</math>, <math>P_{TOT}</math>, <math>I_{AR}</math> values, and <a href="#">note 1, 4</a> on <a href="#">Table 2</a></li> <li>– Modified: <math>R_{thj-case}</math> value on <a href="#">Table 3</a></li> <li>– Modified: <math>R_{DS(on)}</math> on <a href="#">Table 4</a></li> <li>– Modified: typical values on <a href="#">Table 5</a> and <a href="#">6</a></li> <li>– Modified: typical and max values on <a href="#">Table 7</a></li> <li>– Inserted: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li> <li>– Document staus promoted from preliminary data to production data</li> </ul>

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