# STL42P4LLF6

## P-channel 40 V, 0.0155 Ω typ.,42 A, STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

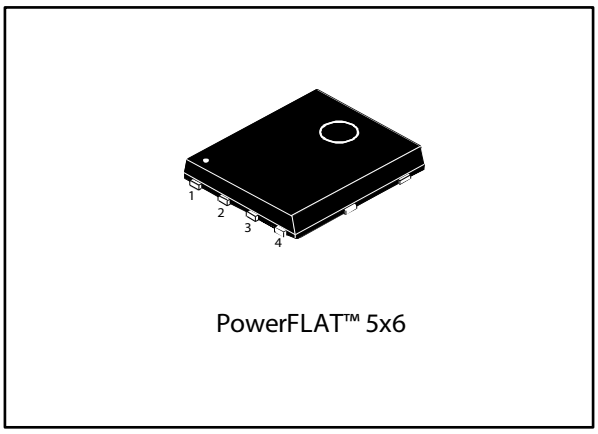
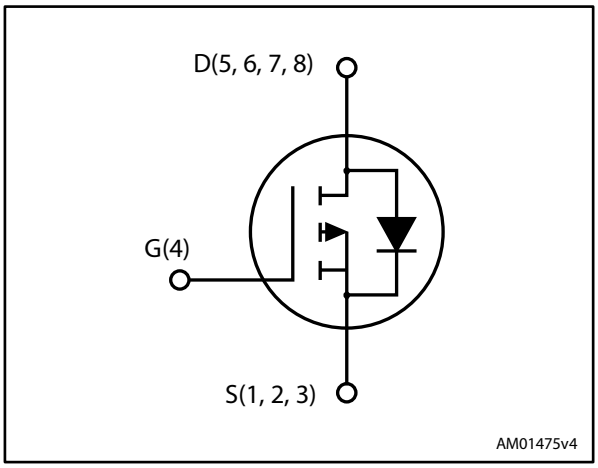



**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STL42P4LLF6 | 40 V | 0.018 Ω | 42 A | 75 W |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

## Applications

- Switching applications

## Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

**Table 1: Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL42P4LLF6 | 42P4LLF6 | PowerFLAT™ 5x6 | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 40 | V |
| $V_{GS}$ | Gate-source voltage | ± 20 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | 42 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 100 °C | 29 | A |
| $I_D$ (1)(3) | Drain current (pulsed) | 168 | A |
| $I_D$ (2) | Drain current (continuous) at $T_{pcb}$= 25 °C | 10 | A |
| $I_D$ (2) | Drain current (continuous) at $T_{pcb}$= 100 °C | 7.5 | A |
| $I_{DM}$ (2)(3) | Drain current (pulsed) | 40 | A |
| $P_{TOT}$ (1) | Total dissipation at $T_C$ = 25 °C | 75 | W |
| $P_{TOT}$ (2) | Total dissipation at $T_{pcb}$= 25 °C | 4.8 | W |
| $T_{stg}$ | Storage temperature | -55 to 175 | °C |
| $T_j$ | Maximum junction temperature | 175 | °C |

**Notes:**

(1)The value is limited by $R_{thj\text{-}case}$.

(2)The value is limited by $R_{thj\text{-}pcb}$.

(3)Pulse width is limited by safe operating area.

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 2.00 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb, single operation | 31.3 | °C/W |

**Notes:**

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, steady state

For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4: Static**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 40 | | | V |
| $I_{DSS}$ | Zero gate voltage Drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 40 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 40 V, $T_C$ = 125 °C | | | 10 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | | 2.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 5 A | | 0.0105 | 0.018 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$= 5 A | | 0.021 | 0.026 | |

**Table 5: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 2850 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 270 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 180 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 20 V, $I_D$ = 10 A, $V_{GS}$ = 4.5 V (see *Figure 14: "Gate charge test circuit"*) | - | 22 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 9.4 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 7.3 | - | nC |
| $R_G$ | Gate input resistance | $I_D$ = 0 A, gate DC bias = 0 V, f = 1 MHz, magnitude of alternative signal = 20 mV | - | 1.4 | - | Ω |

**Table 6: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 20 V, $I_D$ = 5 A $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 13: "Switching times test circuit for resistive load"*) | - | 43 | - | ns |
| $t_r$ | Rise time | | - | 47 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 148 | - | ns |
| $t_f$ | Fall time | | - | 19 | - | ns |

For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

**Table 7: Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SD}$ (1) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 5 A | - | | 1.1 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A, di/dt = 100 A/µs, $V_{DD}$ = 32 V, $T_j$ = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*) | - | 26 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 21 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 1.7 | | A |

**Notes:**

(1)Pulse test: pulse duration = 300 µs, duty cycle 1.5%

For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2.1 Electrical characteristics (curves)

**Figure 2: Safe operating area**

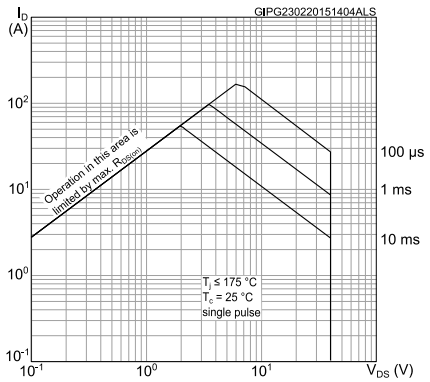



**Figure 3: Thermal impedance**

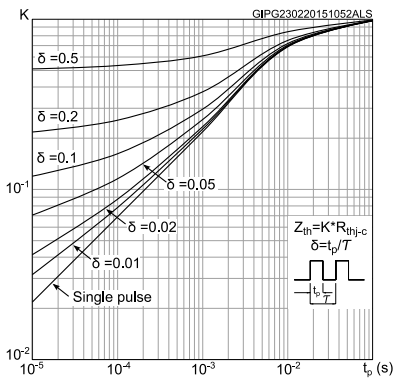



**Figure 4: Output characteristics**

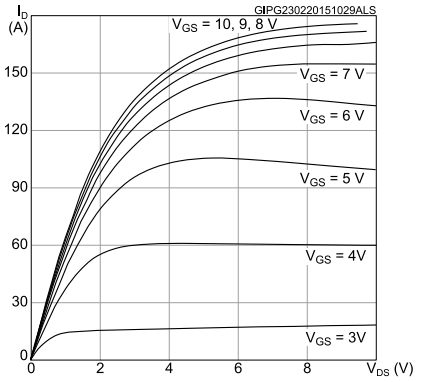



**Figure 5: Transfer characteristics**

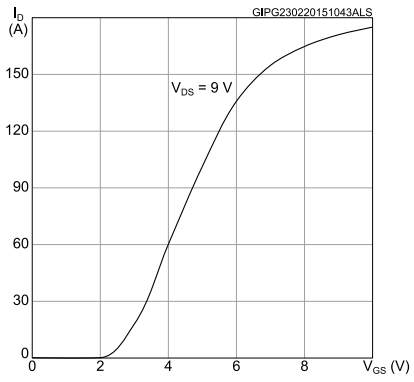



**Figure 6: Normalized gate threshold voltage vs temperature**

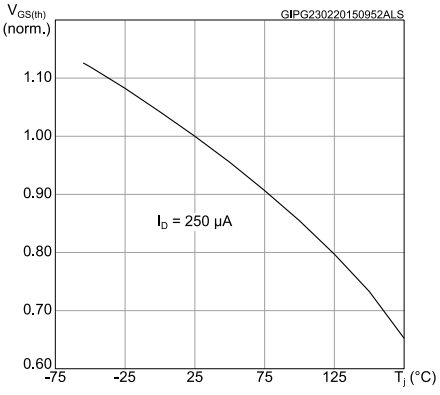



**Figure 7: Normalized V(BR)DSS vs temperature**

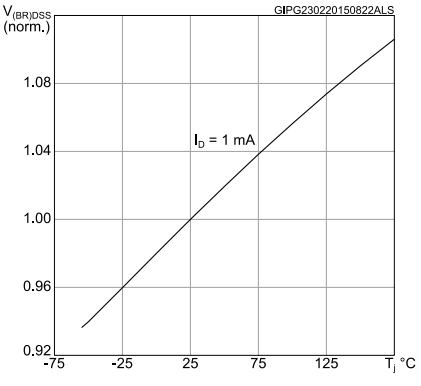


**Figure 8: Static drain-source on-resistance**

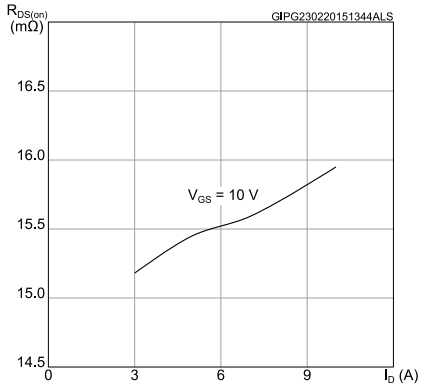



**Figure 9: Normalized on-resistance vs. temperature**

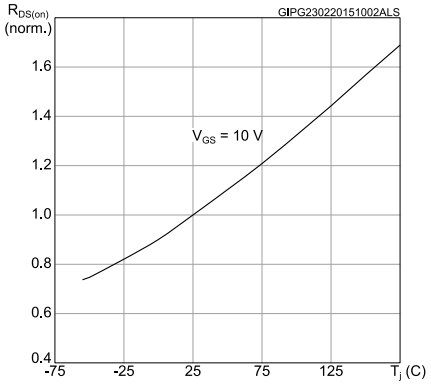



**Figure 10: Gate charge vs gate-source voltage**

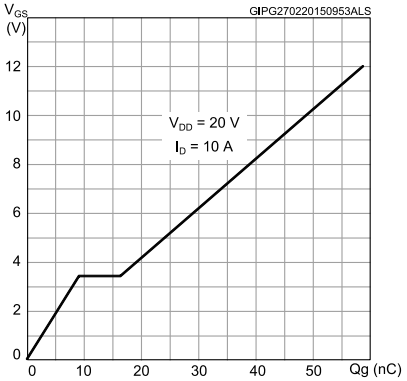



**Figure 11: Capacitance variations voltage**

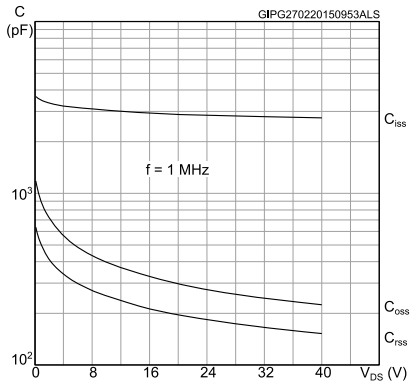
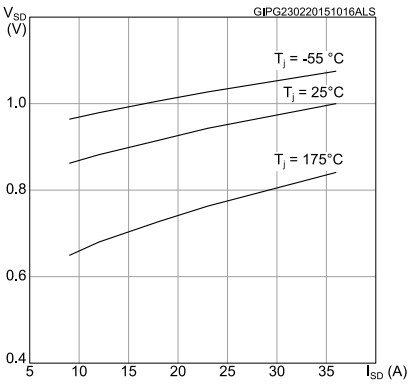



**Figure 12: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13: Switching times test circuit for resistive load**

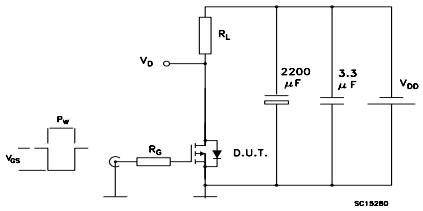



**Figure 14: Gate charge test circuit**

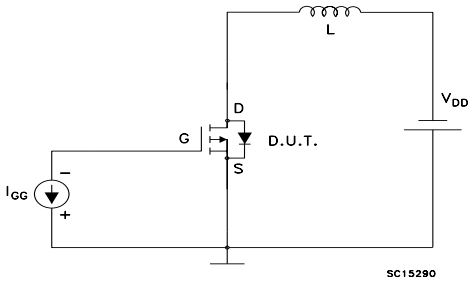
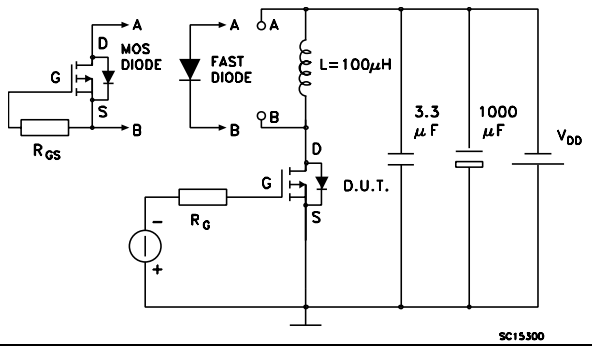



**Figure 15: Test circuit for inductive load switching and diode recovery times**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 5x6 type R package information

**Figure 16: PowerFLAT™ 5x6 type R package outline**

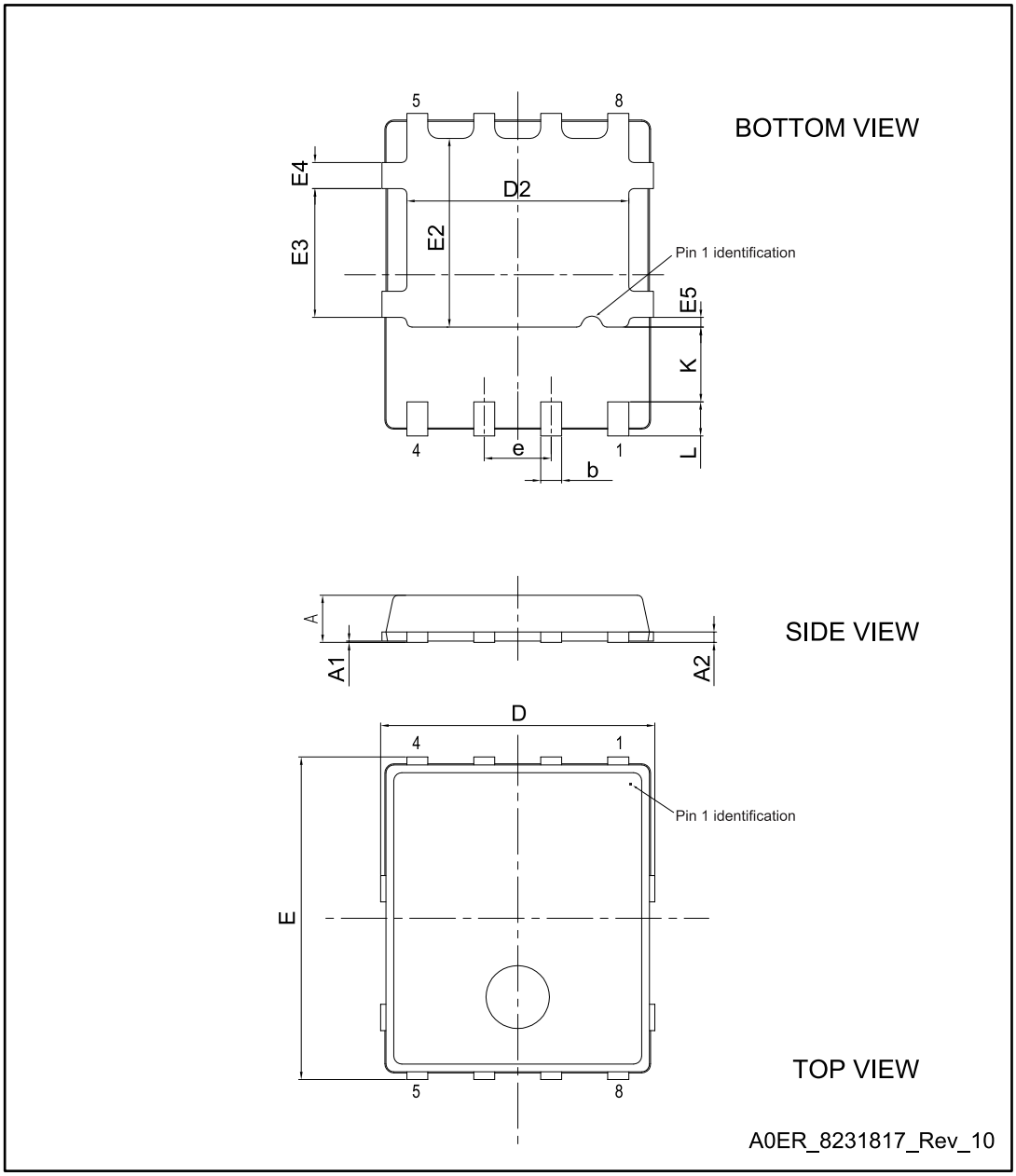
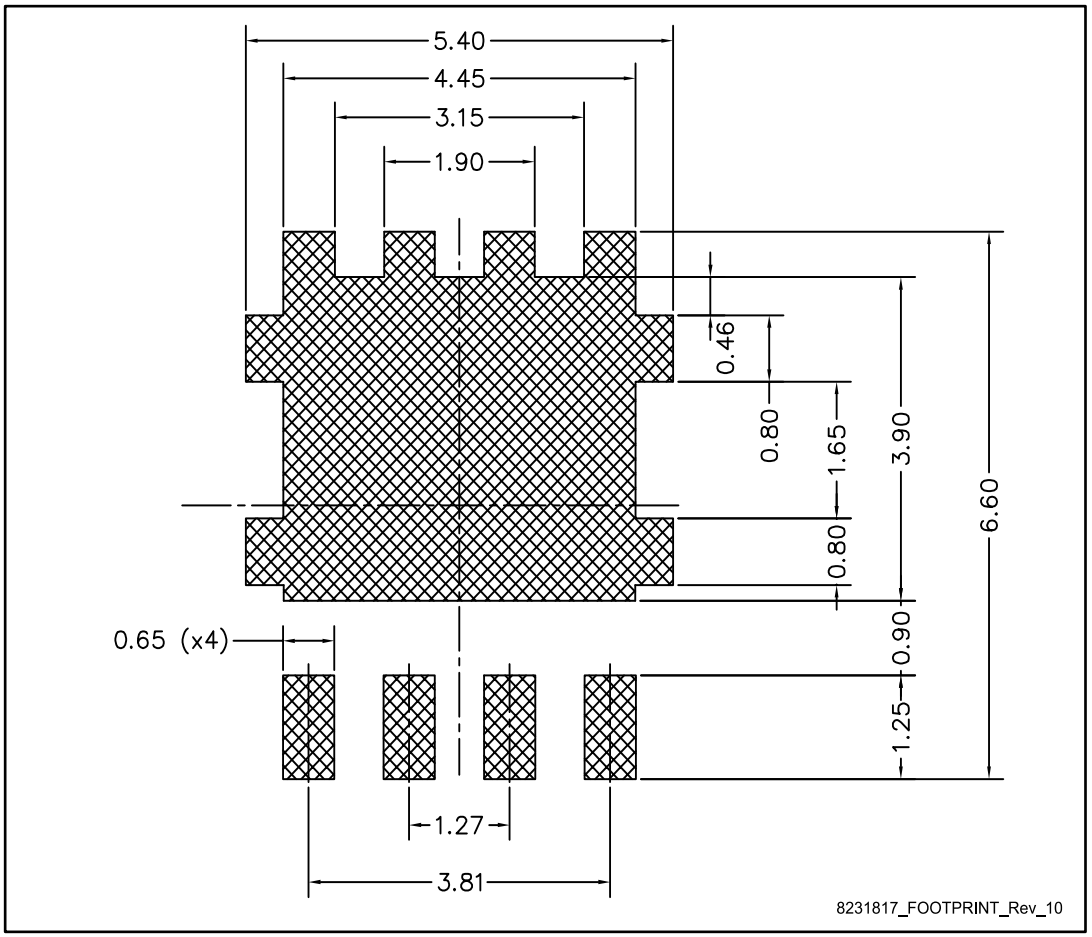


**Table 8: PowerFLAT™ 5x6 type R mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | 5.00 | 5.20 | 5.40 |
| E | 5.95 | 6.15 | 6.35 |
| D2 | 4.11 | | 4.31 |
| e | | 1.27 | |
| L | 0.60 | | 0.80 |
| K | 1.275 | | 1.575 |
| E3 | 2.35 | | 2.55 |
| E4 | 0.40 | | 0.60 |
| E5 | 0.08 | | 0.28 |

**Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)**



## 4.2 PowerFLAT™ 5x6 packing information

**Figure 18: PowerFLAT™ 5x6 tape (dimensions are in mm)**

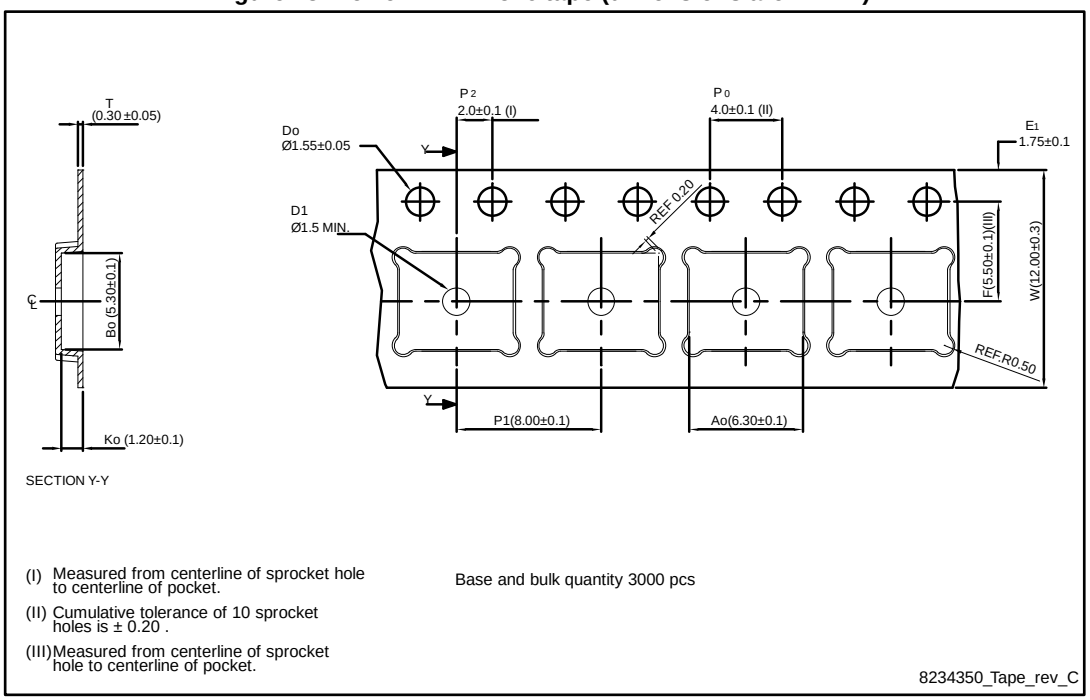



**Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape**

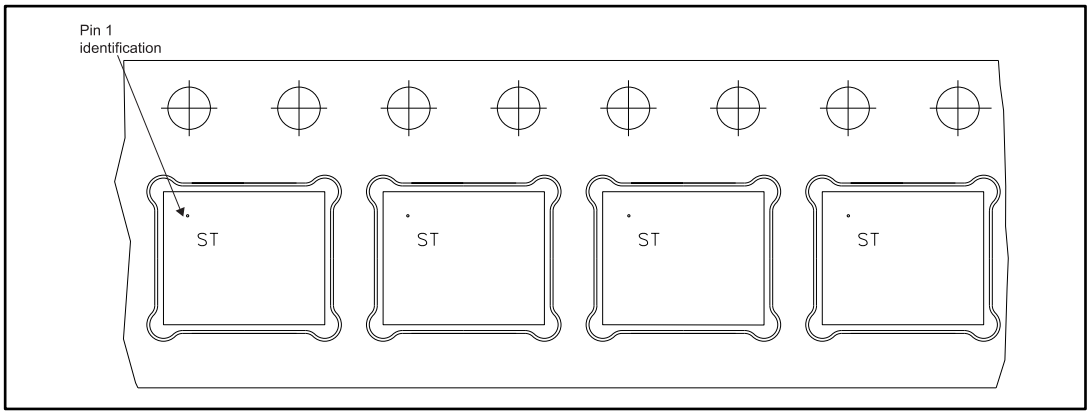
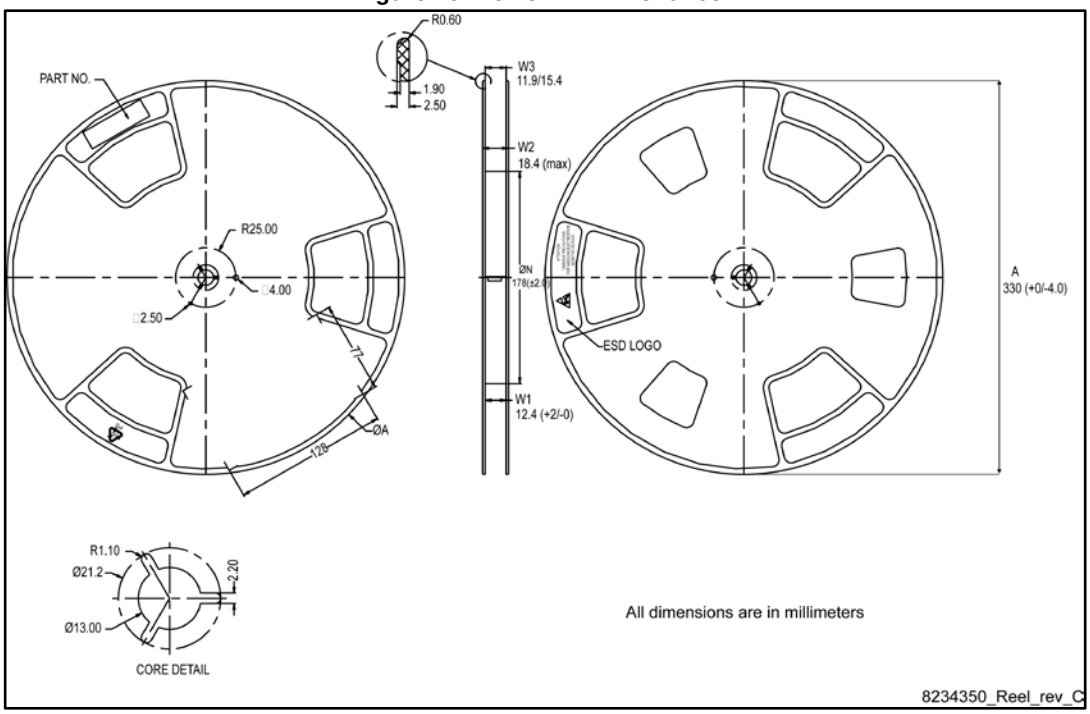


**Figure 20: PowerFLAT™ 5x6 reel**



# 5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 28-Jan-2014 | 1 | Initial release. |
| 24-Mar-2015 | 2 | Text edits throughout document<br>On cover page, updated title, description and features table<br>Renamed and updated Table 4: Static<br>Updated Table 5: Dynamic<br>Updated Table 6: Switching times<br>Updated Table 7: Source-drain diode<br>Added Section 2.1: Electrical characteristics (curves)<br>Renamed and updated Section 4.1 PowerFLAT™ 5x6 type R package information<br>Renamed and updated Section 5 Packing information |

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