

**64 Kbit (8K x 8) AutoStore nvSRAM**

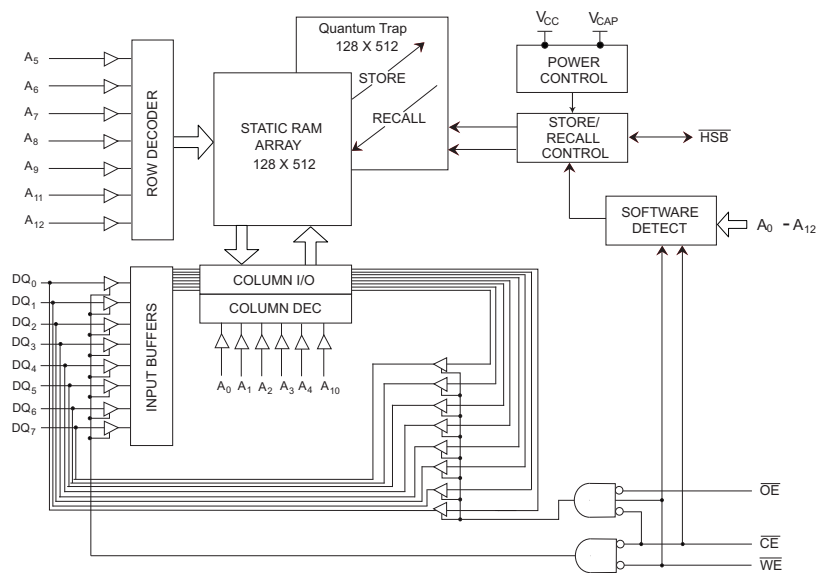
**Features**

- 35 ns and 55 ns access times
- Hands off automatic STORE on power down with external 68 µF capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, hardware, or AutoStore™ on power down
- RECALL to SRAM initiated by software or power up
- Unlimited Read, Write, and Recall cycles
- 1,000,000 STORE cycles to QuantumTrap
- 100 year data retention to QuantumTrap
- Single 5V±10% operation
- Military temperature
- 28-pin (300mil) CDIP and 28-pad LCC packages

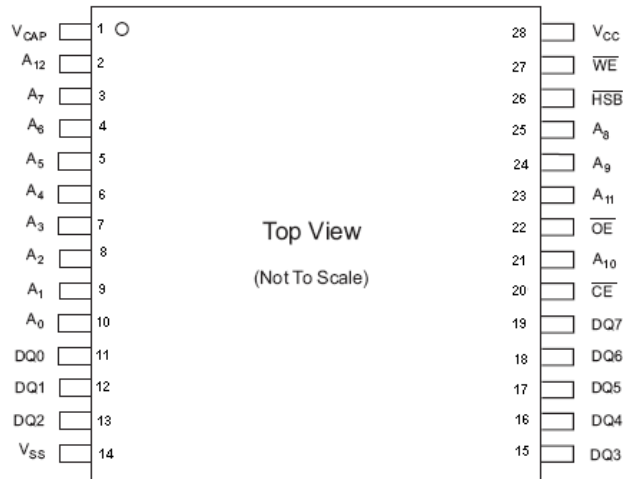
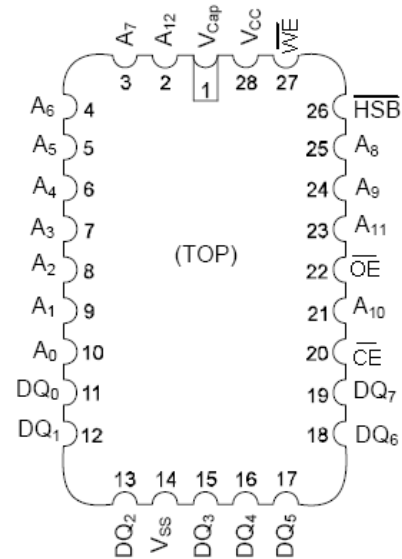
**Functional Description**

The Cypress STK12C68-5 is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control. A hardware STORE is initiated with the HSB pin.

**Logic Block Diagram**



## Pinouts

**Figure 1. Pin Diagram - 28-Pin DIP**

**Figure 2. Pin Diagram - 28-Pin LLC**


## Pin Definitions

Pin Name	Alt	IO Type	Description
A <sub>0</sub> -A <sub>12</sub>		Input	<b>Address Inputs.</b> Used to select one of the 8,192 bytes of the nvSRAM.
DQ <sub>0</sub> -DQ <sub>7</sub>		Input or Output	<b>Bidirectional Data IO Lines.</b> Used as input or output lines depending on operation.
WE	W	Input	<b>Write Enable Input, Active LOW.</b> When the chip is enabled and WE is LOW, data on the IO pins is written to the specific address location.
CE	E	Input	<b>Chip Enable Input, Active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
OE	G	Input	<b>Output Enable, Active LOW.</b> The active LOW OE input enables the data output buffers during read cycles. Deasserting OE HIGH causes the IO pins to tri-state.
V <sub>SS</sub>		Ground	<b>Ground for the Device.</b> The device is connected to ground of the system.
V <sub>CC</sub>		Power Supply	<b>Power Supply Inputs to the Device.</b>
HSB		Input or Output	<b>Hardware Store Busy (HSB).</b> When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected (connection optional).
V <sub>CAP</sub>		Power Supply	<b>AutoStore Capacitor.</b> Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

## Device Operation

The STK12C68-5 nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM Read and Write operations are inhibited. The STK12C68-5 supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

## SRAM Read

The STK12C68-5 performs a Read cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are LOW while WE and HSB are HIGH. The address specified on pins A<sub>0-12</sub> determines the 8,192 data bytes accessed. When the Read is initiated by an address transition, the outputs are valid after a delay of t<sub>AA</sub> (Read cycle 1). If the Read is initiated by CE or OE, the outputs are valid at t<sub>ACE</sub> or at t<sub>DOE</sub>, whichever is later (Read cycle 2). The data outputs repeatedly respond to address changes within the t<sub>AA</sub> access time without the need for transitions on any control input pins, and remains valid until another address change or until CE or OE is brought HIGH, or WE or HSB is brought LOW.

## SRAM Write

A Write cycle is performed whenever  $\overline{CE}$  and  $\overline{WE}$  are LOW and HSB is HIGH. The address inputs must be stable prior to entering the Write cycle and must remain stable until either CE or WE goes HIGH at the end of the cycle. The data on the common IO pins DQ<sub>0-7</sub> are written into the memory if it has valid t<sub>SD</sub>, before the end of a WE controlled Write or before the end of an CE controlled Write. Keep OE HIGH during the entire Write cycle to avoid data bus contention on common IO lines. If OE is left LOW, internal circuitry turns off the output buffers t<sub>HZWE</sub> after WE goes LOW.

## AutoStore Operation

The STK12C68-5 stores data to nvSRAM using one of three storage operations:

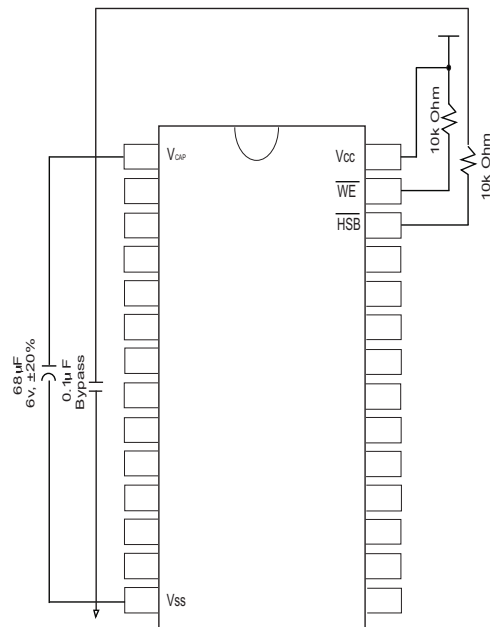
1. Hardware store activated by  $\overline{HSB}$
2. Software store activated by an address sequence
3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the STK12C68-5.

During normal operation, the device draws current from V<sub>CC</sub> to charge a capacitor connected to the V<sub>CAP</sub> pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V<sub>CC</sub> pin drops below V<sub>SWITCH</sub>, the part automatically disconnects the V<sub>CAP</sub> pin from V<sub>CC</sub>. A STORE operation is initiated with power provided by the V<sub>CAP</sub> capacitor.

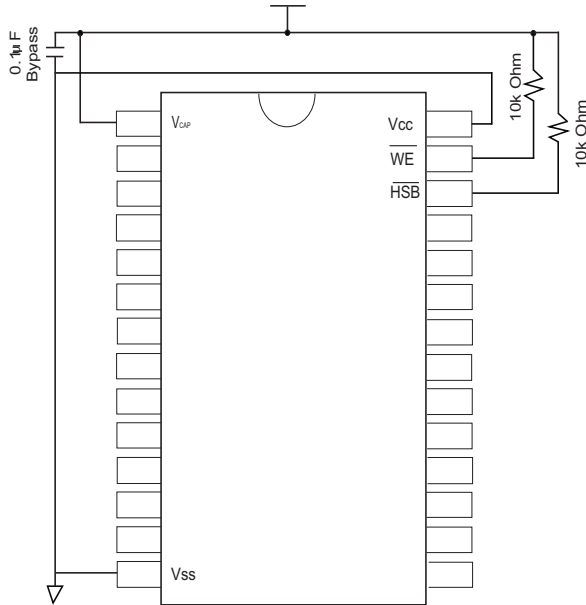
Figure 3 shows the proper connection of the storage capacitor (V<sub>CAP</sub>) for automatic store operation. A charge storage capacitor between 68 μF and 220 μF (±20%) rated at 6V must be provided. The voltage on the V<sub>CAP</sub> pin is driven to 5V by a charge pump internal to the chip. A pull up is placed on WE to hold it inactive during power up.

Figure 3. AutoStore Mode



In system power mode, both V<sub>CC</sub> and V<sub>CAP</sub> are connected to the +5V power supply without the 68 μF capacitor. In this mode, the AutoStore function of the STK12C68-5 operates on the stored system charge as power goes down. The user must, however, guarantee that V<sub>CC</sub> does not drop below 3.6V during the 10 ms STORE cycle.

To reduce unnecessary nonvolatile stores, AutoStore, and Hardware Store operations are ignored, unless at least one Write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a Write operation has taken place. An optional pull up resistor is shown connected to HSB. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.

**Figure 4. AutoStore Inhibit Mode**


If the power supply drops faster than 20 us/volt before  $V_{CC}$  reaches  $V_{SWITCH}$ , then a 2.2 ohm resistor must be connected between  $V_{CC}$  and the system supply to avoid momentary excess of current between  $V_{CC}$  and  $V_{CAP}$ .

### AutoStore Inhibit Mode

If an automatic STORE on power loss is not required, then  $V_{CC}$  is tied to ground and +5V is applied to  $V_{CAP}$  (Figure 4). This is the AutoStore Inhibit mode, where the AutoStore function is disabled. If the STK12C68-5 is operated in this configuration, references to  $V_{CC}$  are changed to  $V_{CAP}$  throughout this data sheet. In this mode, STORE operations are triggered through software control or the HSB pin. To enable or disable Autostore using an IO port pin see [Preventing Store](#) on page 5. It is not permissible to change between these three options “on the fly”.

### Hardware STORE (HSB) Operation

The STK12C68-5 provides the  $\overline{HSB}$  pin for controlling and acknowledging the STORE operations. The HSB pin is used to request a hardware STORE cycle. When the HSB pin is driven LOW, the STK12C68-5 conditionally initiates a STORE operation after  $t_{DELAY}$ . An actual STORE cycle only begins if a Write to the SRAM takes place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress.

SRAM Read and Write operations, that are in progress when HSB is driven LOW by any means, are given time to complete before the STORE operation is initiated. After HSB goes LOW, the STK12C68-5 continues SRAM operations for  $t_{DELAY}$ . During  $t_{DELAY}$ , multiple SRAM Read operations take place. If a Write is in progress when HSB is pulled LOW, it allows a time,  $t_{DELAY}$  to complete. However, any SRAM Write cycles requested after HSB goes LOW are inhibited until HSB returns HIGH.

During any STORE operation, regardless of how it is initiated, the STK12C68-5 continues to drive the HSB pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the STK12C68-5 remains disabled until the HSB pin returns HIGH.

If  $\overline{HSB}$  is not used, it is left unconnected.

### Hardware RECALL (Power Up)

During power up or after any low power condition ( $V_{CC} < V_{RESET}$ ), an internal RECALL request is latched. When  $V_{CC}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a RECALL cycle is automatically initiated and takes  $t_{HRECALL}$  to complete.

If the STK12C68-5 is in a Write state at the end of power up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 Kohm resistor is connected either between WE and system  $V_{CC}$  or between CE and system  $V_{CC}$ .

### Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK12C68-5 software STORE cycle is initiated by executing sequential CE controlled Read cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of Reads from specific addresses is used for STORE initiation, it is important that no other Read or Write accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following Read sequence is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0F, Initiate STORE cycle

The software sequence is clocked with  $\overline{CE}$  controlled Reads or  $\overline{OE}$  controlled Reads. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that Read cycles and not Write cycles are used in the sequence. It is not necessary that  $\overline{OE}$  is LOW for a valid sequence. After the  $t_{STORE}$  cycle time is fulfilled, the SRAM is again activated for Read and Write operation.

### Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of Read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of  $\overline{CE}$  controlled Read operations is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ

4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0E, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time, the SRAM is again ready for Read and Write operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

## Data Protection

The STK12C68-5 protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and Write operations. The low voltage condition is detected when  $V_{CC}$  is less than  $V_{SWITCH}$ . If the STK12C68-5 is in a Write mode (both CE and WE are low) at power up after a RECALL or after a STORE, the Write is inhibited until a negative transition on CE or WE is detected. This protects against inadvertent writes during power up or brown out conditions.

## Noise Considerations

The STK12C68-5 is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1  $\mu\text{F}$  connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

## Hardware Protect

The STK12C68-5 offers hardware protection against inadvertent STORE operation and SRAM Writes during low voltage conditions. When  $V_{CAP} < V_{SWITCH}$ , all externally initiated STORE operations and SRAM Writes are inhibited. AutoStore can be completely disabled by tying  $V_{CC}$  to ground and applying +5V to  $V_{CAP}$ . This is the AutoStore Inhibit mode; in this mode, STORES are only initiated by explicit request using either the software sequence or the HSB pin.

## Low Average Active Power

CMOS technology provides the STK12C68-5 the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 5 and Figure 6 shows the relationship between  $I_{CC}$  and Read or Write cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{CC} = 5.5\text{V}$ , 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK12C68-5 depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of Reads to Writes
- CMOS versus TTL input levels
- The operating temperature
- The  $V_{CC}$  level

Figure 5. Current Versus Cycle Time (Read)

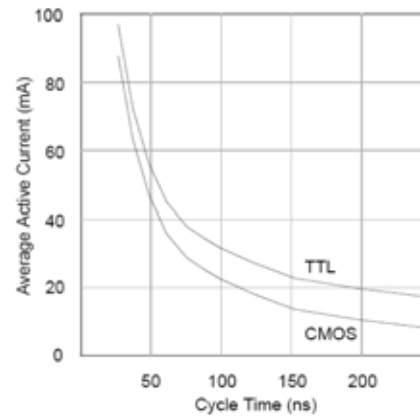
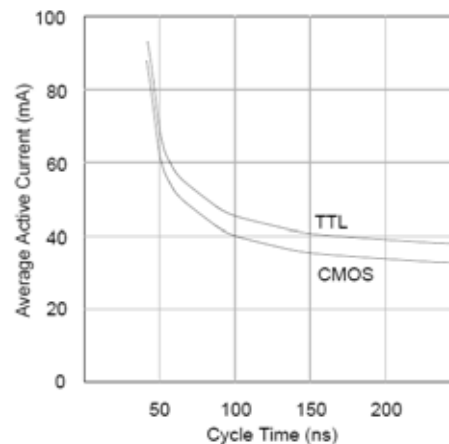


Figure 6. Current Versus Cycle Time (Write)



## Preventing Store

The STORE function is disabled by holding  $\overline{HSB}$  high with a driver capable of sourcing 30 mA at a  $V_{OH}$  of at least 2.2V, because it must overpower the internal pull down device. This device drives  $\overline{HSB}$  LOW for 20  $\mu\text{s}$  at the onset of a STORE. When the STK12C68-5 is connected for AutoStore operation (system  $V_{CC}$  connected to  $V_{CC}$  and a 68  $\mu\text{F}$  capacitor on  $V_{CAP}$ ) and  $V_{CC}$  crosses  $V_{SWITCH}$  on the way down, the STK12C68-5 attempts to pull  $\overline{HSB}$  LOW. If  $\overline{HSB}$  does not actually get below  $V_{IL}$ , the part stops trying to pull  $\overline{HSB}$  LOW and abort the STORE attempt.

## Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprograms these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware must not assume that an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.

- Power up boot firmware routines must rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- The Vcap value specified in this data sheet includes a minimum and a maximum value size. The best practice is to meet this requirement and not exceed the maximum Vcap value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers who want to use a larger Vcap value to make sure there is extra store charge must discuss their Vcap size selection with Cypress.

**Table 1. Hardware Mode Selection**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{HSB}}$	A12–A0	Mode	IO	Power
H	X	H	X	Not Selected	Output High Z	Standby
L	H	H	X	Read SRAM	Output Data	Active <sup>[3]</sup>
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High Z	$I_{CC2}$ <sup>[1]</sup>
L	H	H	0x0000 0x1555 0x0AAA 0x1FFF 0x10F0 0x0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active $I_{CC2}$ <sup>[2, 3]</sup>
L	H	H	0x0000 0x1555 0x0AAA 0x1FFF 0x10F0 0x0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active <sup>[2, 3]</sup>

### Notes

1. HSB STORE operation occurs only if an SRAM Write is done since the last nonvolatile cycle. After the STORE (if any) completes, the part goes into standby mode, inhibiting all operations until HSB rises.
2. The six consecutive addresses must be in the order listed.  $\overline{\text{WE}}$  must be high during all six consecutive  $\overline{\text{CE}}$  controlled cycles to enable a nonvolatile cycle.
3. IO state assumes  $\text{OE} \leq V_{IL}$ . Activation of nonvolatile cycles does not depend on state of OE.



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C  
 Temperature under Bias ..... -55°C to +125°C  
 Voltage on Input Relative to GND.....-0.5V to 7.0V  
 Voltage on Input Relative to Vss.....-0.6V to  $V_{CC} + 0.5V$

Voltage on  $DQ_{0-7}$  or  $\overline{HSB}$  .....-0.5V to  $V_{CC} + 0.5V$   
 Power Dissipation..... 1.0W  
 DC output Current (1 output at a time, 1s duration) .... 15 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Military	-55°C to +125°C	4.5V to 5.5V

## DC Electrical Characteristics

Over the operating range ( $V_{CC} = 4.5V$  to  $5.5V$ ) [4]

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{CC1}$	Average $V_{CC}$ Current	$t_{RC} = 35$ ns $t_{RC} = 55$ ns Dependent on output loading and cycle rate. Values obtained without output loads. $I_{OUT} = 0$ mA.		75 55	mA mA
$I_{CC2}$	Average $V_{CC}$ Current during STORE	All Inputs Do Not Care, $V_{CC} = \text{Max}$ Average current for duration $t_{STORE}$		3	mA
$I_{CC3}$	Average $V_{CC}$ Current at $t_{RC} = 200$ ns, 5V, 25°C Typical	$WE \geq (V_{CC} - 0.2V)$ . All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.		10	mA
$I_{CC4}$	Average $V_{CAP}$ Current during AutoStore Cycle	All Inputs Do Not Care, $V_{CC} = \text{Max}$ Average current for duration $t_{STORE}$		2	mA
$I_{SB1}$ [5]	$V_{CC}$ Standby Current (Standby, Cycling TTL Input Levels)	$t_{RC} = 35$ ns, $\overline{CE} \geq V_{IH}$ $t_{RC} = 55$ ns, $\overline{CE} \geq V_{IH}$		24 19	mA mA
$I_{SB2}$ [5]	$V_{CC}$ Standby Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ . All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ . Standby current level after nonvolatile cycle is complete. Inputs are static. $f = 0$ MHz.		2.5	mA
$I_{IX}$	Input Leakage Current	$V_{CC} = \text{Max}$ , $V_{SS} \leq V_{IN} \leq V_{CC}$	-1	+1	$\mu A$
$I_{OZ}$	Off State Output Leakage Current	$V_{CC} = \text{Max}$ , $V_{SS} \leq V_{IN} \leq V_{CC}$ , $\overline{CE}$ or $OE \geq V_{IH}$ or $WE \leq V_{IL}$	-5	+5	$\mu A$
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage		$V_{SS} - 0.5$	0.8	V
$V_{OH}$	Output HIGH Voltage	$I_{OUT} = -4$ mA	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OUT} = 8$ mA		0.4	V
$V_{BL}$	Logic '0' Voltage on $\overline{HSB}$ Output	$I_{OUT} = 3$ mA		0.4	V
$V_{CAP}$	Storage Capacitor	Between Vcap pin and Vss, 6V rated. 68 $\mu F \pm 20\%$ nom.	54	260	$\mu F$

### Notes

- $V_{CC}$  reference levels throughout this data sheet refer to  $V_{CC}$  if that is where the power supply connection is made, or  $V_{CAP}$  if  $V_{CC}$  is connected to ground.
- $\overline{CE} \geq V_{IH}$  does not produce standby current levels until any nonvolatile cycle in progress has timed out.

**Data Retention and Endurance**

Parameter	Description	Min	Unit
DATA <sub>R</sub>	Data Retention	100	Years
NV <sub>C</sub>	Nonvolatile STORE Operations	1,000	K

**Capacitance**

In the following table, the capacitance parameters are listed.<sup>[6]</sup>

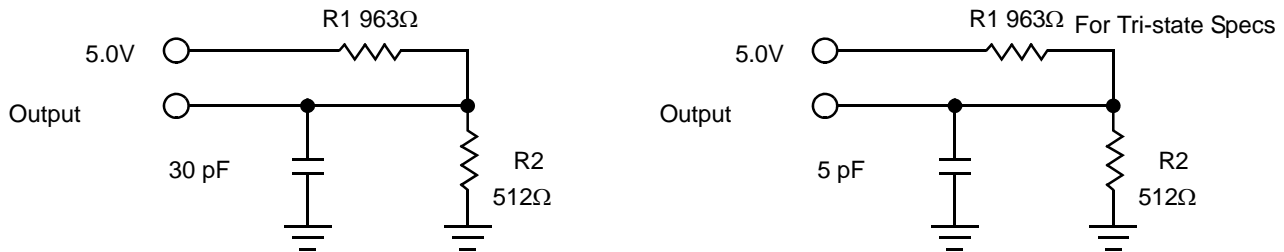
Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 0 to 3.0 V	8	pF
C <sub>OUT</sub>	Output Capacitance		7	pF

**Thermal Resistance**

In the following table, the thermal resistance parameters are listed.<sup>[6]</sup>

Parameter	Description	Test Conditions	28-CDIP	28-LCC	Unit
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	TBD	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

Figure 7. AC Test Loads



**AC Test Conditions**

Input Pulse Levels ..... 0V to 3V  
 Input Rise and Fall Times (10% to 90%) ..... ≤5 ns  
 Input and Output Timing Reference Levels ..... 1.5

**Note**

6. These parameters are guaranteed by design and are not tested.



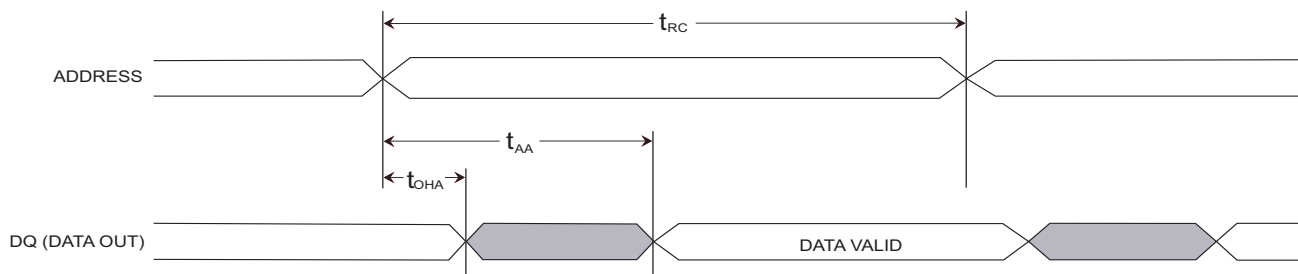
## AC Switching Characteristics

### SRAM Read Cycle

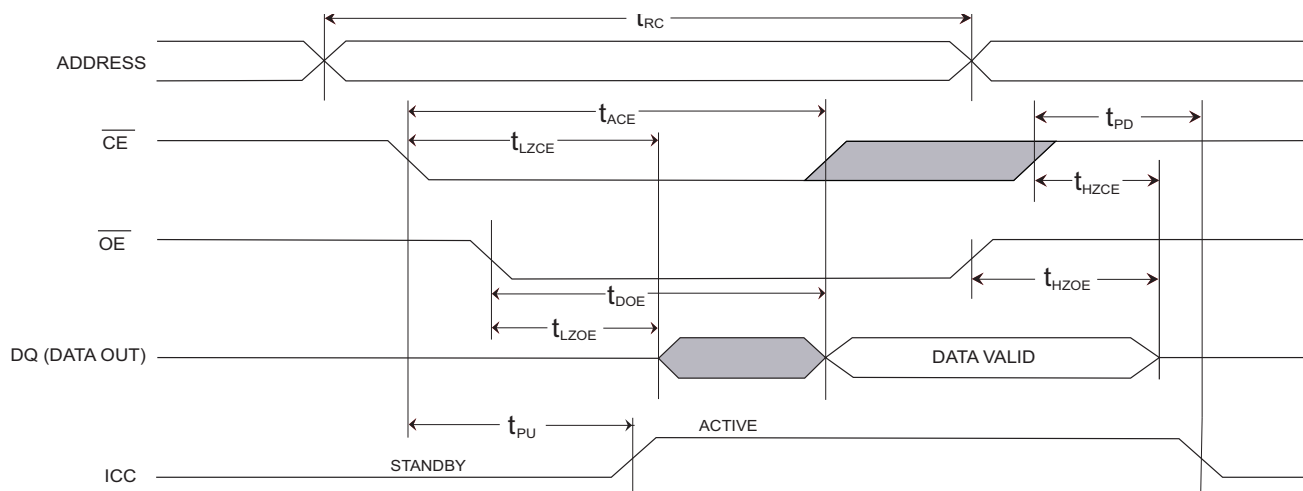
Parameter		Description	35 ns		55 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
$t_{ACE}$	$t_{ELQV}$	Chip Enable Access Time		35		55	ns
$t_{RC}^{[7]}$	$t_{AVAV}, t_{ELEH}$	Read Cycle Time	35		55		ns
$t_{AA}^{[8]}$	$t_{AVQV}$	Address Access Time		35		55	ns
$t_{DOE}$	$t_{GLQV}$	Output Enable to Data Valid		15		35	ns
$t_{OHA}^{[8]}$	$t_{AXQX}$	Output Hold After Address Change	5		5		ns
$t_{LZCE}^{[9]}$	$t_{ELQX}$	Chip Enable to Output Active	5		5		ns
$t_{HZCE}^{[9]}$	$t_{EHQZ}$	Chip Disable to Output Inactive		10		12	ns
$t_{LZOE}^{[9]}$	$t_{GLQX}$	Output Enable to Output Active	0		0		ns
$t_{HZOE}^{[9]}$	$t_{GHQZ}$	Output Disable to Output Inactive		10		12	ns
$t_{PU}^{[6]}$	$t_{ELICCH}$	Chip Enable to Power Active	0		0		ns
$t_{PD}^{[6]}$	$t_{EHICCL}$	Chip Disable to Power Standby		35		55	ns

### Switching Waveforms

**Figure 8. SRAM Read Cycle 1: Address Controlled** <sup>[7, 8]</sup>



**Figure 9. SRAM Read Cycle 2:  $\overline{CE}$  and  $\overline{OE}$  Controlled** <sup>[7]</sup>

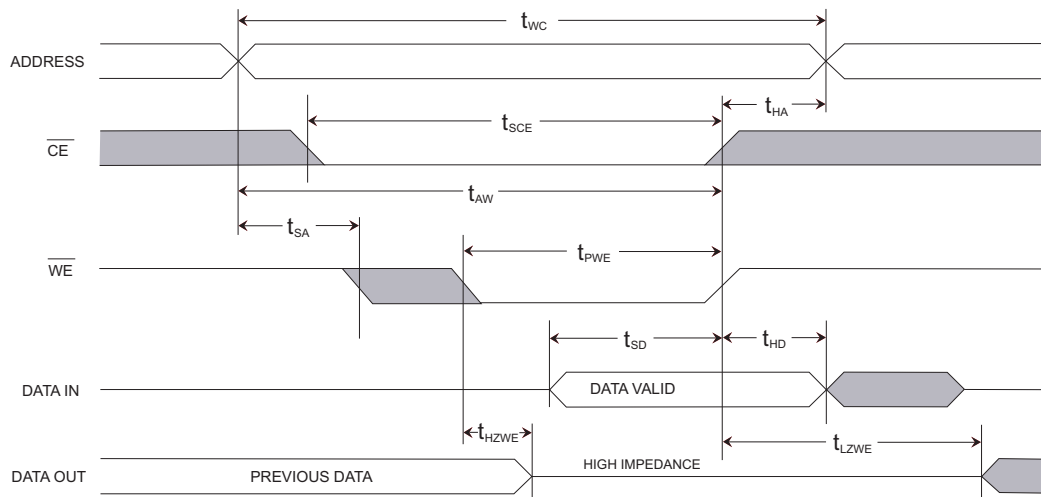
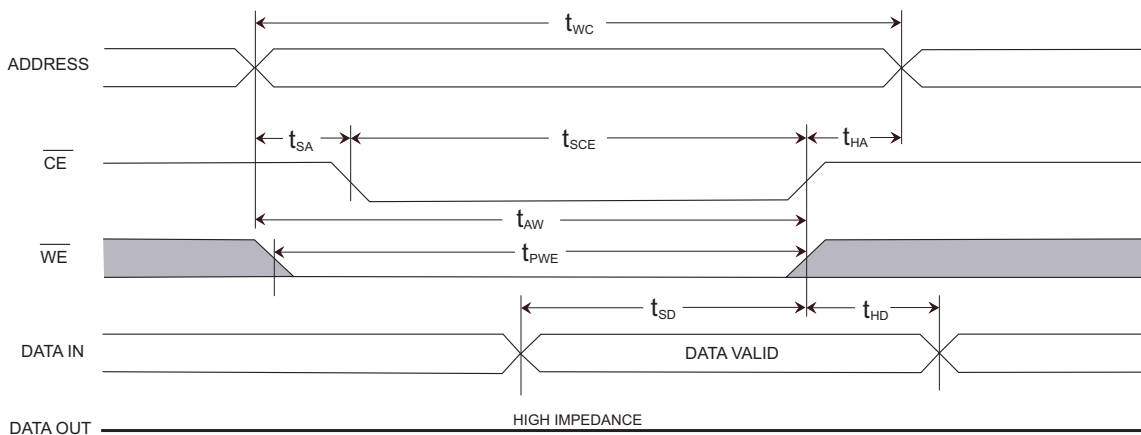


#### Notes

7.  $\overline{WE}$  and  $\overline{HSB}$  must be High during SRAM Read cycles.
8. Device is continuously selected with  $\overline{CE}$  and  $\overline{OE}$  both Low.
9. Measured  $\pm 200$  mV from steady state output voltage.

**SRAM Write Cycle**

Parameter		Description	35 ns		55 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
$t_{WC}$	$t_{AVAV}$	Write Cycle Time	35		55		ns
$t_{PWE}$	$t_{WLWH}, t_{WLEH}$	Write Pulse Width	25		45		ns
$t_{SCE}$	$t_{ELWH}, t_{ELEH}$	Chip Enable To End of Write	25		45		ns
$t_{SD}$	$t_{DVWH}, t_{DVEH}$	Data Setup to End of Write	12		25		ns
$t_{HD}$	$t_{WHDX}, t_{EHDX}$	Data Hold After End of Write	0		0		ns
$t_{AW}$	$t_{AVWH}, t_{AVEH}$	Address Setup to End of Write	25		45		ns
$t_{SA}$	$t_{AVWL}, t_{AVEH}$	Address Setup to Start of Write	0		0		ns
$t_{HA}$	$t_{WHAX}, t_{EHAX}$	Address Hold After End of Write	0		0		ns
$t_{HZWE}^{[9,10]}$	$t_{WLQZ}$	Write Enable to Output Disable		13		15	ns
$t_{LZWE}^{[9]}$	$t_{WHQX}$	Output Active After End of Write	5		5		ns

**Switching Waveforms**
**Figure 10. SRAM Write Cycle 1:  $\overline{WE}$  Controlled** <sup>[11, 12]</sup>

**Figure 11. SRAM Write Cycle 2:  $\overline{CE}$  Controlled** <sup>[11, 12]</sup>

**Notes**

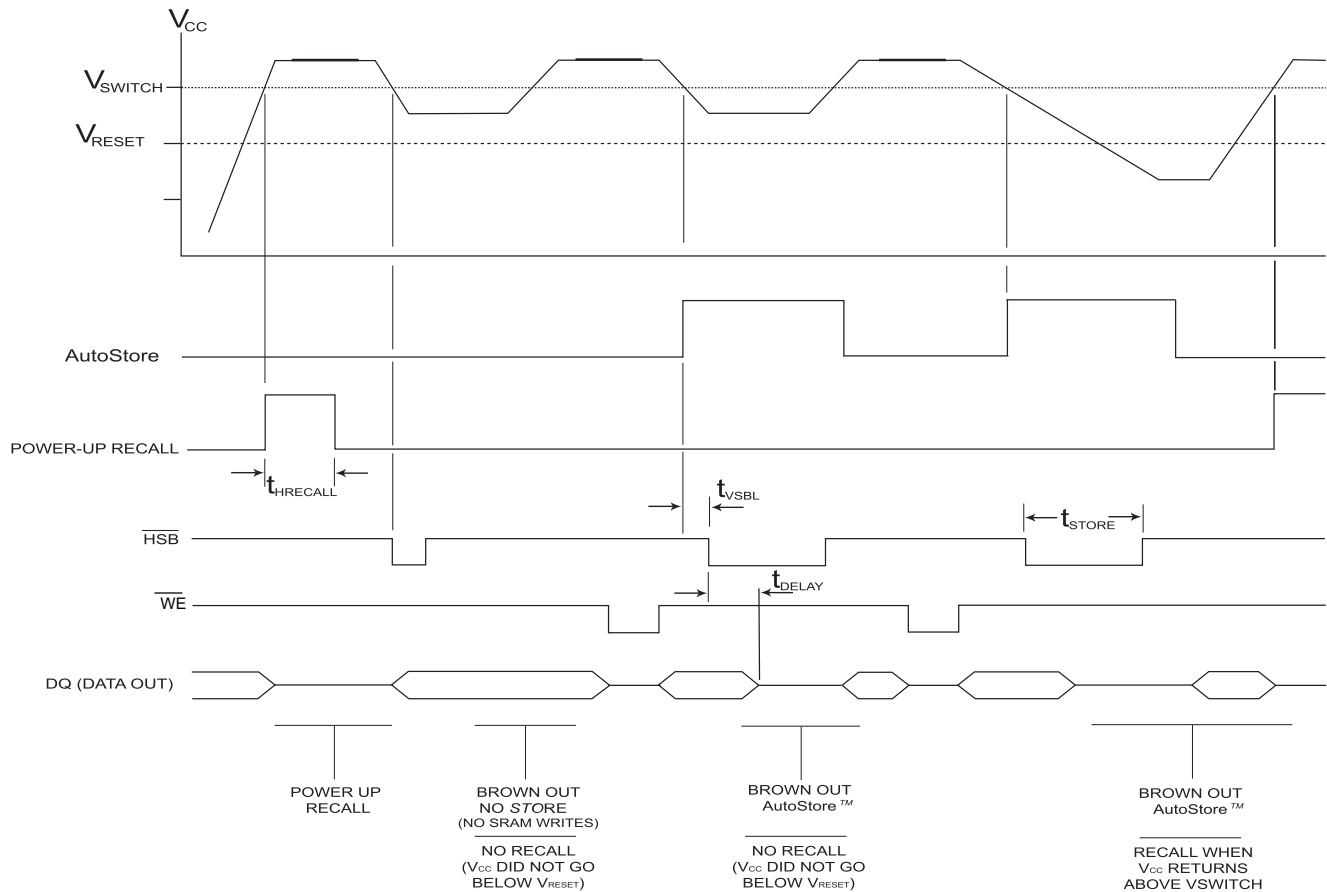
10. If  $\overline{WE}$  is Low when  $\overline{CE}$  goes Low, the outputs remain in the high impedance state.
11. HSB must be high during SRAM Write cycles.
12.  $\overline{CE}$  or  $\overline{WE}$  must be greater than  $V_{IH}$  during address transitions.

### AutoStore or Power Up RECALL

Parameter	Alt	Description	STK12C68-5		Unit
			Min	Max	
$t_{HRECALL}$ [13]	$t_{RESTORE}$	Power up RECALL Duration		550	$\mu$ s
$t_{STORE}$ [14, 15, 16]	$t_{HLHZ}$	STORE Cycle Duration		10	ms
$t_{DELAY}$ [9, 15]	$t_{HLQZ}$ , $t_{BLQZ}$	Time Allowed to Complete SRAM Cycle	1		$\mu$ s
$V_{SWITCH}$		Low Voltage Trigger Level	4.0	4.5	V
$V_{RESET}$		Low Voltage Reset Level		3.9	V
$t_{VCCRISE}$		$V_{CC}$ Rise Time	150		$\mu$ s
$t_{VSBL}$ [11]		Low Voltage Trigger ( $V_{SWITCH}$ ) to HSB Low		300	ns

### Switching Waveform

Figure 12. AutoStore/Power Up RECALL



#### Notes

13.  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .
14.  $\overline{CE}$  and  $\overline{OE}$  low for output behavior.
15.  $\overline{CE}$  and  $\overline{OE}$  low and  $\overline{WE}$  high for output behavior.
16.  $\overline{HSB}$  is asserted low for 1us when  $V_{CAP}$  drops through  $V_{SWITCH}$ . If an SRAM Write has not taken place since the last nonvolatile cycle,  $\overline{HSB}$  is released and no store takes place.

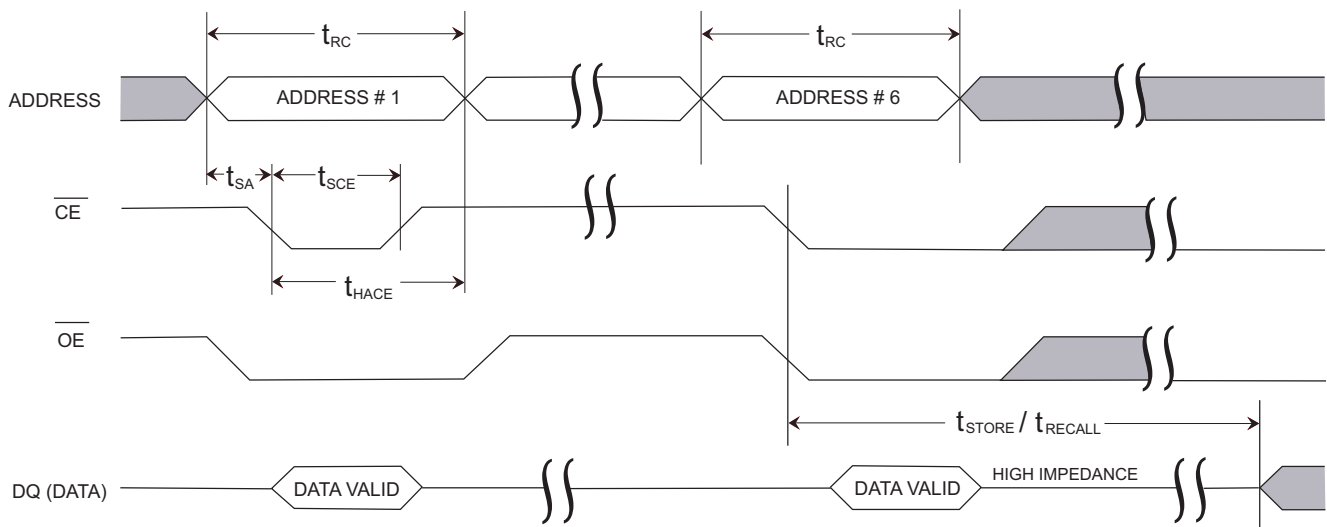
### Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. <sup>[18]</sup>

Parameter	Alt	Description	35 ns		55 ns		Unit
			Min	Max	Min	Max	
$t_{RC}^{[14]}$	$t_{AVAV}$	STORE/RECALL Initiation Cycle Time	35		55		ns
$t_{SA}^{[17]}$	$t_{AVEL}$	Address Setup Time	0		0		ns
$t_{CW}^{[17]}$	$t_{ELEH}$	Clock Pulse Width	25		30		ns
$t_{HACE}^{[17]}$	$t_{ELAX}$	Address Hold Time	20		20		ns
$t_{RECALL}$		RECALL Duration		20		20	$\mu$ s

### Switching Waveform

Figure 13.  $\overline{CE}$  Controlled Software STORE/RECALL Cycle <sup>[18]</sup>



#### Notes

17. The software sequence is clocked on the falling edge of  $\overline{CE}$  without involving  $\overline{OE}$  (double clocking aborts the sequence).

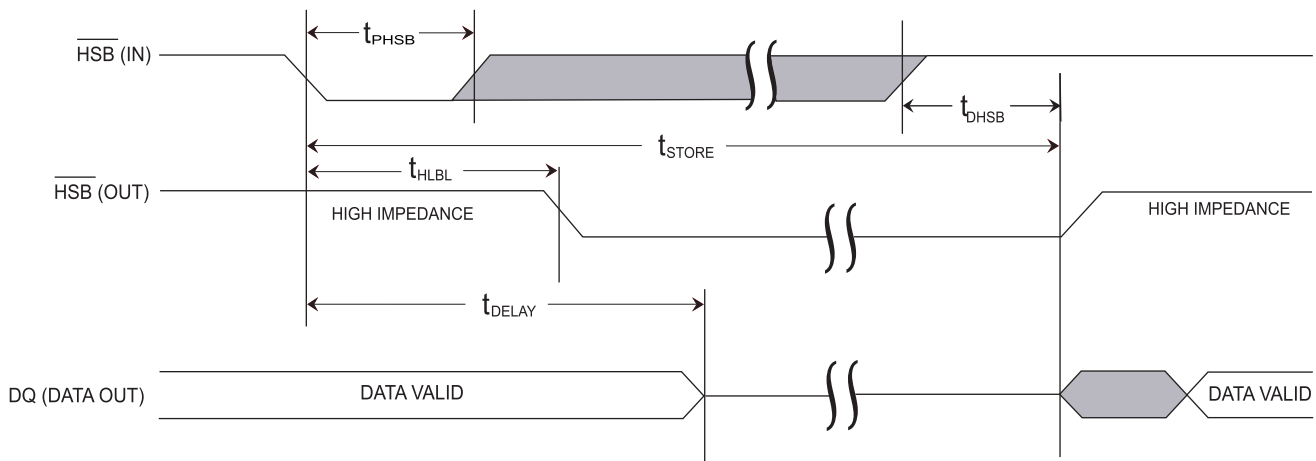
18. The six consecutive addresses must be read in the order listed in Table 1 on page 6.  $\overline{WE}$  must be HIGH during all six consecutive cycles.

### Hardware STORE Cycle

Parameter	Alt	Description	STK12C68-5		Unit
			Min	Max	
$t_{STORE}^{[9, 14]}$	$t_{HLHZ}$	STORE Cycle Duration		10	ms
$t_{DHSB}^{[14, 19]}$	$t_{RECOVER}, t_{HHQX}$	Hardware STORE High to Inhibit Off		700	ns
$t_{PHSB}$	$t_{HLHX}$	Hardware STORE Pulse Width	15		ns
$t_{HLBL}$		Hardware STORE Low to STORE Busy		300	ns

### Switching Waveform

Figure 14. Hardware STORE Cycle

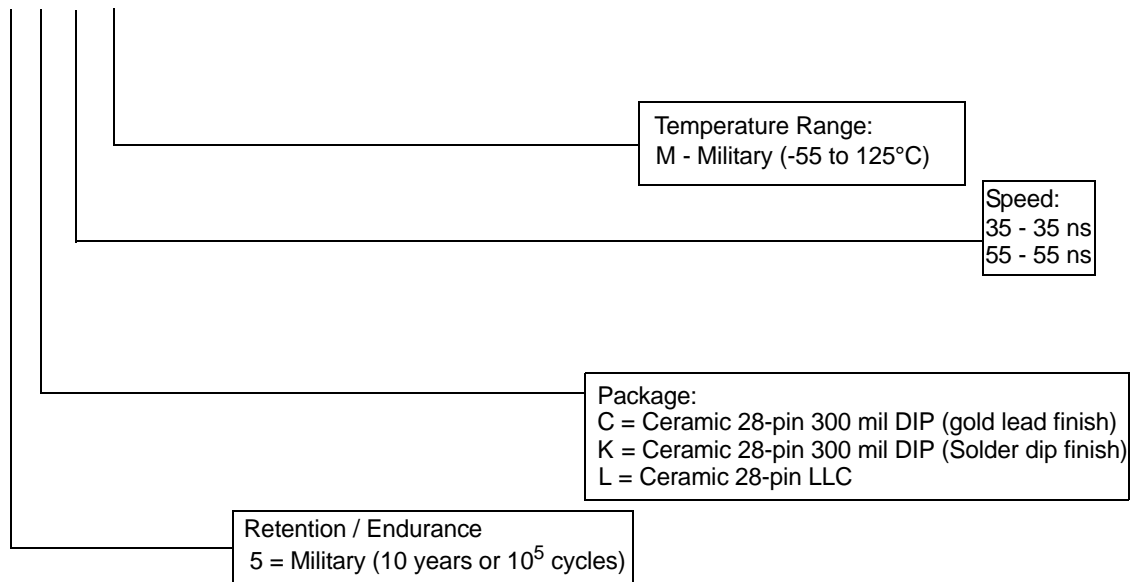


**Note**

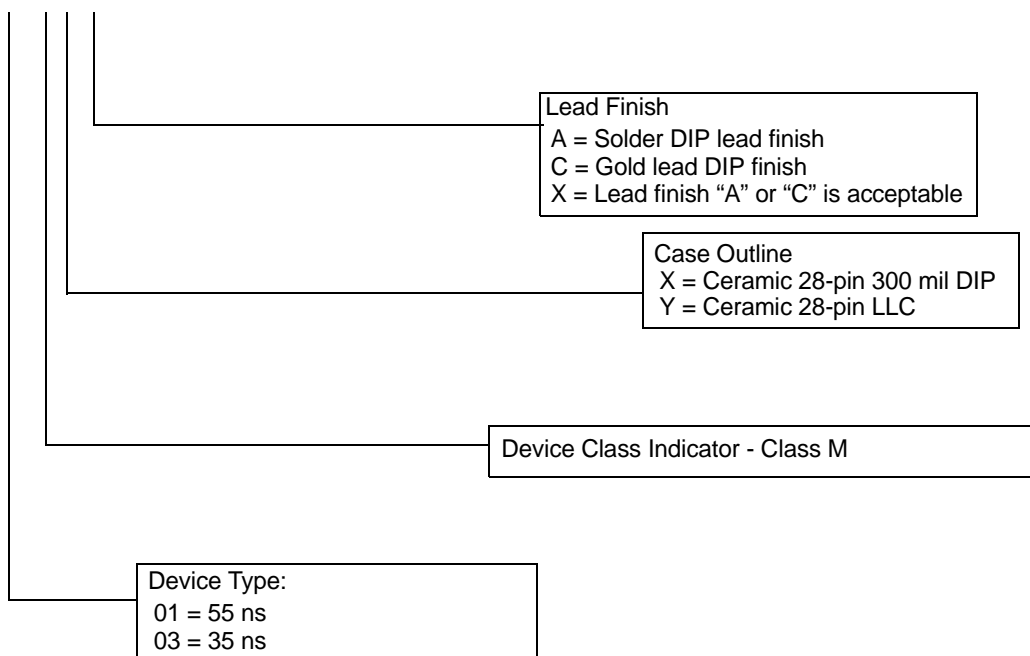
19.  $t_{DHSB}$  is only applicable after  $t_{STORE}$  is complete.

**Part Numbering Nomenclature**

**STK12C68 - 5 C 35 M**



**SMD5962 - 94599 01 MX X**





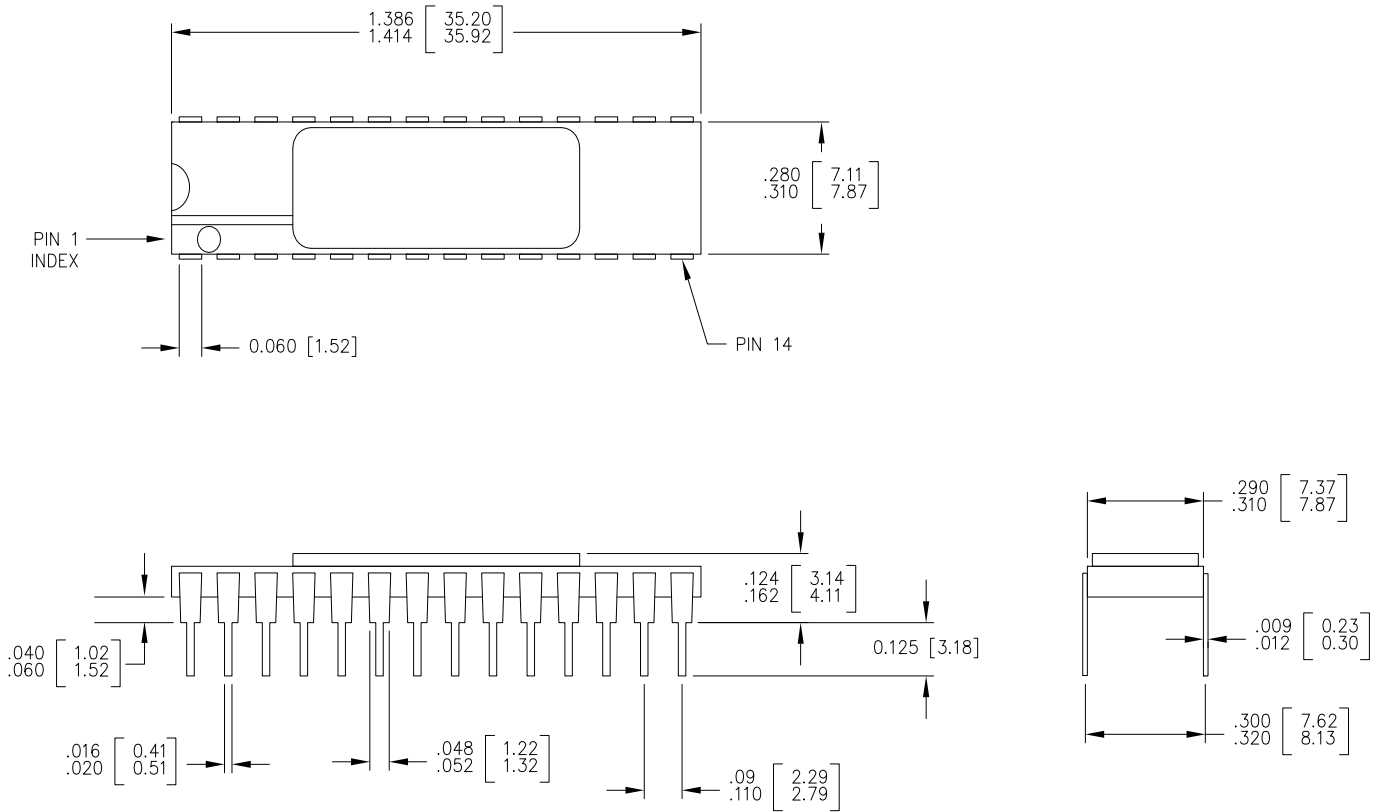
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
35	STK12C68-5C35M	001-51695	28-pin CDIP (300 mil)	Military
	STK12C68-5K35M	001-51695	28-pin CDIP (300 mil)	
	STK12C68-5L35M	001-51696	28-pin LCC (350 mil)	
55	STK12C68-5C55M	001-51695	28-pin CDIP (300 mil)	
	STK12C68-5K55M	001-51695	28-pin CDIP (300 mil)	
	STK12C68-5L55M	001-51696	28-pin LCC (350 mil)	

The above table contains Final information. Contact your local Cypress sales representative for availability of these parts

**Package Diagrams**

**Figure 15. 28-Pin (300-Mil) Side Braze DIL (001-51695)**

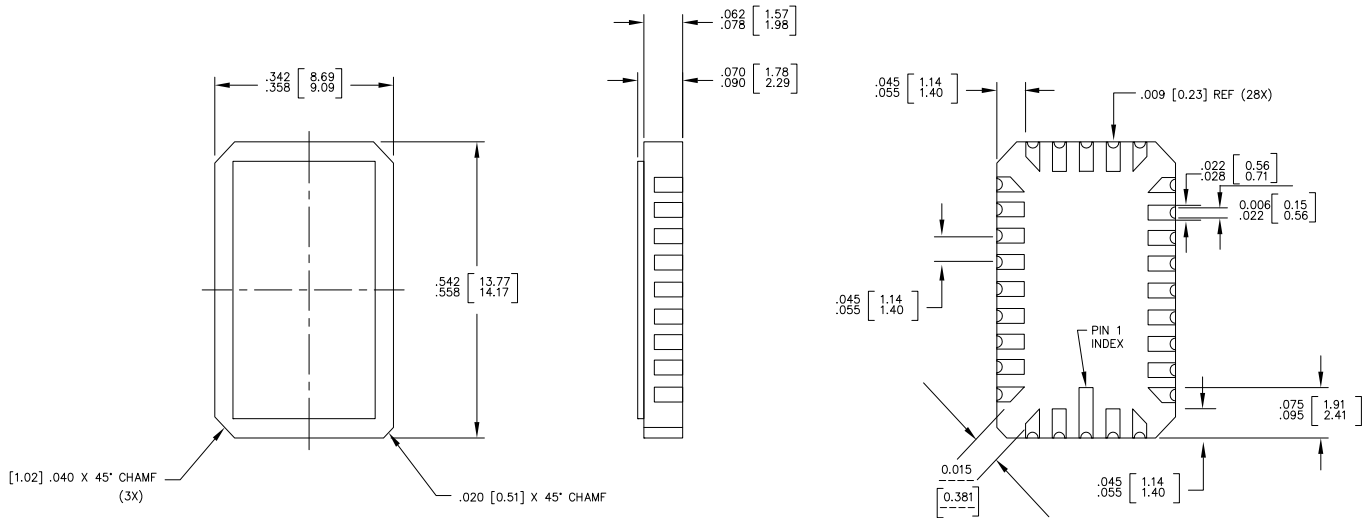


1. ALL DIMENSIONS ARE IN MILLIMETERS AND INCHS [MIN/MAX]
2. PACKAGE WEIGHT : TBD
3. JEDEC REFERENCE : MO-058

001-51695 \*\*

## Package Diagrams (continued)

Figure 16. 28-Pad (350-Mil) LCC (001-51696)



- 1. ALL DIMENSION ARE IN INCHES AND MILLIMETERS [MIN/MAX]
- 2. JEDEC 95 OUTLINE# MO-041
- 3. PACKAGE WEIGHT : TBD

001-51696 \*\*

**Document History Page**

<b>Document Title: STK12C68-5 (SMD5962-94599), 64 Kbit (8K x 8) AutoStore nvSRAM</b>				
<b>Document Number: 001-51026</b>				
Rev	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2666844	GVCH/PYRS	03/02/09	New data sheet

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