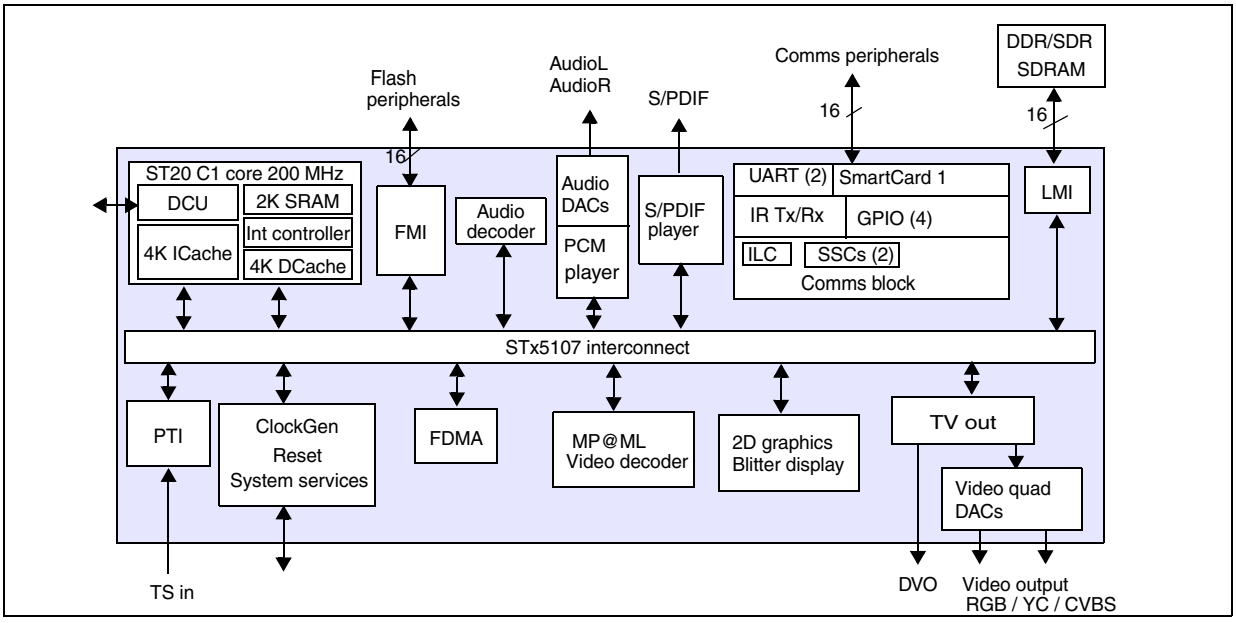
STi5107

Low-cost interactive set-top box decoder

Data Brief

Features

- Enhanced ST20 32-bit VL-RISC CPU
- Unified memory interface
  - up to166 MHz,16-bit wide SDR/DDR SDRAM interface
- Programmable flash memory interface
- Programmable transport interface (PTI)
  - single transport stream input
  - support for DVB transport streams
- MPEG-2 MP@ML video decoder
- Graphics and display
  - 3 display planes
  - 8 bpp CLUT graphics
  - 2D paced blitter engine with fill function
  - digital video output: compliant with CCIR 601/CCIR 656
- PAL/NTSC/SECAM encoder
  - RGB, CVBS, Y/C and YUV outputs with four 10-bit DAC outputs.
  - encoding of CGMS, Teletext, WSS, VPS, close caption
- Audio subsystem
  - simultaneous MPEG audio decode and output of Dolby streams on S/PDIF
  - IEC958/IEC1937 digital audio output interface
  - integrated stereo audio DAC system
- Central DMA controller
- On-chip peripherals
  - 2 ASCs (UARTs) with Tx and Rx FIFOs
  - 3 banks of 8-bit and 1 bank of 7-bit parallel I/O
  - 1 smartcard interface and clock generator
  - infrared transmitter/receiver
  - integrated VCXO
- Advanced security ready
- JTAG/TAP interface
- Package
  - 23 mm x 23mm PBGA32
  - 24 mm x 24 mm LQFP216



1 Description

1.1 General

The STi5107 is the latest in the family of Omega2 set-top box ICs providing a high-performance, low-cost system-on-chip(SoC) for MPEG processing in cable, satellite or digital terrestrial STBs. It is a pin compatible IC derived from the STx5105, that supports multiple platform using a unified architecture. STi5107 is compatible with the latest CA advanced security specifications.

The STi5107 delivers enhanced performance with respect to previous devices. Main memory is based upon a single 16-bit external SDR/DDR SDRAM.

The display architecture of the device is based upon a high performance blitter engine that supports CLUT8 and RGB16 formats for background, video and OSD/graphics displays. It makes the porting of middleware easier with greater rendering.

1.2 Applications

Typical applications are shown in the *Figure 1*, *Figure 2* and *Figure 3*.

Figure 1. Basic terrestrial pay TV

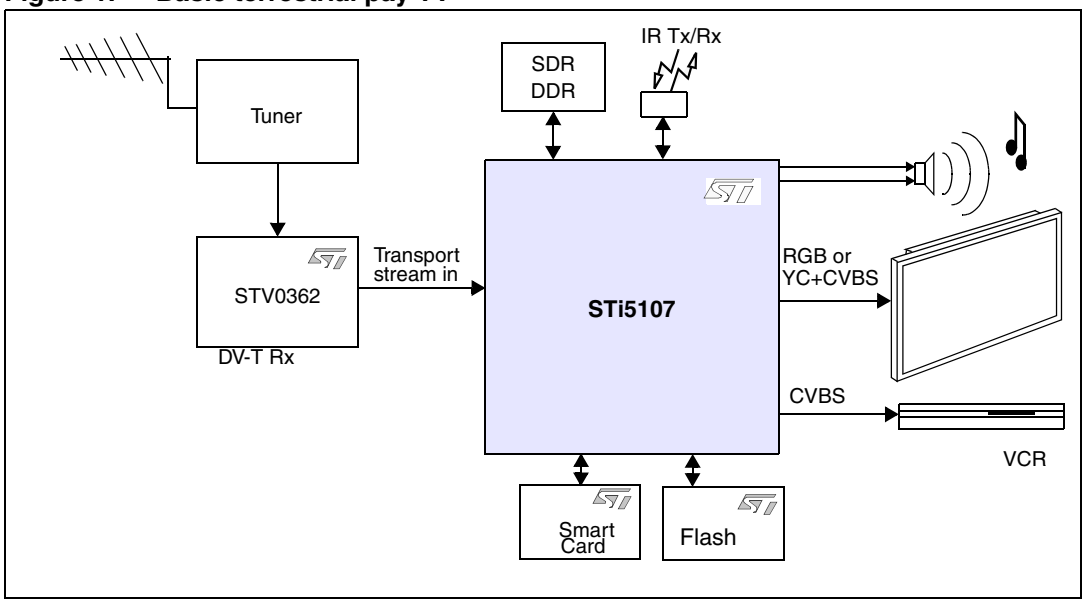


Figure 2. Basic satellite pay TV receiver

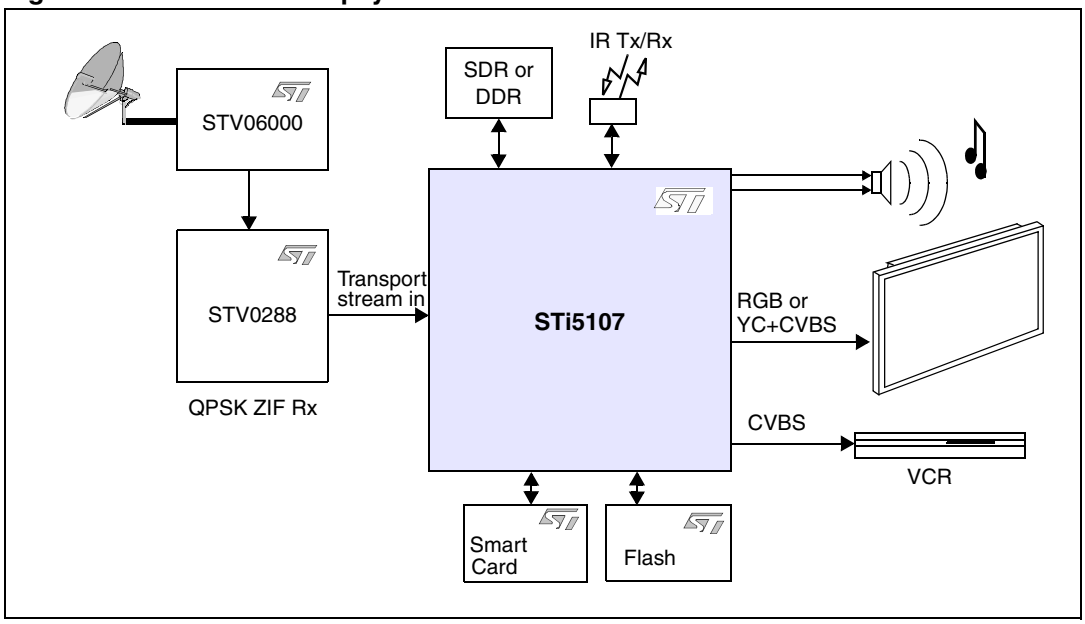
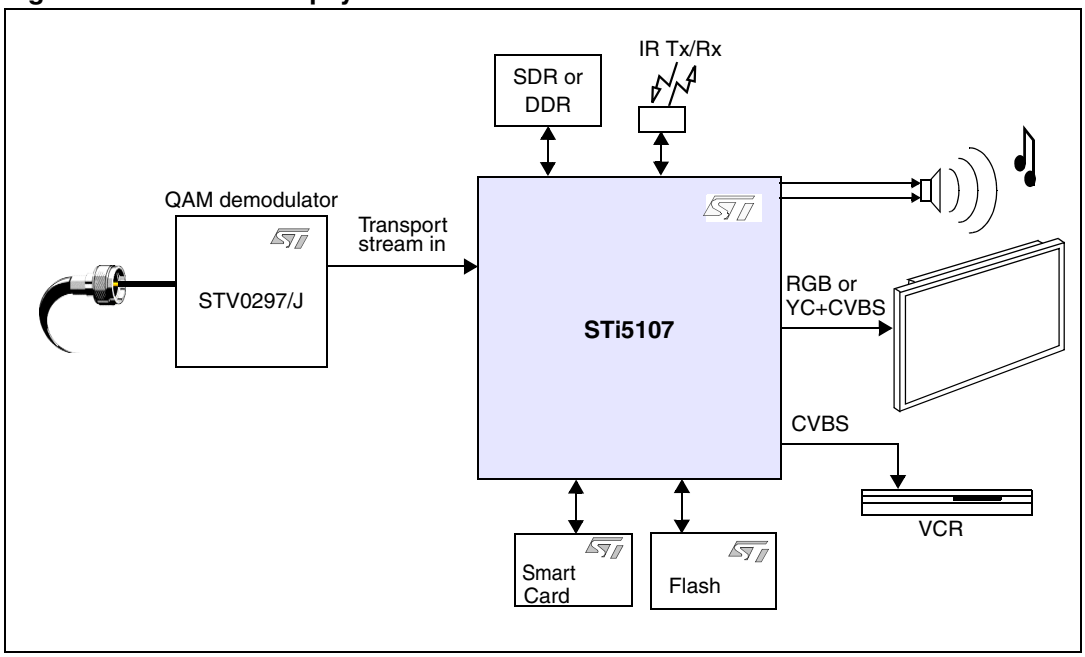


Figure 3. Basic cable pay TV receiver



1.3 Main features

- Enhanced ST20 32-bit VL-RISC CPU
  - 200 MHz, single cycle cache/4-Kbyte instruction cache, 4 Kbyte data cache, 2 Kbyte SRAM
- Unified memory interface
  - up to166 MHz,16-bit wide SDR/DDR SDRAM interface
- Programmable flash memory interface
  - 4 separately configurable banks, 8/16-bits wide
  - SRAM, peripheral, flash, SFlash™ support
  - support for low cost DVB-CI
- Programmable transport interface (PTI)
  - single transport stream input
  - support for DVB transport streams
  - integrated DVB, ICAM descramblers
- MPEG-2 MP@ML video decoder
  - fully programmable horizontal and vertical SRCs
- Graphics and display
  - 3 display planes
  - 8 bpp CLUT graphics, 256 x 30 bits (AYCbCr) CLUT entries. 16 bpp true color graphics, RGB565, ARGB1555, ARGB4444 formats. Link-list control
  - alpha blending, antialiasing, antiflutter, antiflicker filters
  - 2D paced blitter engine with fill function
  - blitter based display compositor
  - digital video output: compliant with CCIR 601/CCIR 656
- PAL/NTSC/SECAM encoder
  - RGB, CVBS, Y/C and YUV outputs with four 10-bit DAC outputs. RGB/CVBS or YUV/CVBS or YC/CVBS
  - encoding of CGMS, Teletext, WSS, VPS, close caption
- Audio subsystem
  - MPEG-1 layers I/II
  - simultaneous MPEG audio decode and output of Dolby streams on S/PDIF
  - IEC958/IEC1937 digital audio output interface
  - integrated stereo audio DAC system
- Central DMA controller
- On-chip peripherals
  - 2 ASCs (UARTs) with Tx and Rx FIFOs
  - 3 banks of 8-bit and 1 bank of 7-bit parallel I/O
  - 1 smartcard interface and clock generator
  - 2 SSCs for I^2C/SPI master/slave interfaces
  - infrared transmitter/receiver
  - integrated VCXO
  - low-power / RTC / watchdog controller

- Advanced security ready
  - compatible with latest CA requirement
- JTAG/TAP interface
- Package
  - 23 mm x 23 mm PBGA324
  - 24 mm x 24 mm LQFP216

2 Architecture features

2.1 Introduction

The STi5107 is a low-cost Omega2 MPEG device that delivers high performance and integrates features that provide an overall system cost reduction. The device implements a fully unified DDR/SDR SDRAM based memory architecture that integrates the Omega2 video decoder cell, together with a blitter engine and a multichannel DMA controller to provide enhanced performance for graphics and real-time stream transfers.

Transfer of data such as pixmaps, audio streams, stills and PES can be performed efficiently using the STi5107 DMA.

A true-color mode provides OSD graphics allowing the display of RGB16 formats: RGB565, ARGB1555 and ARGB4444. This directly supports up to 65,536 colors in a region. Alpha blending by region or by pixel is available for mixing with video and background layers.

The above feature set, guaranties smooth user interface and high performance for demanding middleware such as MHP™.

2.2 Omega2 (STBus) interconnect

The Omega2 multipath unified interconnect provides high on-chip bandwidth and low latency accesses between modules. The interconnect operates hierarchically, with latency-critical modules placed at the top level. The multipath router allows simultaneous access paths between modules, and simultaneous read and write phases from different transactions to and from the modules.

2.3 Processor core

The ST20-C106 processor core comprises the well established ST20C1+ CPU running at 200 MHz. It provides a diagnostic controller unit (for low intrusion, real-time debugging), a memory (4-Kbyte instruction cache, 4-Kbyte data cache and 2-Kbyte SRAM) and a 16 input priority-level interrupt controller. ST20 has been recognized as the best in class for real time, mutitasking and low memory footprint CPU. Thanks to ST's royalty free operating system (0S20) and the full toolset suite, it makes the perfect development environment for STB application.

2.4 Memory subsystem

The STi5107 has a local memory interface (LMI) and a peripheral/flash memory interface (FMI).

The STi5107's LMI is used for all data requirements in unified memory applications, including graphics, video and audio buffers. It provides 16-bit wide SDR/DDR SDRAM interface that can operate at 166 MHz for both SDR or DDR memories.

The FMI provides support for 16-bit wide peripherals, flash and synchronous flash.

Instructions can execute in place from flash/SFlash™ on the FMI or can be copied to SDRAM on the LMI. The following sections overview the different memory interfaces.

2.4.1 Local memory interface

The LMI is a 16-bit wide SDR/DDR SDRAM interface with a peak bandwidth of 532 Mbyte/s (DDR running @166 MHz). It supports 64-MBit, 128-Mbit, 256-Mbit, or 512-Mbit SDRAM. The LMI provides a fully cacheable address space for data and instructions, with data cacheability controlled in 512 Kbyte blocks for up to 8 Mbytes.

2.4.2 Flash memory interface

The FMI provides a glueless interface to SRAM, flash, SFlash and peripherals, in up to four configurable banks over a 16-bit wide interface. Bus cycle strobe timings can be programmed from 0 to 15 phases for slower peripherals.

Support is provided for control of DVB-CI and ATAPI connection.

2.5 Transport stream processing

The STi5107 supports single transport stream input.

It is possible to support DVB-CI configurations as shown in *Figure 4* and *Figure 5*.

Figure 4. Dual DVB-CI support

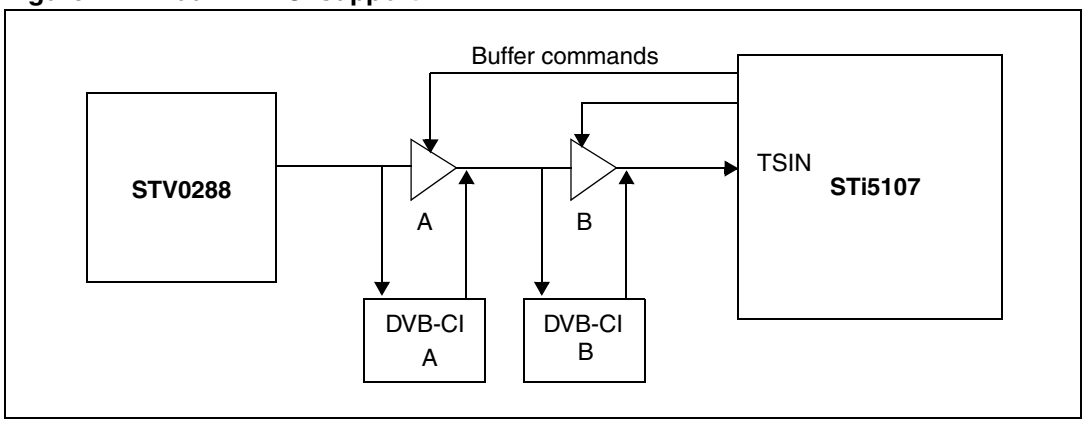
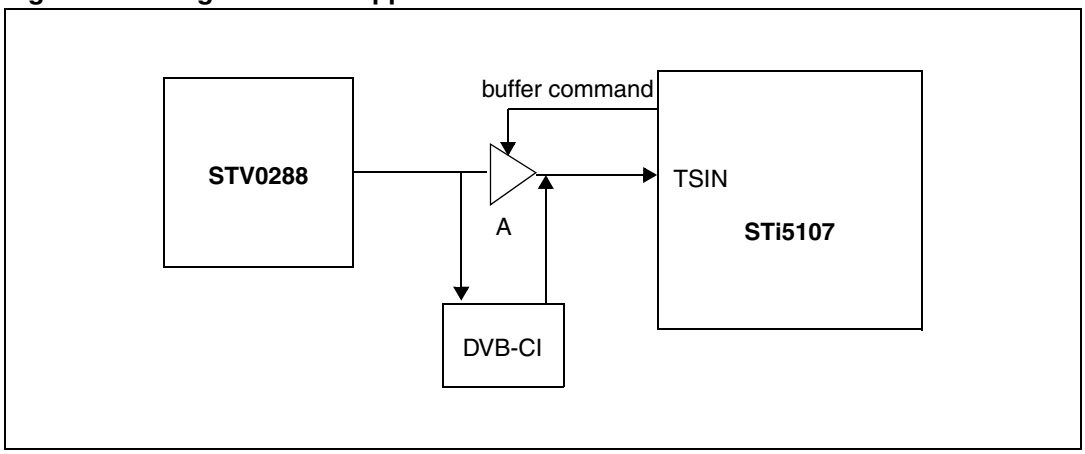


Figure 5. Single DVB-CI support



Programmable transport interface (PTI)

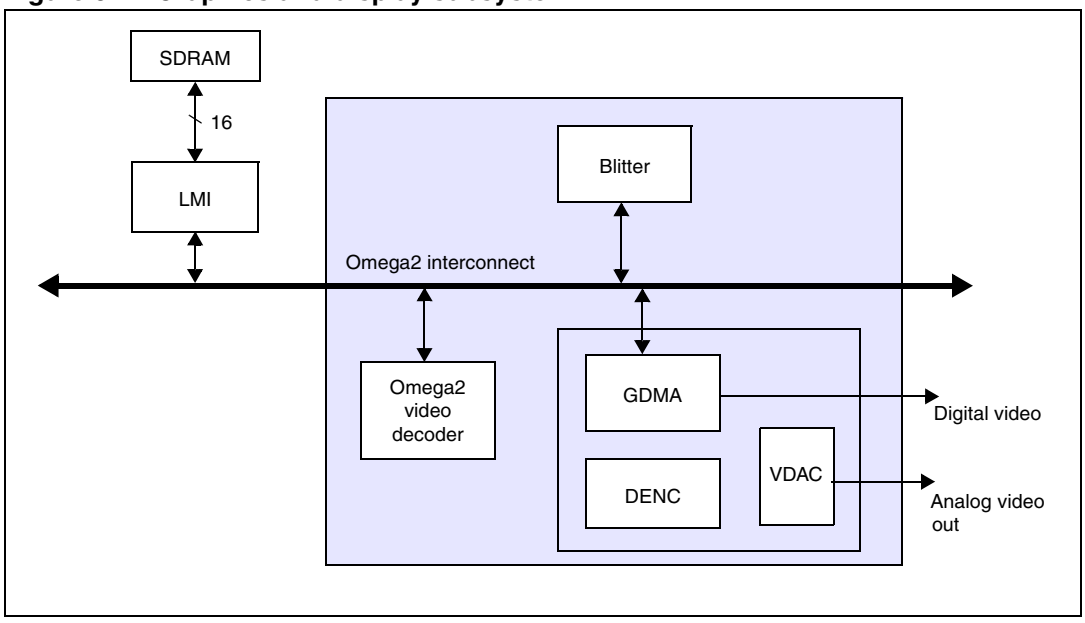
The PTI hardware performs the following functions:

- descrambling, demultiplexing and data filtering,
- PES data is transferred by DMA to audio and video decoders via circular buffers,
- section data is transferred by DMA to separate buffers for further processing by the CPU,
- DVB transport streams with data rates up to 100 Mbit/s,
- PID filtering to select the audio, video and data packets to be processed,
- can support 48 PID slots.
- descramble streams using the following ciphers:
  - DVB-CSA,
  - NDS specific streams that are supported by the integrated ICAM functionality.
- has a section filter core that filters DVB standard sections using 96x 8-byte or 48x 16-byte filters.

2.6 MPEG graphics and display processing

The MPEG graphics and display architecture shown in *Figure 6* provides the graphics, video-stream processing and display capabilities of the STi5107.

Figure 6. Graphics and display subsystem



Video decode and display

The video decoder is based on the Omega2 cell and provides a memory to memory decode into YC 4:2:0 macroblock format, it is able to provide simple resizing based on x2 and x0.5.

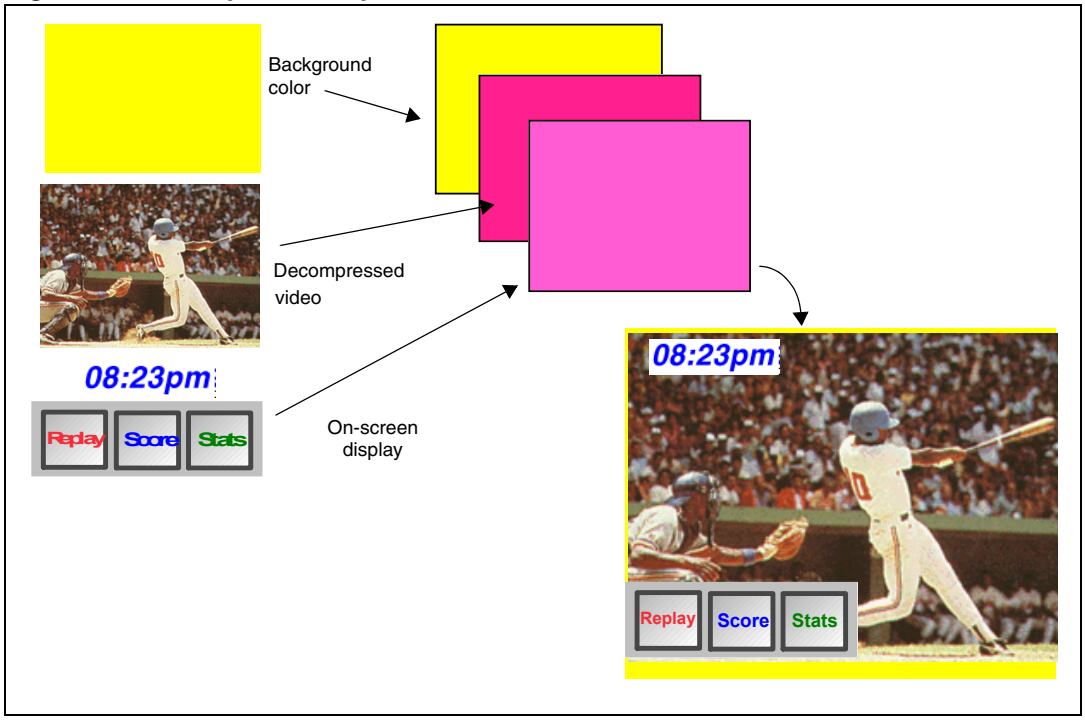
The GDMA retrieves the final composition from main memory and transfers it to the DENC, which in turn drives the output video DAC.

2.7 Graphics and display

2.7.1 Display

The STi5107 uses blitter based display architecture that allows the user to build a complex user interface with background color, still picture, video plane and on-screen display (OSD) as illustrated in *Figure 7*.

Figure 7. Example of composition



2.7.2 OSD plane

The OSD plane is managed as a set of horizontal bands with a specification comprising configuration, bitmap and, for CLUT formats, palette information for each region. The OSD operates in one of two modes, palette mode or true color mode.

- **Palette mode**: Each region can be independently specified with a resolution of 8 bpp. Regions are frame based. Each region palette can support up to 256 colors with up to 24 bits resolution per color entry.
- **True color mode**: Each region can be independently specified with a 16 bpp resolution in one of the following direct color formats: RGB565, ARGB1555, or ARGB444.

A vertical inter-field, anti flicker filter is provided to reduce flicker on interlace displays. It is available for both palette and true color modes.

2.7.3 Display mixing

Display planes are mixed by the blitter using alpha blending between planes. Mixing of the OSD plane with the lower layers is achieved using one of the following on a per region basis.

- A 4-bit alpha blending component per region (true color mode and palette mode without antialiasing enabled).
- An individual 6-bit alpha component per color (palette mode with antialiasing enabled).
- Alpha with pixel (ARGB1555 or ARGB4444, true color mode only).

2.7.4 Digital video output

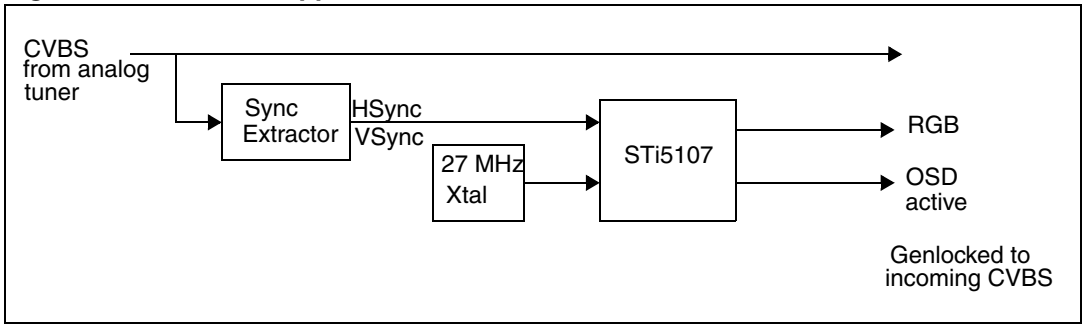
The display provides a digital video output, that supports both CCIR601 and CCIR656 modes.

2.7.5 Genlocking

Genlocking locks the STx5107 OSD to an incoming analog signal. The RGB signals contain OSD that can be overlaid on top of analog CVBS, allowing single OSD for both digital and analog reception. The OSD active signal can be used as a fast blanking signal to switch between CVBS and RGB, as illustrated in *Figure 8*.

The STx5107 does not require any external PLL to lock its own pixel clock. It uses its own internal PLL, which reduces the overall BOM.

Figure 8. Genlock support STi5107



2.8 Digital encoder

The digital converter process YCbCr 4:4:4/4:2:2 from main memory, which the blitter has generated and produces standard analog baseband PAL/SECAM/NTSC signal, and component (YUV/RGB).

The digital encoder can handle interlaced mode in all standards. ITU-T 601 aspect ratio displays can be supported in all standards. The digital encoder performs closed-caption, CGMS, WSS, Teletext and VPS encoding and allows Macrovision™ 7.01/ 6.1 copy protection.

One integrated quad-DAC provides four analog TV outputs, on which it is possible to output either (CVBS + RGB) or (CVBS + YUV) or (S - VHS (Y/C) + CVBS1 + CVBS2).

2.9 Audio subsystem

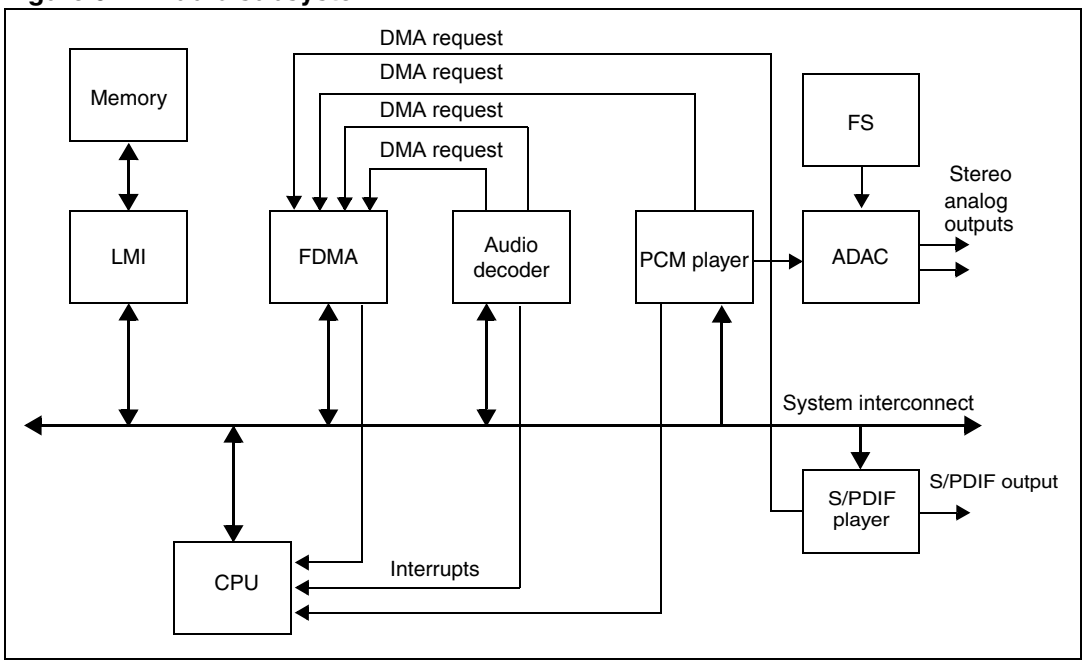
The audio subsystem supports audio decoding of MPEG-1 layers I, II.

Simultaneous MPEG-1 audio decoding and compressed output of Dolby streams on the S/PDIF is supported.

Audio sample rates of 32 kHz, 44.1 kHz and 48 kHz are supported.

The audio subsystem is illustrated in *Figure 9*.

Figure 9. Audio subsystem



The audio subsystem consists of the following units:

- audio decoder,
- S/PDIF player, PCM player,
- integrated 24-bit stereo audio DAC system,
- audio/digital frequency synthesizer: generates the PCM and sample rate clocks.

2.10 Central DMA controller

The STi5107 has a multichannel, burst-capable direct memory access controller that supports the following:

- fast 2D unaligned memory to memory transfers of graphics and stills,
- real time stream transfers to and from memory with or without pacing. These channels are suitable for transfers with external peripherals, for audio and video stream transfers within the STi5107.

2.11 Internal peripherals

The STi5107 has many dedicated internal peripherals for digital TV receiver applications, including:

- one smartcard controller,
- two ASCs (UARTs) which are generally used by the smartcard controllers or for modem application,
- two SSCs for I²C master/slave interfaces, with SPI support,
- four GPIO ports,
- infrared blaster/decoder interface module,
- DVB common interface support,
- a fully integrated digital VCXO,
- an interrupt level controller,
- a low-power/RTC/watchdog controller,
- DCU toolset support,
- a JTAG/TAP interface.

2.12 Clock generation

All system clocks are generated using the clock generator block. This contains two high-frequency PLLs (532 MHz/400 MHz) that are divided down to produce a series of phase-related programmable clock channels.

The STi5107 has a clock master. The Flash clock output may be phase aligned to optimize the external bus performance of the FMI.

VCXO functionality has been integrated using a special purpose frequency synthesizer, thus removing the need for an external varactor diode or VCXO module.

3 Revision history

Table 1. Document revision history

Date	Revision	Changes
05-Dec-2006	1	Initial release.