STHDMI002A

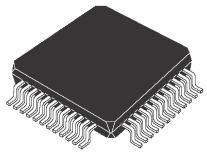
Wide bandwidth, 2 to 1 HDMI switch with single enable

Features

- Compatible with HDMI v1.2, DVI v1.0 digital interfaces
- 165MHz speed operation supports all video formats up to 1080p and SXGA (1280 x 1024 at 75Hz)
- Data rate per channel for UXGA: 1.65Gbps
- Low R_{ON}: 5.5 Ω(typ)
- V_{CC} operating range: 3.135V to 3.465V
- Low current consumption: 20µA
- ESD human body model HBM Voltage:
  - ±2KV for all I/Os
- Channel ON capacitance: 6pF (typ)
- Switching speed: 9ns
- Near-zero propagation delay: 250ps
- Low crosstalk: -32dB at 825MHz
- Bit-to-bit skew: 200ps
- Very low ground bounce in flow through mode
- Data and control inputs provide an undershoot clamp diode
- Wide bandwidth minimizes skew and jitter
- Hot insertion capable
- Isolated Digital Display Control (DDC) bus for unused ports
- 5V tolerance to all DDC and HPD_SINK inputs
- Supports bi-directional operation
- Available in the TQFP48 package
- –40°C to 85°C operating temperature range

Applications

- Advanced TVs
- Front projectors
- LCD TVs
- PDPs
- LCD monitors
- Notebook PCs
- STB and DVD players



TQFP48

Description

The STHDMI002A is a differential Single Pole Double Throw (SPDT) 2 to 1, low Ron, bi-directional HDMI switch designed for advanced TV applications supporting HDMI/DVI which demand high definition superior image quality. The differential signal from the 2 ports of HDMI is multiplexed through the switch to form a single output HDMI channel going to the HDMI receiver while the unselected output goes to the high-Z state.

It is designed for very low cross-talk, low bit-to-bit skew, high channel-to-channel noise isolation and low I/O capacitance. The switch offers very little or practically no attenuation of the high-speed signals at the outputs, thus preserving the signal integrity to pass stringent requirements.

The STHDMI002A also includes the DDC as well as the HPD line switching. The pin layout is optimized for easy PCB routing to the HDMI connector and HDMI receivers.

The maximum DVI/HDMI data rate of 1.65Gbps provides the resolution required by the advanced HDTV and PC graphics.

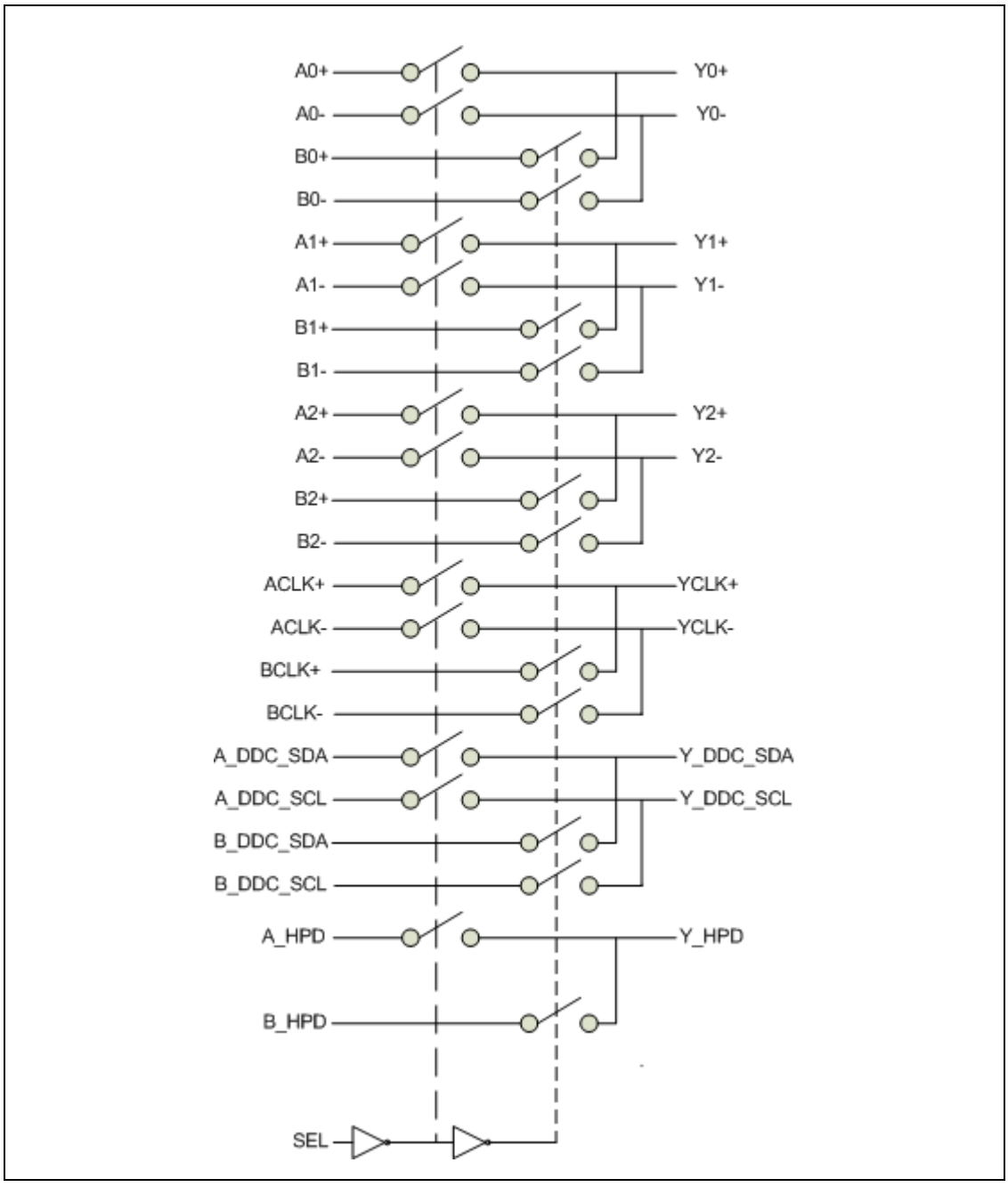
Advantages

STHDMI002A provides the ability to switch a single source output to various display devices or switch video display devices between multiple sources. It reduces the overall BOM costs by eliminating the need for more costly multi input-output controllers.

Contents

1 Functional diagram

Figure 1. Functional diagram



2 Functional description

The STHDMI002A routes physical layer signals for high bandwidth digital video and is compatible with low voltage differential signaling standards like TMDS. The device multiplexes differential outputs from a video source to one of the two corresponding outputs to a common display. The low on-resistance and low I/O capacitance of STHDMI002A result in a very small propagation delay. The device integrates SPDT-type switches for 3 differential data TMDS channels and 1 differential clock channel. Additionally it integrates the switches for DDC and HPD lines switching.

The I²C interface of the selected input port is linked to the I²C interface of the output port, and the hot plug detector (HPD) of the selected input port is output to HPD_SINK. For the unused ports, the I²C interfaces are isolated, and the HPD pins are also isolated.

2.1 HPD pins

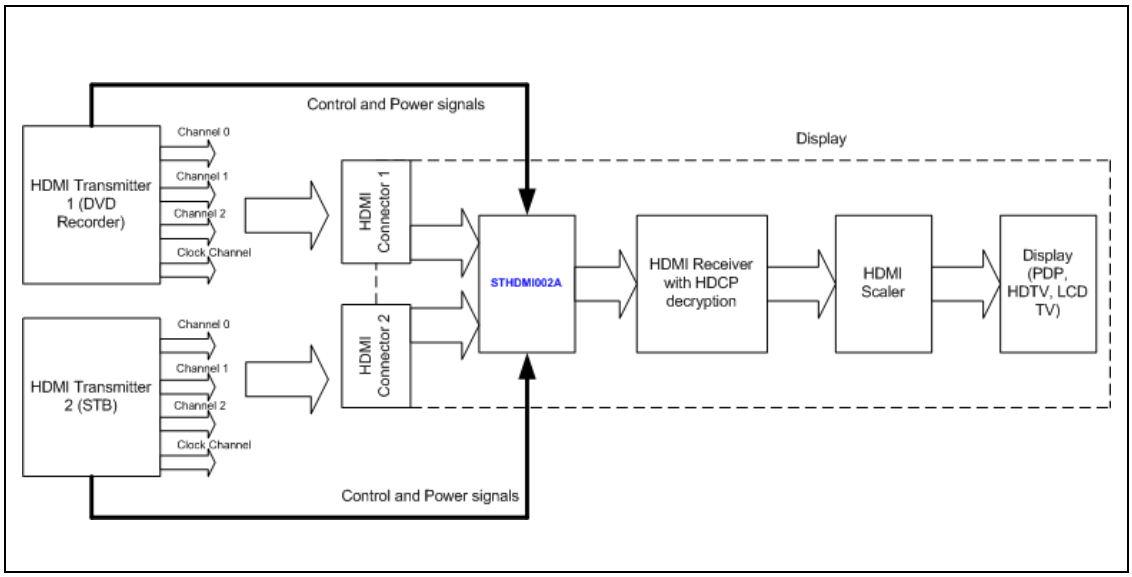
The input of the Y_HPD is 5V tolerant, allowing direct connection to 5V signals. The switch is able to pass both 0V and 5V signal levels. The HPD switch resistance depends on the input voltage level. At low (near to 0V) input voltage levels, the resistance is 20Ω typically and at high (near to 5V) input voltage levels, the resistance is 150Ω typically.

2.2 DDC channels

The DDC channels are designed with a bi-directional NMOS gate, providing 5V signal tolerance. The 5V tolerance allows direct connection to a standard I²C bus, thus eliminating the need for a level shifter. When the input is a 5V, the NMOS switch is turned off and the pull up resistor on either side of the switch determines the high voltage potential.

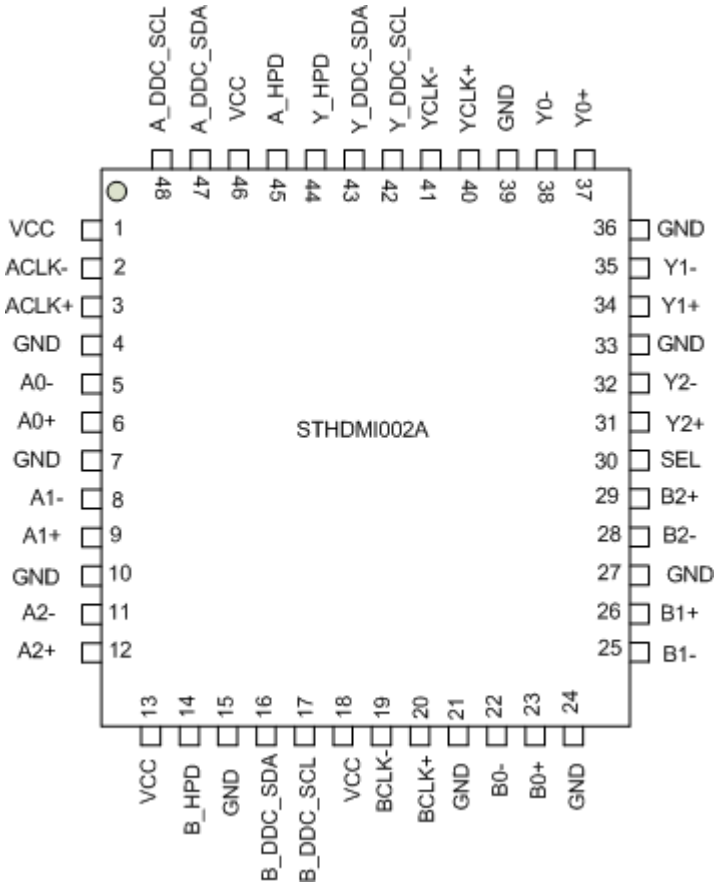
3 Application diagram

Figure 2. Application diagram



4 Pin configuration

Figure 3. Pin connections



TQFP48 (pitch = 0.5mm)

Table 1. Pin description

Pin number	Pin Name	Type	Function
1	VCC	Power	Supply voltage (3.3V ± 5%)
2	ACLK-	Input	TMDS Clock- for port A
3	ACLK+	Input	TMDS Clock+ for port A
4	GND	Power	Ground
5	A0-	Input	TMDS Data 0- for port A
6	A0+	Input	TMDS Data 0+ for port A
7	GND	Power	Ground
8	A1-	Input	TMDS Data 1- for port A
9	A1+	Input	TMDS Data 1+ for port A
10	GND	Power	Ground
11	A2-	Input	TMDS Data 2- for port A
12	A2+	Input	TMDS Data 2+ for port A
13	VCC	Power	Supply voltage (3.3V ± 5%)
14	B_HPD	Output	Hot Plug Detect (HPD) output for port B
15	GND	Power	Ground
16	B_DDC_SDA	I/O	DDC SDA input for port B
17	B_DDC_SCL	I/O	DDC SCL input for port B
18	VCC	Power	Supply voltage (3.3V ± 5%)
19	BCLK-	Input	TMDS Clock- for port B
20	BCLK+	Input	TMDS Clock+ for port B
21	GND	Power	Ground
22	B0-	Input	TMDS Data 0- for port B
23	B0+	Input	TMDS Data 0+ for port B
24	GND	Power	Ground
25	B1-	Input	TMDS Data 1- for port B
26	B1+	Input	TMDS Data 1+ for port B
27	GND	Power	Ground
28	B2-	Input	TMDS Data 2- for port B
29	B2+	Input	TMDS Data 2+ for port B
30	SEL	Input	Select control input to select port A or port B
31	Y2+	Output	TMDS Data2+ output
32	Y2-	Output	TMDS Data2- output
33	GND	Power	Ground
34	Y1+	Output	TMDS Data1+ output

Table 1. Pin description

Pin number	Pin name	Type	Function
35	Y1-	Output	TMDS Data1- output
36	GND	Power	Ground
37	Y0+	Output	TMDS Data0+ output
38	Y0-	Output	TMDS Data0- output
39	GND	Power	Ground
40	YCLK+	Output	TMDS Clock+ output
41	YCLK-	Output	TMDS Clock- output
42	Y_DDC_SCL	I/O	DDC SCL output
43	Y_DDC_SDA	I/O	DDC SDA output
44	Y_HPD	Input	Sink side hot plug detector input High : 5V power signal asserted from source to sink and EDID is ready Low : No 5V power signal is asserted from source to sink or EDID is not ready
45	A_HPD	Output	Hot Plug Detect (HPD) output for port A
46	VCC	Power	Supply voltage (3.3V ± 5%)
47	A_DDC_SDA	I/O	DDC SDA input for port A
48	A_DDC_SCL	I/O	DDC SCL input for port A

4.1 Function table

Table 2. Function table

SEL	Signal status	DDC Status	HPD Status
L	Y= TMDS Data, Clock for port A Port B is in ‘Z’ state	Y = DDC for port A DDC for port B is ‘Z’	Y= HPD for port A HPD for port B is ‘Z’
H	Y=TMDS Data, Clock for port B Port A is in ‘Z’ state	Y = DDC for port B DDC for port A is ‘Z’	Y= HPD for port B HPD for port A is ‘Z’

5 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage to Ground		-0.5 to +4.0	V
V_I	DC Input Voltage (TMDS A,B ports)		1.7 to +4.0	V
	SEL		-0.5 to +4.0	V
	A_DDC_SDA, A_DDC_SCL, B_DDC_SDA, B_DDC_SCL, Y_DDC_SDA, Y_DDC_SCL, Y_HPD, A_HPD, B_HPD		-0.5 to +6.0	V
V_{IC}	DC control input voltage		-0.5 to +4.0	V
I_O	DC output current		120	mA
T_{STG}	Storage temperature		-65 to +150	°C
T_L	Lead temperature (10 sec)		300	°C
V_{ESD}	Electrostatic discharge voltage on IOs(1)1	Human body model	-2 to +2	kV
		Contact discharge	-2 to +2	kV

1. In accordance with the MIL STD 883 method 3015

Table 4. Thermal data

Symbol	Description	Value	Unit
R_{thJA}	Thermal Resistance Junction-ambient	TBA	°C/W

6 DC electrical characteristics

T_A = -40 to +85 °C, V_{CC} = 3.3V ± 5%

Table 5. DC electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage (SEL pin)	High level guaranteed	2.0			V
V_{IL}	LOW level input voltage (SEL pin)	Low level guaranteed	-0.5		0.8	V
V_{IK}	Clamp Diode voltage (All IOs)	V_{CC} = 3.465V, I_{IN} = -18mA		-0.8	-1.2	V
I_{IH}	Input high current (SEL pin, A, B data ports)	V_{CC} = 3.465V, V_{IN} = V_{CC}			±5	µA
I_{IL}	Input low current (SEL pin, A, B data ports)	V_{CC} = 3.465V, V_{IN} = GND			±5	µA
I_{OFF}	Power down leakage current	V_{CC} = 0V; Outputs (Y-port) = 0V; Inputs (A-port) = 3.465V; Inputs (B-port) = 3.465V			±5	µA
R_{ON}	Switch ON resistance (1)	V_{CC} = 3.135 V, V_{IN} = 1.5 to V_{CC} I_{IN} = -40mA		5.5	7.5	Ω
R_{FLAT}	ON resistance flatness (1) (2)	V_{CC} = 3.135 V, V_{IN} = 1.5 to V_{CC} I_{IN} = -40mA		0.8		Ω
ΔR_{ON}	ON resistance match between channels $\Delta R_{ON} = R_{ONMAX} - R_{ONMIN}$ (1) (3)	V_{CC} = 3.135 V, V_{IN} = 1.5 to V_{CC} I_{IN} = -40mA		1.0	1.3	Ω
DDC I/O Pins						
$I_{I(leak)}$	Input leakage current	V_{CC} = 3.465V V_I (max) = 5.3V on isolated DDC ports Y= 0.0V		0.1	+2	µA
I_{OFF}	Power down leakage current	V_{CC} = 0V; Outputs (Y-port) = 0V; Inputs (A-port) = 5.3V; Inputs (B-port) = 5.3V			±5	µA
$C_{I/O}$	Switch off capacitance Switch on capacitance	V_I=0V, V_{CC}=3.3V, T= 25°C F = 1 MHz		5 9		pF pF

Table 5. DC electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_{ON}	Switch resistance	V_{CC} = 3.3V I_O=3mA; V_O=0.0V		32		Ω
		V_{CC} = 3.3V I_O=3mA; V_O=0.4V		36		Ω
		V_{CC} = 3.3V I_O=3mA; V_O=0.8V		42		Ω
		V_{CC} = 3.3V I_O=3mA; V_O=1.5V		62		Ω
Status pins (Y_HPD)						
$I_{I(leak)}$	Input leakage current	V_{CC} = 3.465V V_I (max) = 5.3V on isolated HPD port Y= 0.0V		0.1	+2	µA
I_{OFF}	Power down leakage current	V_{CC} = 0V; (Y-port) = 0V; (A-port) = 5.3V; (B-port) = 5.3V			±5	µA
Status pins (A_HPD, B_HPD)						
$C_{I/O}$	Switch off capacitance Switch on capacitance	V_I=0V, V_{CC}=3.3V, T= 25°C F = 1 MHz		5 9		pF pF
R_{ON}	Switch resistance	V_{CC} = 3.3V I_O=3mA; V_O=0.0V		24		Ω
		V_{CC} = 3.3V I_O=3mA; V_O=5.0V		150		Ω

1. Measured by voltage drop between channels at the indicated current through the switch. On-resistance is determined by the lower of the two voltages.
2. Flatness is defined as the difference between the R_{ONMAX} and the R_{ONMIN} of the on resistance over the specified range.
3. ΔR_{ON} measured at the same $V_{CC,}$ temperature and voltage level.

6.1 Capacitance

T_A = 25°C, f = 1MHz

Table 6. Capacitance

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V		2	3	pF
C_{OFF}	Port x0 to Port x1, Switch off (Note 4)	V_{IN} = 0V		4	6	pF
C_{ON}	Capacitance switch on (x to x0 or x to x1) (1)	V_{IN} = 0V		6	12	pF

1. x = Port Y; x0 = Port A; x1 = Port B

6.2 Power supply characteristics

T_A = -40 to +85 °C

Table 7. Power supply characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{CC}	Quiescent power supply current	V_{CC} = 3.465 V, V_{IN} = V_{CC} or GND		50	500	µA

6.3 Dynamic electrical characteristics

T_A = -40 to +85 °C, V_{CC} = 3.3V ± 5%

Table 8. Dynamic electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
X_{TALK}	Non-adjacent channel Cross-talk	R_L = 100Ω, f = 370MHz		-32		dB
		R_L = 100Ω, f = 825MHz		-31		dB
O_{IRR}	Off Isolation	R_L = 100Ω, f = 370MHz		-36		dB
		R_L = 100Ω, f = 825MHz		-30		dB
BW	-3dB bandwidth			850		MHz
D_R	Data rate per channel			1.65		Gbps

6.4 Dynamic switching characteristics

T_A = -40 to +85 °C, V_{CC} = 3.3V ± 5%

Table 9. Dynamic switching characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PD}	Propagation delay	V_{CC} = 3.135V to 3.465V		0.30		ns
t_{PZH}, t_{PZL}	Line Enable Time, SEL to x to x0 or x to x1	V_{CC} = 3.135V to 3.465V	0.5	6.5	9	ns
t_{PHZ}, t_{PLZ}	Line Disable Time, SEL to x to x0 or x to x1	V_{CC} = 3.135V to 3.465V	0.5	6.5	8.5	ns
$t_{SK(O)}$	Output skew between center port to any other port	V_{CC} = 3.135V to 3.465V		0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transition of the same output (t_{PHL} - $t_{PLH)}$	V_{CC} = 3.135V to 3.465V		0.1	0.2	ns
DDC I/O pins						
$t_{PD(DDC)}$	Propagation delay from A_DDC_SDA/ B_DDC_SDA to Y_DDC_SDA or A_DDC_SCL/B_DDC_SCL to Y_DDC_SCL or Y_DDC_SDA to A_DDC_SDA/ B_DDC_SDA	C_L = 10pF			2.5	ns
t_{PZH}, t_{PZL}	Line Enable Time, SEL to x to x0 or x to x1	V_{CC} = 3.135V to 3.465V		6.5	9	ns
t_{PHZ}, t_{PLZ}	Line Disable Time, SEL to x to x0 or x to x1	V_{CC} = 3.135V to 3.465V		6.5	8.5	ns
Status pins (Y_HPD, A_HPD, B_HPD)						
$t_{PD(HPD)}$	Propagation delay (from Y_HPD to the active port of HPD)	C_L = 10pF			2.5	ns
t_{PZH}, t_{PZL}	Line Enable Time, SEL to x to x0 or x to x1	V_{CC} = 3.135V to 3.465V		6.5	9	ns
t_{PHZ}, t_{PLZ}	Line Disable Time, SEL to x to x0 or x to x1	V_{CC} = 3.135V to 3.465V		6.5	8.5	ns

Note: x = Port Y; x0 = Port A; x1 = Port B

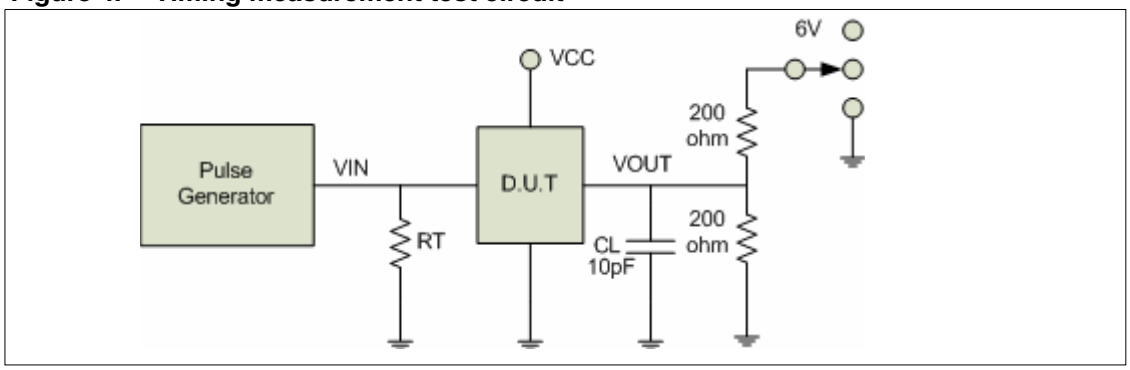
6.5 ESD performance

Table 10. ESD performance

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ESD	MIL STD 883 method 3015 (all pins)	Human Body Model (HBM)		±2		kV

7 Test circuit for electrical characteristics

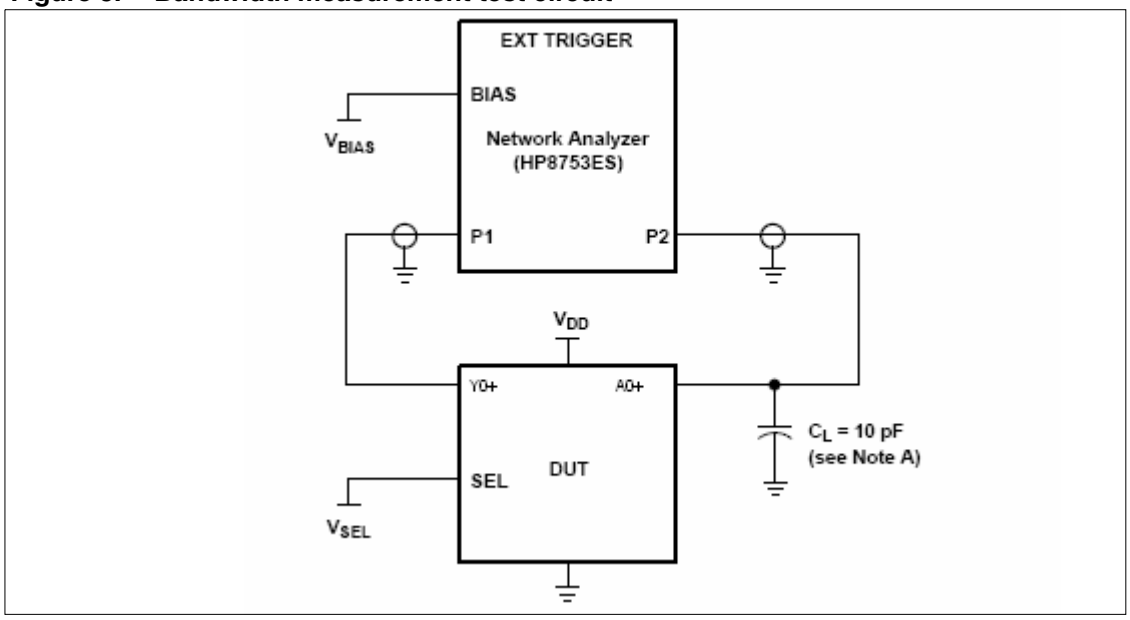
Figure 4. Timing measurement test circuit



Note: 1 CL = Load capacitance: includes jig and probe capacitance.

2 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

Figure 5. Bandwidth measurement test circuit



Note: C_L includes probe and jig capacitance

Frequency response is measured at the output of the ON channel. For example, when VSEL = 0 and Y0+ is the input, the output is measured at A0+. All unused analog I/O ports are left open.

HP8753ES set up:

Average = 4

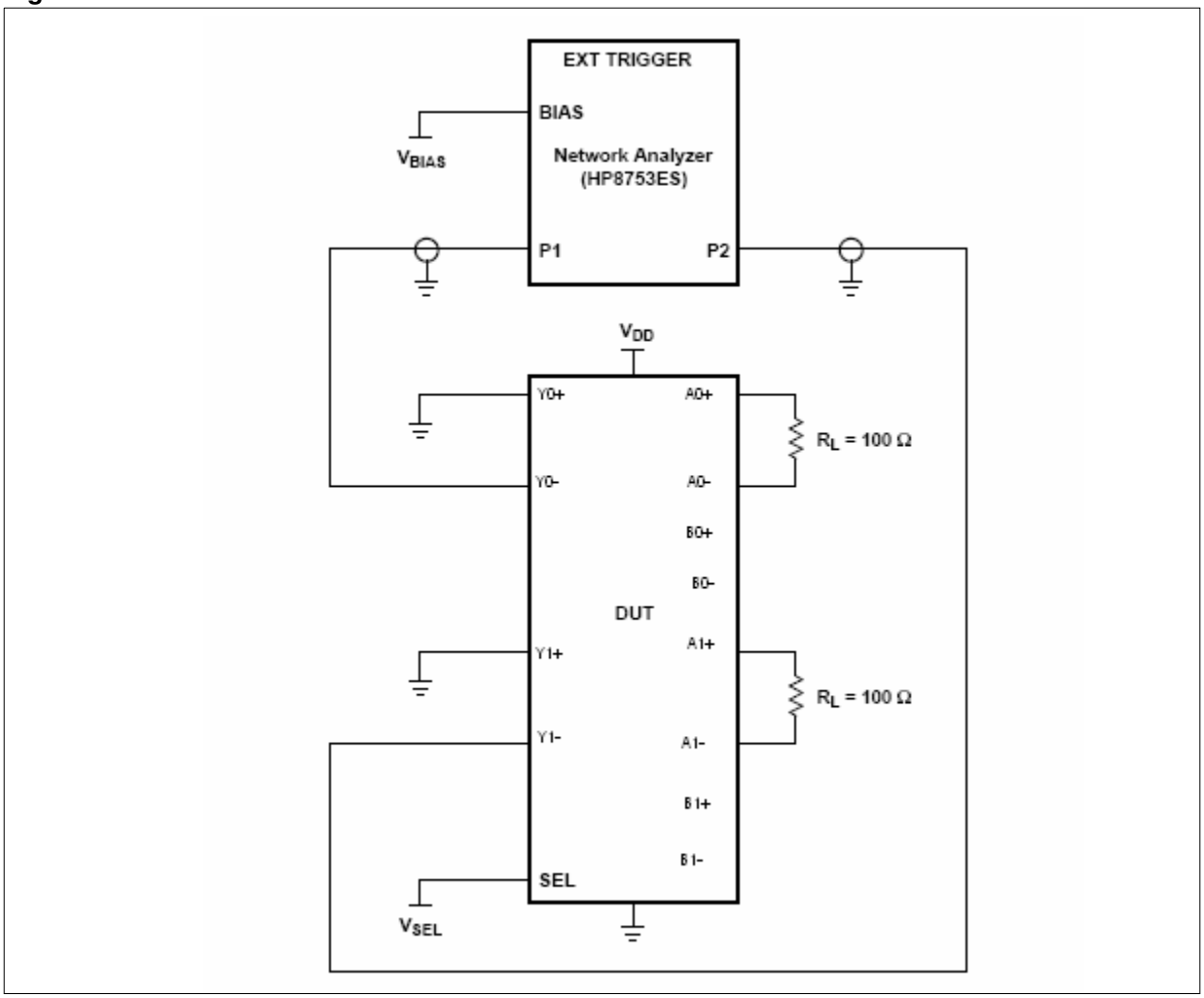
RBW = 3kHz

VBIAS = 0.35V

ST = 2s

P1 = 0dBm

Figure 6. Crosstalk measurement test circuit



Note: 1 CL includes probe and jig capacitance

2 A 50Ω termination resistor is needed to match the loading network analyzer

Crosstalk is measured at the output of the non-adjacent ON channel. For example, when VSEL = 0, and Y0- is the input, the output is measured at Y1-. All unused analog input ports (Y) are connected to GND and output ports (A,B) are left open.

HP8753ES set up:

Average = 4

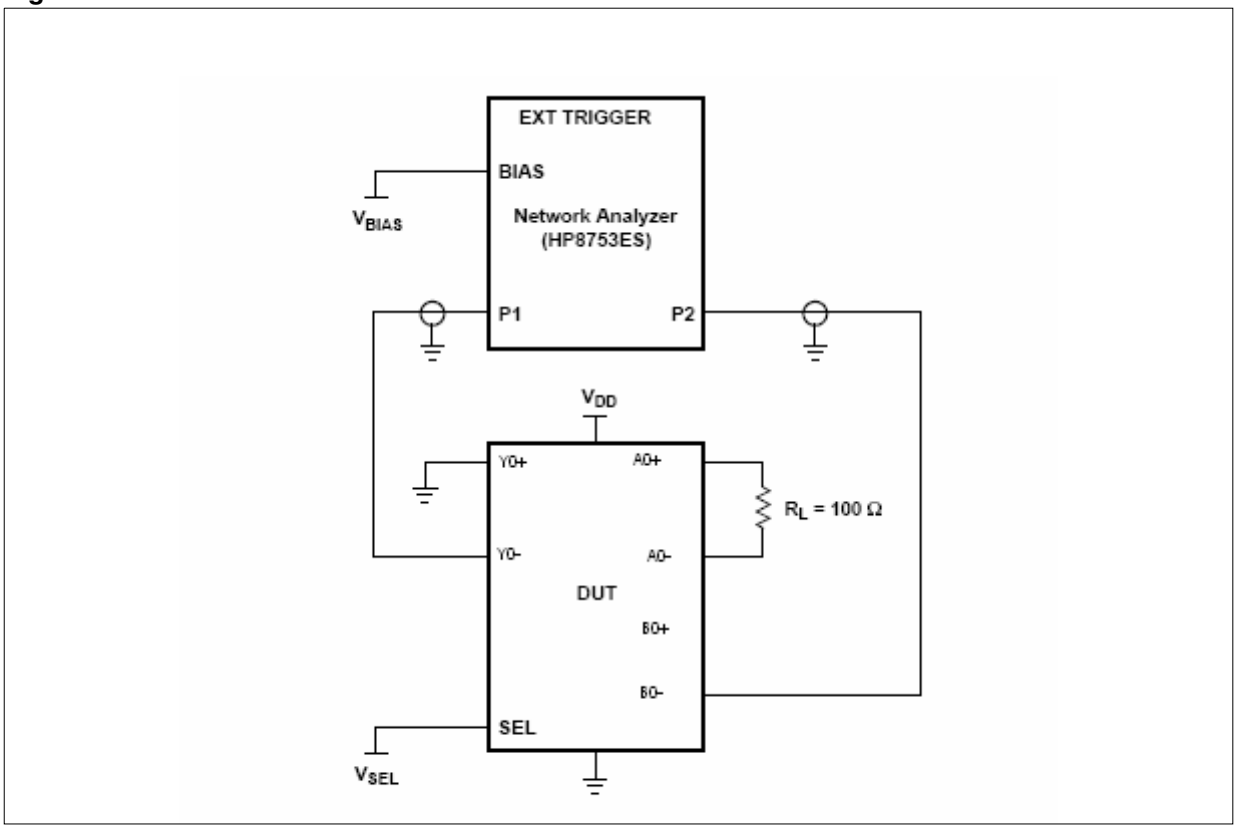
RBW = 3kHz

VBIAS = 0.35V

ST = 2s

P1 = 0dBm

Figure 7. Off-isolation measurement test circuit



Note: 1 CL includes probe and jig capacitance

2 A 50Ω termination resistor is needed to match the loading network analyzer

Off-isolation is measured at the output of the OFF channel. For example, when VSEL=0, and Y0- is the input, the output is measured at B0-. All unused analog input ports (Y) are connected to GND and output ports (A,B) are left open.

HP8753ES set up:

Average = 4

RBW = 3kHz

VBIAS = 0.35V

ST = 2s

P1 = 0dBm

8 Timing waveforms

Figure 8. Propagation delay times

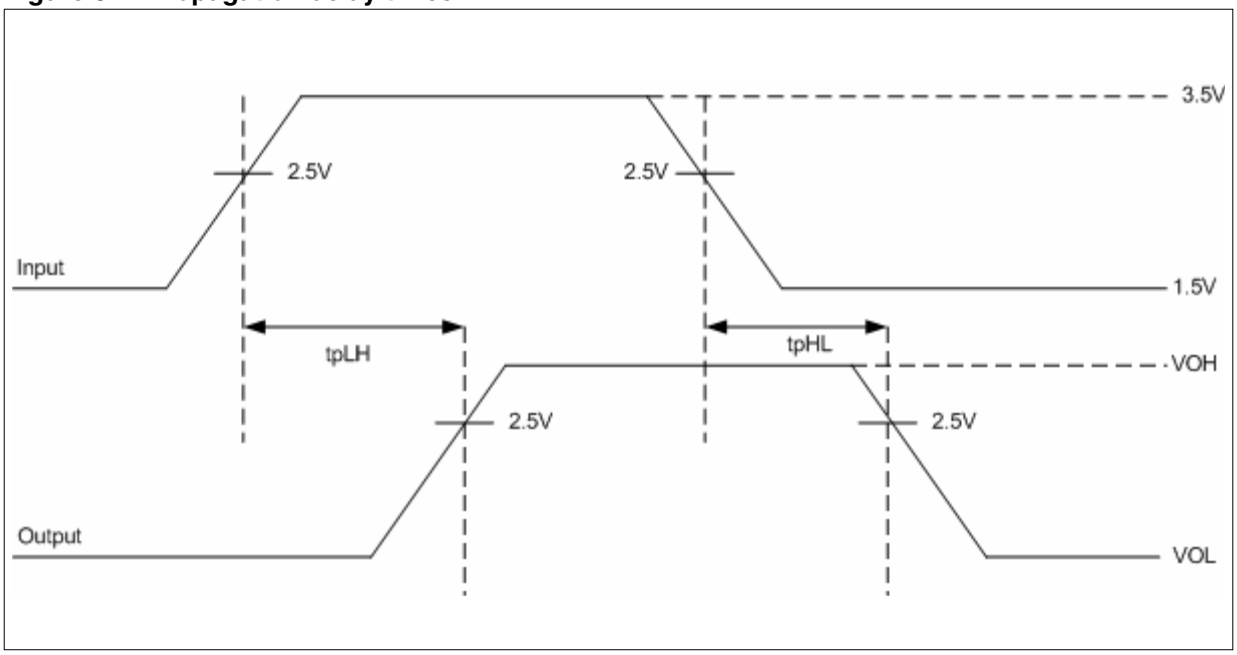


Figure 9. Enable and disable times

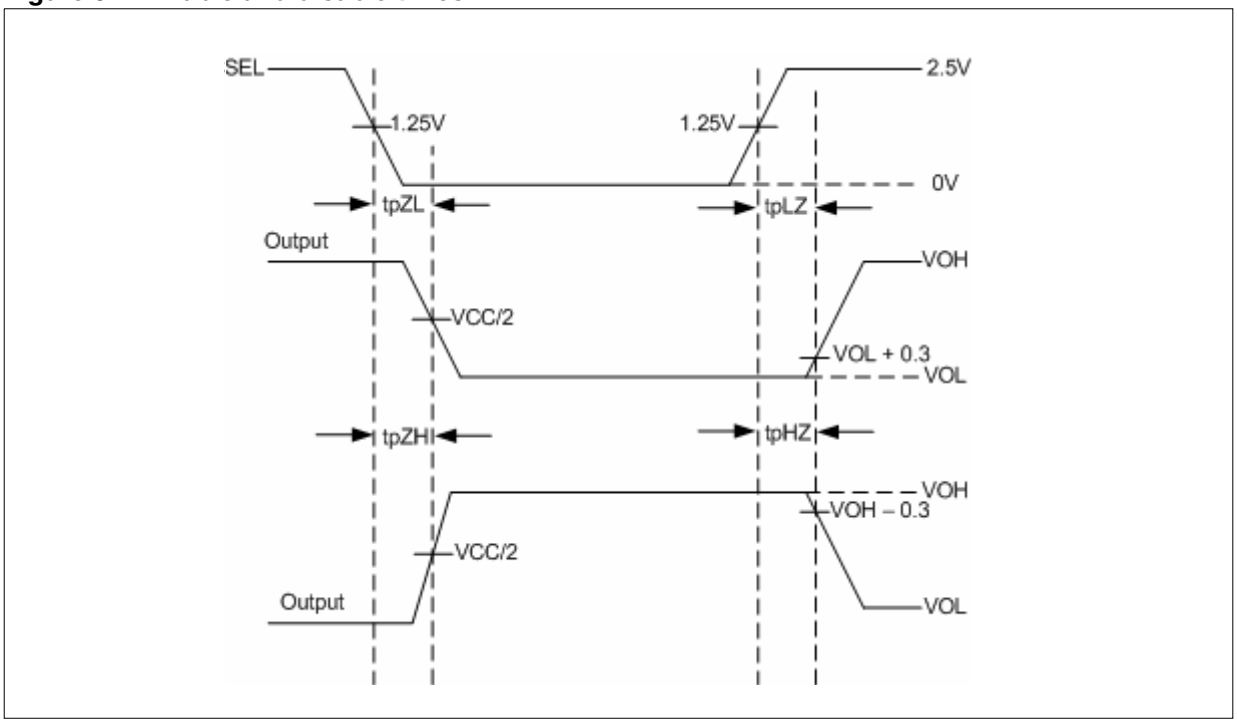


Figure 10. Output skew

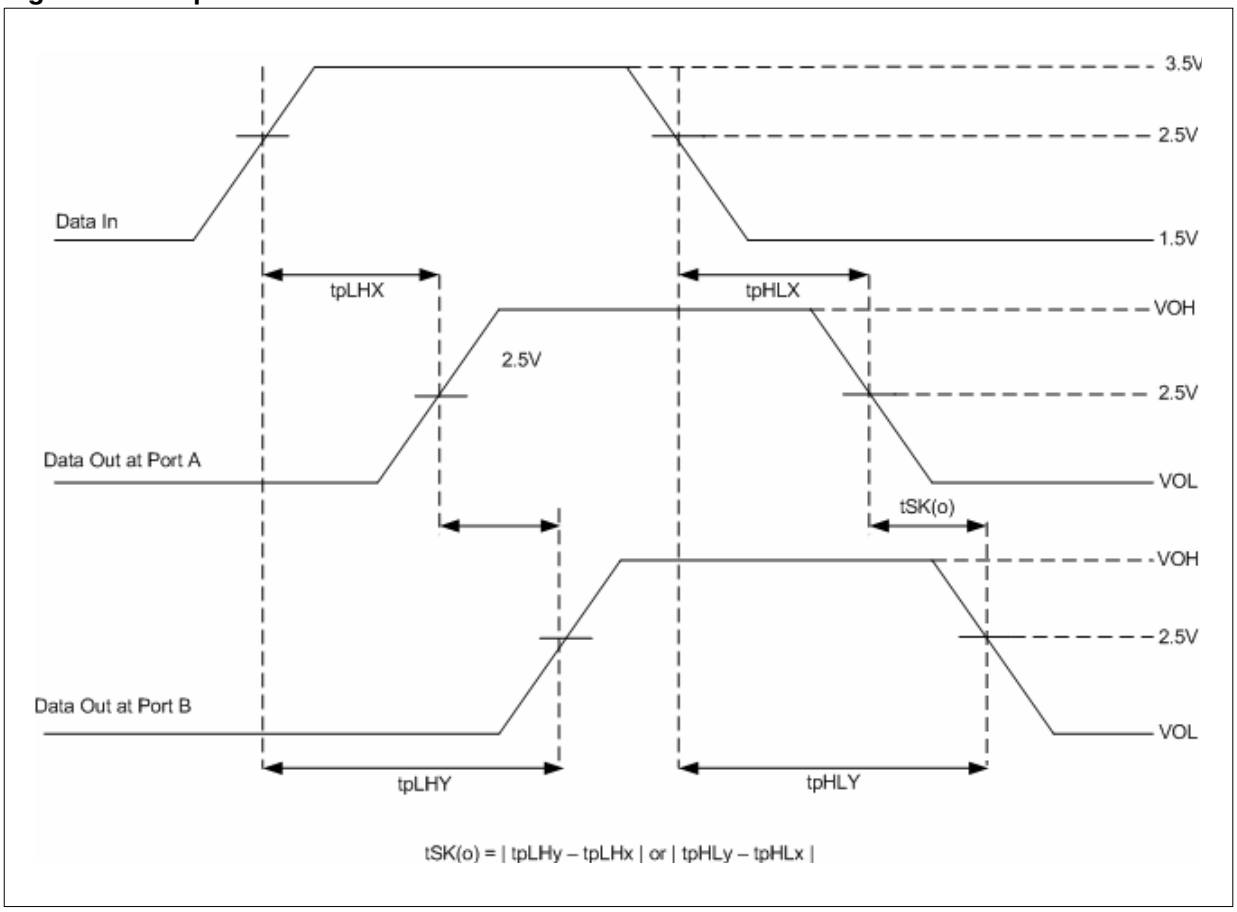
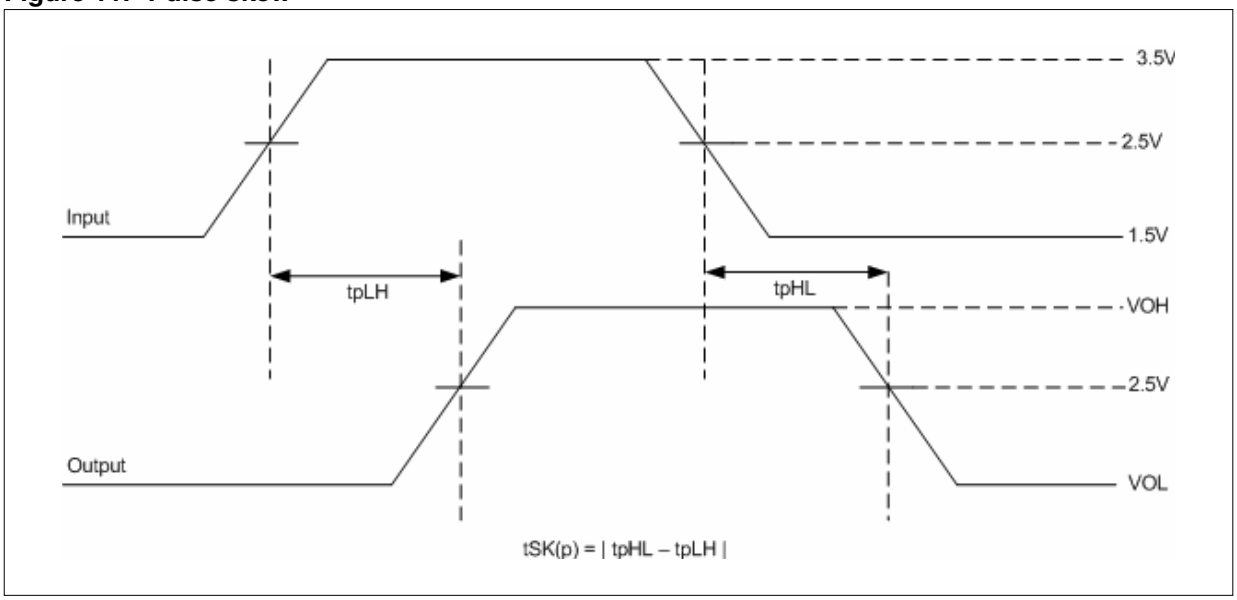


Figure 11. Pulse skew



9 Application information

9.1 Power supply sequencing

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply V_{CC} before applying any signals to the input/output or control pins.

9.2 Supply bypassing

Bypass each of the V_{CC} pins with 0.1µF and 1nF capacitors in parallel as close to the device as possible, with the smaller-valued capacitor as close to the V_{CC} pin of the device as possible.

9.3 Differential traces

The high-speed TMDS inputs are the most critical parts for the device. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device.

a) Maintain 100-Ω differential transmission line impedance into and out of the STHDMI002A.

b) Keep an uninterrupted ground plane below the high-speed I/Os.

c) Keep the ground-path vias to the device as close as possible to allow the shortest return current path.

d) Layout of the TMDS differential inputs should be with the shortest stubs from the connectors.

Output trace characteristics affect the performance of the STHDMI002A. Use controlled impedance traces to match trace impedance to both the transmission medium impedance and termination resistor. Run the differential traces close together to minimize the effects of the noise. Reduce skew by matching the electrical length of the traces. Avoid discontinuities in the differential trace layout. Avoid 90 degree turns and minimize the number of vias to further prevent impedance discontinuities.

10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 12. TQFP48 package dimensions

TQFP48 MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
L	0.45	0.60	0.75
L1		1.00	
T	0.70	0.15	0.20
T1	0.10	0.13	1.15
a	0°		7°
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
e		0.500	
ccc / ddd		0.08	

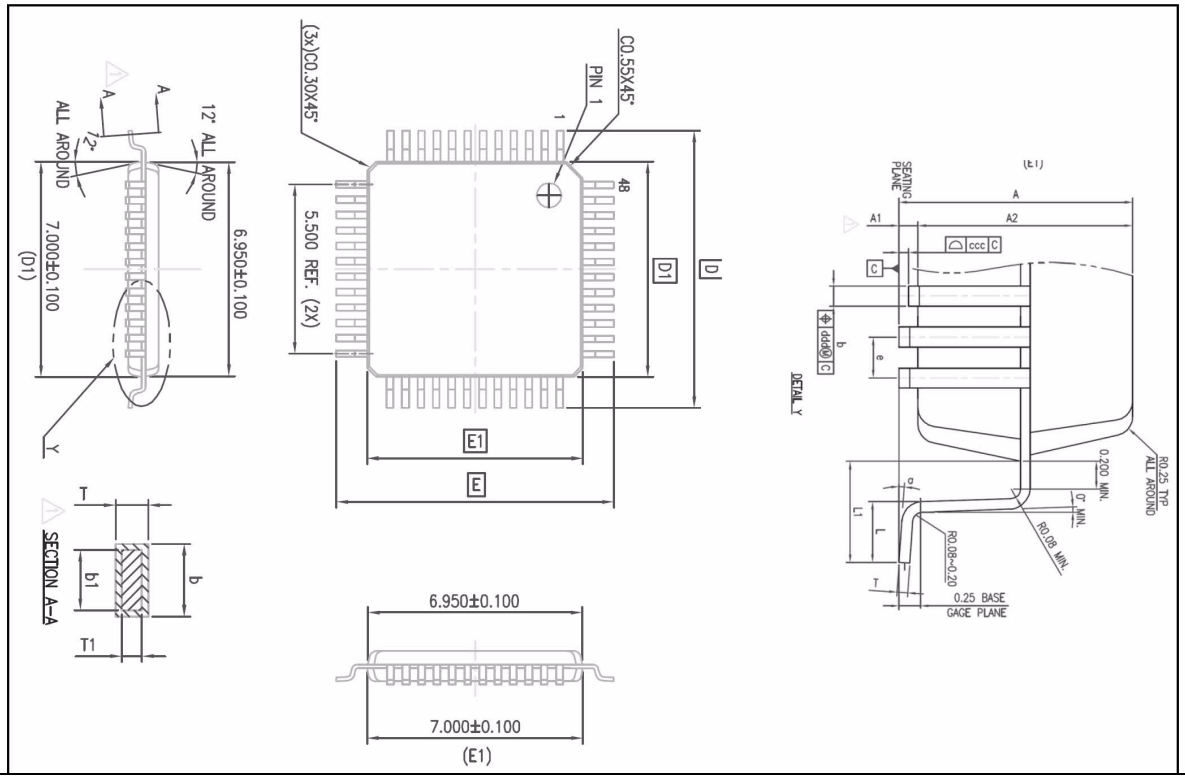
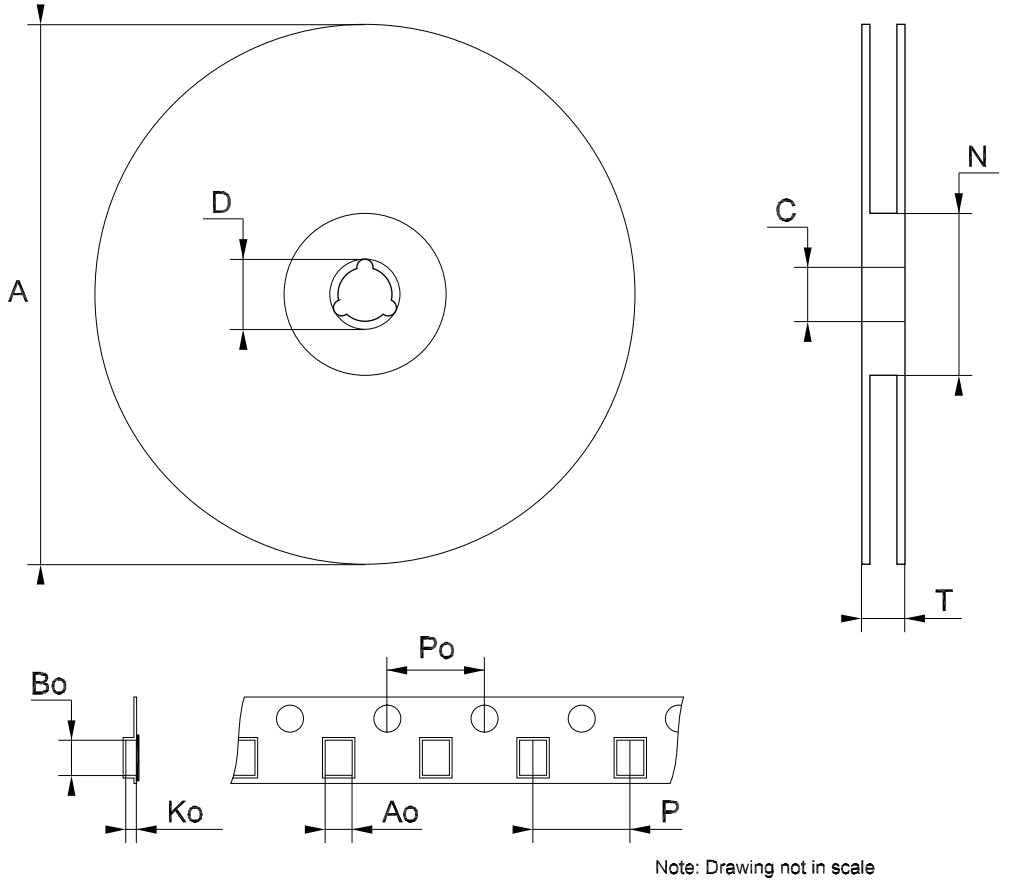


Figure 13. TQFP48 Tape and reel dimensions

Tape & Reel TQFP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	9.5		9.7	0.374		0.382
Bo	9.5		9.7	0.374		0.382
Ko	2.1		2.3	0.083		0.091
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

11 Order codes

Table 11. Order codes

Part number	Temperature range	Package	Packing
STHDMI002ABTR	–65° C to +150° C	TQFP48	Tape and reel

12 Revision history

Table 12. Revision history

Date	Revision	Change
10-Oct-2006	1	First release

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