



# STGF10NB60SD

N-channel 10A - 600V - TO-220FP  
PowerMESH™ IGBT

## General features

Type	V <sub>CES</sub>	V <sub>CE(sat)</sub> (Max)@ 25°C	I <sub>C</sub> @100°C
STGF10NB60SD	600V	<1.8V	7A

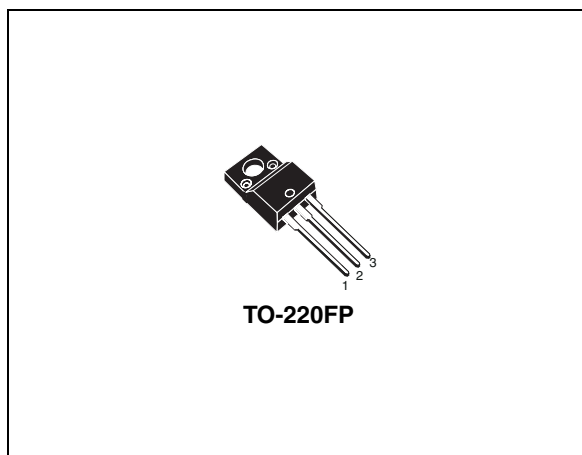
- High input impedance (voltage driven)
- Low on-voltage drop
- High current capability
- Co-packaged with turboswitch™ antiparallel diode

## Description

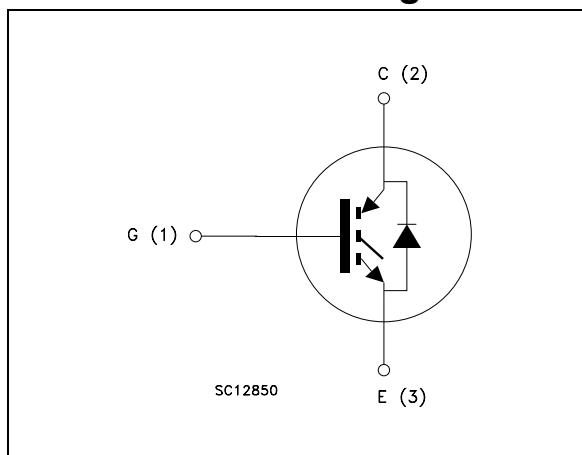
Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “S” identifies a family optimized achieve minimum on-voltage drop for low frequency applications (<1kHz).

## Applications

- Light dimmer
- Static relays
- Motor control



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STGF10NB60SD	GF10NB60SD	TO-220FP	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CES}$	Collector-emitter voltage ( $V_{GS} = 0$ )	600	V
$I_C$	Collector current (continuous) at 25°C	20	A
$I_C$	Collector current (continuous) at 100°C	7	A
$I_{CM}^{(1)}$	Collector current (pulsed)	100	A
$V_{GE}$	Gate-emitter voltage	$\pm 20$	V
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	25	W
$V_{ISO}$	Insulation withstand voltage A.C.(t = 1sec; $T_C=25^\circ\text{C}$ )	2500	V
$T_{stg}$	Operating junction temperature	- 55 to 150	°C
$T_j$	Storage temperature		

1. Pulse width limited by max. junction temperature.

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case Max	5	°C/W
Rthj-amb	Thermal resistance junction-ambient Max	62.5	°C/W

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 250\mu A, V_{GE} = 0$	600			V
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1mA, V_{GE} = 0$	20			V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	$V_{GE} = 15V, I_C = 5A, T_j = 25^{\circ}C$		1.15		V
		$V_{GE} = 15V, I_C = 10A, T_j = 25^{\circ}C$		1.35	1.8	V
		$V_{GE} = 15V, I_C = 10A, T_j = 125^{\circ}C$		1.25		V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 250\mu A$	2.5		5	V
$I_{CES}$	Collector-emitter leakage current ( $V_{CE} = 0$ )	$V_{CE} = \text{Max rating}, T_j = 25^{\circ}C$			10	$\mu A$
		$V_{CE} = \text{Max rating}, T_j = 125^{\circ}C$			100	$\mu A$
$I_{GES}$	Gate-emitter leakage current ( $V_{CE} = 0$ )	$V_{GE} = \pm 20V, V_{CE} = 0$			$\pm 100$	nA
$g_{fs}$	Forward transconductance	$V_{CE} = 25V, I_C = 10A$	5			S

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{ies}$ $C_{oes}$ $C_{res}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{CE} = 25V, f = 1MHz, V_{GE} = 0$		610		pF
				65		pF
				12		pF
$Q_g$	Total gate charge	$V_{CE} = 400V, I_C = 10A,$ $V_{GE} = 15V$		33		nC
$I_{CL}$	Turn-off SOA minimum current	$V_{clamp} = 480V, R_G = 1k\Omega,$ $T_j = 125^{\circ}C$	20			A

**Table 5. Switching on/off (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 480\text{ V}$ , $I_C = 10\text{ A}$ $R_G = 1\text{ K}\Omega$ , $V_{GE} = 15\text{ V}$ $T_J = 25^\circ\text{C}$ (see Figure 15)		0.7		$\mu\text{s}$
$t_r$	Current rise time			0.46		$\mu\text{s}$
$(di/dt)_{on}$	Turn-on current slope				8	$\text{A}/\mu\text{s}$
$E_{on}^{(1)}$	Turn-on switching losses				0.6	mJ
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 480\text{ V}$ , $I_C = 10\text{ A}$ $R_G = 1\text{ K}\Omega$ , $V_{GE} = 15\text{ V}$ $T_J = 25^\circ\text{C}$ (see Figure 15)		2.2		$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time			1.2		$\mu\text{s}$
$t_f$	Current fall time			1.2		$\mu\text{s}$
$E_{off}^{(2)}$	Turn-off switching losses				5.0	mJ
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 480\text{ V}$ , $I_C = 10\text{ A}$ $R_G = 1\text{ K}\Omega$ , $V_{GE} = 15\text{ V}$ $T_J = 125^\circ\text{C}$ (see Figure 15)		3.8		$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time			1.2		$\mu\text{s}$
$t_f$	Current fall time			1.9		$\mu\text{s}$
$E_{off}^{(2)}$	Turn-off switching losses				8.0	mJ

1.  $E_{on}$  is the turn-on losses when a typical diode is used in the test circuit in figure 2  $E_{on}$  include diode recovery energy. If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature ( $25^\circ\text{C}$  and  $125^\circ\text{C}$ )

2. Turn-off losses include also the tail of the collector current

**Table 6. Collector-emitter diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_f$	Forward current				7	A
$I_{fm}$	Forward current pulsed				56	A
$V_f$	Forward on-voltage	$I_f = 3.5\text{ A}$		1.4	1.9	V
		$I_f = 3.5\text{ A}$ , $T_J = 125^\circ\text{C}$		1.15		V
$t_{rr}$	Reverse recovery time	$I_f = 7\text{ A}$ , $V_R = 20\text{ V}$ , $T_J = 125^\circ\text{C}$ , $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 18)		50		ns
$Q_{rr}$	Reverse recovery charge			70		nC
$I_{rrm}$	Reverse recovery current				2.7	

## 2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

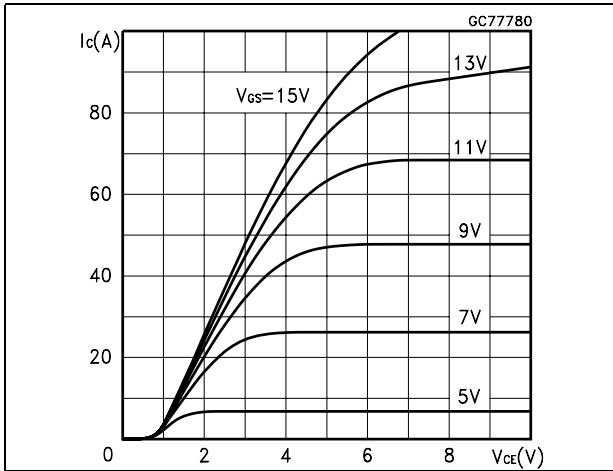


Figure 2. Transfer characteristics

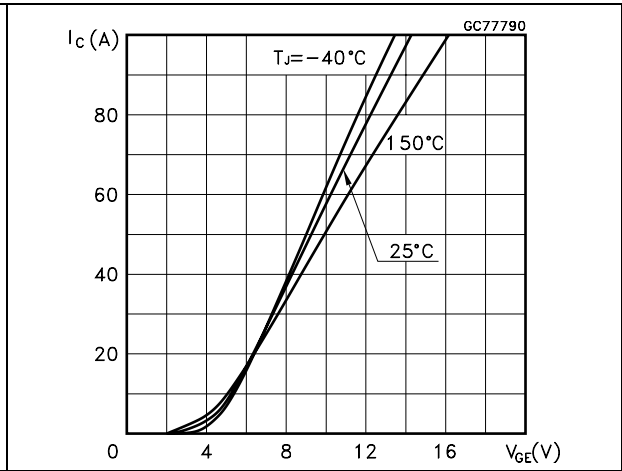


Figure 3. Transconductance

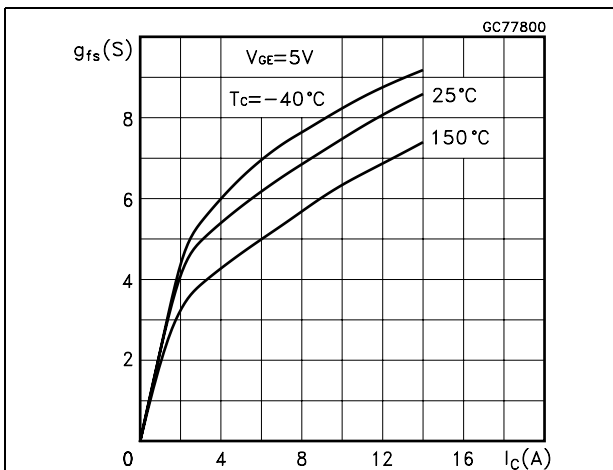


Figure 4. Collector-emitter on voltage vs temperature

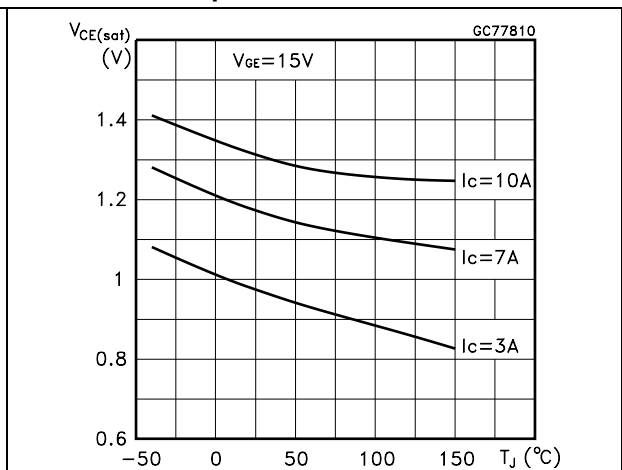


Figure 5. Collector-emitter on voltage vs collector current

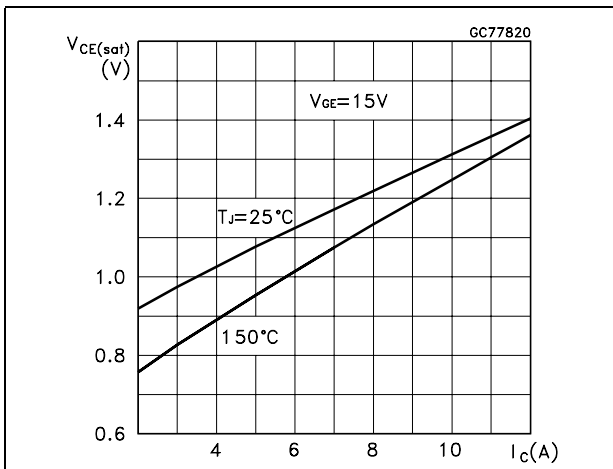


Figure 6. Normalized gate threshold vs temperature

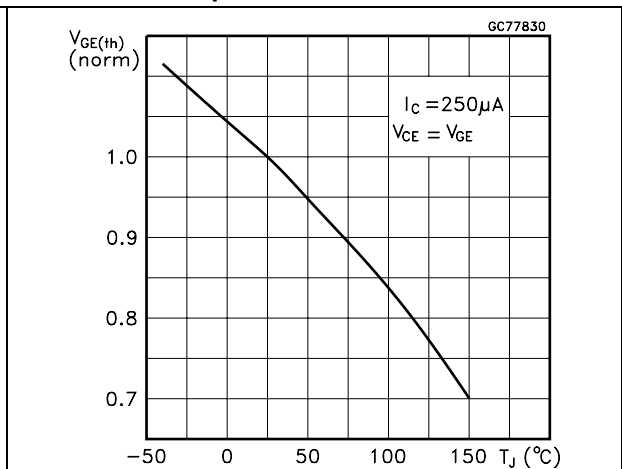


Figure 7. Normalized breakdown voltage vs temperature

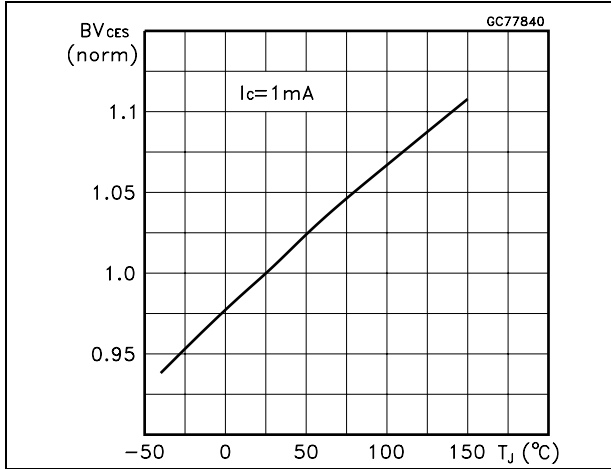


Figure 8. Gate charge vs gate-emitter voltage

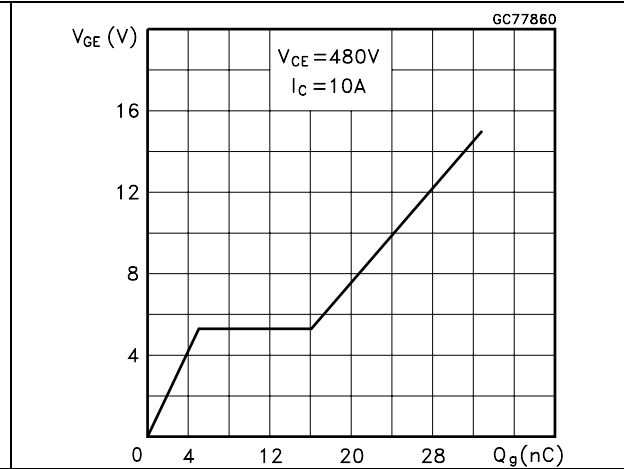


Figure 9. Capacitance variations

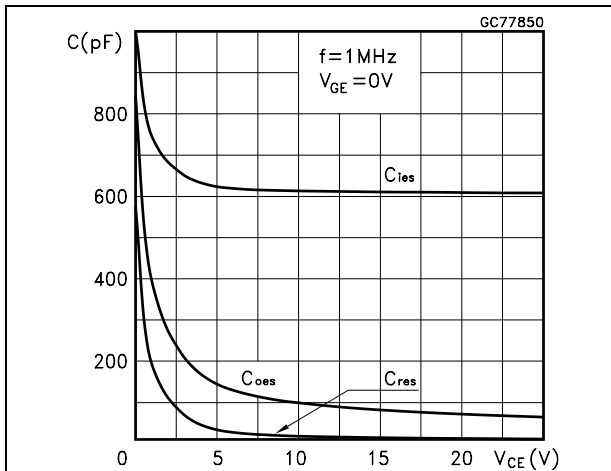


Figure 10. Switching losses vs temperature

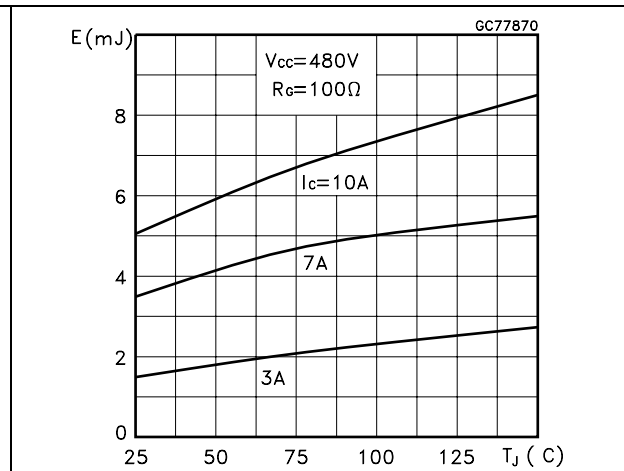


Figure 11. Switching losses vs gate resistance

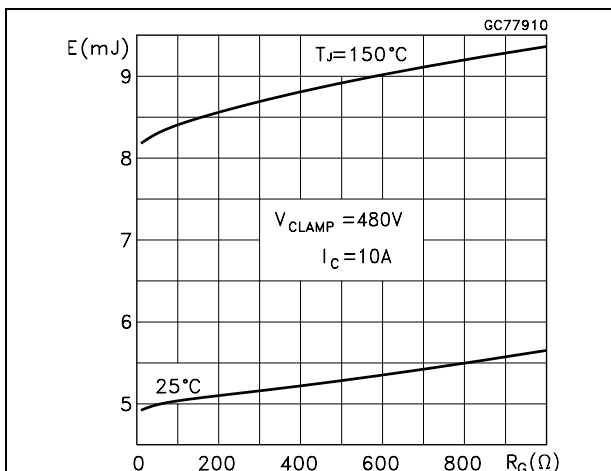


Figure 12. Switching losses vs collector current

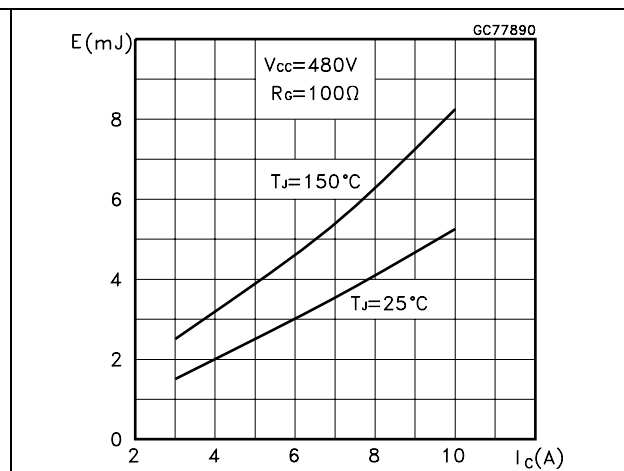


Figure 13. Thermal impedance

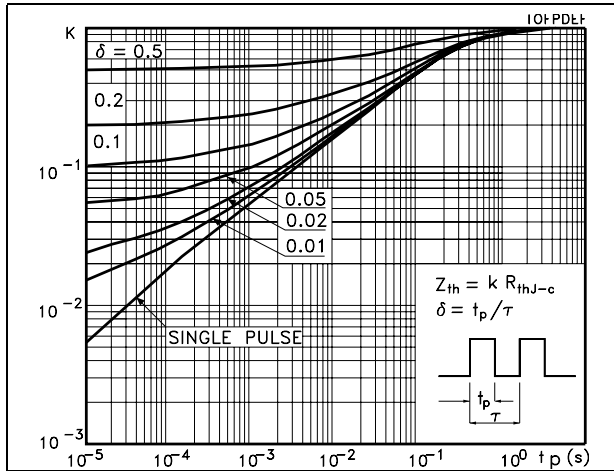
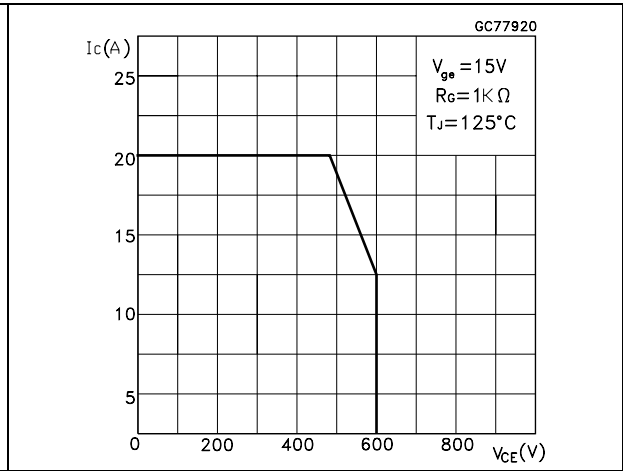


Figure 14. Turn-off SOA





### 3 Test circuit

Figure 15. Test circuit for inductive load switching

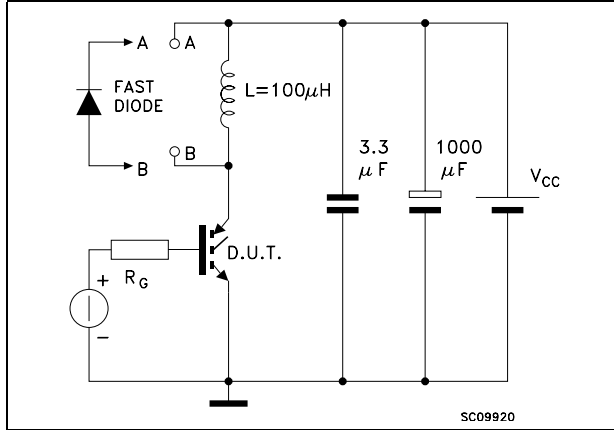


Figure 16. Gate charge test circuit

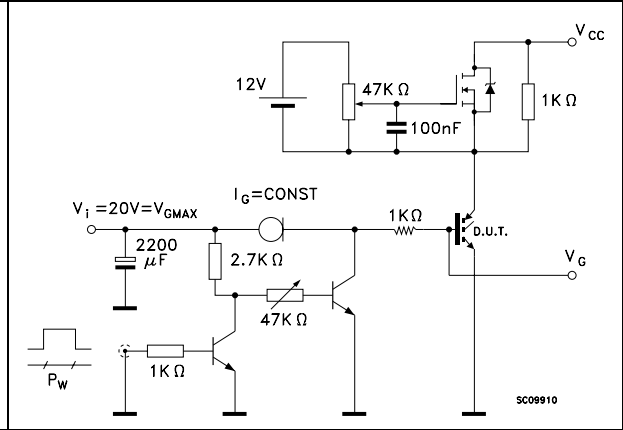


Figure 17. Switching waveforms

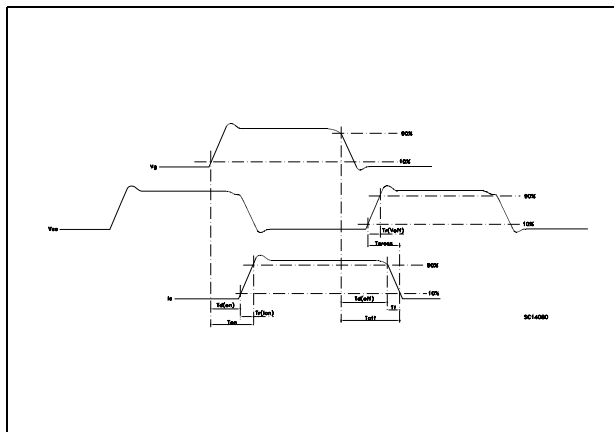
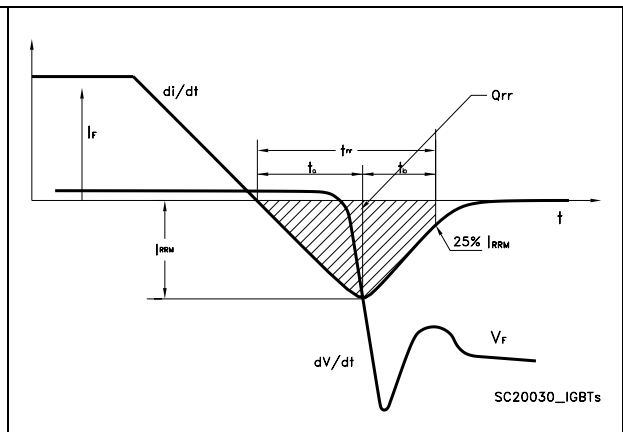


Figure 18. Diode recovery times waveform

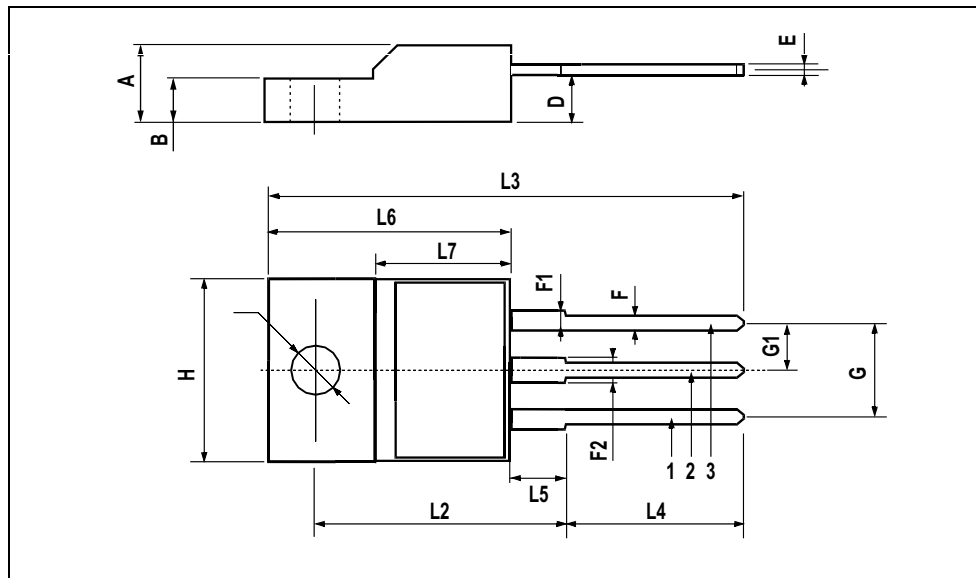


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

## TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



## 5 Revision history

Table 7. Revision history

Date	Revision	Changes
15-May-2006	2	New template

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