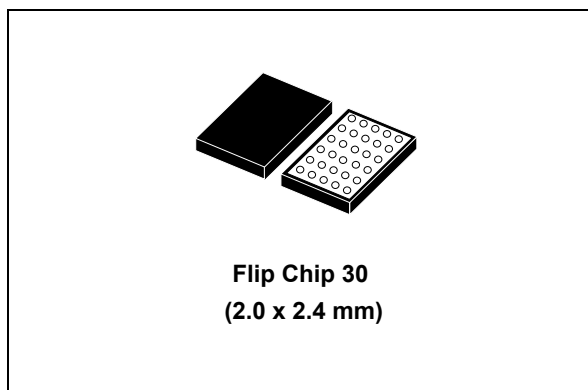


## Low voltage high bandwidth quad DPDT switch

Datasheet - production data



### Features

- Ultralow power dissipation
  - $I_{CC} = 1 \mu\text{A}$  (max.) at  $T_A = 85^\circ\text{C}$
- Low “ON” resistance
  - $R_{ON} = 5.4 \Omega$  ( $T_A = 25^\circ\text{C}$ ) at  $V_{CC} = 4.3 \text{ V}$
  - $R_{ON} = 6.6 \Omega$  ( $T_A = 25^\circ\text{C}$ ) at  $V_{CC} = 3.0 \text{ V}$
- Wide operating voltage range
  - $V_{CC}$  (OPR.) = 1.65 V to 4.3 V
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at  $V_{CC} = 2.3 \text{ V}$  to 3.0 V
- 4 select pins controlling 2 switches each
- Typical bandwidth (-3 dB) at 800 MHz on all channels
- USB (2.0) high speed (480 Mbps) signal switching compliant
- Integrated fail safe function
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance exceeds JESD22 2000-V human body model (A114-A)

### Applications

- Mobile phones

### Description

The STG3820 device is a high-speed CMOS low voltage quad analog DPDT (dual pole dual throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate C<sup>2</sup>MOS technology. It is designed to operate from 1.65 V to 4.3 V, making this device ideal for portable applications.

The SEL<sub>m-n</sub> input is provided to control the switches. The switches nS1 and mS1 are ON (connected to common ports D<sub>n</sub> and D<sub>m</sub> respectively) when the SEL<sub>m-n</sub> input is held high and OFF (high impedance state exists between the two ports) when the SEL<sub>m-n</sub> is held low. The switches nS2 and mS2 are ON (connected to common port D<sub>n</sub> and D<sub>m</sub> respectively) when the SEL<sub>m-n</sub> input is held low and OFF (high impedance state exists between the two ports) when the SEL<sub>m-n</sub> is held high.

The STG3820 device has an integrated fail safe function to withstand overvoltage condition when the device is powered off. Additional key features are fast switching speed, break-before-make-delay time and ultralow power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

**Table 1. Device summary**

Order code	Package	Packing
STG3820BJR	Flip Chip 30 (2.0 x 2.4 mm)	Tape and reel

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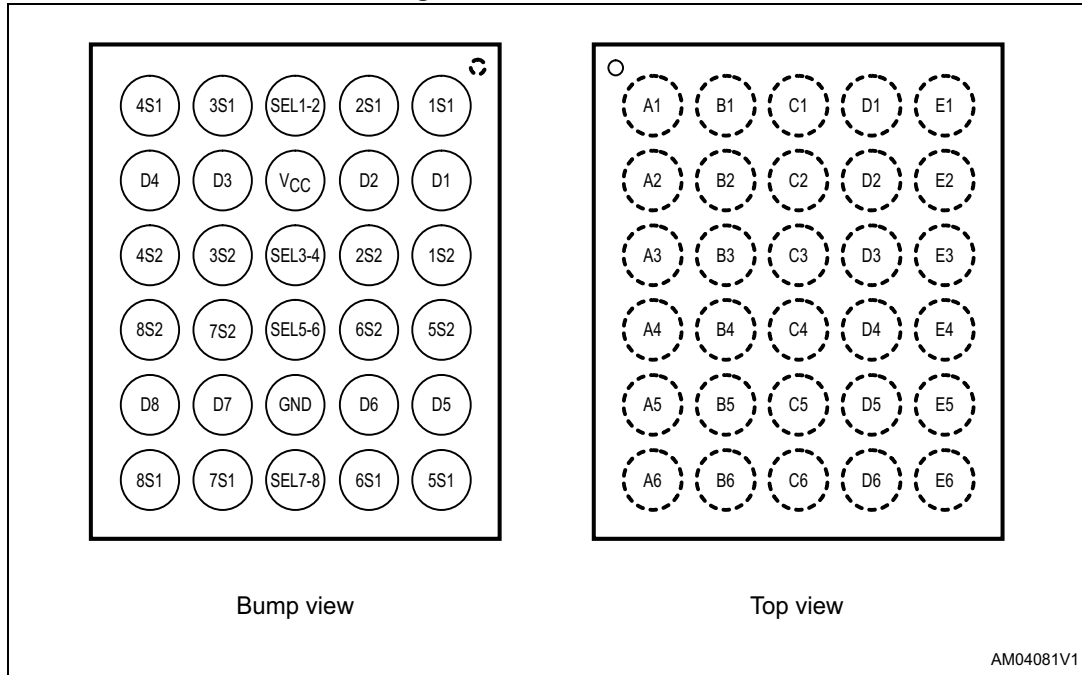
# Contents

<b>1</b>	<b>Pin settings</b> .....	<b>3</b>
	1.1 Pin connection .....	3
	1.2 Pin description .....	3
<b>2</b>	<b>Logic diagram</b> .....	<b>5</b>
<b>3</b>	<b>Maximum ratings</b> .....	<b>6</b>
	Recommended operating conditions .....	6
<b>4</b>	<b>Electrical characteristics</b> .....	<b>7</b>
<b>5</b>	<b>Test circuits</b> .....	<b>12</b>
<b>6</b>	<b>Package information</b> .....	<b>16</b>
<b>7</b>	<b>Revision history</b> .....	<b>19</b>

# 1 Pin settings

## 1.1 Pin connection

Figure 1. Pin connection



AM04081V1

## 1.2 Pin description

Table 2. Pin assignment

Pin number	Symbol	Name and function
A1	1S1	Independent channel for switch 1
A2	D1	Common channel for switch 1
A3	1S2	Independent channel for switch 1
A4	5S2	Independent channel for switch 5
A5	D5	Common channel for switch 5
A6	5S1	Independent channel for switch 5
B1	2S1	Independent channel for switch 2
B2	D2	Common channel for switch 2
B3	2S2	Independent channel for switch 2
B4	6S2	Independent channel for switch 6
B5	D6	Common channel for switch 6
B6	6S1	Independent channel for switch 6

Table 2. Pin assignment (continued)

Pin number	Symbol	Name and function
C1	SEL1-2	Switch 1-2 selection control
C2	VCC	Positive supply voltage
C3	SEL3-4	Switch 3-4 selection control
C4	SEL5-6	Switch 5-6 selection control
C5	GND	Ground (0 V)
C6	SEL7-8	Switch 7-8 selection control
D1	3S1	Independent channel for switch 3
D2	D3	Common channel for switch 3
D3	3S2	Independent channel for switch 3
D4	7S2	Independent channel for switch 7
D5	D7	Common channel for switch 7
D6	7S1	Independent channel for switch 7
E1	4S1	Independent channel for switch 4
E2	D4	Common channel for switch 4
E3	4S2	Independent channel for switch 4
E4	8S2	Independent channel for switch 8
E5	D8	Common channel for switch 8
E6	8S1	Independent channel for switch 8



### 3 Maximum ratings

Stressing the device above the rating listed in [Table 4: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Table 5: Recommended operating conditions](#) of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	-0.5 to 6.0	V
$V_I$	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
$V_{IC}$	DC control input voltage	-0.5 to 5.5	V
$V_O$	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IKC}$	DC input diode current on control pin ( $V_{SEL} < 0$ V)	-50	mA
$I_{IK}$	DC input diode current ( $V_{SEL} < 0$ V)	$\pm 50$	mA
$I_{OK}$	DC output diode current	$\pm 20$	mA
$I_O$	DC output current	$\pm 128$	mA
$I_{OP}$	DC output current peak (pulse at 1 ms, 10% duty cycle)	$\pm 300$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or ground current	$\pm 100$	mA
$P_D$	Power dissipation at $T_A = 70$ °C	1120	mW
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_L$	Lead temperature (10 sec.)	300	°C

### Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply voltage	1.65 to 4.3	V	
$V_I$	Input voltage	0 to $V_{CC}$	V	
$V_{IC}$	Control input voltage	0 to 4.3	V	
$V_O$	Output voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating temperature	-40 to 85	°C	
dt/dv	Input rise and fall time control input	$V_L = 1.65$ V to 2.7 V	0 to 20	ns/V
		$V_L = 3.0$ V to 4.3 V	0 to 10	

## 4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V <sub>CC</sub> (V)	Test conditions	Value					Unit
				T <sub>A</sub> = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	High level input voltage	1.65 – 1.95		0.65	–	–	0.65	–	V
		2.3 – 2.5		V <sub>CC</sub>	–	–	V <sub>CC</sub>	–	
		2.7 – 3.0		1.2	–	–	1.2	–	
		3.3 – 3.6		1.3	–	–	1.3	–	
		4.3		1.4	–	–	1.4	–	
V <sub>IL</sub>	Low level input voltage	1.65 – 1.95		–	–	0.25	–	0.25	V
		2.3 – 2.5		–	–	0.25	–	0.25	
		2.7 – 3.0		–	–	0.25	–	0.25	
		3.3 – 3.6		–	–	0.30	–	0.30	
		4.3		–	–	0.40	–	0.40	
R <sub>PEAK</sub>	Switch ON peak resistance	1.8	V <sub>S</sub> = 0 V to V <sub>CC</sub> I <sub>S</sub> = 8 mA	–	17.0	19.6	–	–	Ω
		2.7		–	7.5	8.7	–	–	
		3.0		–	6.6	7.6	–	–	
		3.7		–	5.8	6.7	–	–	
		4.3		–	5.4	6.2	–	–	
R <sub>ON</sub>	Switch ON resistance	3.0	V <sub>S</sub> = 3 V I <sub>S</sub> = 8 mA	–	5.1	5.8	–	–	Ω
		3.0	V <sub>S</sub> = 0.4 V I <sub>S</sub> = 8 mA	–	6.3	7.3	–	–	
ΔR <sub>ON</sub>	ON resistance match between channels <sup>(1)</sup>	1.8	V <sub>S</sub> at R <sub>ON</sub> MAX I <sub>S</sub> = 8 mA	–	–	–	–	–	Ω
		2.7		–	–	–	–	–	
		3.0		–	0.3	–	–	–	
		3.7		–	–	–	–	–	
		4.3		–	–	–	–	–	

Table 6. DC specifications (continued)

Symbol	Parameter	V <sub>CC</sub> (V)	Test conditions	Value					Unit
				T <sub>A</sub> = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
R <sub>FLAT</sub>	ON resistance flatness <sup>(2)</sup>	1.8	V <sub>S</sub> = 0 V to 0.4 V I <sub>S</sub> = 8 mA	–	4.5	–	–	–	Ω
		1.8	V <sub>S</sub> = 0 V to V <sub>CC</sub> I <sub>S</sub> = 8 mA	–	9.5	–	–	–	
		2.7		–	2.2	–	–	–	
		3.0		–	1.8	–	–	–	
		3.7		–	1.6	–	–	–	
		4.3		–	1.6	–	–	–	
I <sub>OFF</sub>	OFF state leakage current (Sn), (D)	4.3	V <sub>S</sub> = 0.3 or 4 V	-20	–	20	-100	100	nA
I <sub>IN</sub>	Input leakage current	0 to 4.3	V <sub>SEL</sub> = 0 to 4.3 V	-0.2	–	0.2	-1.0	1.0	μA
I <sub>CC</sub>	Quiescent supply current	1.65 to 4.3	V <sub>SEL</sub> = V <sub>CC</sub> or GND	-0.2	–	0.2	-1.0	1.0	μA
I <sub>CCLV</sub>	Quiescent supply current for low voltage driving <sup>(3)</sup>	4.3	V <sub>SEL</sub> = 1.65 V	–	±37	±50	–	±100	μA
			V <sub>SEL</sub> = 1.80 V	–	±33	±40	–	±50	
			V <sub>SEL</sub> = 2.60 V	–	±11	±20	–	±30	

1. ΔR<sub>ON</sub> = max. |mSN - nSN|, where m = 1 to 8 and n = 1 to 8, N = 1, 2.
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
3. Measurement is for one SEL pin.



Table 7. AC electrical characteristics ( $C_L = 35 \text{ pF}$ ,  $R_L = 50 \text{ } \Omega$ ,  $t_r = t_f \leq 5 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ (V)	Test conditions	Value					Unit
				$T_A = 25 \text{ } ^\circ\text{C}$			$-40 \text{ to } 85 \text{ } ^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	
$t_{PLH}$ , $t_{PHL}$	Propagation delay	1.65 - 1.95		–	0.21	–	–	–	ns
		2.3 - 2.7		–	0.15	–	–		
		3.0 - 3.3		–	0.14	–	–		
		3.6 - 4.3		–	0.13	–	–		
$t_{ON}$	Turn-on time	1.65 - 1.95	$V_S = 0.8 \text{ V}$	–	36	–	–	–	ns
		2.3 - 2.7	$V_S = 1.5 \text{ V}$	–	20	23	–	26	
		3.0 - 3.3		–	15	17	–	20	
		3.6 - 4.3		–	13	15	–	17	
$t_{OFF}$	Turn-off time	1.65 - 1.95	$V_S = 0.8 \text{ V}$	–	29	–	–	–	ns
		2.3 - 2.7	$V_S = 1.5 \text{ V}$	–	19	22	–	25	
		3.0 - 3.3		–	14	16	–	18	
		3.6 - 4.3		–	11	13	–	14	
$t_D$	Break-before-make time delay	1.65 - 1.95	$C_L = 35 \text{ pF}$ $R_L = 50 \text{ } \Omega$ $V_S = 1.5 \text{ V}$	–	10	–	–	–	ns
		2.3 - 2.7		–	7	–	–		
		3.0 - 3.3		–	6	–	–		
		3.6 - 4.3		–	4	–	–		
Q	Charge injection	1.65	$C_L = 100 \text{ pF}$ $V_{GEN} = 0 \text{ V}$ $R_{GEN} = 0 \text{ } \Omega$	–	3.9	–	–	–	pC
		2.3		–	4.8	–	–		
		3.0		–	5.2	–	–		
		4.3		–	6.4	–	–		

Table 8. AC electrical characteristics ( $C_L = 5 \text{ pF}$ ,  $R_L = 50 \text{ } \Omega$ ,  $T_A = 25 \text{ } ^\circ\text{C}$ )

Symbol	Parameter	$V_{CC}$ (V)	Test conditions	Value					Unit
				$T_A = 25 \text{ } ^\circ\text{C}$			$-40 \text{ to } 85 \text{ } ^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	
OIRR	OFF isolation <sup>(1)</sup>	1.65 – 4.3	$V_S = 1 \text{ V}_{RMS}$ , $f = 1 \text{ MHz}$ signal = 0 dBm	–	-78	–	–	–	dB
			$V_S = 1 \text{ V}_{RMS}$ , $f = 10 \text{ MHz}$ signal = 0 dBm	–	-57	–	–	–	
Xtalk	Crosstalk	1.65 – 4.3	$V_S = 1 \text{ V}_{RMS}$ , $f = 1 \text{ MHz}$ signal = 0 dBm	–	-78	–	–	–	dB
			$V_S = 1 \text{ V}_{RMS}$ , $f = 10 \text{ MHz}$ signal = 0 dBm	–	-58	–	–	–	
BW	-3dB bandwidth	3.0 – 4.3	$R_L = 50 \text{ } \Omega$ signal = 0 dBm	–	800	–	–	–	MHz
$C_{IN}$	Control pin input capacitance		$V_{CC} = 0 \text{ V}$	–	2	–	–	–	pF
$C_{Sn}$	Sn port capacitance	3.3	F = 240 MHz, switch is enabled	–	6	–	–	–	pF
			F = 240 MHz, switch is disabled	–	2	–	–	–	
$C_D$	D port capacitance	3.3	F = 240 MHz	–	8	–	–	–	pF

1. Off isolation =  $20 \text{ Log}_{10} (V_D/V_S)$ ,  $V_D$  = output,  $V_S$  = input to off switch.

Table 9. USB related AC electrical characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Test conditions	Value					Unit
				T <sub>A</sub> = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t <sub>SK(0)</sub>	Channel-to-channel skew	3.0 - 3.6	C <sub>L</sub> = 10 pF	–	26	–	–	–	ps
t <sub>SK(P)</sub>	Skew of opposite transition of the same output	3.0 - 3.6	C <sub>L</sub> = 10 pF	–	60	–	–	–	ps
T <sub>J</sub>	Total jitter	3.0 - 3.6	R <sub>L</sub> = 50 Ω C <sub>L</sub> = 10 pF t <sub>R</sub> = t <sub>F</sub> = 750 ps at 480 Mbps	–	130	–	–	–	ps

# 5 Test circuits

Figure 3. On-resistance

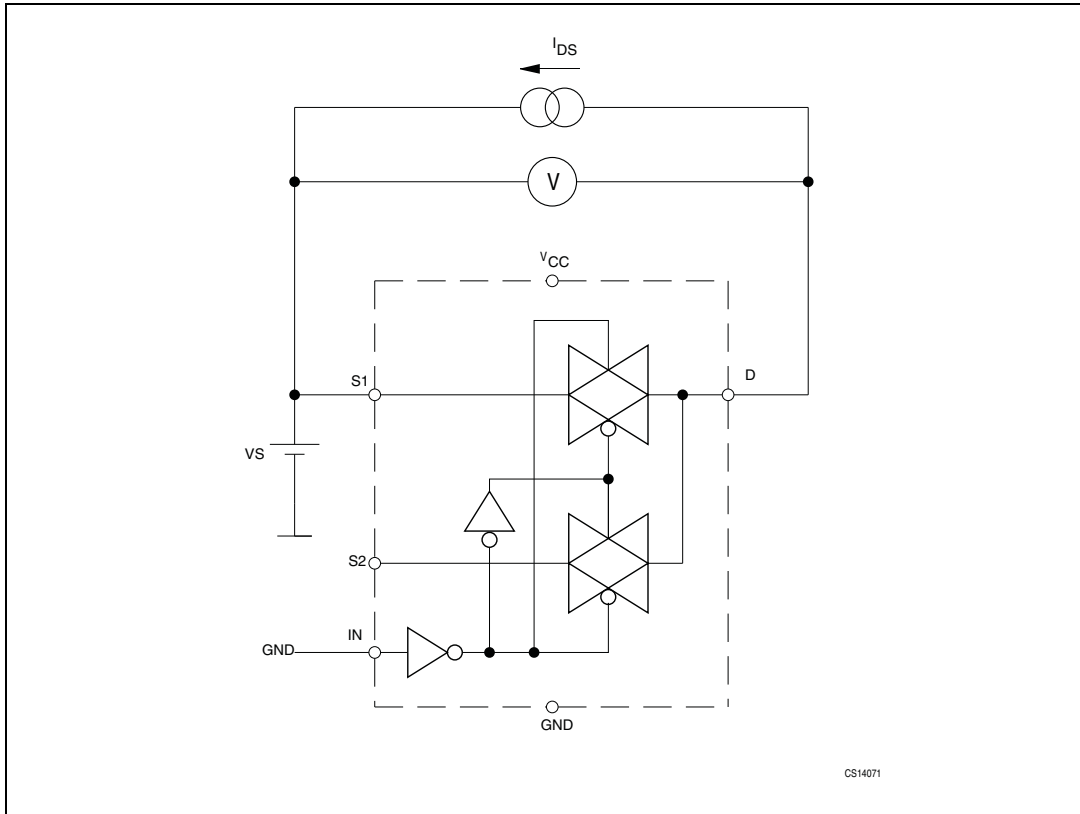


Figure 4. Bandwidth

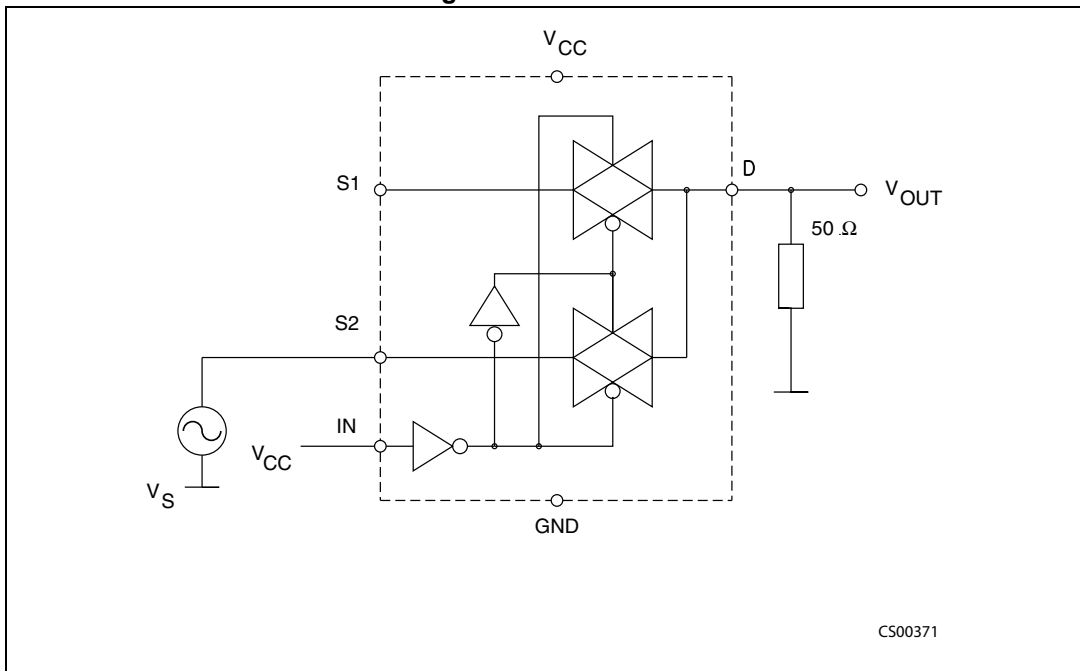


Figure 5. Off leakage

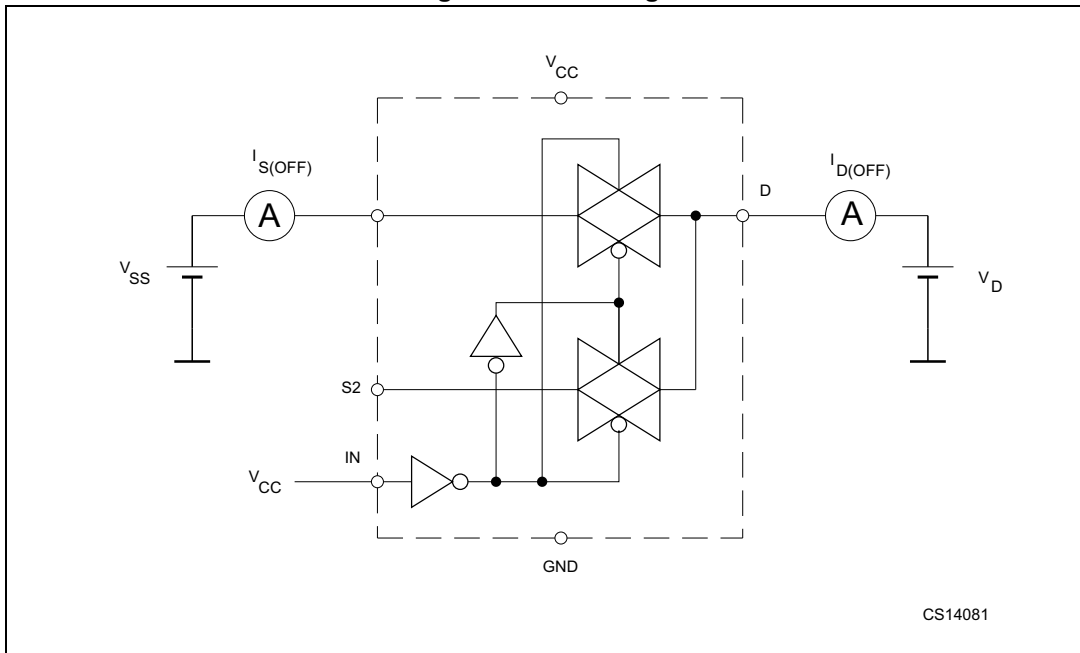


Figure 6. Channel to channel crosstalk

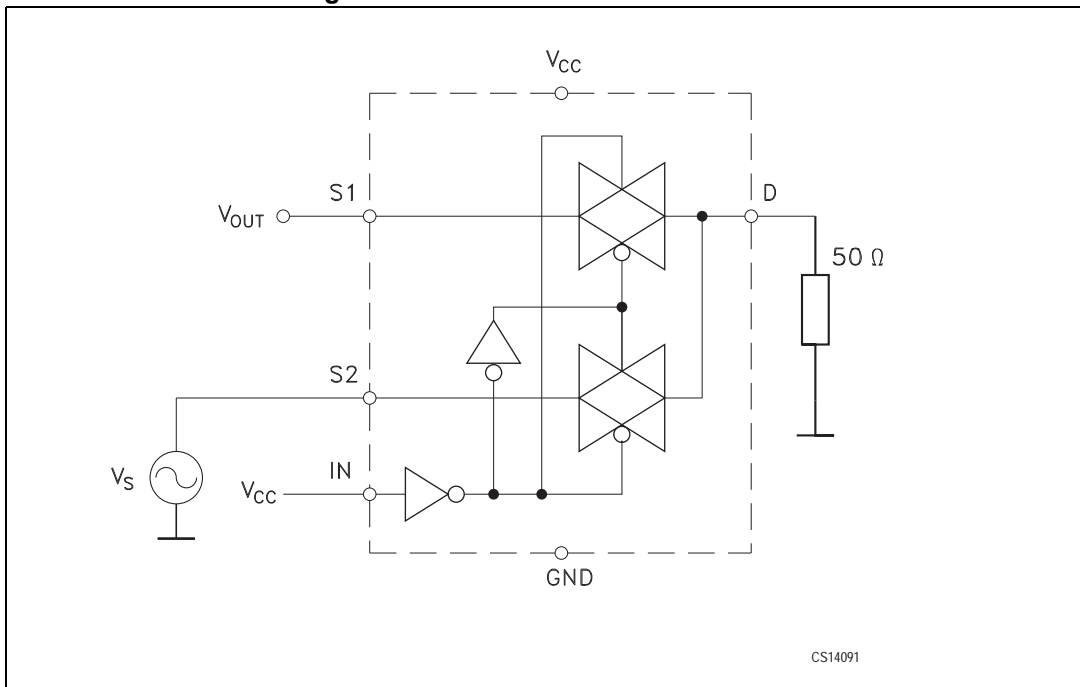


Figure 7. Off isolation

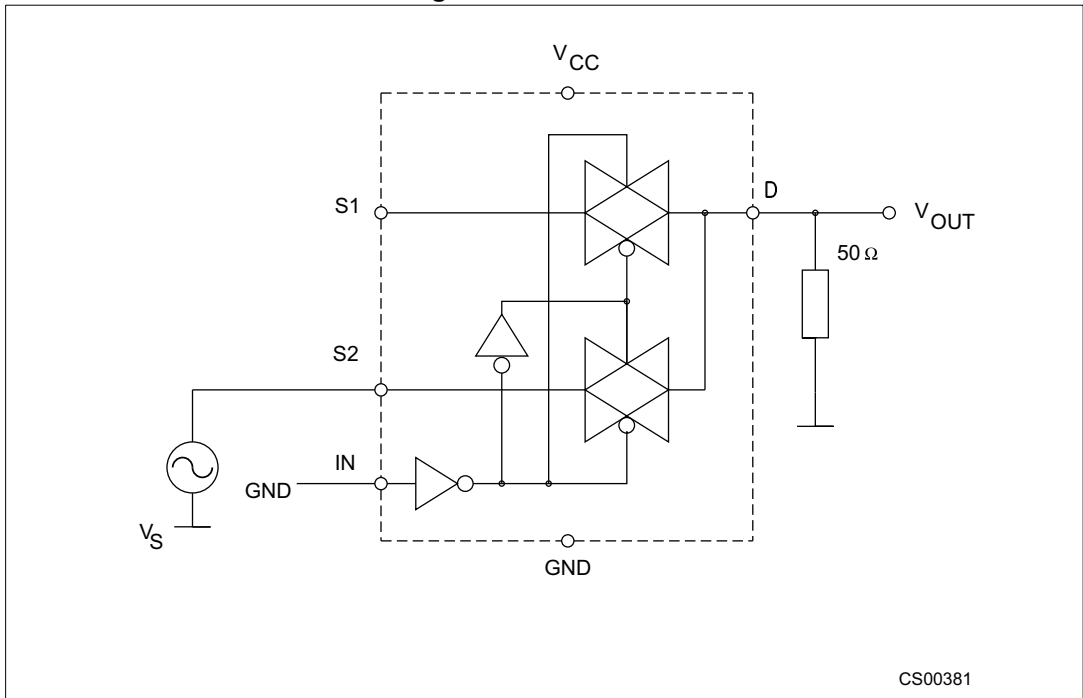
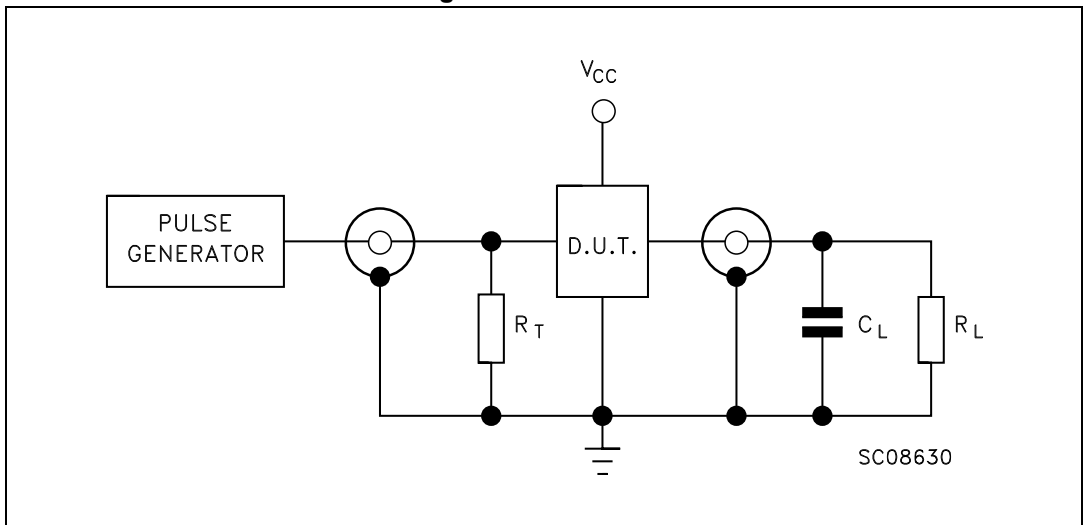


Figure 8. Test circuit



Note:  $C_L = 5/35\text{ pF}$  or equivalent: (includes jig capacitance).  
 $R_L = 50\ \Omega$  or equivalent.  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\ \Omega$ ).

Figure 9. Break-before-make time delay

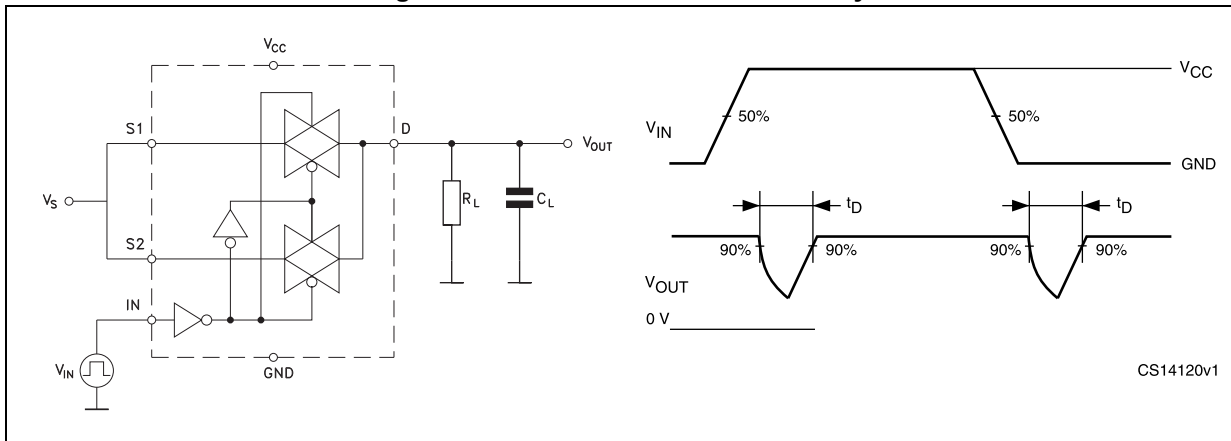


Figure 10. Switching time and charge injection ( $V_{GEN} = 0\text{ V}$ ,  $R_{GEN} = 0\ \Omega$ ,  $R_L = 1\text{ M}\Omega$ ,  $C_L = 100\text{ pF}$ )

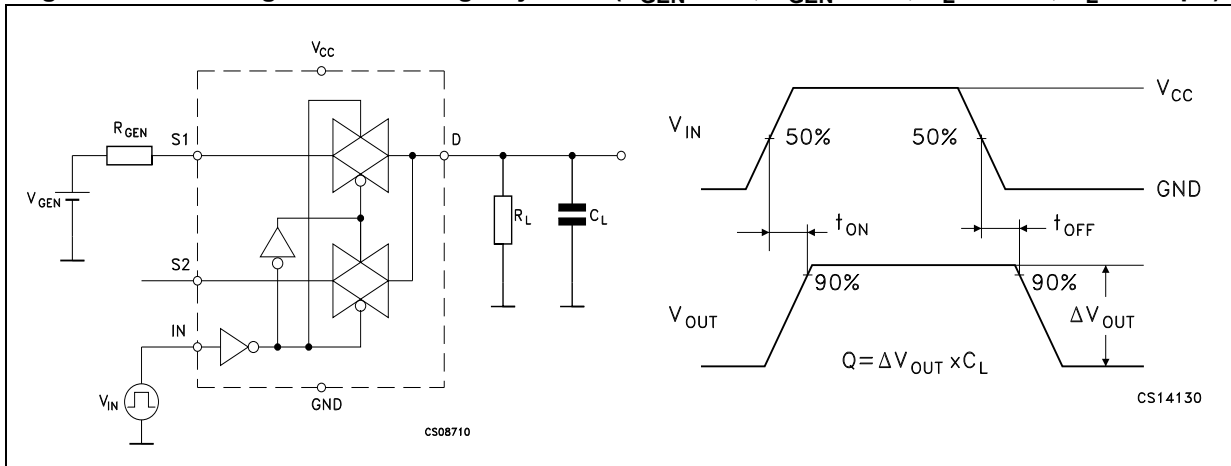
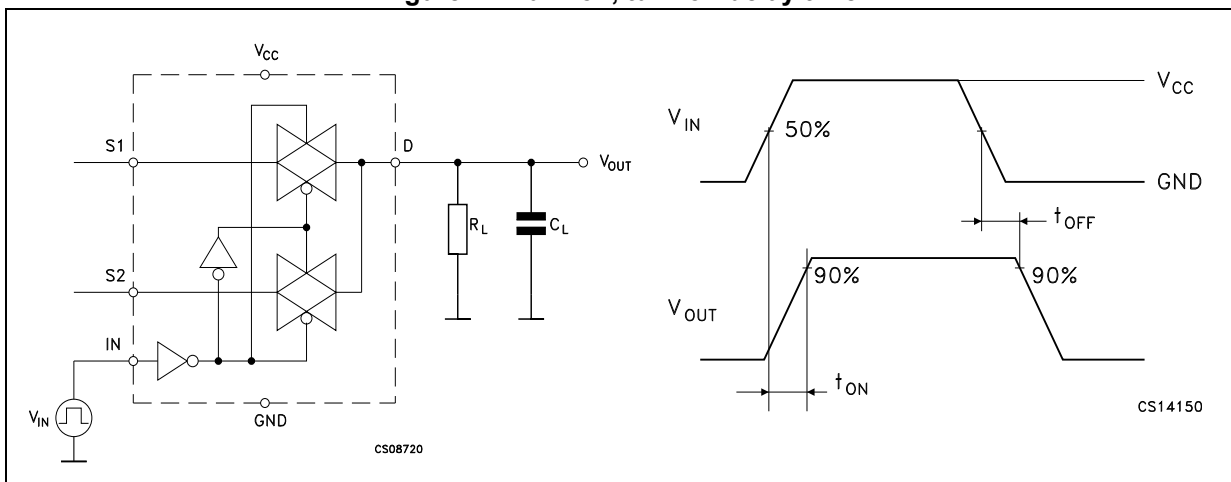


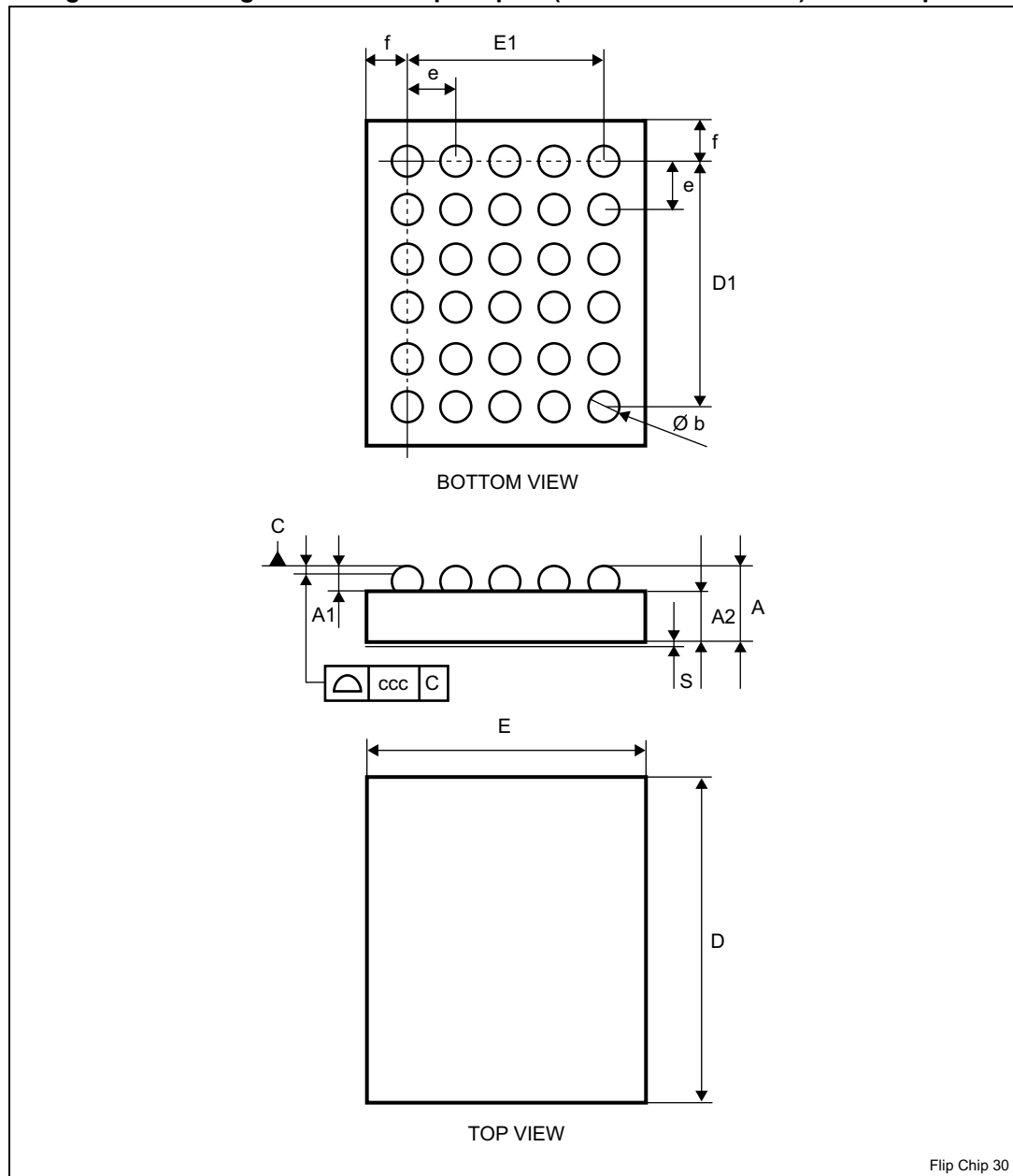
Figure 11. Turn-on, turn-off delay time



## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Figure 12. Package outline for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch**





**Table 10. Mechanical data for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch**

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.565	0.625	0.685
A1	0.17	0.205	0.24
A2	0.355	0.375	0.395
b	0.215	0.255	0.295
D	2.1	2.4	2.43
D1	–	2.0	–
E	1.97	2.0	2.03
E1	–	1.6	–
e	0.36	0.4	0.44
f	0.19	0.2	0.21
ccc	–	0.05	–
\$	0.040	0.045	0.05

**Figure 13. Footprint recommendations for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch**

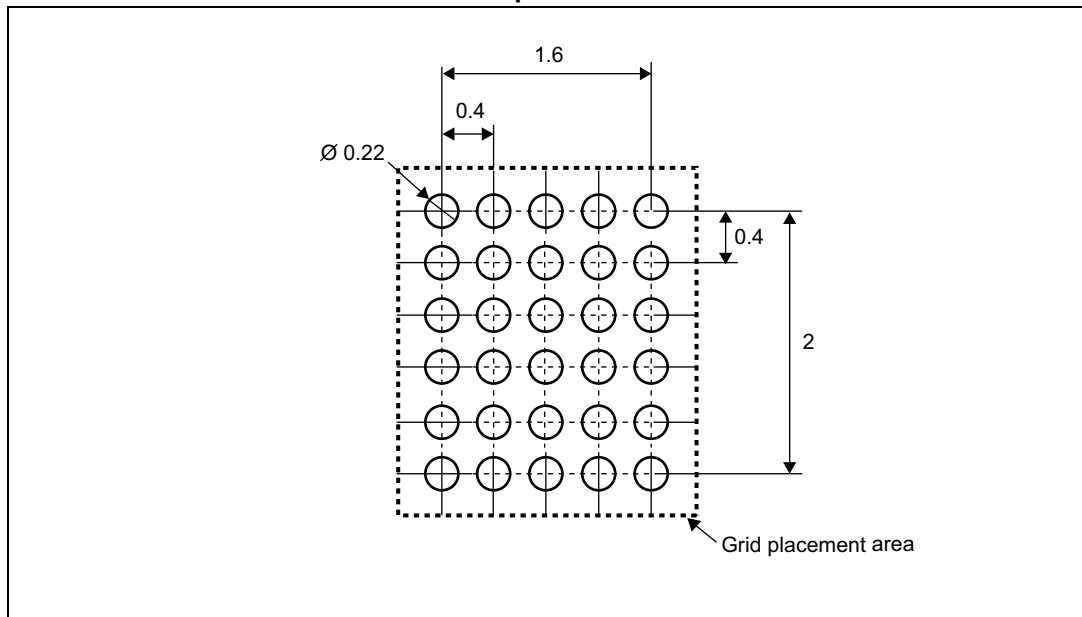


Figure 14. Tape information for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch

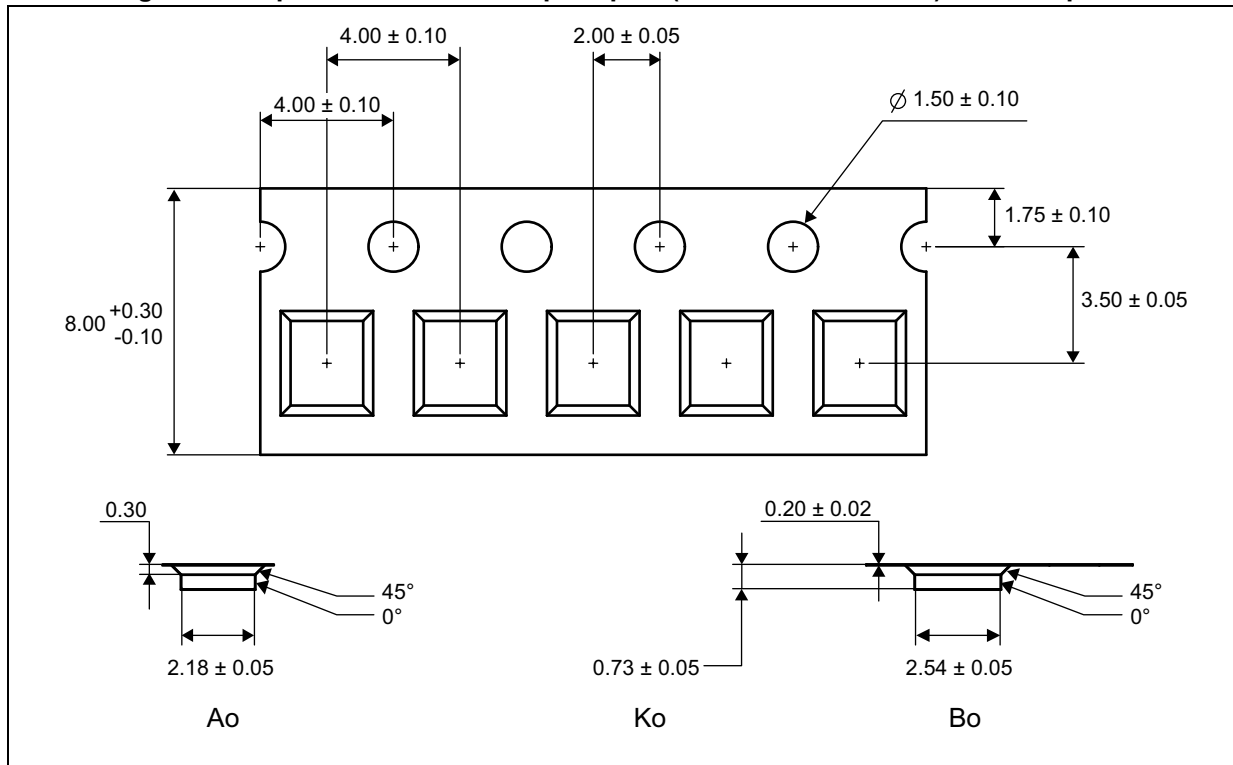
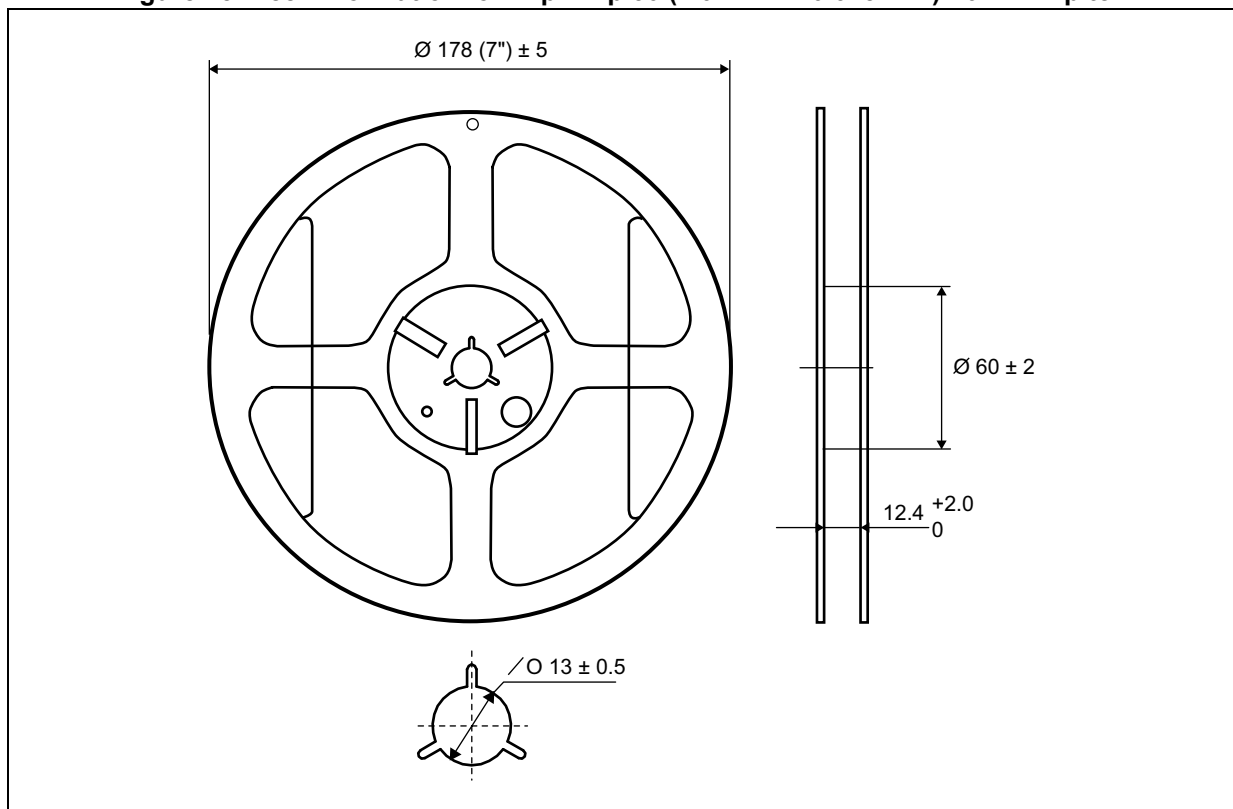


Figure 15. Reel information for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch



## 7 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
18-Dec-2009	1	Initial release.
19-Jan-2011	2	Document reformatted, added <a href="#">Contents</a> , updated <a href="#">Figure 12</a> and <a href="#">Figure 13</a> , corrected typo in <a href="#">Features</a> , <a href="#">Table 1</a> , <a href="#">Section 1: Pin settings</a> , <a href="#">Table 2</a> , <a href="#">Table 7</a> , <a href="#">Table 8</a> , notes below <a href="#">Figure 8</a> , title of <a href="#">Figure 11</a> , <a href="#">Figure 12</a> , <a href="#">Table 10</a> , and <a href="#">Figure 13</a> , corrected name of "Table 11" to <a href="#">Figure 13</a> .
23-Apr-2013	3	Moved <a href="#">Description</a> to page 1. Redrawn <a href="#">Figure 1</a> . Updated <a href="#">Section 3</a> (added/updated cross-references, updated $V_{CC}$ value in <a href="#">Table 4</a> ). Redrawn <a href="#">Figure 12</a> to <a href="#">Figure 15</a> . Updated <a href="#">Figure 12</a> (removed superfluous reference to note). Updated title of <a href="#">Figure 14</a> and <a href="#">Figure 15</a> (added "Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch"). Minor corrections throughout document.
06-Aug-2013	4	Updated <a href="#">Table 8 on page 10</a> (replaced $C_{ON}$ and $C_{OFF}$ symbol by $C_{sn}$ and $C_D$ symbol).

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