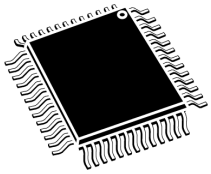
STFPC311

Front panel controller/driver with standby power management

Features

- IC front panel controller/driver
- Timing power standby management controller
- IC power supply from 3.3V (V_{DD}) to –30V (V_{SS})
- Integrated VFD driver and controller
- Infrared (IR) Remote Control (RC) Decoder (Philips or NEC format)
- Drives many display modes (12 segments/16 digits to 20 segments/8 digits)
- High voltage outputs (V_{DD} - 33.3V max)
- No external resistors necessary for driver outputs (P-channel open- drain with pull-down resistor outputs)
- Key scanning (up to 12mm x 2mm matrix)
- Led ports (4 channels, 20mA, max)
- Serial interface (STB, CLK, D_{IN}, and D_{OUT}) communication protocol
- Dimming circuit (adjustable up to 8 steps)
- Supports auto-increment of display digit, which lightens the load on the MCU
- Programmable 8 hot keys for the IR remote control command
- Programmable 8 hot keys for key scan command
- Low power consumption in standby mode
- 2 general purpose input ports (SW1, SW2)
- Available in PQFP-52 package



PQFP-52

Description

The STFPC311 is a complete, low-cost, integrated solution for controlling and driving a front panel Vacuum Fluorescent Display (VFD). It is ideal for decreasing power consumption in standby mode by reducing the application standby current to a minimum. It also contains a built-in remote control decoder module.

While in the standby mode of operation, a valid key press or signal from infrared decoder will start a proper power-up see *Figure 6 on page 12*.

The STFPC311 integrates a VFD controller with a driver that is run on a 1/8 to 1/16-duty factor. It consists of 12 segments output lines, 8 grid output lines, 8 shared segments/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the STFPC311 through the SPI Interface of a microcontroller (STB, D_{IN}, D_{OUT}, and CLK).

Additionally, this IC can support 2 general purpose input switches (SW1 and SW2).

Features

- DVD players
- VCD players
- AV equipment like Home Stereo
- POS Systems

Order Codes

Part number	Temperature range	Package
STFPC311	-40 to 85°C	PQFP-52

Contents

1 Functional description

The STFPC311 receives serial data from the microcontroller through the SPI interface, latches the data, and then masks the inputs from the MCU. This data consists of commands followed by data. There are 4 types of commands:

- configuration,
- data,
- address, and
- display.

The STFPC311 integrates the supply standby power management functionality, remote control decoder, and a 28-bit VFD driver. Microcontrollers usually run the first two tasks.

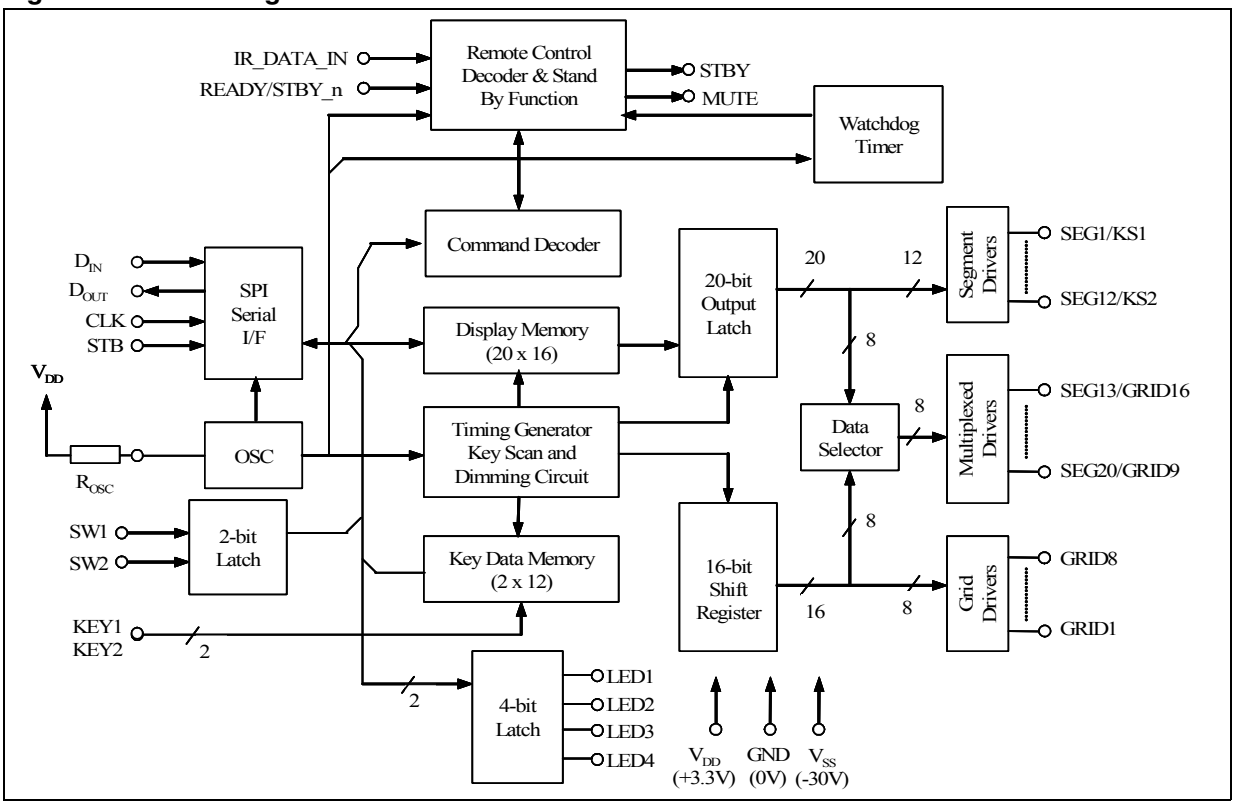
This device reduces the stand-by power consumption of the whole Front Panel application as well as the hardware by integrating the infrared (IR) remote control decoder.

A dedicated supply voltage powers the STFPC311 directly from the main supply board. When power is plugged in, control of the power supply management is done using the following pins:

1. STBY,
2. IR_DATA_IN, and
3. READY.

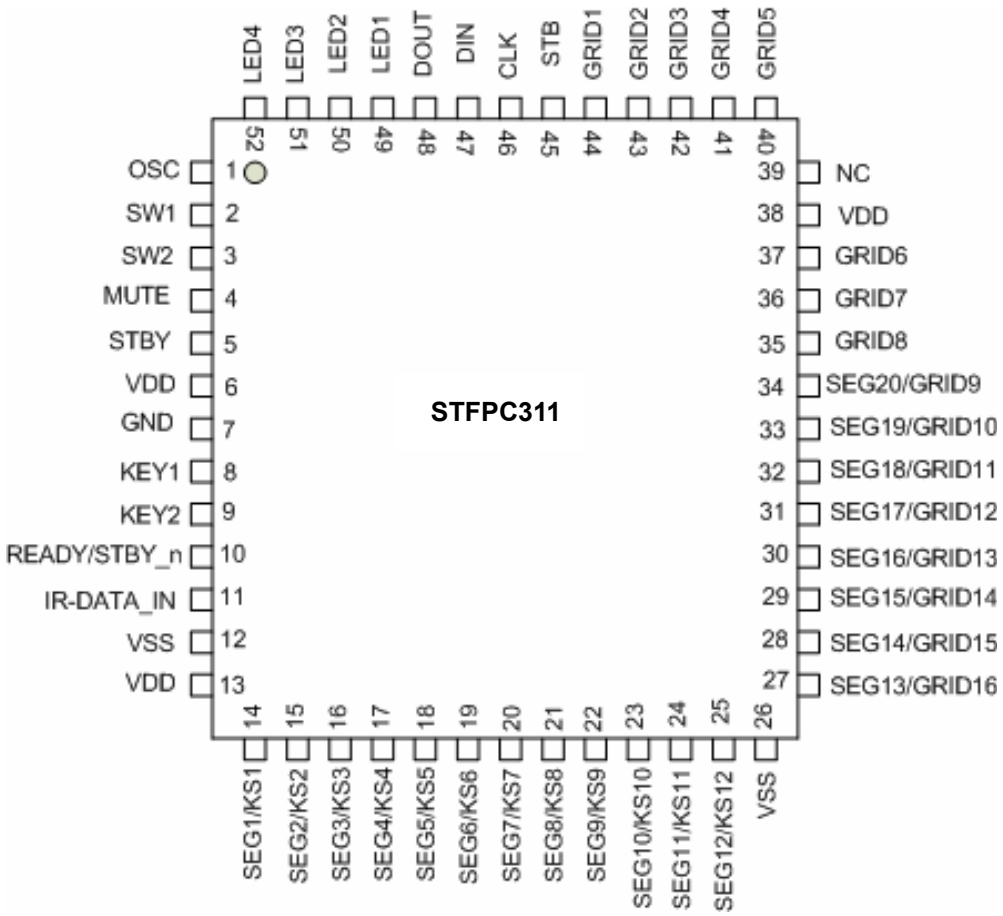
1.1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Connection diagram (top view PQFP-52)



Note: For a description of the behavior of each pin, refer to the Table 1: Pin description on page 6.

2.1 Pin description

Table 1. Pin description

Pin №	Symbol	Type	Name and function
1	OSC	I	This is the oscillator input pin. Connect this pin to an external resistor.
2, 3	SW1, SW2	I	General purpose switch input ports.
4	MUTE	O	High level indicates mute status for audio. Low level indicates normal working.*Note 1*
5S	TBY	O	there is a typo. Pin5 and name is STBY. Standby output to put the MCU in low power mode. It is a command to the main power board. High level indicates stand-by status. Low level indicates normal working. *Note 1*
7	GND	POWER	Connect this pin to system GND.
8, 9	KEY1, KEY2	I	Input data to these pins from external keyboard are latched at end of the display cycle (maximum keyboard size is 12 x 2).
10	READY	I	High level on this pin means that main board chip has been working normally.*Note 1* This pin should never float. It is recommended have a pull-down resistor on this input.
1	IR_DATA_IN	I	Remote control input. Feeds the IR data from photodiode to this pin.
14 to 25	SEG1/KS1 to SEG12/KS12	O	Segment output pins (dual function as key source).
12, 26	V_{SS}	POWER	V_{FD} outputs high voltage pull-down level. V_{DD}--33.3V max.
27 to 34	SEG13/GRID16 to SEG20/GRID9	O	These pins are selectable for segment or grid driving.
35 to 37	GRID8 to GRID6	O	Grid output pins.
6, 13,38	V_{DD}	POWER	3.3V ± 0.3V Core main supply voltage.
39	NC	O	Not used. Left unconnected.
40 to 44	GRID5 to GRID1	O	Grid output pins.
45	STB	I	Initializes the serial interface at the rising or falling edge to make the STFPC31 wait for reception of command. The data input after the falling edge of STB is processed as a command. While the command data is processed, current processing is stopped, and the serial interface is initialized. While STB is high, CLK is ignored and any instruction from the MCU is neglected.
46	CLK	I	Reads serial data at the rising edge, and outputs data at the falling edge.
47	D_{IN}	I	Inputs serial data at the rising edge of the shift clock, starting from the lower bit.
48	D_{OUT}	O	Outputs serial data at the faling edge of the shift clock, starting from the lower bit. This is the N-channel opendrain output pin.
49-52	LED1, LED2, LED3, LED4	O	CMOS outputs (20mA, max).

Note: 1 For a detailed behavioral description of these pins, refer to the "STFPC311 Timing Power Stand-by Sequencer Flow-Chart". See Table 6 on page 12

3 Initialization

After the power is plugged in, the device will supply power to all of the components (including the host processor) by setting STBY to logic low in order to allow the host processor to program the STFPC311. Once the STBY is set to low, the watchdog timer starts to count up to 10s (10s is the default value of the watchdog timer upon power-up). When the READY is asserted within this time, it indicates that the system has booted up well. If the READY pin is not asserted (logic high) within this time (10s), the STFPC311 will put the system into standby mode again by setting STBY to logic high.

If READY is detected as logic high, the watchdog timer will be turned OFF. The main processor should program the remote control hot key and initialize the other parameters of the STFPC311 in preparation for normal operation before the system goes into standby mode. After all of the STFPC311 configuration is finished, the host processor may set the READY to low so that the STFPC311 enters standby mode. The STFPC311 then sets the MUTE pin to logic high to mute the audio output as well as the STBY pin to logic high. As a consequence of this action, the main supply voltage is turned off.

3.1 Normal mode of operation

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3.2 Receive operation

In receive condition, the STFPC311 waits for a valid command from the MCU. The receive circuit of STFPC311 receives 8 bit serial data, latches the data and then masks the inputs from the MCU. Refer to *Figure 28 on page 32* for receive timing.

3.3 Transmit operation

In transmit condition, the STFPC311 sends the 8-bit serial data (LSB transmitted first) whenever a key is pressed or IR data is received. STFPC311 transmits data on the falling edge of CLK. Refer to *Figure 29 on page 32* for transmit timing.

3.4 Standby or power-down mode

Once the STFPC311 detects the status change of the READY to a logic low or after the preset waiting time (1s to 15s) has elapsed, the STFPC311 sets the STBY pin to a logic high to turn off the power. The MUTE signal is set to high before the power is turned off. The STFPC311 always senses the level on the READY pin during normal operation.

3.5 IR Decoding

Encoded IR data from photodiode is supplied to the IR_DATA_IN input pin. The data is decoded by the internal remote control decoder module of STFPC311. In standby mode, the remote control decoder recognizes a set of predefined commands (such as STANDBY, PLAY, and OPEN/CLOSE), and takes appropriate action to manage the power supply.

These predefined commands are known as "hot keys" and are programmable. The decoded IR commands are passed on to the main processor through the SPI interface by sending 3 bytes of data on the D_{OUT} pin.

3.6 Watchdog timer

The watchdog timer is used to detect an out-of-control microprocessor. The watch dog timer is implemented in the STFPC311 to detect the abnormal processor behavior or processor-hung condition. The default state of the watchdog timer is 10s when the device powers-up. It is initialized by writing to the watchdog register and can be programmed to up to 15s (4-bit watchdog timer, present in the configuration mode setting command).

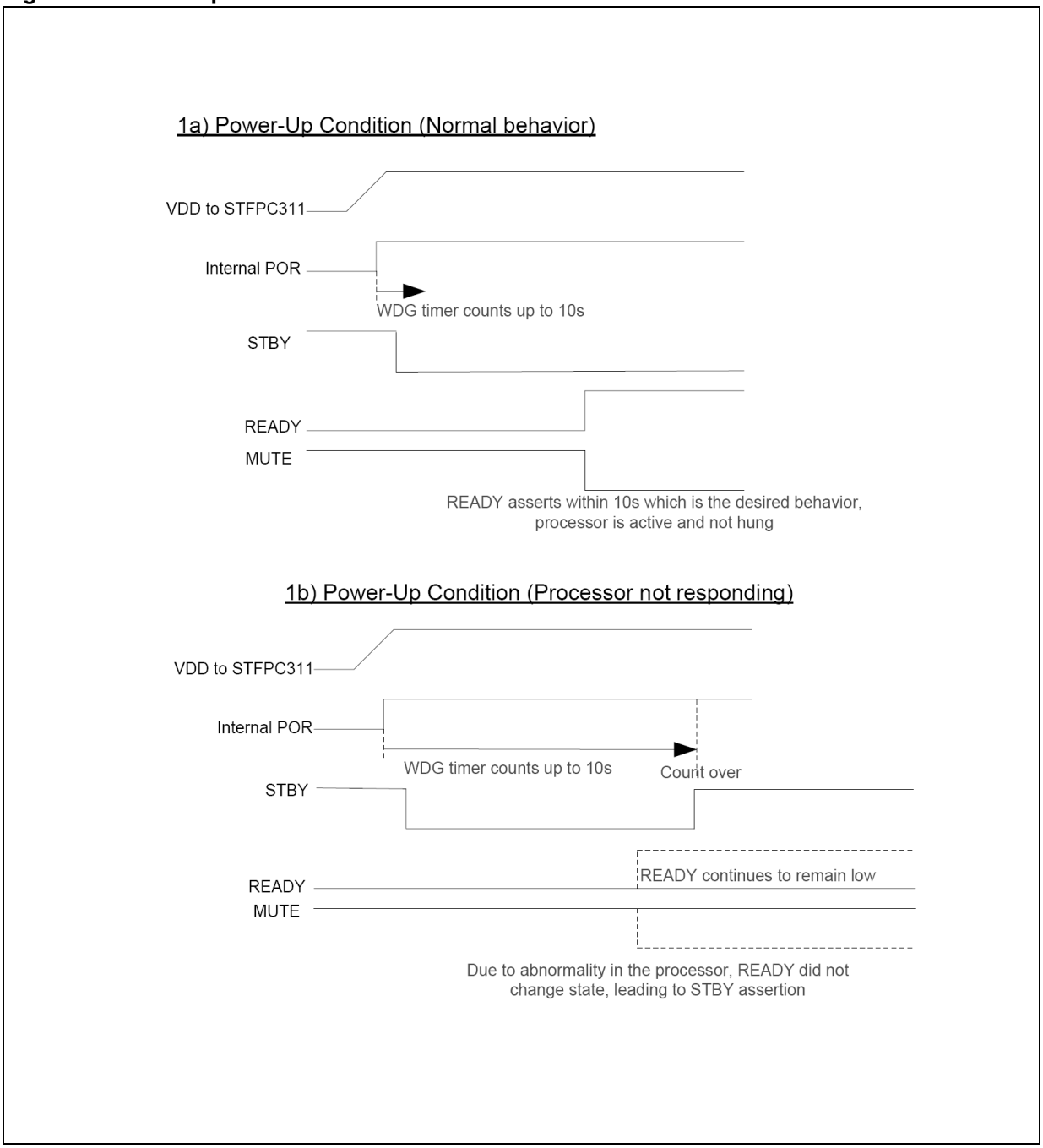
If the processor does not reset the timer within the specified period, the STFPC311 will put the entire system into standby mode to reset the appliance that has stopped abnormally. The action to take when the watchdog timer has reached its count is to set the Watchdog Action register. The watchdog timer can be reset by the host processor by sending a command to reset the watchdog timer. The time-out period then starts over again. If the processor needs to be reset as a result of a hung condition (signalled using the STBY output of the STFPC311), the watchdog timer uses the amount of the time-out programmed into the Watchdog Register by the user to generate an interrupt.

Note: The accuracy of the timer is within ±10% the selected resolution. This depends on the value of the external bias resistor, as it determines the internal clock frequency.

The watchdog function is automatically set to 10s upon power-up and the Watchdog Interrupt is cleared. This boot-up watchdog timer is used to make sure that if the host processor hangs during the first boot-up, the STFPC311 will put the system to standby mode. During the first boot-up, the watchdog timer is disabled after the first READY signal is received.

3.6.1 Watchdog timer operation during power-up

Figure 3. Power-up condition



Note: Watchdog timer is turned off by default upon READY assertion.

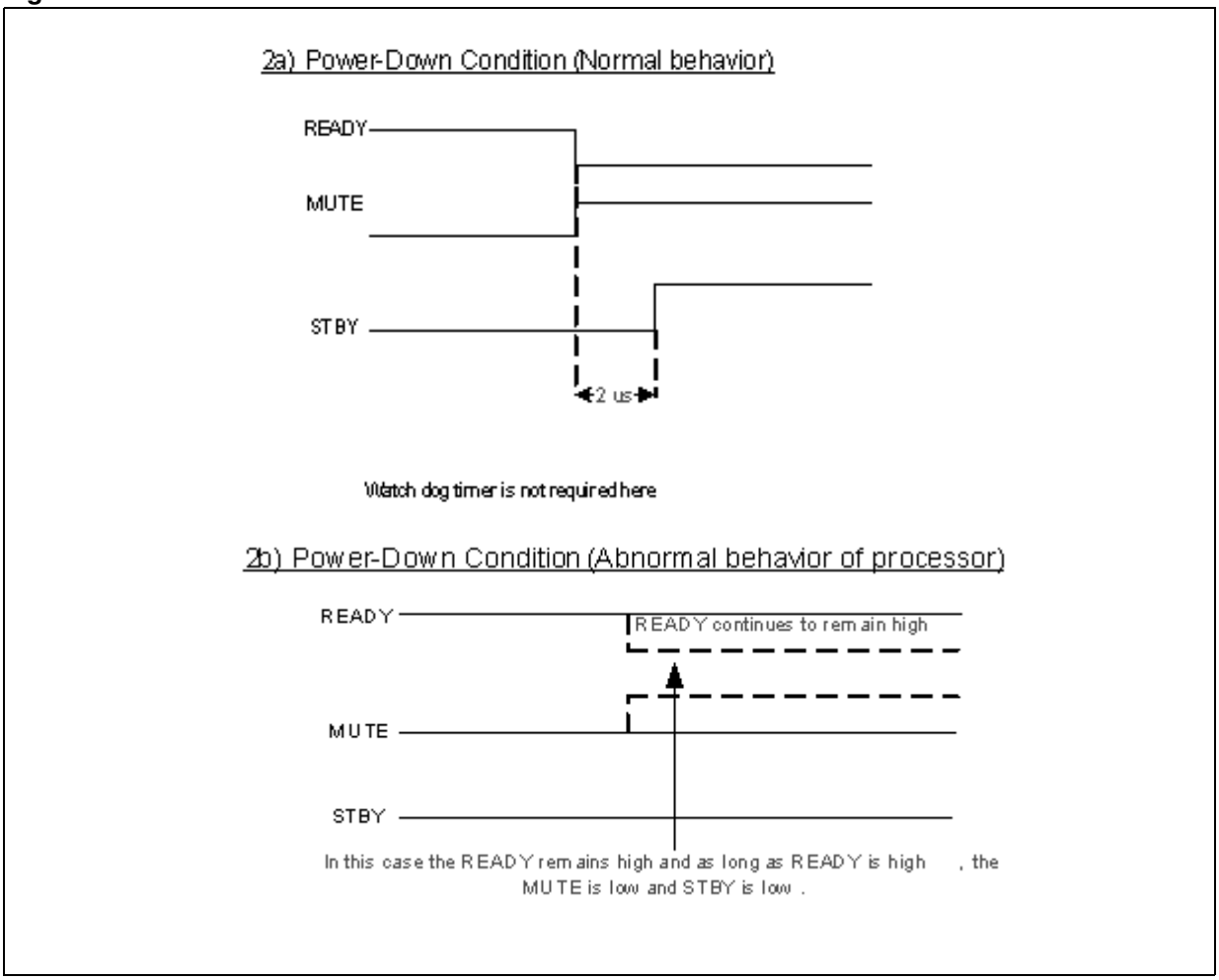
If Watchdog is to be kept on during READY high condition, the WDG registers must be set accordingly by proper commands through SPI bus.

In this power-up condition, the watchdog timer is triggered by internal POR pulse.

During power-up, the watchdog timer value is 10s.

3.6.2 Watchdog timer operation during power-down

Figure 4. Power-down condition



Note: The watchdog timer can be kept on during normal conditions when READY is high (depending on the user's settings).

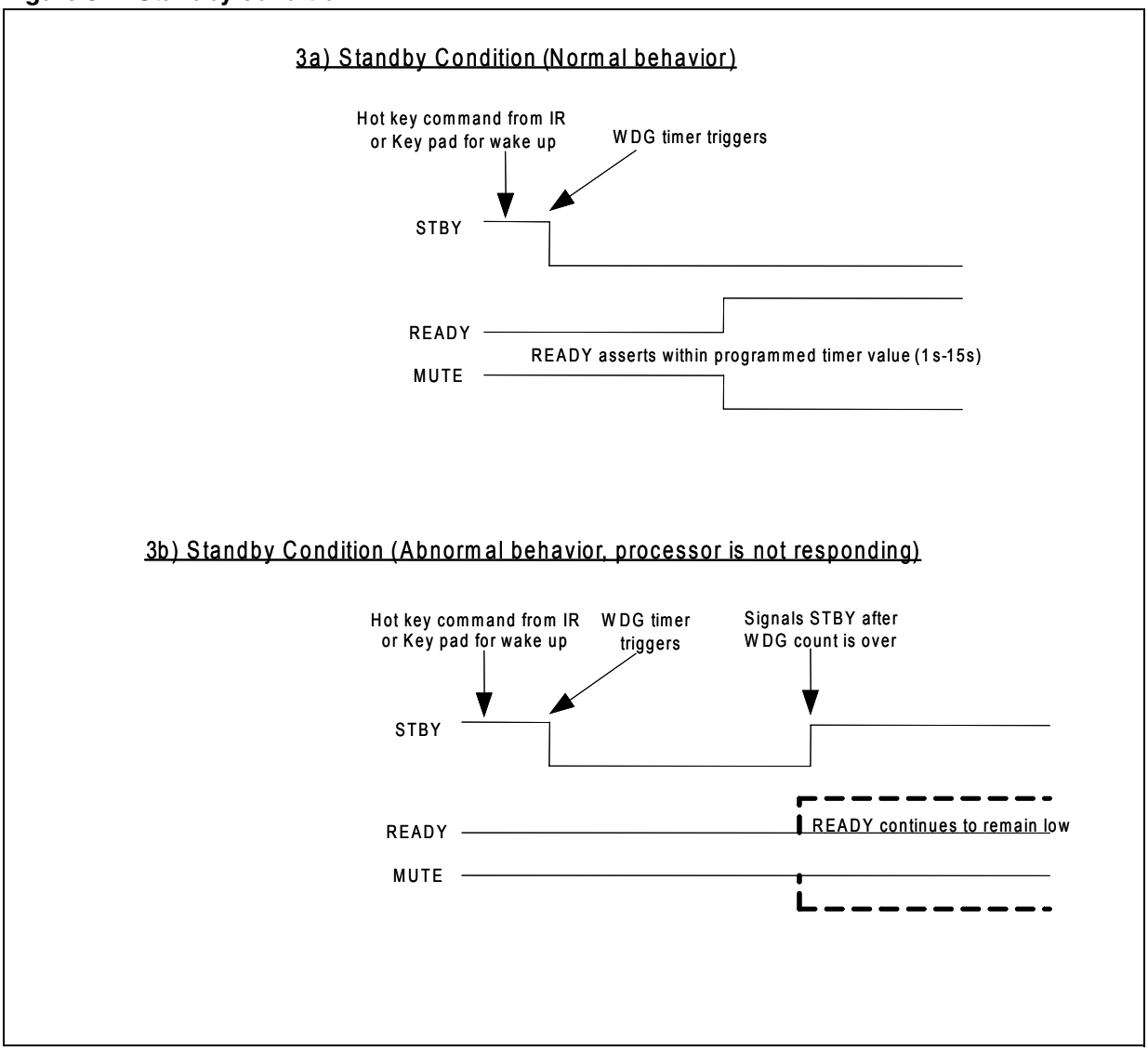
In this condition, the watchdog timer can be disabled or enabled. If the watchdog timer is enabled, the timer needs to be cleared before the programmed count of the timer is reached. If the programmed count is reached, the STBY will be asserted.

Caution: It is advisable not to enable the watchdog timer during normal operation.

3.6.3 Watchdog timer operation during standby

- When a hot-key signal is detected either from the front panel or remote control during standby, the STBY de-asserts.
- The de-assertion of the STBY triggers the watchdog timer.
- The timer value is the programmed value that is set by the user (1s-15s). If the user did not change the value before entering standby, then it remains 10s.
- Also note: that The watchdog timer is off when the STFPC311 is in the standby mode to save power.

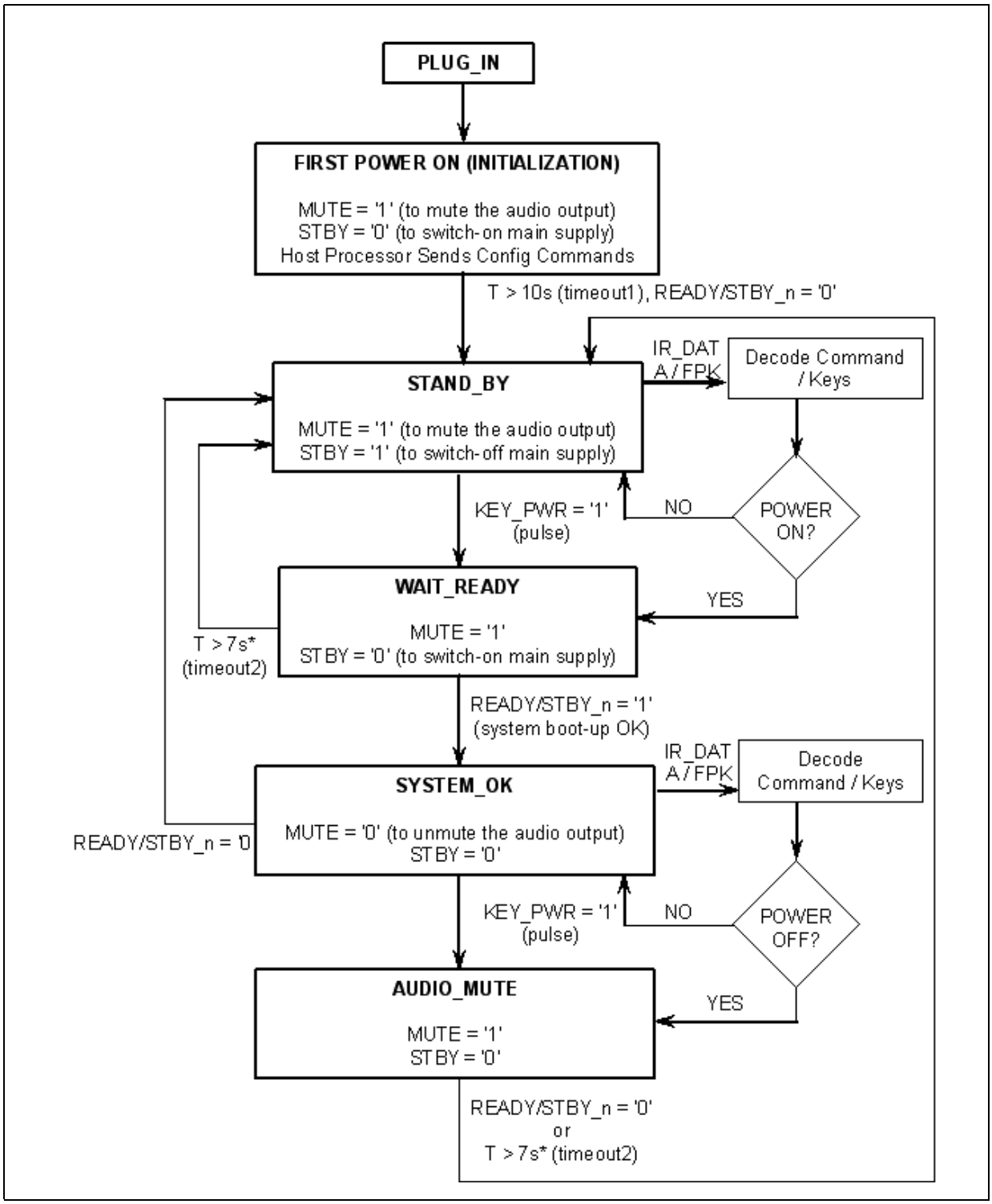
Figure 5. Standby condition



The watchdog timer is triggered by a de-assertion of the STBY signal or by the internal Power-on Reset signal. It is not affected by the STB pin.

3.7 Flow charts

Figure 6. Timing power standby sequencer flow chart



* Programmable from 1 to 15s.

† FPK = Front Panel Keys

Figure 7. IR RC command and front panel key operation flowchart.

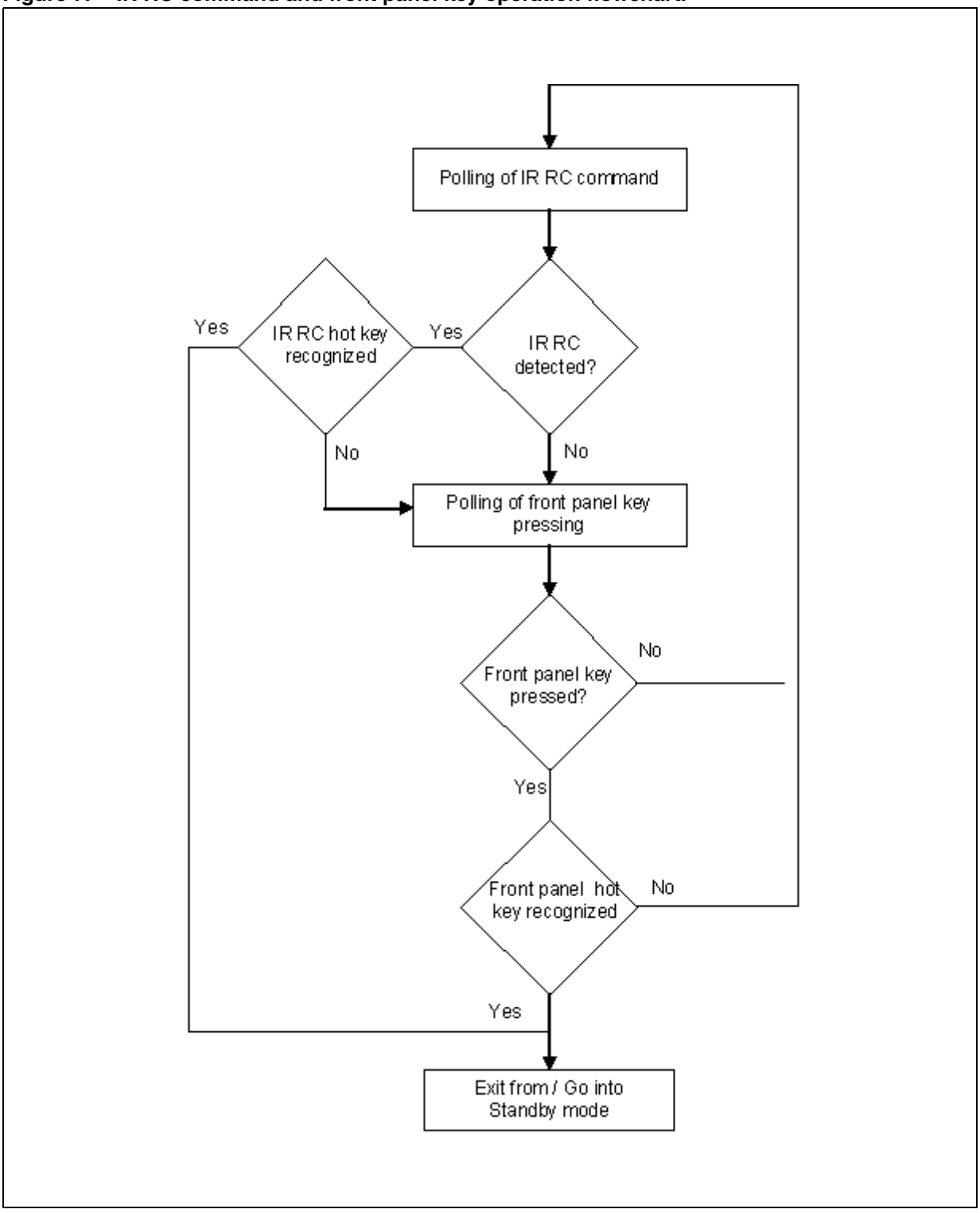


Figure 8. Watchdog timer first power-up operation

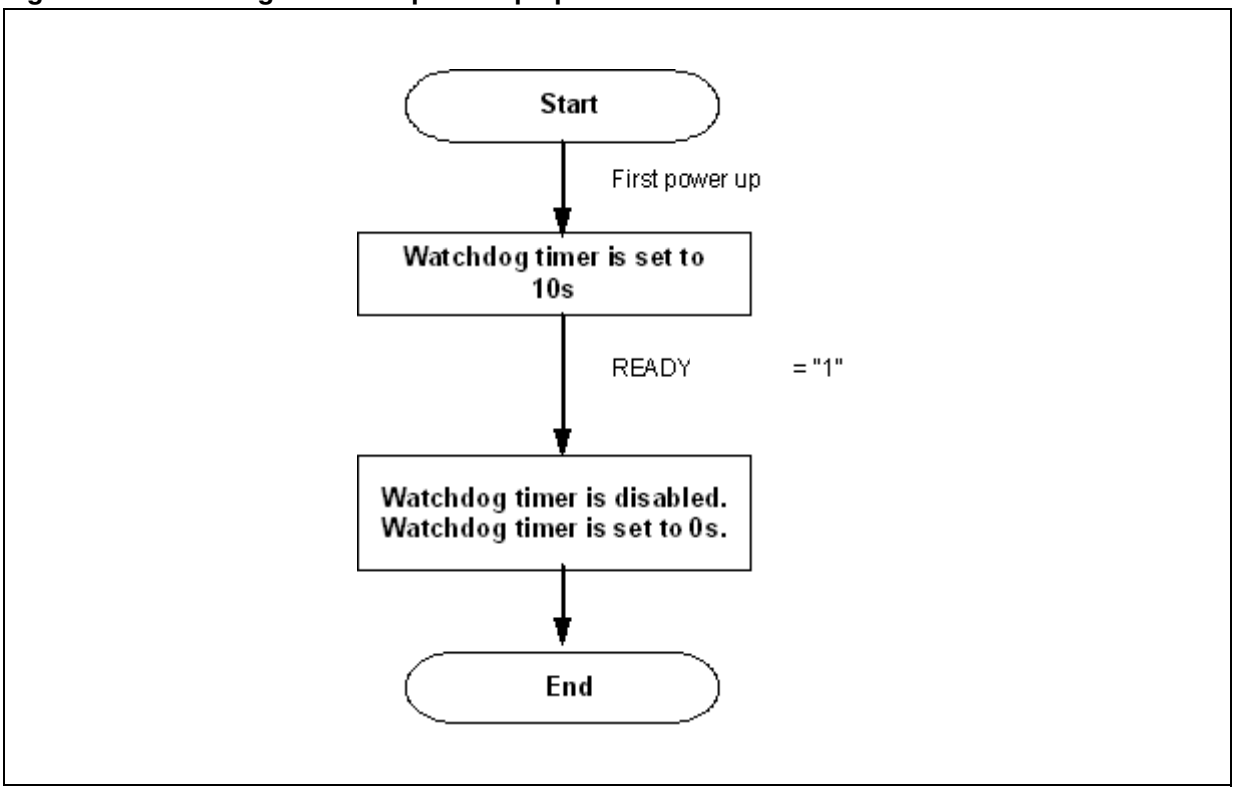
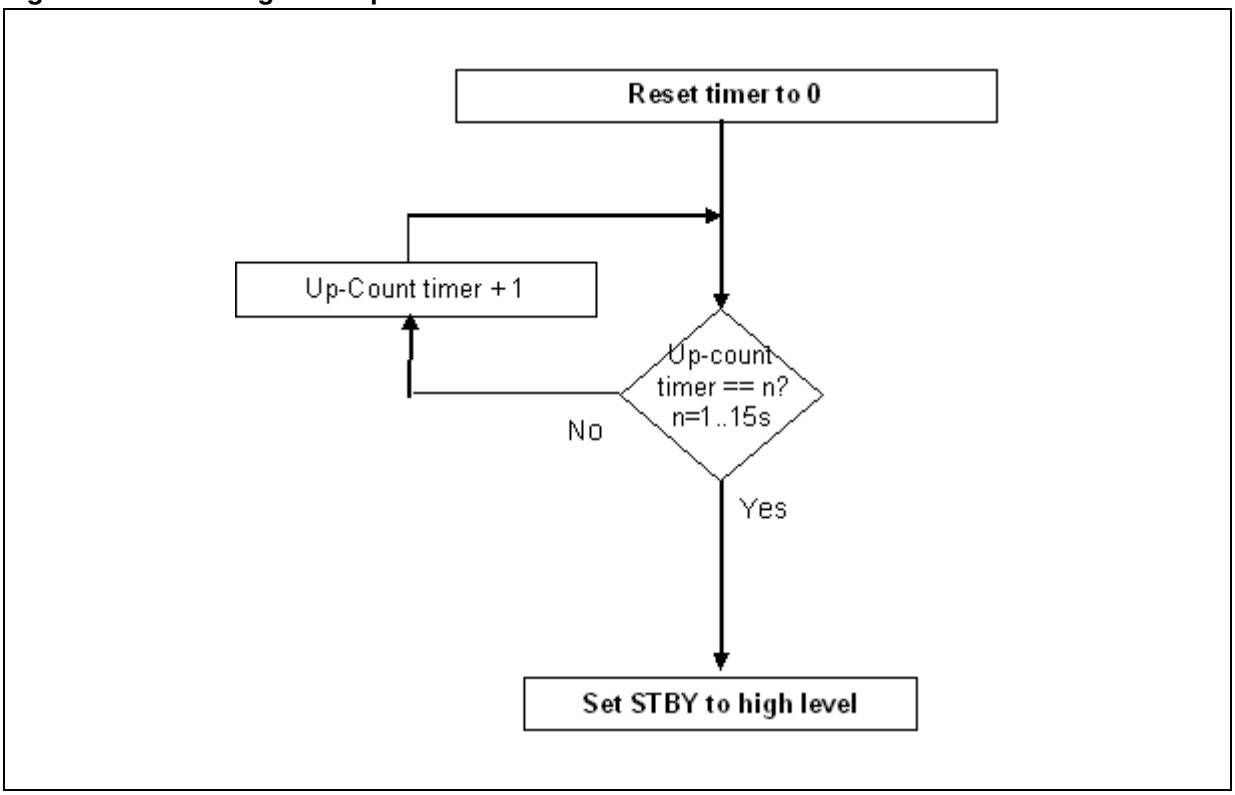


Figure 9. Watchdog timer operation



4 Display RAM address and display mode

The display RAM stores the data transmitted from an external device to the STFPC311 through the serial interface and is assigned addresses, in units of 8-bits see : *Table 2.*

Only the lower 4 bits of the addresses assigned to Seg_{17} through Seg_{20} are valid, the higher 4 bits are ignored.

Note: The common grid/segment outputs are grid-based. The grid has to be enabled before any segments can be turned on. If data is written for a segment before enabling its grid, there is nothing on the display.

Table 2. Assigned addresses

Seg_1	Seg_4	Seg_8	Seg_{12}	Seg_{16}	Seg_{20}
00 H_L	00 H_U	01 H_L	01 H_U	02 H_L	DIG_1
03 H_L	03 H_U	04 H_L	04 H_U	05 H_L	DIG_2
06 H_L	06 H_U	07 H_L	07 H_U	08 H_L	DIG_3
09 H_L	09 H_U	0A H_L	0A H_U	0B H_L	DIG_4
0C H_L	0C H_U	0D H_L	0D H_U	0E H_L	DIG_5
0F H_L	0F H_U	10 H_L	10 H_U	11 H_L	DIG_6
12 H_L	12 H_U	13 H_L	13 H_U	14 H_L	DIG_7
15 H_L	15 H_U	16 H_L	16 H_U	17 H_L	DIG_8
18 H_L	18 H_U	19 H_L	19 H_U	1A H_L	DIG_9
1B H_L	1B H_U	1C H_L	1C H_U	1D H_L	DIG_{10}
1E H_L	1E H_U	1F H_L	1F H_U	20 H_L	DIG_{11}
21 H_L	21 H_U	22 H_L	22 H_U	23 H_L	DIG_{12}
24 H_L	24 H_U	25 H_L	25 H_U	26 H_L	DIG_{13}
27 H_L	27 H_U	28 H_L	28 H_U	29 H_L	DIG_{14}
2A H_L	2A H_U	2B H_L	2B H_U	2C H_L	DIG_{15}
2D H_L	2D H_U	2E H_L	2E H_U	2F H_L	DIG_{16}

b_0 b_3	b_4 b_7
XX H_L	XX H_U
Lower 4 bits	Higher 4 bits

The data of each key is stored READ by a read command, starting from the least significant bit. see *Figure 11.*.

When the most significant bit of data ($Seg_{12}b_7$) has been read, the least significant bit of the next data (Seg_1b_0) is read.

Figure 10. Key matrix (12 x 2 configuration) and key-input data storage RAM

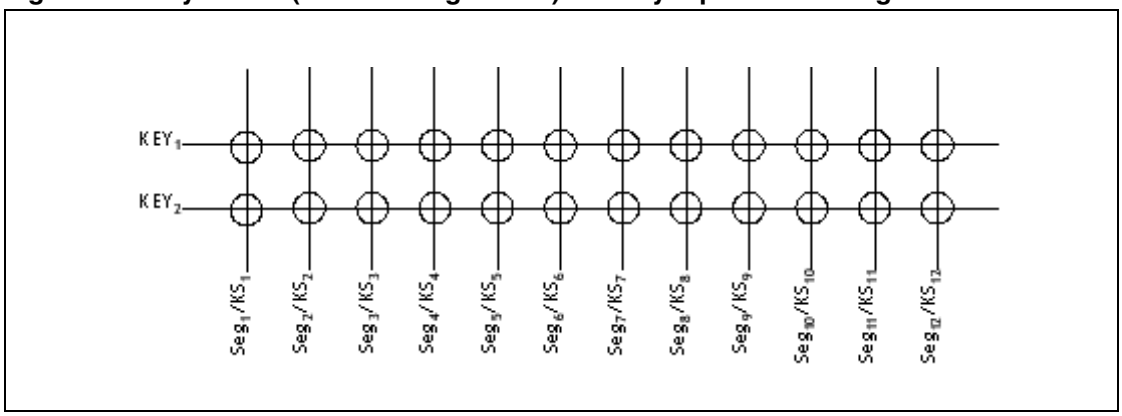
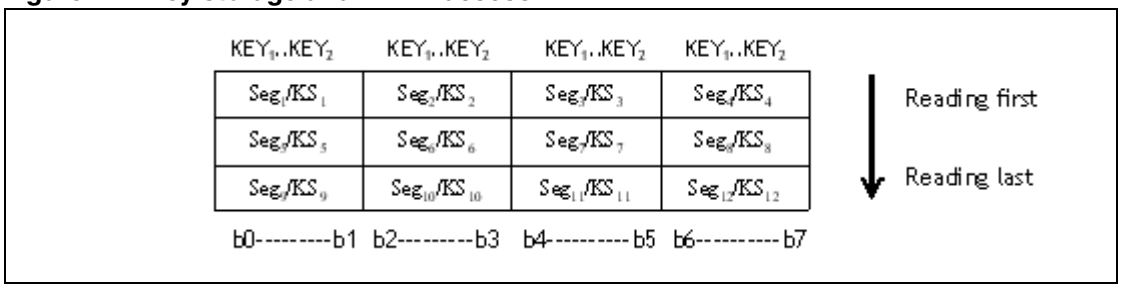


Figure 11. Key storage and READ access

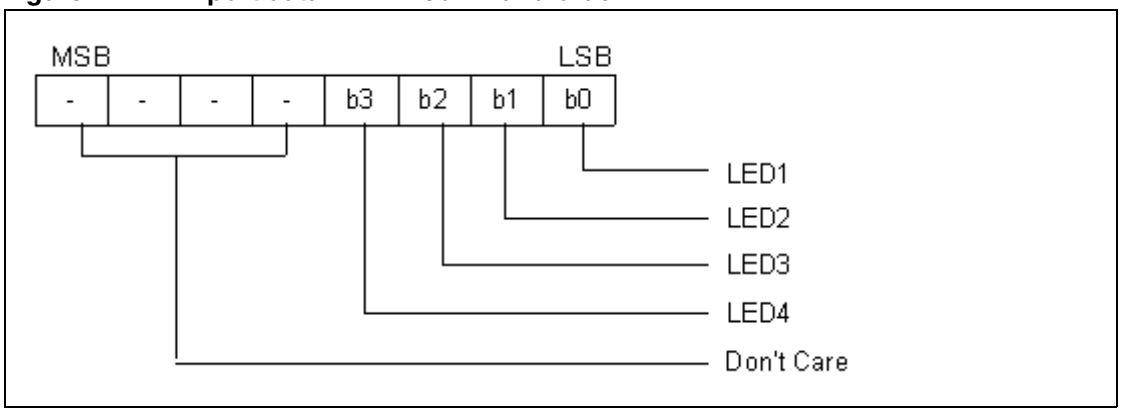


5 Data

5.1 LED Port

Data is written to the LED port by a WRITE command, starting from the least significant bit of the port see *Figure 12.* When a bit of this port is set to 0, the corresponding LED lights up; when the bit is set to a 1, the LED turns off. The data of Bits 5 through 8 are ignored. Upon first power-up, all of the LEDs are turned off.

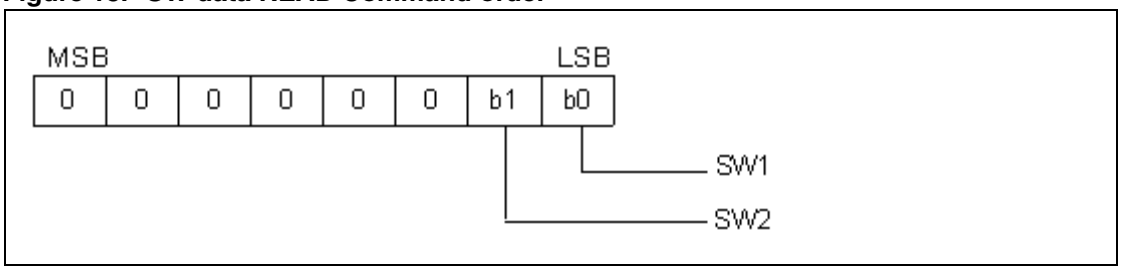
Figure 12. LED port data WRITE command order



5.2 SW Data

The SW data are read by the appropriate READ command, starting from the least significant bit see *Figure 13.* Bits 3 through 8 of the SW data are 0.

Figure 13. SW data READ Command order



6 Commands

A command sets the display mode and status of the VFD driver. The first 1-byte input to the STFPC311 through the D_{IN} pin after the STB pin goes low is regarded as a command. If STB is set to high while commands/data are transmitted, the serial communication is initialized and the commands/data being transmitted are invalid (however, the commands/data already transmitted remain valid).

6.1 Configuration mode setting command

This command initializes the STFPC311 and performs any one of the following functions see *Figure 14.*

a) Selects the number of segments and number of grids (1/8 to 1/16 duty, 12 segments to 20 segments). When this command is executed, the display is turned off. To resume display, the Display ON command must be executed. If the same mode is selected, nothing is performed.

b) Selects the remote control protocol to use.

c) Sets the watchdog timer. The watchdog timer is configurable from 1s to 15s or turned off completely.

d) Sets the watchdog action to perform when the watchdog timer counts. Two actions are allowed: no action, and set STBY to (logic) high level.

Figure 14. STFPC311 Configuration mode setting command order

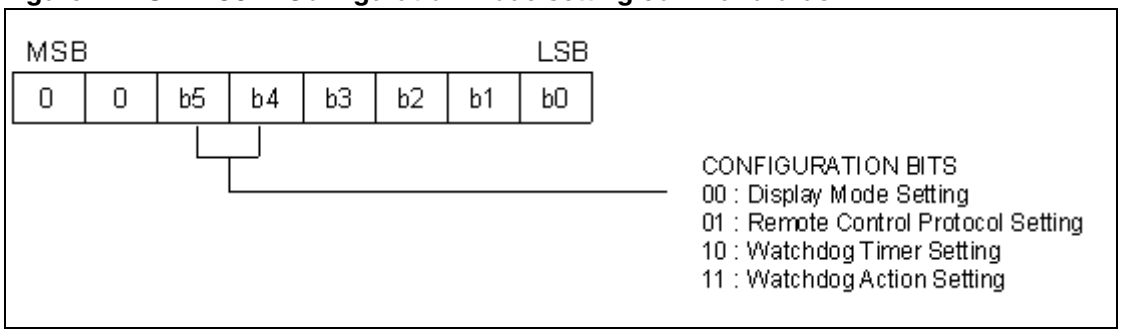


Table 3. STFPC311 Configuration mode bit 3 through bit 0 settings

DISPLAY MODE SETTING 0XXX : 8 digits, 20 segments 1000 : 9 digits, 19 segments 1001 : 10 digits, 18 segments 1010 : 11 digits, 17 segments 1011 : 12 digits, 16 segments 1100 : 13 digits, 15 segments 1101 : 14 digits, 14 segments 1110 : 15 digits, 13 segments 1111 : 16 digits, 12 segments	REMOTE CONTROL PROTOCOL SETTING 0000 : RC Disable 0010 : RC-5 0011 : RC-6 0100 : NEC	
	WATCHDOG TIMER SETTING 0000 : Turned off 0001 : 1 seconds 1111 : 15 seconds xxxx : No. of seconds in BCD format	WATCHDOG ACTION SETTING 0000 : No action 0001 : Issue STANDBY

Note: Based on Bit 5 through Bit 4 settings.

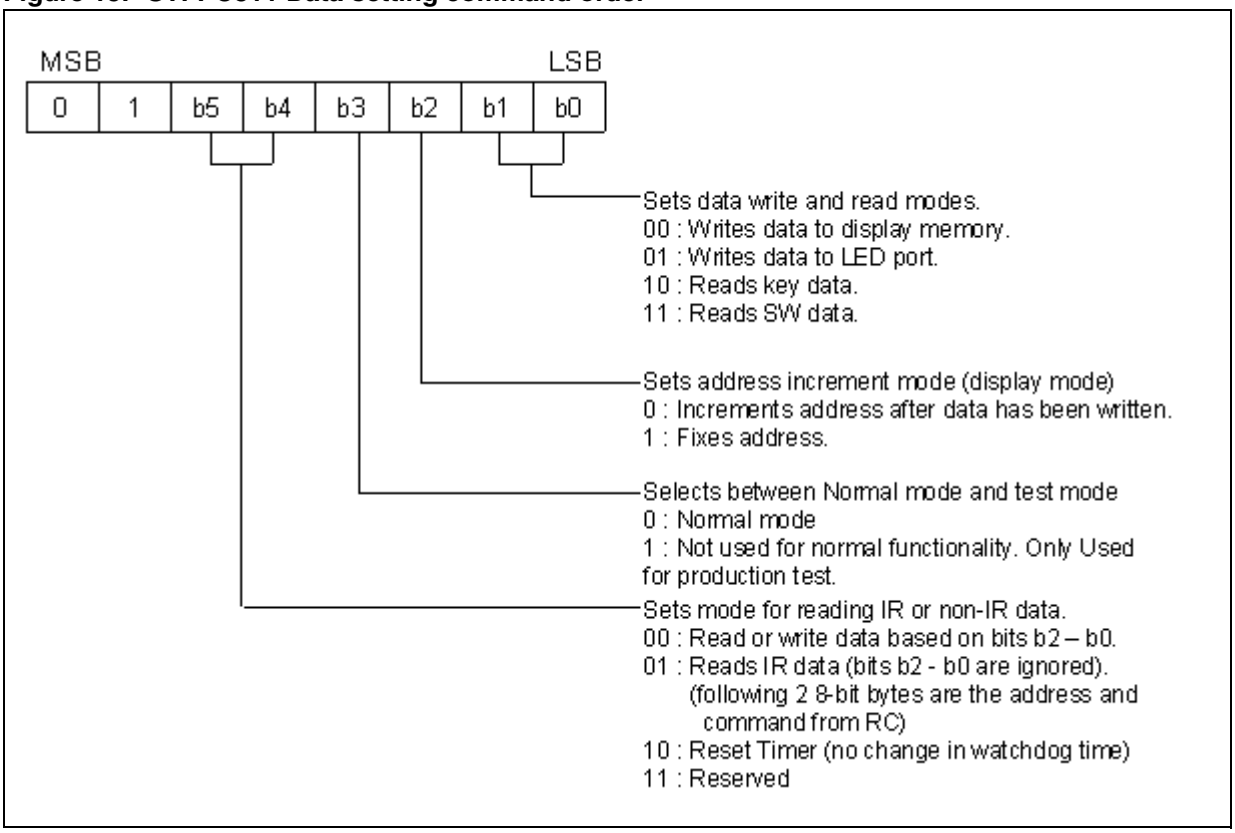
Upon power application, the following modes are selected:

- Display Mode Setting: the 16-digit, 12-segment mode is selected (default: display off and key-scan on).
- Remote Control Protocol Setting: RC-5.
- Watchdog Timer Setting: Turned on with 10s. After the first command is processed by STFPC311, the watchdog timer is turned off until it is turned on by the host.
- Watchdog action: Issue Standby.

6.2 Data setting command

This command sets the data WRITE and READ modes see *Figure 15*.

Figure 15. STFPC311 Data setting command order



When the application is powered-up, the normal operation mode and address increment mode is set with the default display memory address set to 00H. In the auto-increment address mode, the address command is sent once, followed by the data bytes.

Alternatively, the data command can be sent, followed by the data bytes. In this case, when new display data is to be written, the last value of the address will be used and then incremented. Upon reaching the last display memory address, the address jumps to 00H.

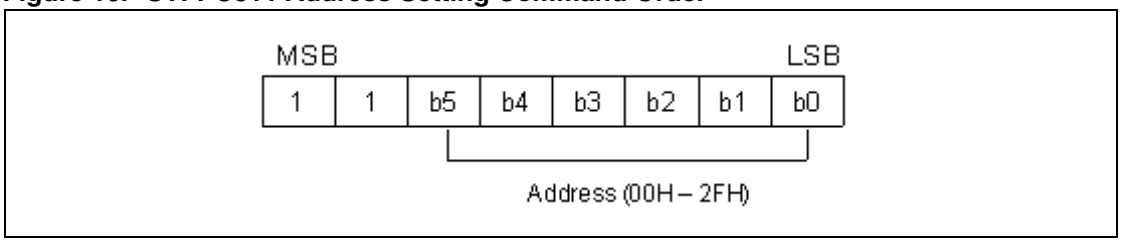
For fixed address mode, the address command has to be sent, followed by the display data. When next byte of data is to be written, the address command has to be sent again before the new display data byte.

For RC-5 data reception (after the photodiode), a binary 1 is represented by a high-to-low transition, and a binary 0 is represented by a low-to-high transition. For RC-6 (Mode 0) data reception, a binary 1 is represented by a low-to-high transition, and a binary 0 is represented by a high-to-low transition. Whenever Bit 5 is a '1', the watchdog timer is reset.

6.3 Address setting command

This command sets an address of the display memory. If address 30H or higher is set, the data is ignored until a correct address is set.

Figure 16. STFPC311 Address Setting Command Order



6.4 Display control and hotkey setting command

When the application is powered-up, the 1/16-pulse width is set and the display is turned OFF.

See *Figure 17* and *Figure 4*. All hot keys are disabled.

Figure 17. STFPC311 Display control and hot key setting command order

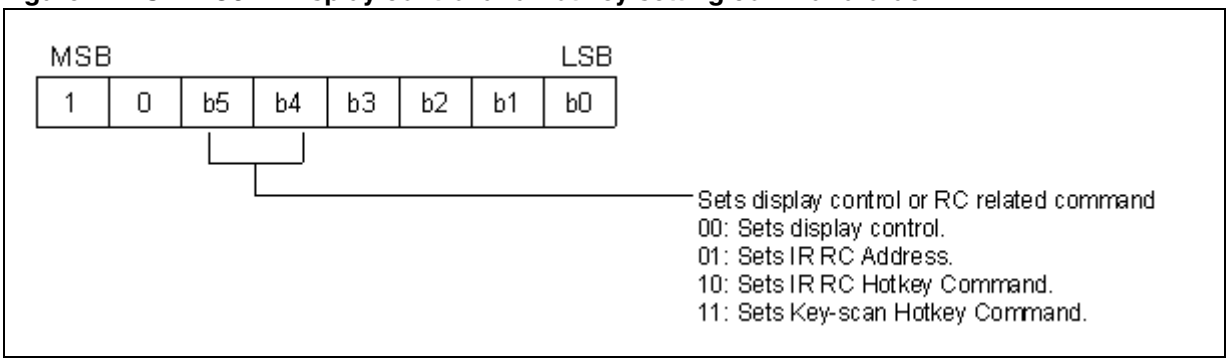


Table 4. STFPC311 Address setting mode bit 3 through bit 0 settings

When b5 b4 = 0 0	When b5 b4 = 0 1	When b5 b4 = 1 0
b2..b0 : Sets dimming quantity. 000 : Sets pulse width to 1/16. 001 : Sets pulse width to 2/16. 010 : Sets pulse width to 4/16. 011 : Sets pulse width to 10/16. 100 : Sets pulse width to 11/16. 101 : Sets pulse width to 12/16. 110 : Sets pulse width to 13/16. 111 : Sets pulse width to 14/16. b3 : Turns on/off display 0 : Display off (key scan continues*) 1 : Display on	b3..b0 : Don't care Following 8-bit is sent to indicate the address for RC.	b3..b0 : Address for storing hotkeys 0000 : Location 1 for RC command : : 0111 : Location 8 for RC command When b5 b4 = 1 1 0000 : Location 1 for FPK1 command 0001 : Location 2 for FPK2 command 0010 : Location 3 for FPK3 command Following 8-bit is sent to indicate the RC hotkey to be stored into internal memory *FPKx = Front Panel Key Set x. See next page

7 Programmable hotkeys

7.1 IR Remote control

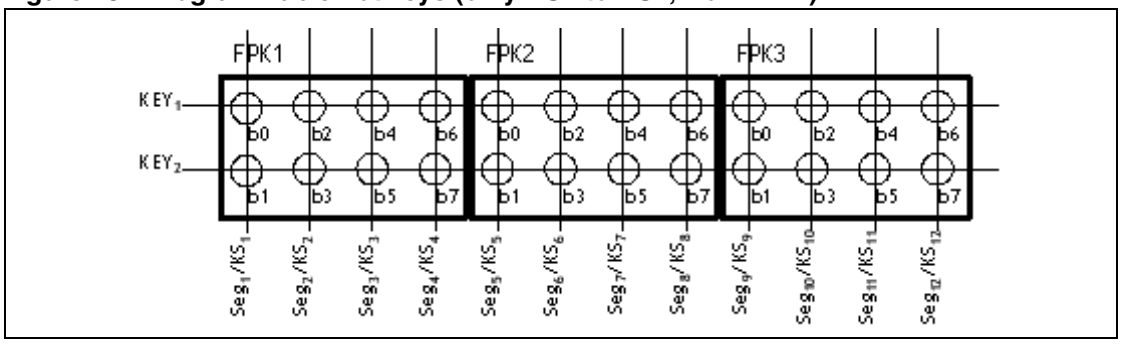
Eight (8) commands are user programmable for hot key functions.

The address of the appliance (8-bit) is stored first into the internal RAM. Then, the command for the hot keys are programmed into the internal RAM. Each hot key memory address could accommodate one byte (8-bits). Usually one byte is reserved for one command. The RC data is only cleared when the READY is pulled low (system goes into STANDBY state).

7.2 Front panel keys

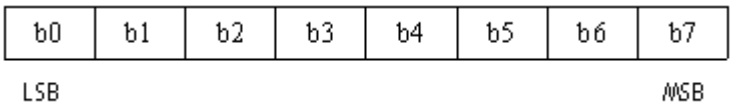
Eight out of 24 keys are user programmable for hot key functions. Only keys from KS1 to KS4 can be programmed.

Figure 18. Programmable hot keys (only KS1 to KS4, Box FPK1)



8 hot keys are to be placed in each address location as indicated by the hotkey setting command.

Figure 19. HOTKEY setting command address locations (8 hot keys)



For example, to store (Seg2/Key2) at the first location of the hot key RAM, the following commands are sent:

- 10110000 (command+address), and
- 00010000 (hot key mask).

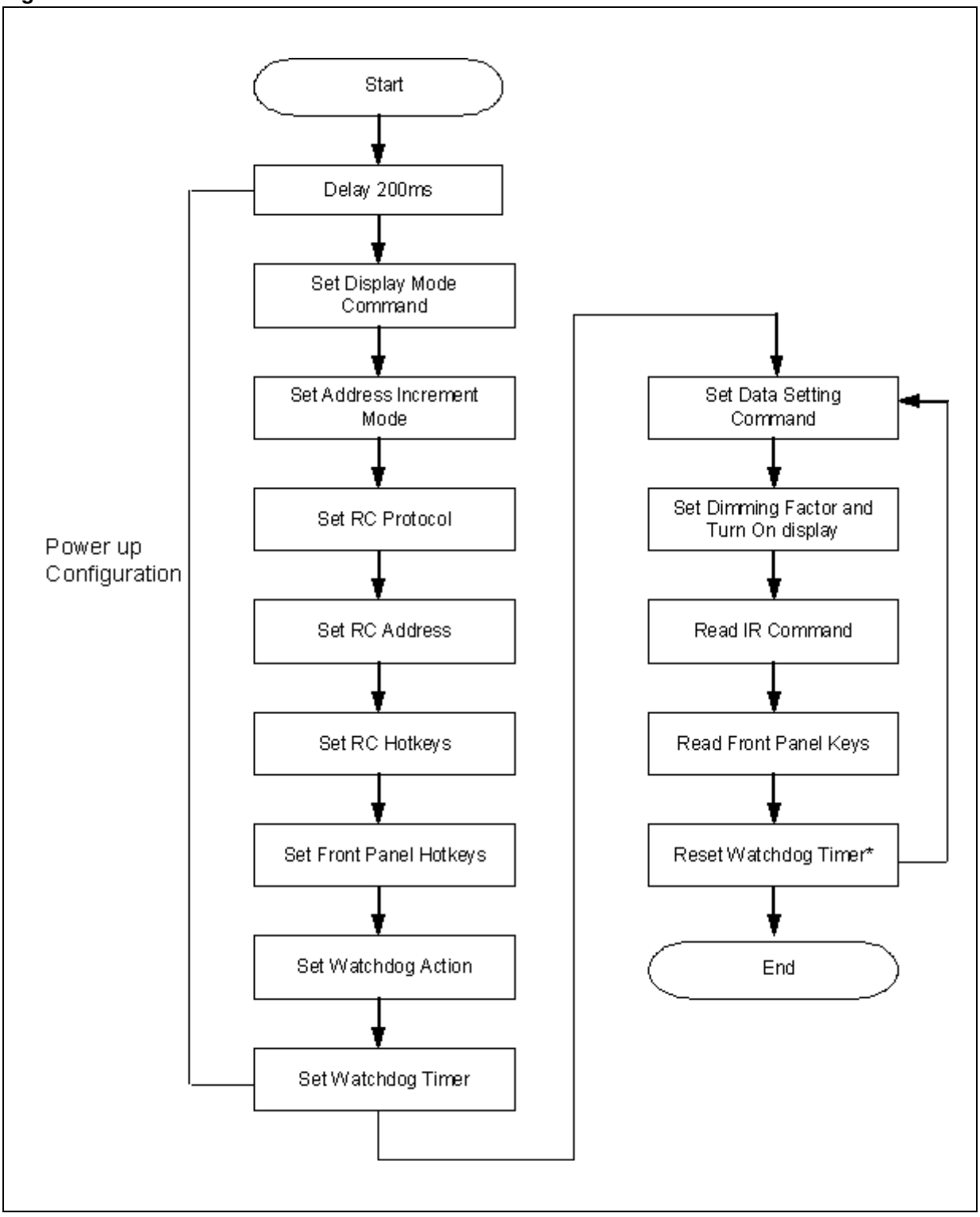
To store (Seg2/Key1), (Seg2/Key2), and (Seg4/Key1), the following commands are sent:

- 10110000 (command+address), and
- 00110010 (hot key mask).

The same commands apply to FPK2 and FPK3 programming.

Note: Note: Reading the hot key values immediately upon STBY de-assertion is recommended. If they are not read within the watchdog preset timer value, the hot key data is cleared.

Figure 20. Recommended software flow



Note: Resetting the front panel controller at ¾ of the set watchdog time is recommended.

8 Default status

8.1 Power-up default status

Table 5. Default States

S. N°	Functions	Default Status
1	Display	OFF
2	Key-scan	ON
3	IR	ON
4	Display mode	12 Seg/16Bit
5	Display address	00H
6	RC Protocol	DC-5
7	LED	OFF
8	Dimming	1/16 Duty factor
9	Hot Kets (IR and FP)	Disabled
10	Watchdog timer	10s

8.2 STANDBY status

The display remains ON during STANDBY only if the -20V is present. If the -20V is absent, the display turns OFF. When the display wakes up from STANDBY and –20V is applied, the display turns ON with previous value.

Switching off the display before entering the STANDBY state is recommended.

When the same display configuration command is sent, the display remains ON. When the display configuration command is changed, the display is OFF.

Only hot key detection can wake the system up from STANDBY condition.

9 Remote control protocols

9.1 RC-5 remote control

RC-5 remote control protocol is based on Bi-phase (also known as Manchester) encoding as shown in Figure 21.

Note: The encoding is set with reference to the IR_DATA_IN signal (after the photo diode). The MSB is transmitted first see Figure 22.

- The first two Start bits (S1 and S2) are synchronization bits. For normal operation, they are always set to '11' on the transmission side. After the photo diode, there is one inversion. The data at the IR_DATA_IN of the STFPC311 is shown in *Figure 23 on page 25*
- The next bit is the Toggle bit. This bit is inverted each time a key on the remote control is pressed.
- Bits A1and A5 are the Address bits. The address bits indicate the intended application that the remote control protocol is used for.
- Bits C1..C6 are the Command bits. The command bits instruct the STFPC311 as to what action is to be taken. The data representing the RC-5 protocol is sent as a byte of data which consists of a Toggle bit and a ‘0’ bit followed by 6 bits of Command data.

Figure 21. Bi-phase encoding

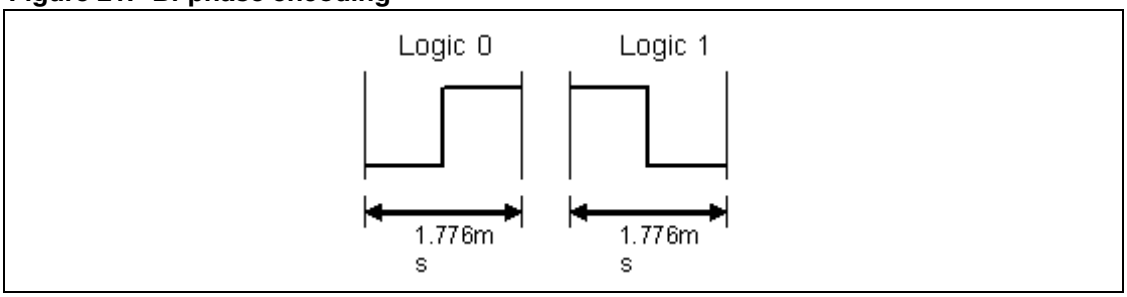


Figure 22. RC-5 protocol frame

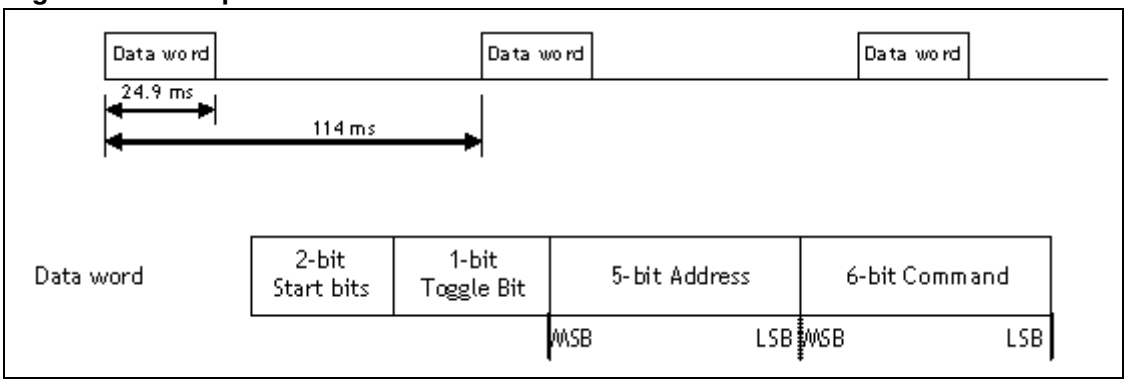
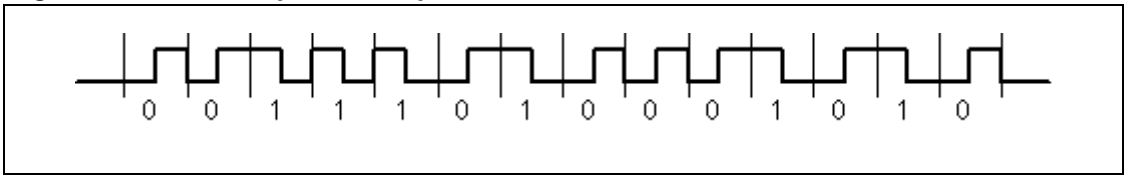


Figure 23. RC-5 reception example

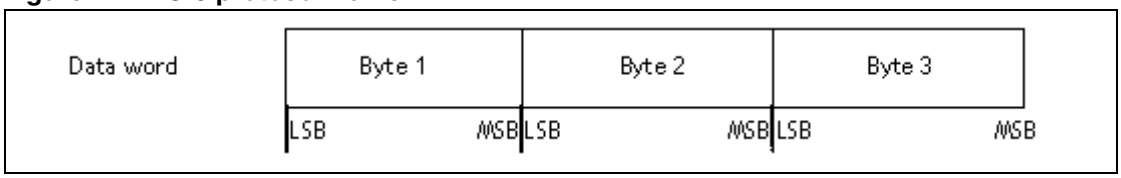


9.2 SPI interface IR data transmission

The IR data is sent on the DOUT pin of the SPI interface when the micro controller issues a IR data read command. The data is sent in 3 bytes with LSB transmitted first as shown in the Figure below:

The RC data consists of RC address, start bit, toggle bit and the RC command received. The extra bits are stuffed with 1's to make it a 3-byte packet. These extra bits at the end of the packet should be ignored.

Figure 24. RC-6 protocol frame



The RC data consists of RC address, start bit, toggle bit and the RC command received. The extra bits are stuffed with 1's to make it a 3-byte packet. These extra bits at the end of the packet should be ignored.

9.3 NEC remote control

This remote control protocol uses pulse distance modulation. Each bit consists of a high level of fixed time "t", followed by a low level that varies in width. A space that is "t" represents a logic '0' and a space that is "3t" represents a logic '1'. t = 0.56ms.

The LSB is transmitted first as shown in *Figure 25*

Figure 25. Pulse distance modulation.

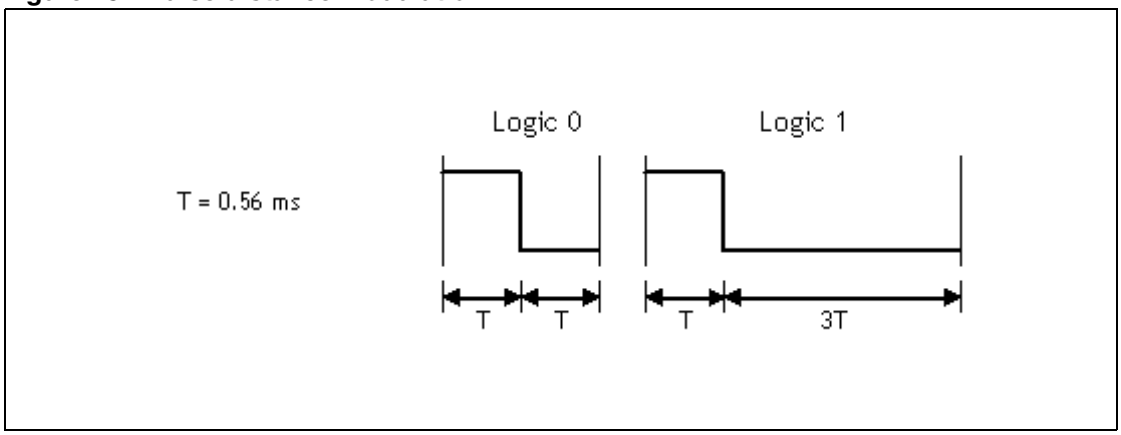
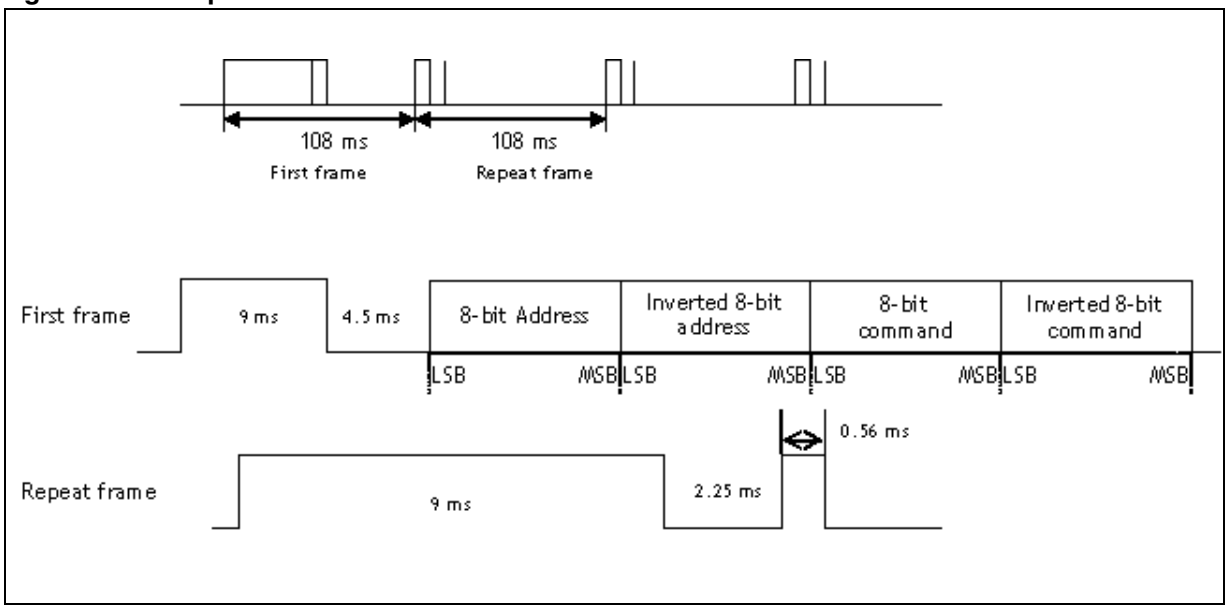


Figure 26. NEC protocol transmission waveforms



10 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum rating (T_A = 25 °C, V_{SS} = 0V)

Symbol	Parameter	Value	Unit
V_{DD}	Logic Supply Voltage	-0.5 to +7.0	V
V_{SS}	Driver Supply Voltage	V_{DD} + 0.5 to V_{DD} - 40	V
V_{I1}	Logic Input Voltage	-0.4 to V_{DD} + 0.5	V
V_{O2}	VFP Driver Output Voltage	V_{SS} - 0.5 to V_{DD}+ 0.5	V
I_{O1}	LED Driver Output Current	+25	mA
I_{O2}	VFP Driver Output Current	-40 (grid) -15 (segment)	mA
P_D	Power Dissipation	1200 (1)	mA
T_A	Operating Ambient Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-65 to +150	°C

1. Derate at -9.6 mW/°C at T_A = 25 °C or higher

Table 7. Recommended operating conditions (T_A = -20 to +70 °C, V_{SS} = 0V)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Logic Supply Voltage	3.0	3.3	3.6	V
V_{IH}	High-Level Input Voltage	0.7V_{DD}		V_{DD}	V
V_{IL}	Low-Level Input Voltage	0		0.3 V_{DD}	V
V_{SS}	Driver Supply Voltage	0		V_{DD}-33.3	V

10.1 Power consumption estimation

The maximum power consumption is comprised of the Vacuum Florescent Display (VFD) driver dissipation, Load Resistance (RL), LED driver dissipation, and dynamic power consumption.

$P_{MAX} = V_{FD} + R_L + LED + P_{DYN}$

Where,

- P_{MAX} = maximum power consumption,
- VFD = Vacuum Florescent Display driver dissipation,
- R_L = load resistance,
- LED = LED driver dissipation, and
- PDYN = dynamic power consumption.

If the segment current (ISEG) = 3mA, grid current (IGRID) = 15mA, and the LED current = 20mA, then:

FIP = (#segments x 6) + [#grids/(#grids +1)] x 30mW,

RL dissipation = (VDD – VSS)2 ÷ 50(segment + 1mW),

LED driver dissipation = #LEDs x 20mW, and

PDYN = VDD x 5mW.

To finish this example:

FIP driver dissipation = 16 x 6 + 12/13 x 30 = 124mW

RL dissipation = 33.32/50 x 17 = 377mW

LED driver dissipation = 2 x 20 = 40

PDYN = 3.3 x 5 = 16.5mW

The maximum power consumption (Total) = 557.5mW

Where,

VSS = –30V,

VDD = 3.3V, and the application is in 16-segment, 12-digit mode.

11 Electrical characteristics

Table 8. Electrical specifications
(T_A = -20 to +70°C, V_{DD} = 3.3V, V_{SS} = 0V, V_{SS} = V_{DD} - 33.3V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OH1}	High-Level Output Voltage	LED1 – LED4, I_{OH1} = -1mA	0.9V_{DD}			V
V_{OL1}	Low-Level Output Voltage	LED1 – LED4, I_{OH2} = 20mA			1	V
V_{OL2}	Low-Level Output Voltage	D_{OUT}, I_{OL2} = 4mA			0.4	V
I_{OH21}	High-Level Output Current	V_O = V_{DD} - 2V, $Seg_1$to Seg_{12}	-3			mA
I_{OH22}	High-Level Output Current	V_O = V_{DD} - 2 V, $Grid_1$to $Grid_8$, Se_{13}g/$Grid_{16}$to Seg_{20}/$Grid_9$	-15			mA
I_{OLEAK}	Driver Leakage Current	V_O = V_{DD} - 33.3 V, driver off			-10	µA
R_L	Output Pull-Down Resistor	Driver output	50	100	150	kΩ
I	Input Current	V_I= V_{DD} or V_{SS}			±1	µA
V_{IH}	High-Level Input Voltage		0.7V_{DD}			V
V_{IL}	Low-Level Input Voltage				0.3V_{DD}	V
V_H	Hysteresis Voltage	CLK, D_{IN}, STB		0.35		V
$I_{DD(DYN)}$	Dynamic Current Consumption	Under no load, display off			5	mA

Table 9. Switching characteristics (T_A = -20 to +70 °C, V_{DD} = 3.3 V, V_{SS} = -30 V)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{OSC}	Oscillation Frequency	R = 33KΩ ±5%		350	500	650	kHz
t_{PLZ}	Propagation Delay Time	CLK ⊴D_{OUT} C_L = 15pF, R_L = 10KΩ				300	ns
t_{PZL}						100	ns
t_{TZH1}	Rise Time	C_L = 300pF	Seg_1 to Seg_{12}			2	µs
t_{TZH2}			$Grid_1$ to $Grid_8$, Seg_{13}/Seg_{16} to Seg_{20}/$Grid_9$			0.5	µs
t_{THZ}	Fall Time	C_L = 300pF, Seg_n, $Grid_n$				120	µs
f_{MAX}	Maximum Clock Frequency	Duty = 50%				1	MHz
C_I	Input Capacitance					15	pF

12 Timing characteristics

Table 10. Timing characteristics (V_{DD}= 3.3V, T_A= -20 to 70°C, unless otherwise noted. Typical values are at T_A= 25°C)

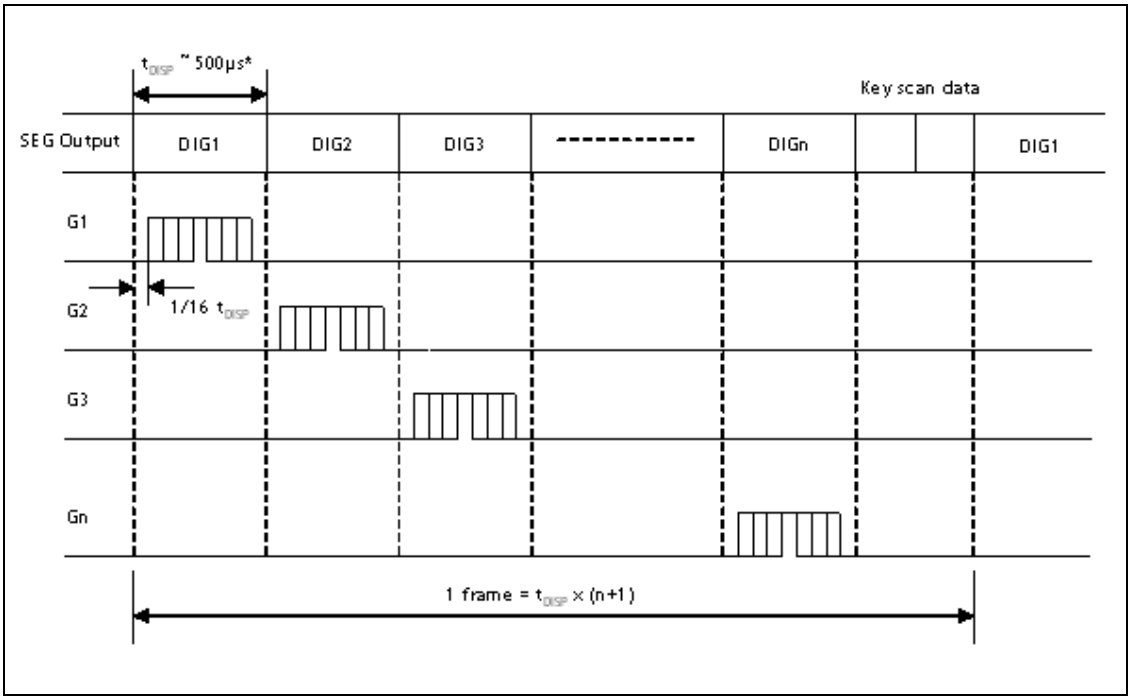
Symbol	Parameter	Test conditions	Values			Unit
			Min.	Typ.	Max.	
PW_{CLK}	Clock Pulse Width		400			ns
PW_{STB}	Strobe Pulse Width		1			µs
t_{SETUP}	Data Setup Time		100			ns
t_{HOLD}	Data Hold Time		100			ns
$t_{CLK-STB}$	Clock-Strobe Time	CLK ↑ → STB↑	1			µs
t_{WAIT}	Wait Time (1)	CLK ↑ → CLK↑	1			µs

1. Refer to page on Serial Communication Format.

The pulse width of the segment signal is derived from the oscillator frequency. The value can be modified by trimming ROSC. One cycle of key scanning consists of one frame and data of 12 x 2 matrices are stored in RAM.

Note: The key scan is only at the end of the frame when the display is ON. When the display is OFF, the key scan takes place continuously. The grid is turned off during the key scan.

Figure 27. Key scanning and display timing



13 Serial communication format

When data is read, a wait time (t_{WAIT}) of 1µs is necessary within the rising edge of the eighth clock that has set the command, and the falling edge of the first clock that has read the data. This is required by the STFPC311 to process its internal commands/data (See *Figure 28*)

Caution: Care must be taken to connect an external pull-up resistor to this pin (1kΩ to 10kΩ) because the D_{OUT} pin is an N-channel, open drain output pin (see *Figure 29*).

Figure 28. Recption (Command/data WRITE)

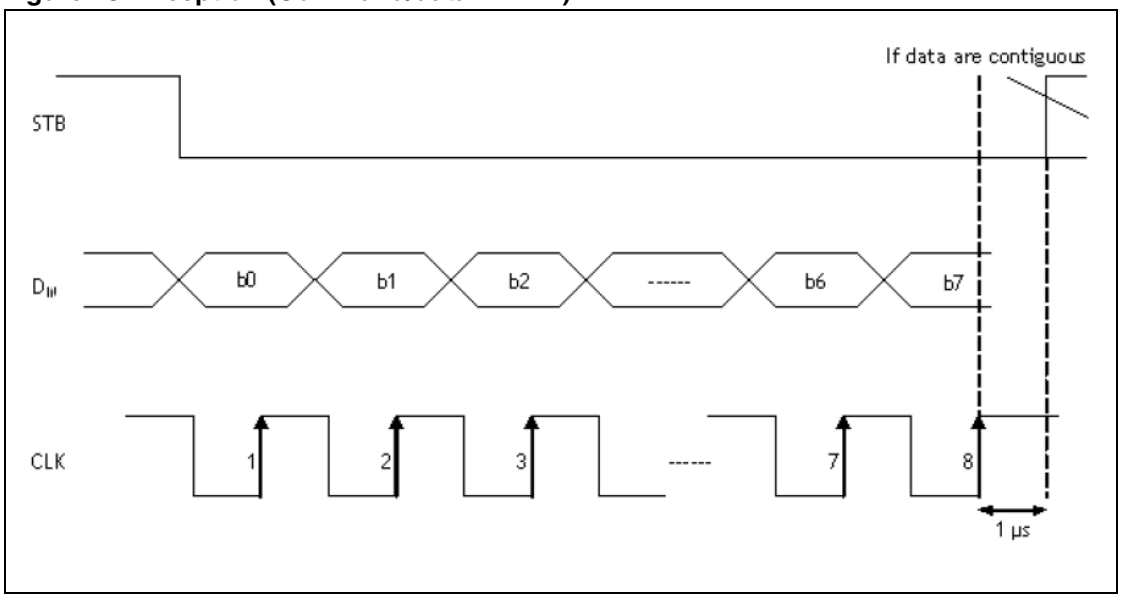


Figure 29. Data transmission (data READ)

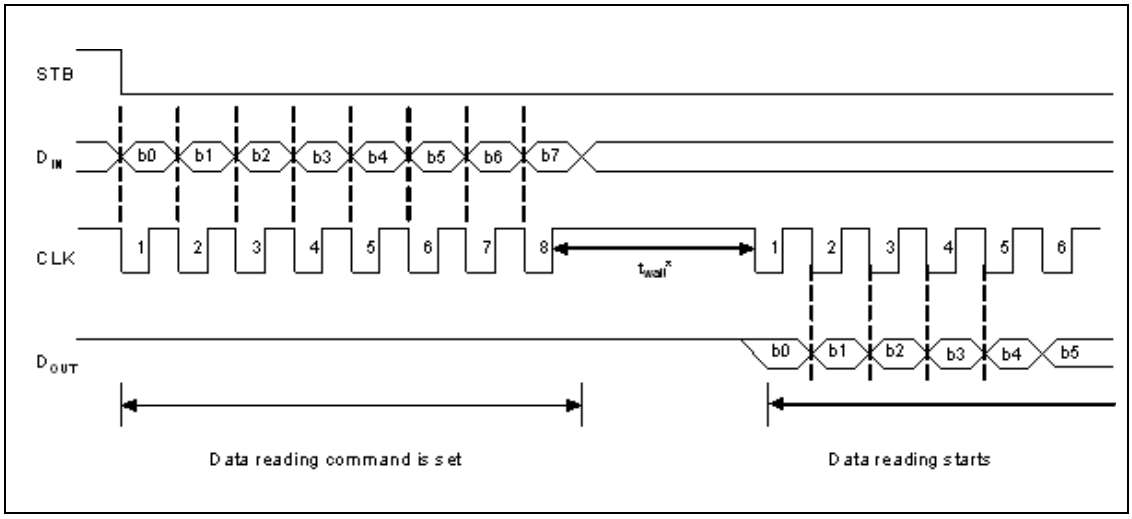
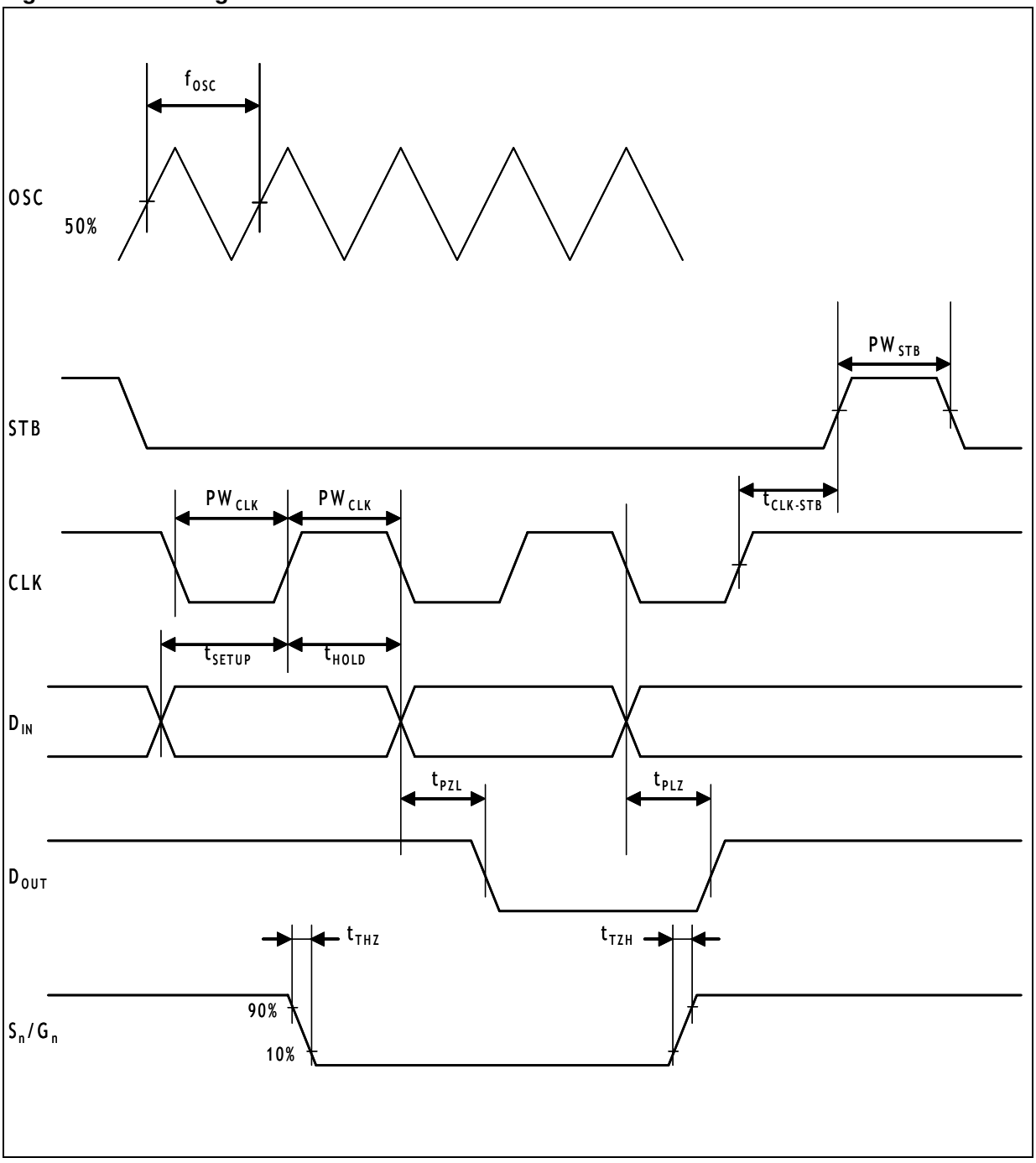
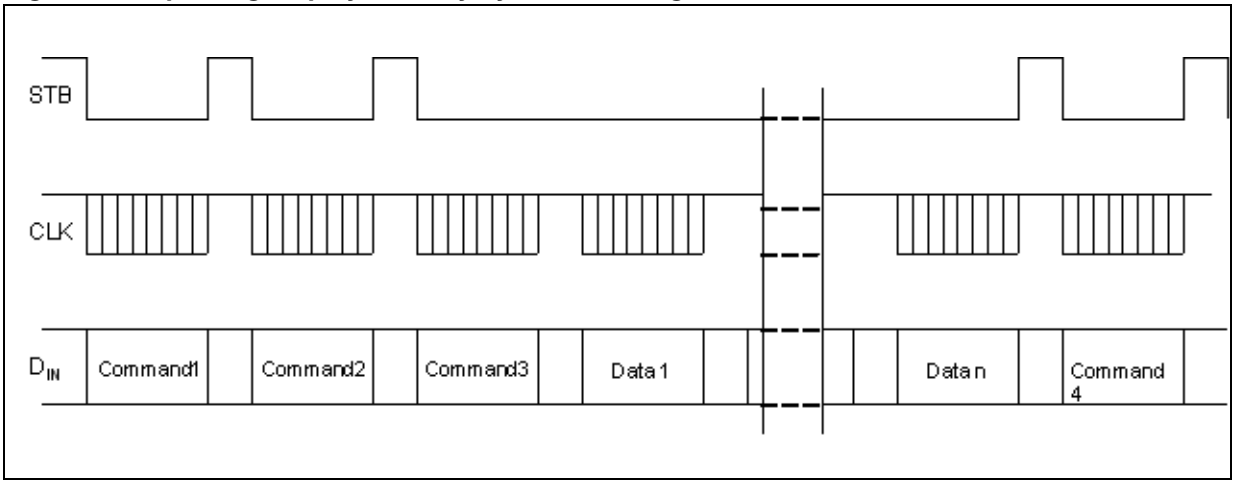


Figure 30. Switching characteristic waveforms



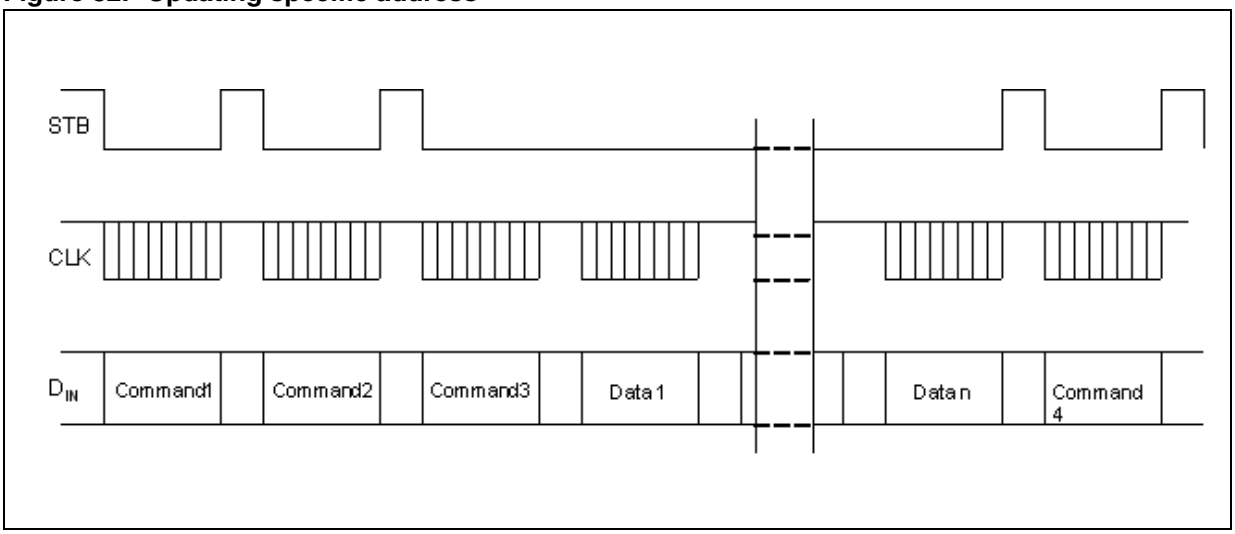
- Command 1: sets display mode
- Command 2: sets data
- Command 3: sets address
- Data 1 to n: transfers display data (22 bytes max.)
- Command 4: controls display

Figure 31. Updating display memory by incrementing address



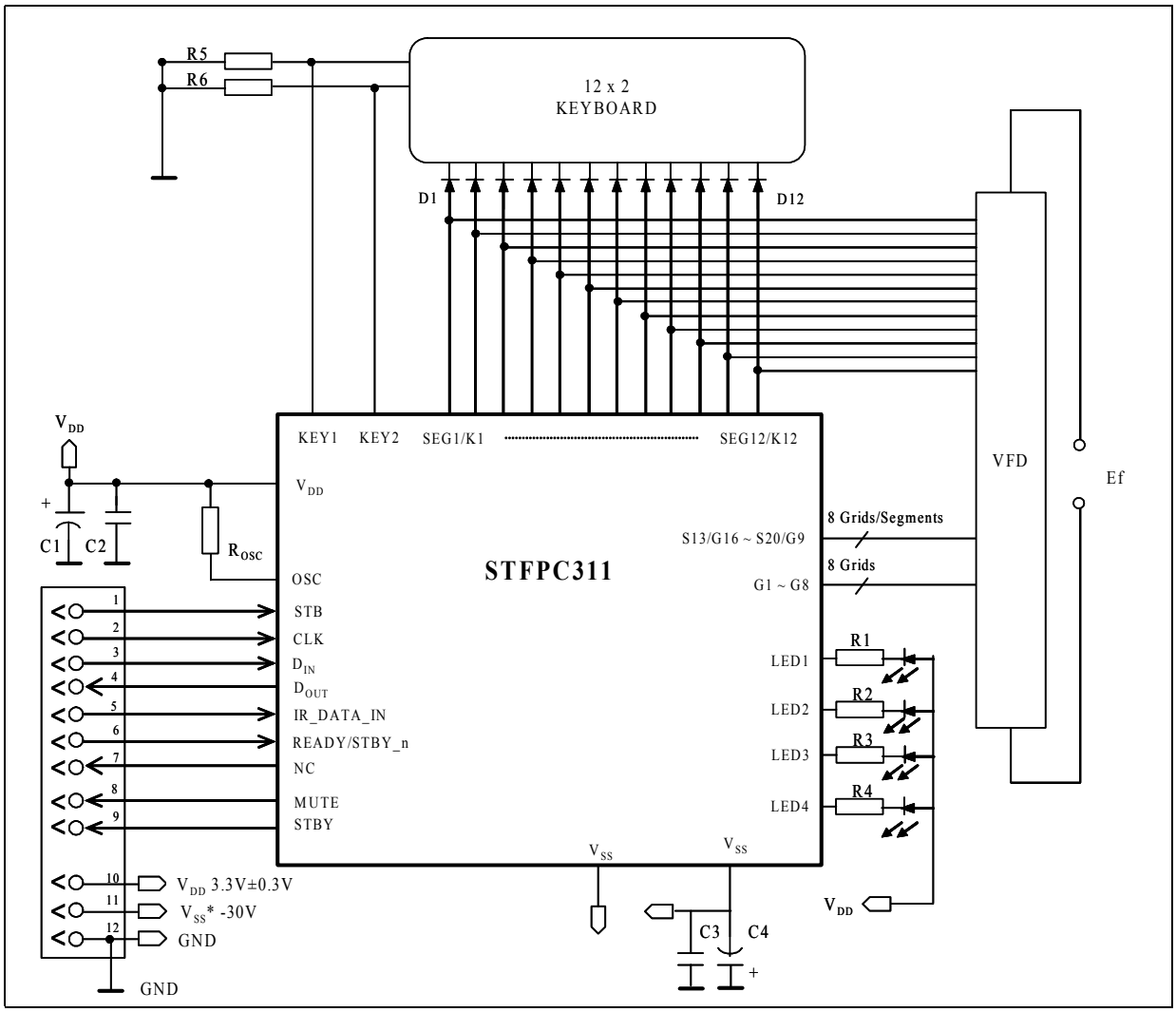
- Command 1: sets data
- Command 2: sets address
- Data: display area

Figure 32. Updating specific address



14 Typical application diagram

Figure 33. Typical application circuit



- R_{OSC} = 33kΩ ± 1% for oscillator resistor;
- R1 ~ R4 = 0.75 ~ 1.2kΩ;
- R5, R6 = 10kΩ for external keyboard pull-down resistor;
- C1 = 33µF-25V electrolytic;
- C2 = 0.01 ~ 0.1µF-25V ceramic;
- C3 = 0.01 ~ 0.1µF-63V ceramic;
- C4 = 33µF-63V electrolytic;
- D1 ~ D12 = 1N4148;
- Ef = filament voltage according with the VFD specs;
- V_{DD} = 3.3V ±10%;

* V_{SS} = down to V_{DD} – 33.3V.

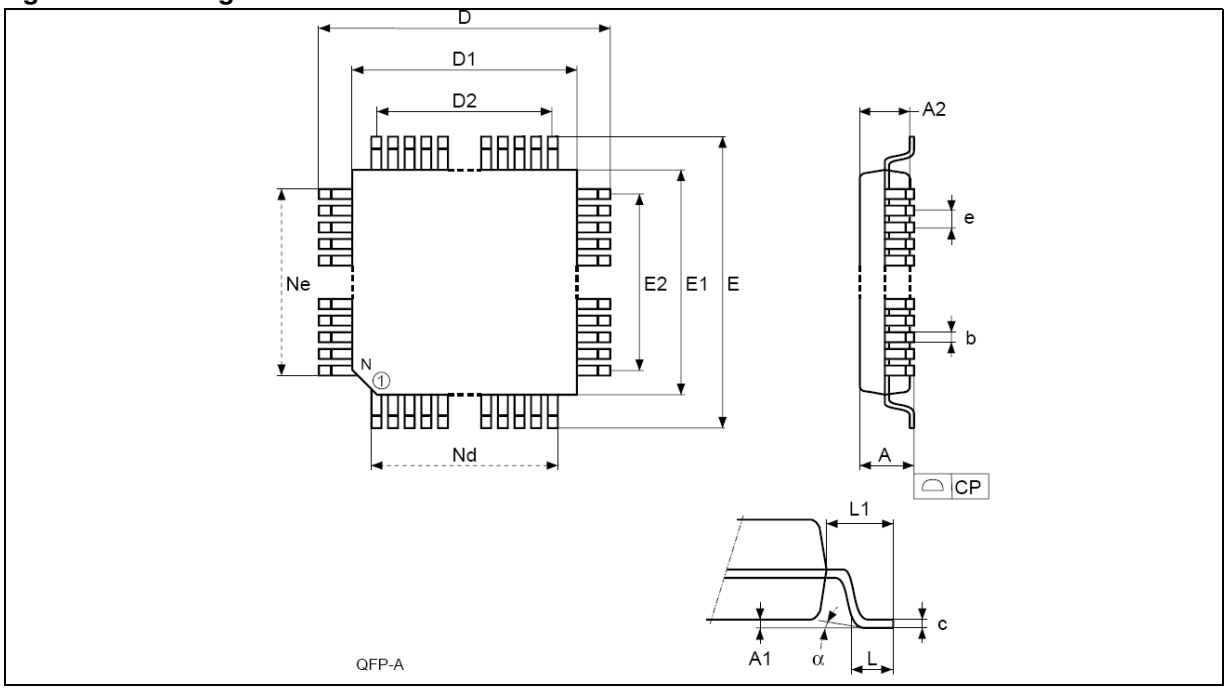
15 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 11. PQFP52 - 10x10x2 mm. plastic quad flatpack, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.350			0
A1			0.250			0
A2	2.000	1.950	2.100	0	0	0
|| a ||	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
b		0.220	0.380		0	0
c		0.110	0.230		0	0
D	13.900	13.650	14.150	1	1	1
D1	10.000	9.800	10.200	0	0	0
D2	7.800	–	–	0	–	–
ddd			0.100			0
E	13.900	13.650	14.150	1	1	1
e	0.650	–	–	0	–	–
E1	10.000	9.800	10.200	0	0	0
E2	7.800	–	–	0	–	–
L	0.880	0.730	1.030	0	0	0
L1	1.950	–	–	0	–	–
N	52			52		
Ne	13			13		
Nd	13			13		

Figure 34. Package dimensions



16 Revision history

Table 12. Revision history

Date	Revision	Change
09-May-2006	1	First release

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