

N-channel 650 V, 0.012 Ω typ., 143 A MDmesh™ M5 Power MOSFET in an ISOTOP package

Datasheet - production data

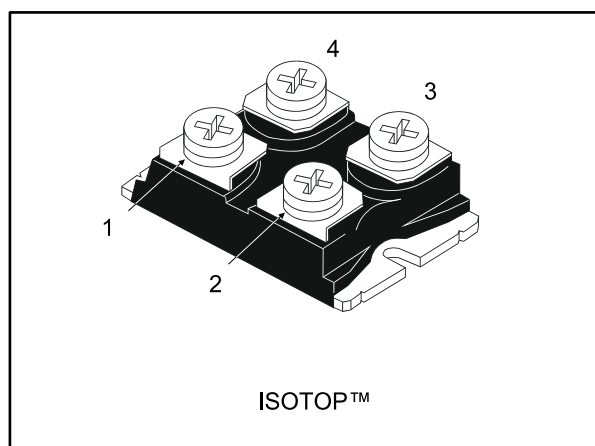
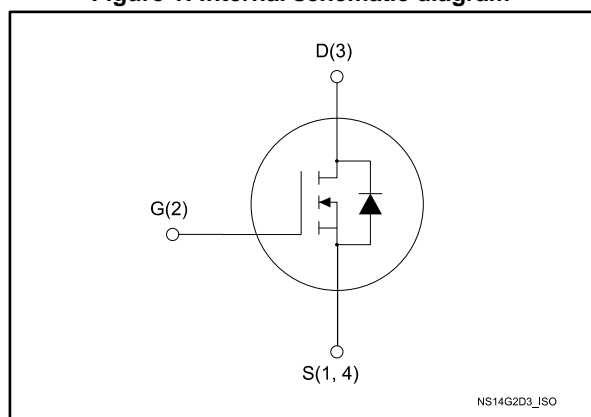


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STE145N65M5	710 V	0.015 Ω	143 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STE145N65M5	145N65M5	ISOTOP	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package information	9
	4.1 ISOTOP package information	10
5	Revision history	12

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	143	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	90	A
$I_{DM}^{(1)}$	Drain current (pulsed)	572	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	679	W
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_j max)	12	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	2420	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ s}$)	2.5	kV
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	

Notes:

⁽¹⁾ Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} \leq 143\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS(\text{peak})} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	0.184	°C/W
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient max	30	°C/W

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			10	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 69\text{ A}$		0.012	0.015	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	18500	-	pF
C_{oss}	Output capacitance		-	413	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	415	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	1950	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, open drain	-	0.7	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 69\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	414	-	nC
Q_{gs}	Gate-source charge		-	114	-	nC
Q_{gd}	Gate-drain charge		-	164	-	nC

Notes:

⁽¹⁾ $C_{o(er)}$ is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾ $C_{o(tr)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400 \text{ V}$, $I_D = 85 \text{ A}$ $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i> and <i>Figure 19: "Switching time waveform"</i>)	-	255	-	ns
$t_{r(V)}$	Voltage rise time		-	11	-	ns
$t_{f(i)}$	Current fall time		-	82	-	ns
$t_{C(off)}$	Crossing time		-	88	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		143	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		572	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 143 \text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 143 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 100 \text{ V}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i>)	-	568		ns
Q_{rr}	Reverse recovery charge		-	14.5		μC
I_{RRM}	Reverse recovery current		-	51		A
t_{rr}	Reverse recovery time	$I_{SD} = 143 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 100 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i>)	-	728		ns
Q_{rr}	Reverse recovery charge		-	24.5		μC
I_{RRM}	Reverse recovery current		-	67		A

Notes:

⁽¹⁾Pulse width is limited by safe operating area

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curves)

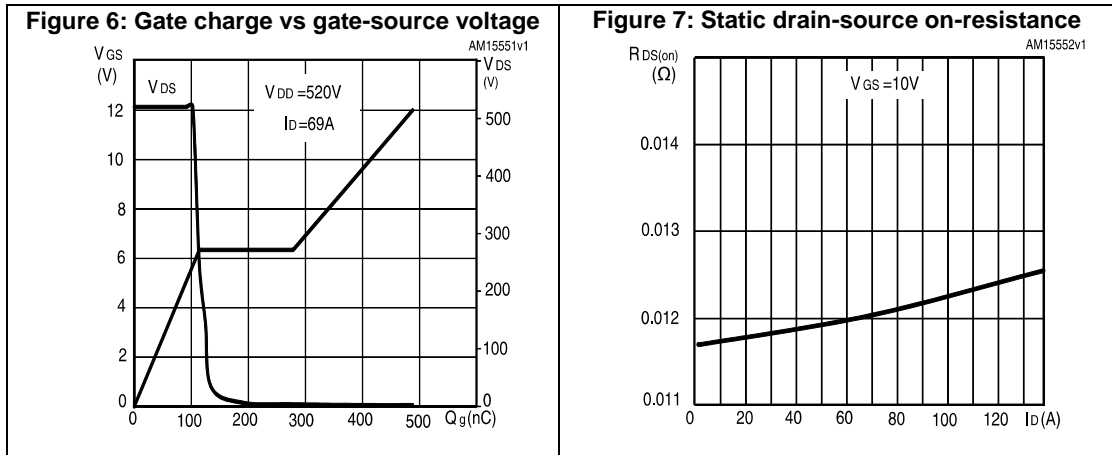
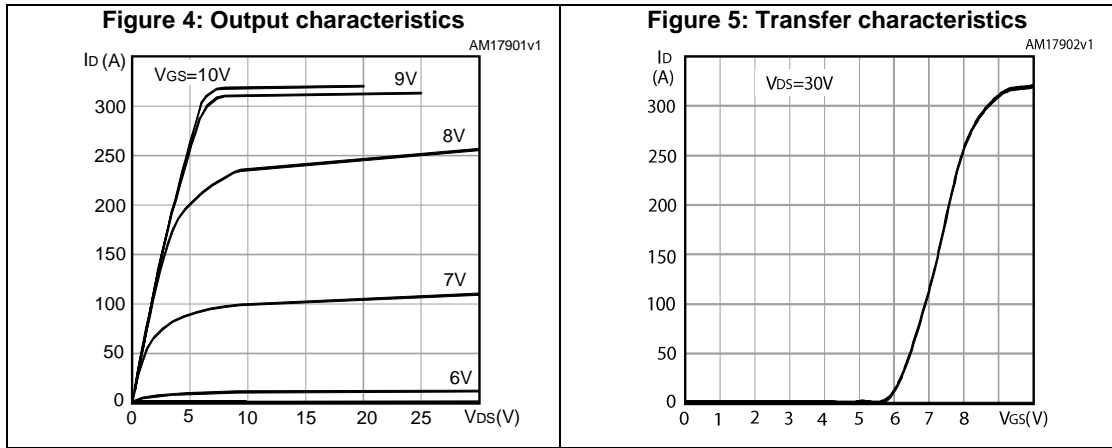
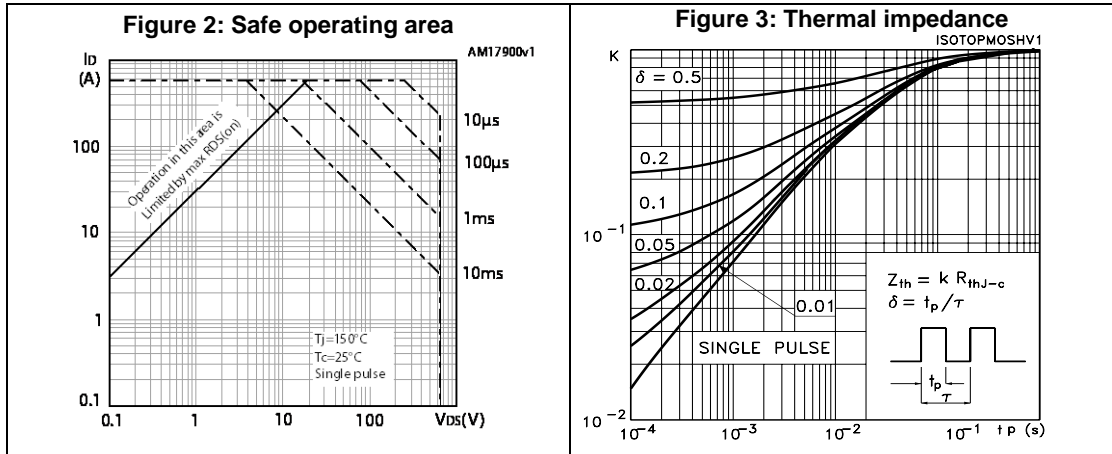


Figure 8: Capacitance variations

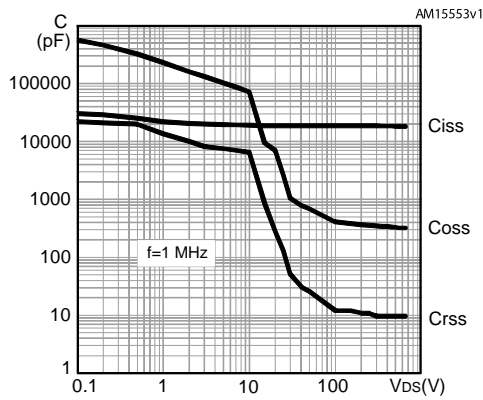


Figure 9: Normalized gate threshold voltage vs temperature

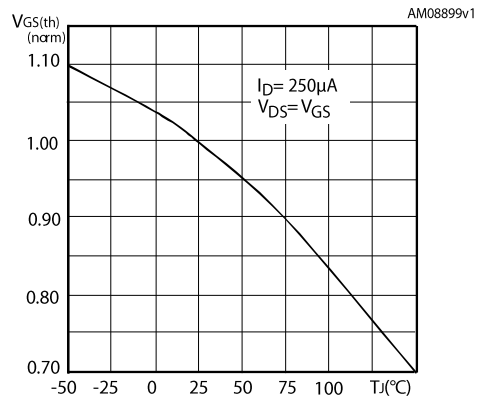


Figure 10: Normalized on-resistance vs temperature

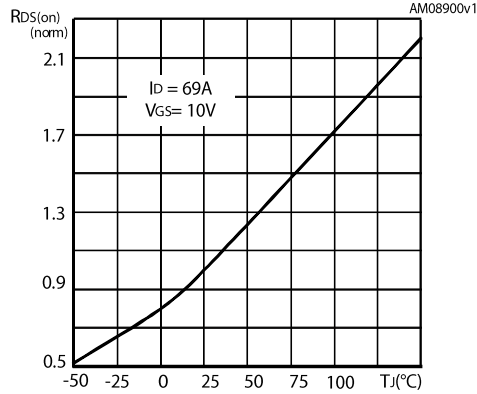


Figure 11: Normalized V_{(BR)DSS} vs temperature

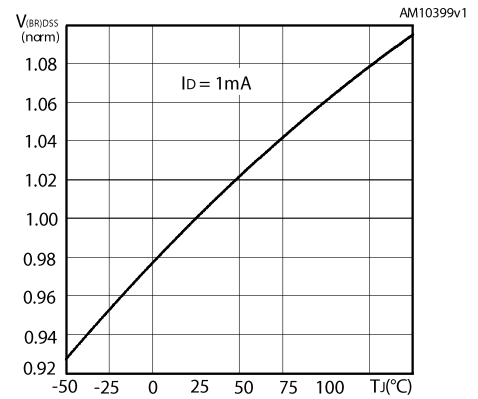


Figure 12: Output capacitance stored energy

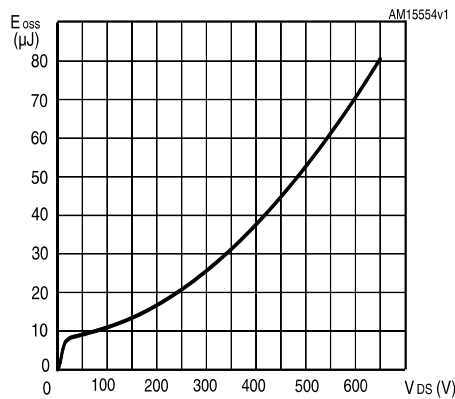
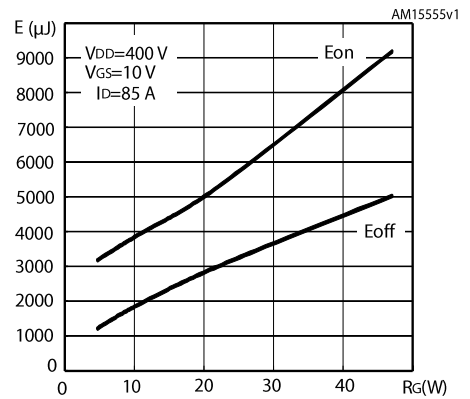


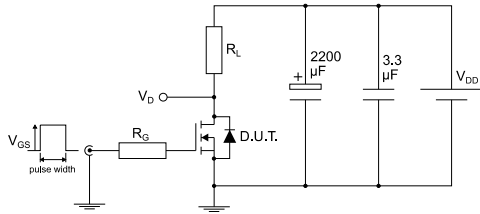
Figure 13: Switching losses vs gate resistance



The previous figure E_{on} includes reverse recovery of a SiC diode.

3 Test circuits

Figure 14: Test circuit for resistive load switching times



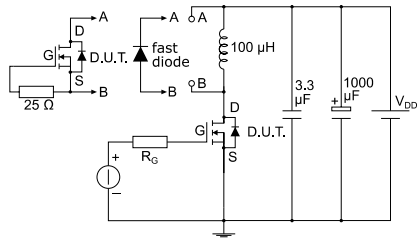
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Figure 15: Test circuit for gate charge behavior



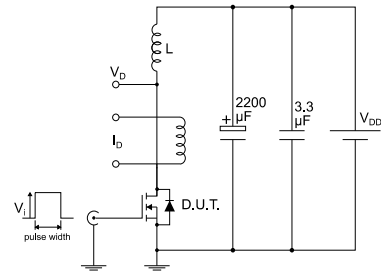
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Figure 16: Test circuit for inductive load switching and diode recovery times



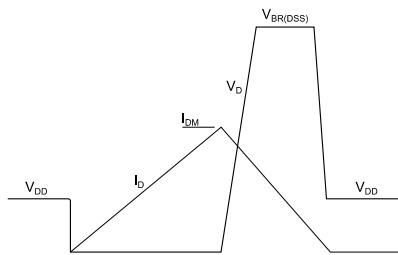
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Figure 17: Unclamped inductive load test circuit



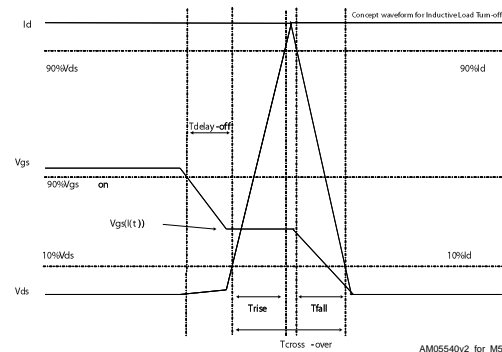
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



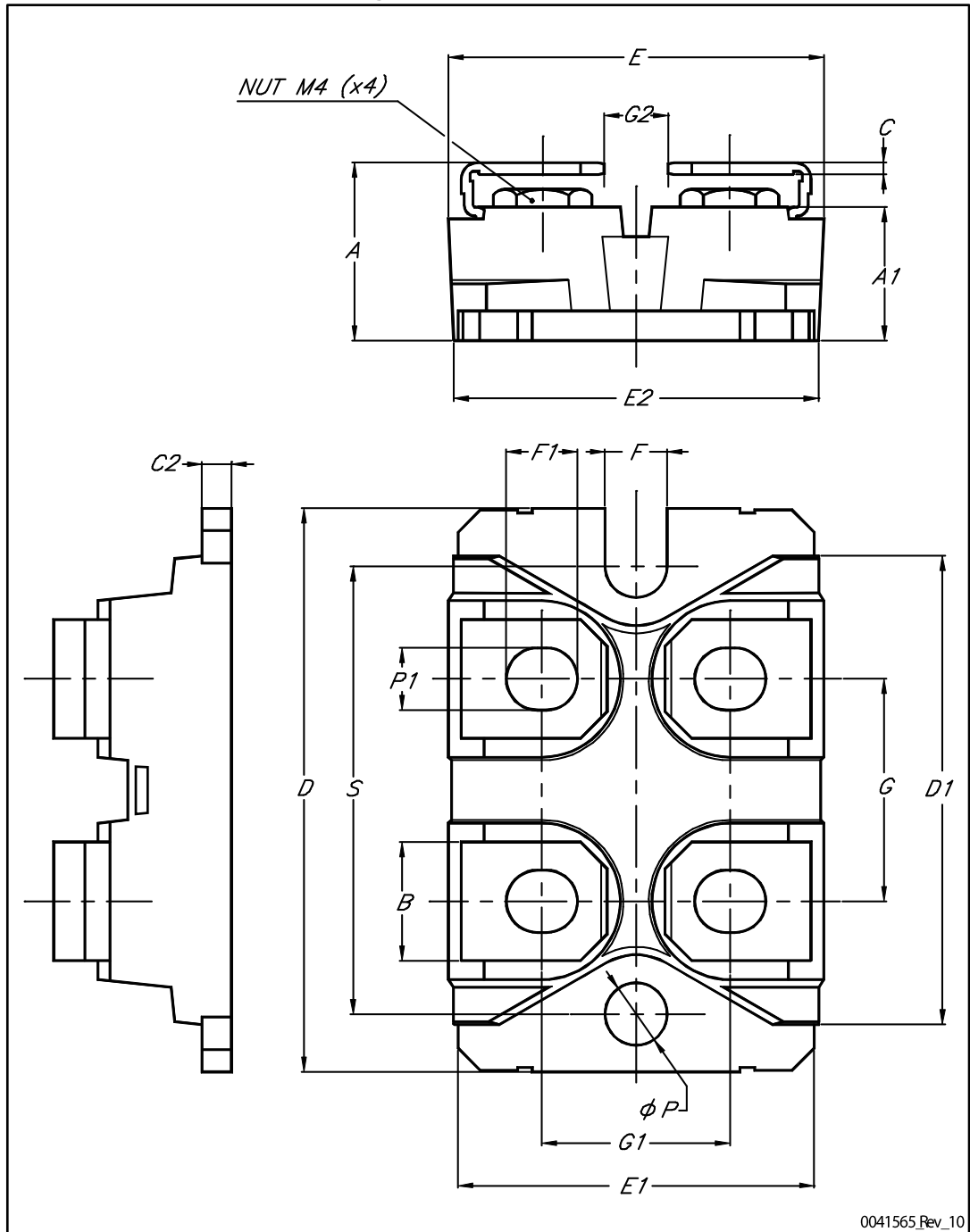
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 ISOTOP package information

Figure 20: ISOTOP outline



0041565_Rev_10

Table 8: ISOTOP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	11.80		12.20
A1	8.90		9.10
B	7.80		8.20
C	0.75		0.85
C2	1.95		2.05
D	37.80		38.20
D1	31.50		31.70
E	25.15		25.50
E1	23.85		24.15
E2		24.80	
G	14.90		15.10
G1	12.60		12.80
G2	3.50		4.30
F	4.10		4.30
F1	4.60		5
ØP	4		4.30
P1	4		4.40
S	30.10		30.30

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
18-Nov-2013	1	First release.
12-Nov-2015	2	Updated title, features and description on cover page. Document status promoted from preliminary to production data. Modified: <i>Table 2: "Absolute maximum ratings"</i> and <i>Figure 12: "Output capacitance stored energy"</i> Minor text changes.

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