



# STD96N3LLH6

N-channel 30 V, 0.0037  $\Omega$ , 80 A, DPAK  
STripFET™ VI DeepGATE™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD96N3LLH6	30 V	0.0042 $\Omega$	80 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate drive power losses

## Application

- Switching applications
  - Automotive

## Description

This product is an N-channel Power MOSFET that utilizes the 6<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

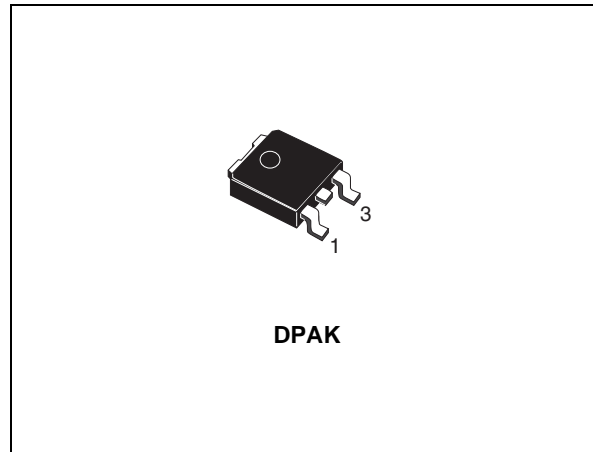


Figure 1. Internal schematic diagram

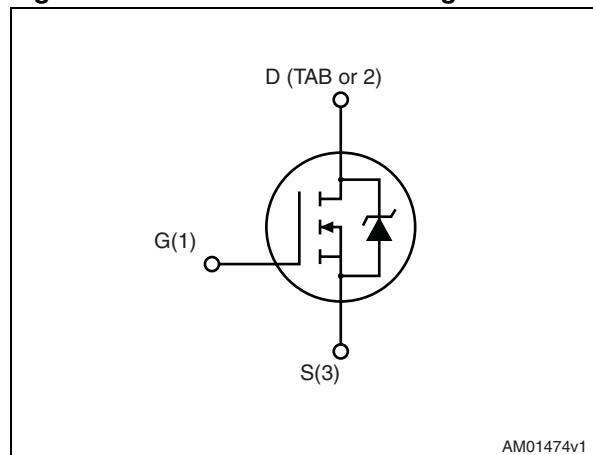


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD96N3LLH6	96N3LLH6	DPAK	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	61	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
	Derating factor	0.47	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	150	mJ
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	175	$^\circ\text{C}$

1. Limited by wire bonding.
2. Pulse width limited by safe operating area.
3. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_{AV} = 55\text{ A}$ ,  $L = 0.1\text{ mH}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.14	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	100	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	$^\circ\text{C/W}$
$T_l$	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

1. When mounted on FR-4 board of  $1\text{ inch}^2$ , 2 oz Cu.

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 30 V V <sub>DS</sub> = 30 V, T <sub>c</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		2.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		0.0037	0.0042	Ω
		V <sub>GS</sub> = 5.5 V, I <sub>D</sub> = 40 A		0.0055	0.007	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f=1 MHz, V <sub>GS</sub> = 0	-	2200	-	pF
C <sub>oss</sub>	Output capacitance			400		pF
C <sub>rss</sub>	Reverse transfer capacitance			280		pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 80 A	-	20	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 4.5 V		8.2		nC
Q <sub>gd</sub>	Gate-drain charge	<a href="#">Figure 13</a>		7.5		nC
Q <sub>gs1</sub>	Pre V <sub>th</sub> gate-to-source charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 80 A <a href="#">Figure 18</a>	-	3.4	-	nC
Q <sub>gs2</sub>	Post V <sub>th</sub> gate-to-source charge			6.2		nC
R <sub>G</sub>	Gate input resistance	f = 1 MHz gate bias Bias = 0 test signal level = 20 mV open drain	-	1	-	Ω

**Table 6. Switching on/off (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD} = 15\text{ V}$ , $I_D = 40\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 5\text{ V}$ <a href="#">Figure 12</a>	-	19 91	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD} = 15\text{ V}$ , $I_D = 40\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 5\text{ V}$ <a href="#">Figure 12</a>	-	24.5 23.4	-	ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40\text{ A}$ , $V_{GS} = 0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 24\text{ V}$ <a href="#">Figure 14</a>	-	28.6		ns
$Q_{rr}$	Reverse recovery charge		-	22.8		nC
$I_{RRM}$	Reverse recovery current		-	1.6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

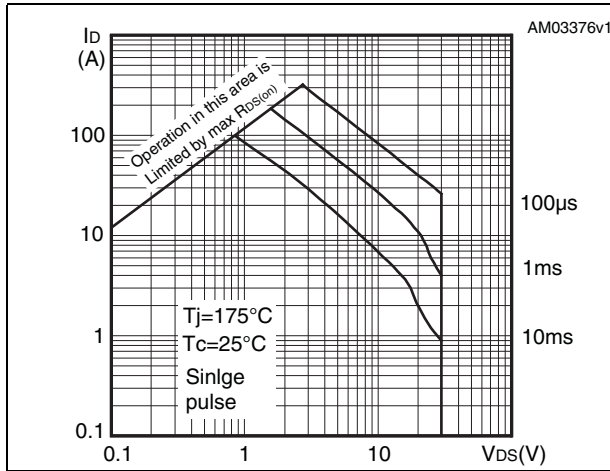


Figure 3. Thermal impedance

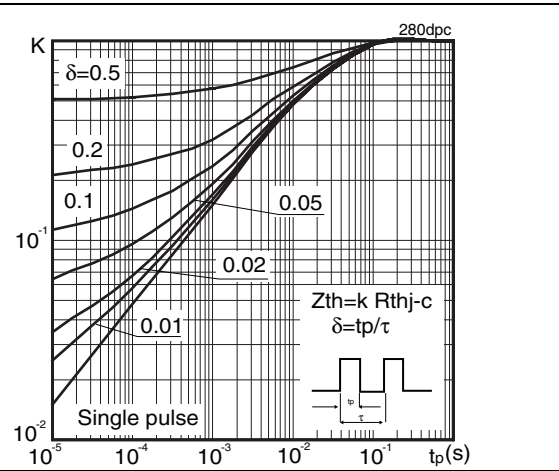


Figure 4. Output characteristics

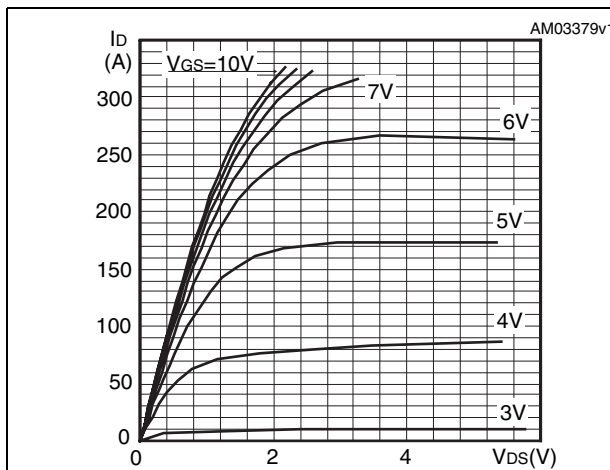


Figure 5. Transfer characteristics

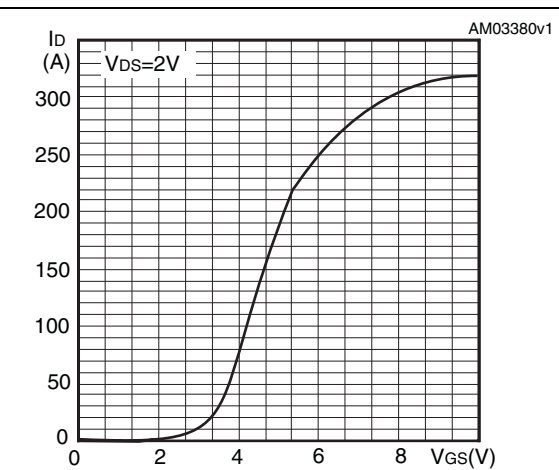


Figure 6. Normalized BV<sub>DSS</sub> vs temperature

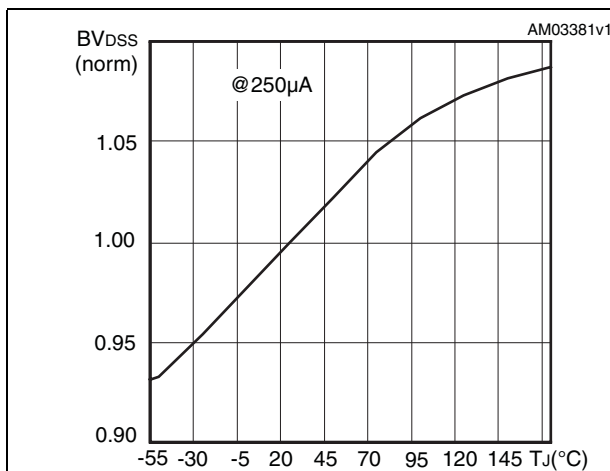


Figure 7. Static drain source on resistance

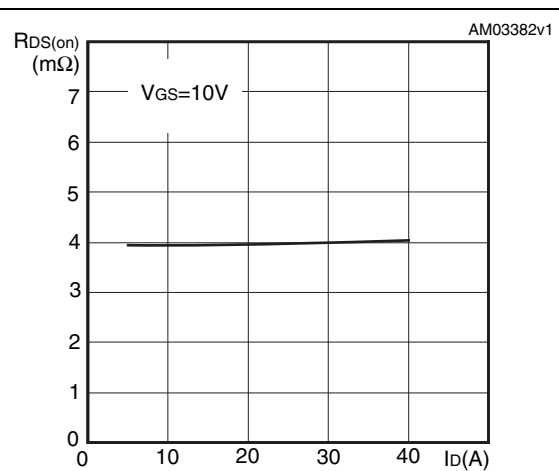


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

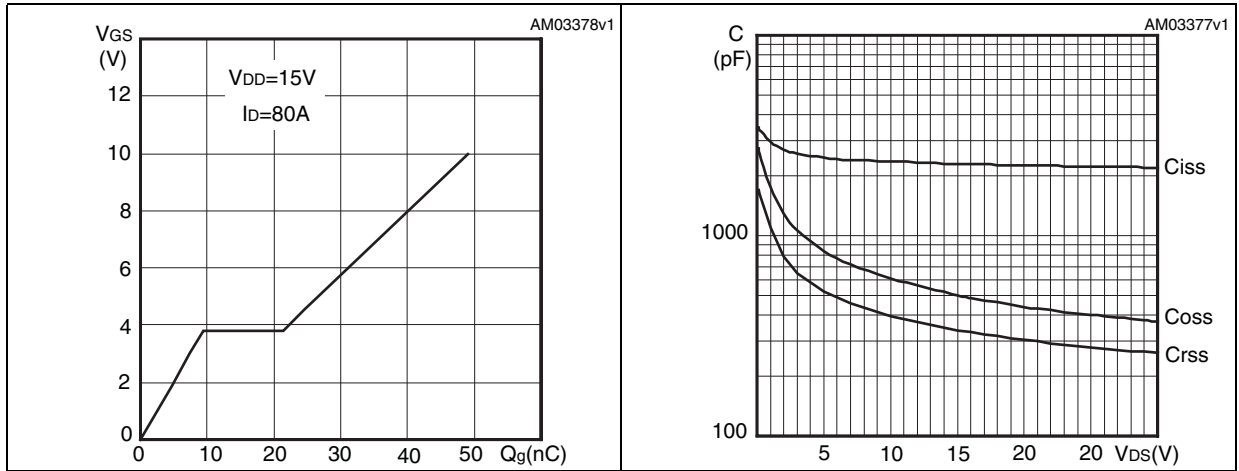
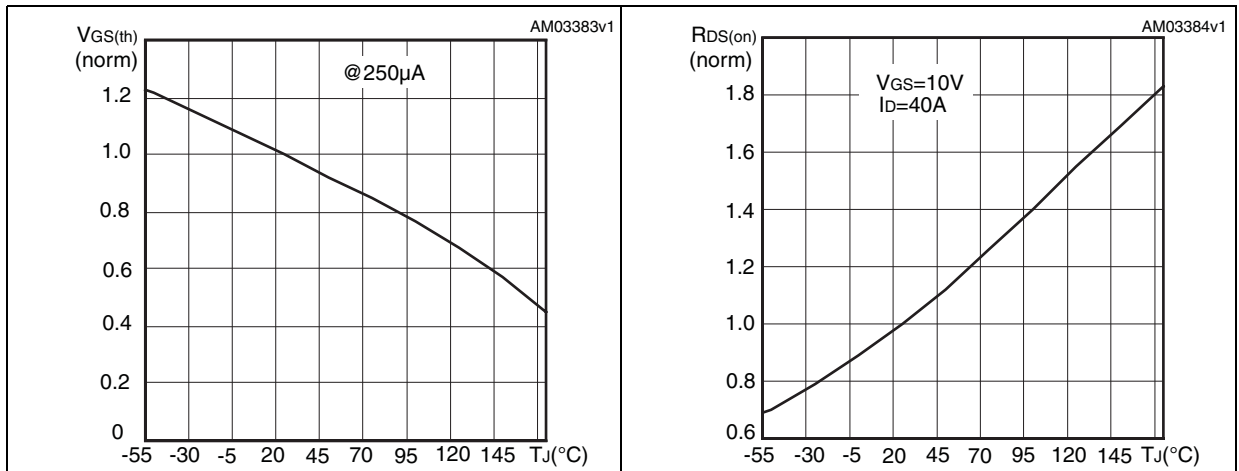
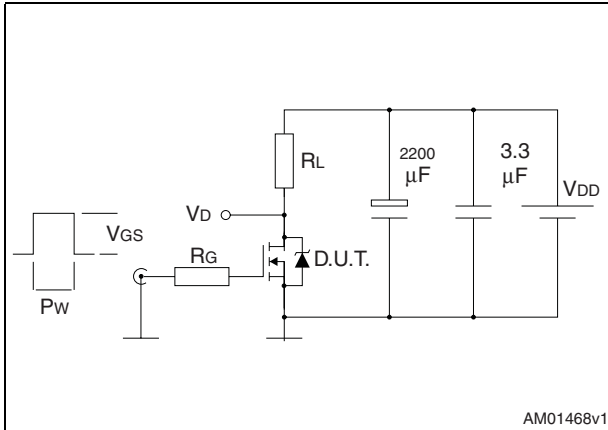


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature



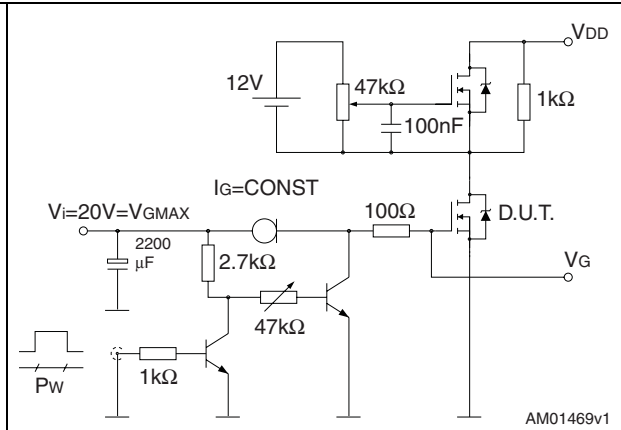
### 3 Test circuits

**Figure 12. Switching times test circuit for resistive load**



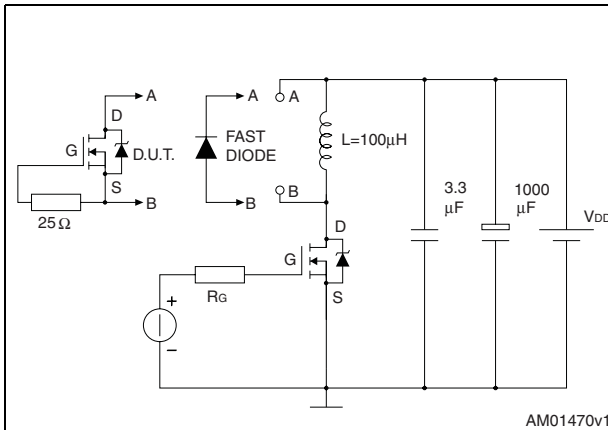
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**Figure 13. Gate charge test circuit**



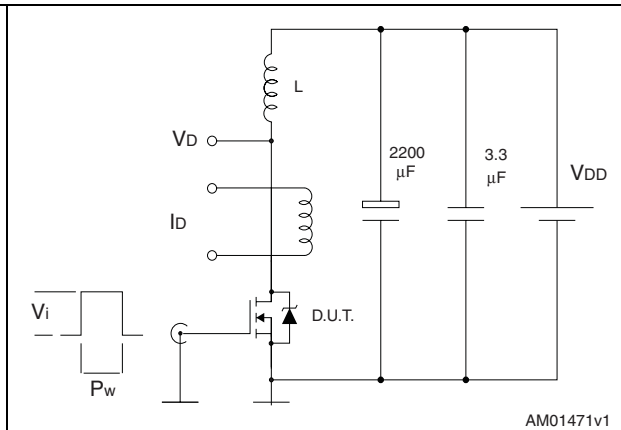
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**Figure 14. Test circuit for inductive load switching and diode recovery times**



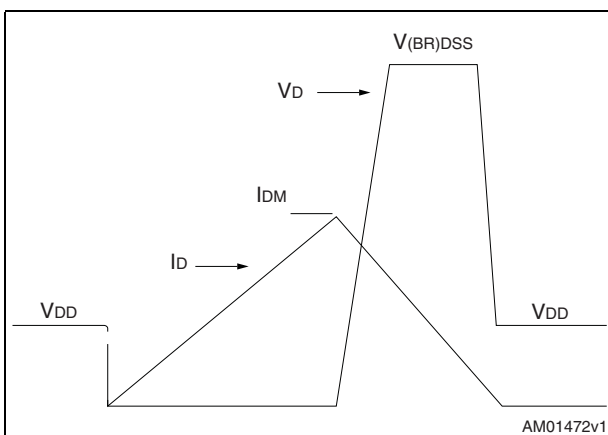
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**Figure 15. Unclamped inductive load test circuit**



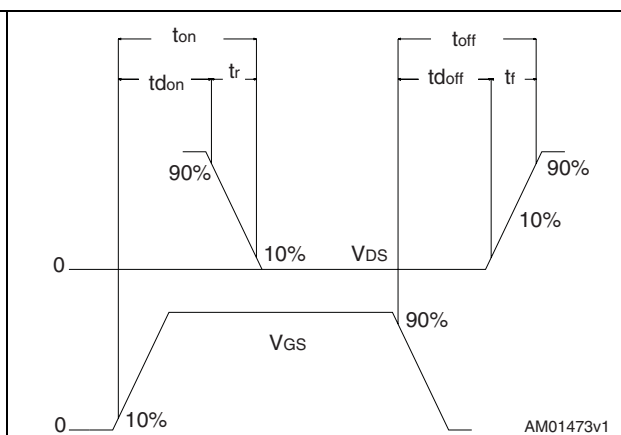
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**Figure 16. Unclamped inductive waveform**



AM01472v1

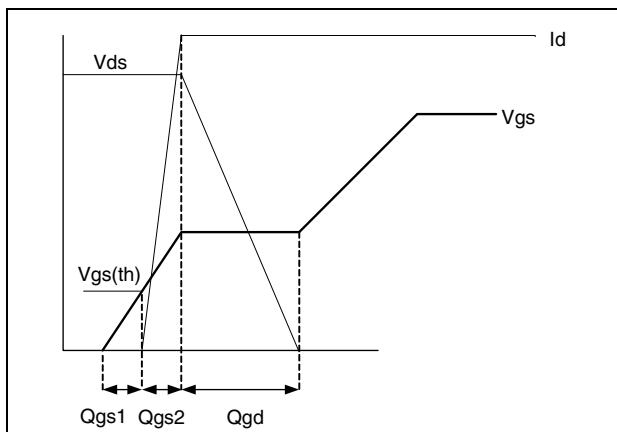
**Figure 17. Switching time waveform**



AM01473v1



Figure 18. Gate charge waveform



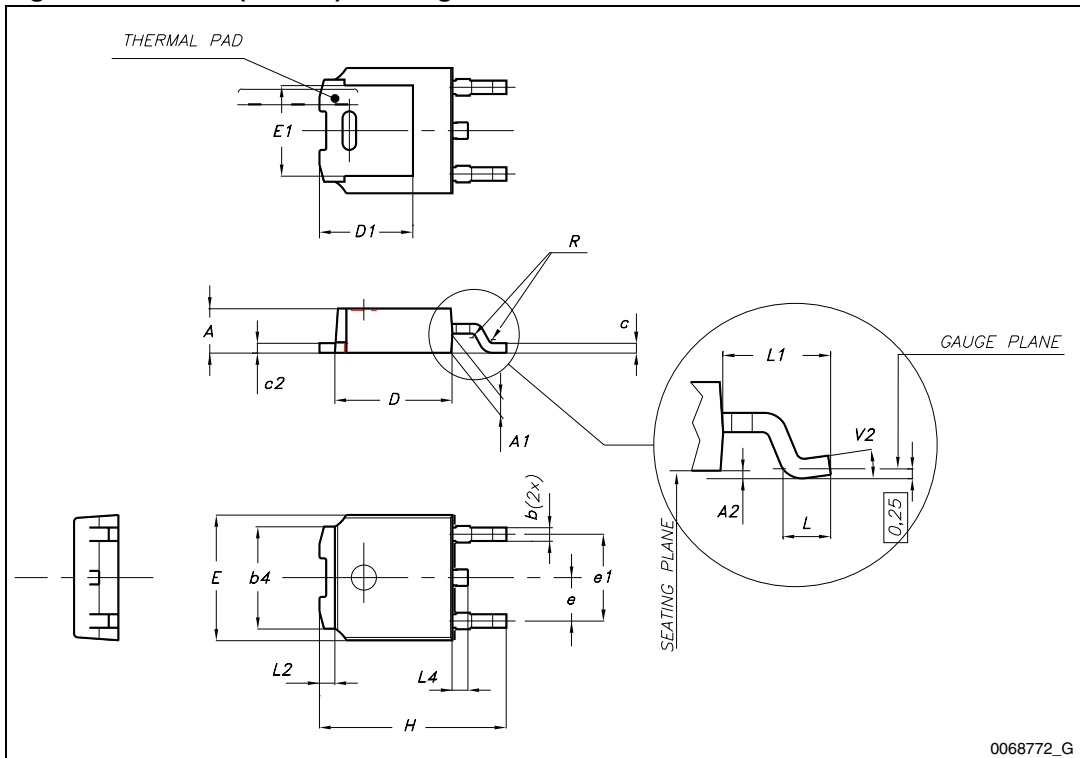
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 8. DPAK (TO-252) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 19. DPAK (TO-252) drawing

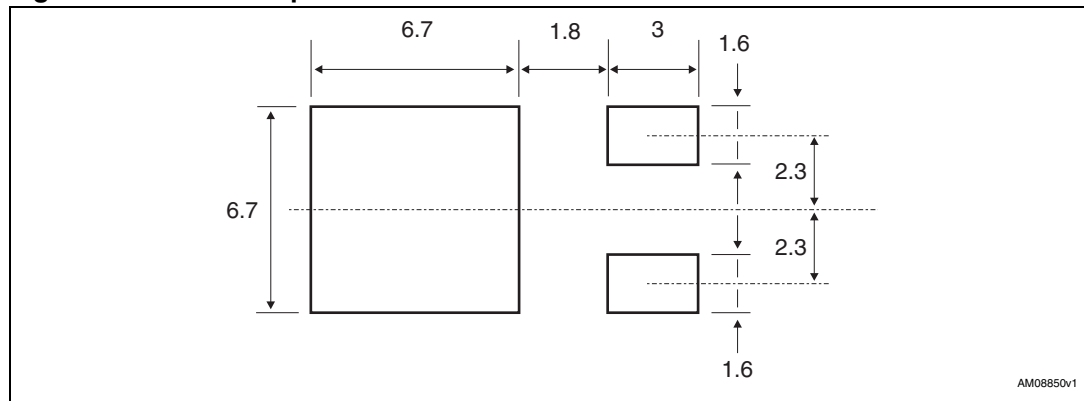


## 5 Packaging mechanical data

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.	2500	
P1	7.9	8.1	Bulk qty.	2500	
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

**Figure 20. DPAK footprint<sup>(a)</sup>**



a. All dimension are in millimeters

Figure 21. Tape for DPAK (TO-252)

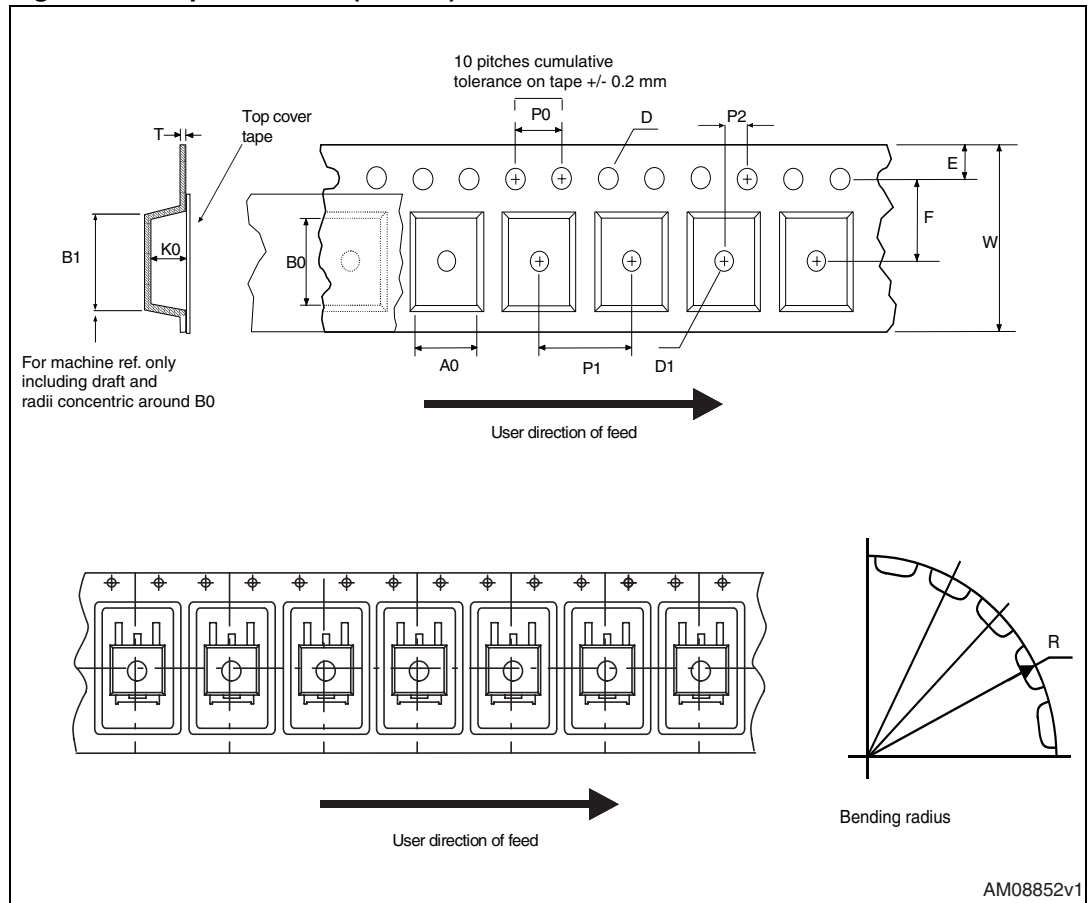
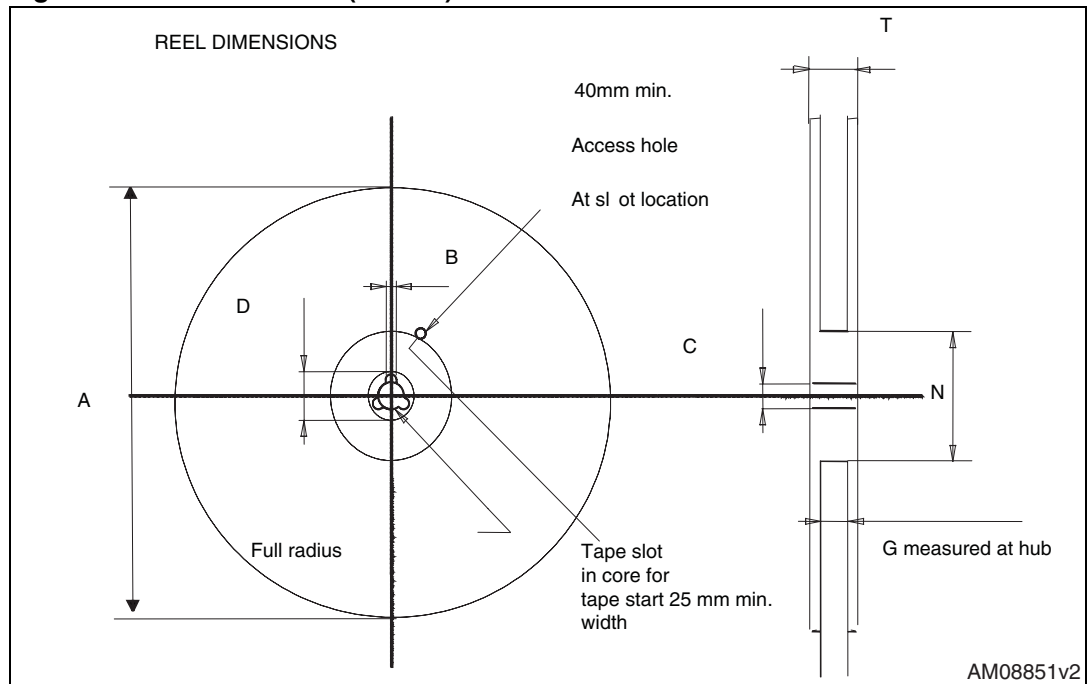


Figure 22. Reel for DPAK (TO-252)



## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-Jan-2011	1	First release.

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