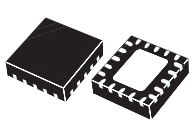
STCF03

High power white LED driver with I²C™ interface

Features

- Buck-boost dc/dc converter
- Drives one power white LED up to 800 mA from 2.7 V to 5.5 V in QFN
- Drives one power white LED up to 800 mA from 3.3 V to 5.5 V in BGA
- Efficient up to 92%
- Output current control
- 1.8 MHz typ. fixed frequency PWM
- Synchronous rectification
- Full I²C control
- Operational modes:
  - Shutdown mode
  - Shutdown + NTC
  - Ready mode + auxiliary red LED
  - Flash mode: up to 800 mA
  - Torch mode: up to 200 mA
- Soft and hard triggering of flash
- Flash and torch dimming with 16 exponential values
- Dimmable red LED indicator auxiliary output
- Internally or externally timed flash operation
- Digitally programmable safety time-out in flash mode
- LED overtemperature detection and protection with external NTC resistor
- Opened and shorted led failure detection and protection
- Chip over temperature detection and protection
- < 1 µA shutdown current



QFN20 (4x4)

TFBGA25 (3x3)

- Packages:
  - QFN20 (4x4)
  - TFBGA25 (3x3)

Applications

- Cell phone and smart phone
- Camera flashes/strobe
- PDAs and digital still cameras

Description

The STCF03 is a high efficiency power supply solution to drive a single flash LED in camera phone, PDAs and other hand-held devices. It is a buck - boost converter to guarantee a proper LED current control over all possible conditions of battery voltage and output voltage; the output current control ensure a good current regulation over the forward voltage spread characteristics of the Flash LED.

Thanks to the high efficiency of the converter allows having the input current taken from the battery remain under 1.5 A. (See continuous description)

Table 1. Device summary

Order code	Package	Packaging
STCF03PNR	QFN20 (4x4 mm)	4500 parts per reel
STCF03TBR (1)	TFBGA25 (3x3 mm)	3000 parts per reel

1. Available on request.

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1 Description (continued)

All the functions of the device are controlled through the I^2C which helps bus that allows to reduce logic pins on the package and to save PCB tracks on the board. Hard and soft-triggering of Flash are both supported. The device includes many functions to protect the chip and the power LED such as: a soft start control, chip over temperature detection and protection as well as opened and shorted LED detection and protection. Besides, a digital programmable Time Out function protects the LED in case of a wrong command from the µP. An optional external NTC resistor is supported to protect the LED against over heating.

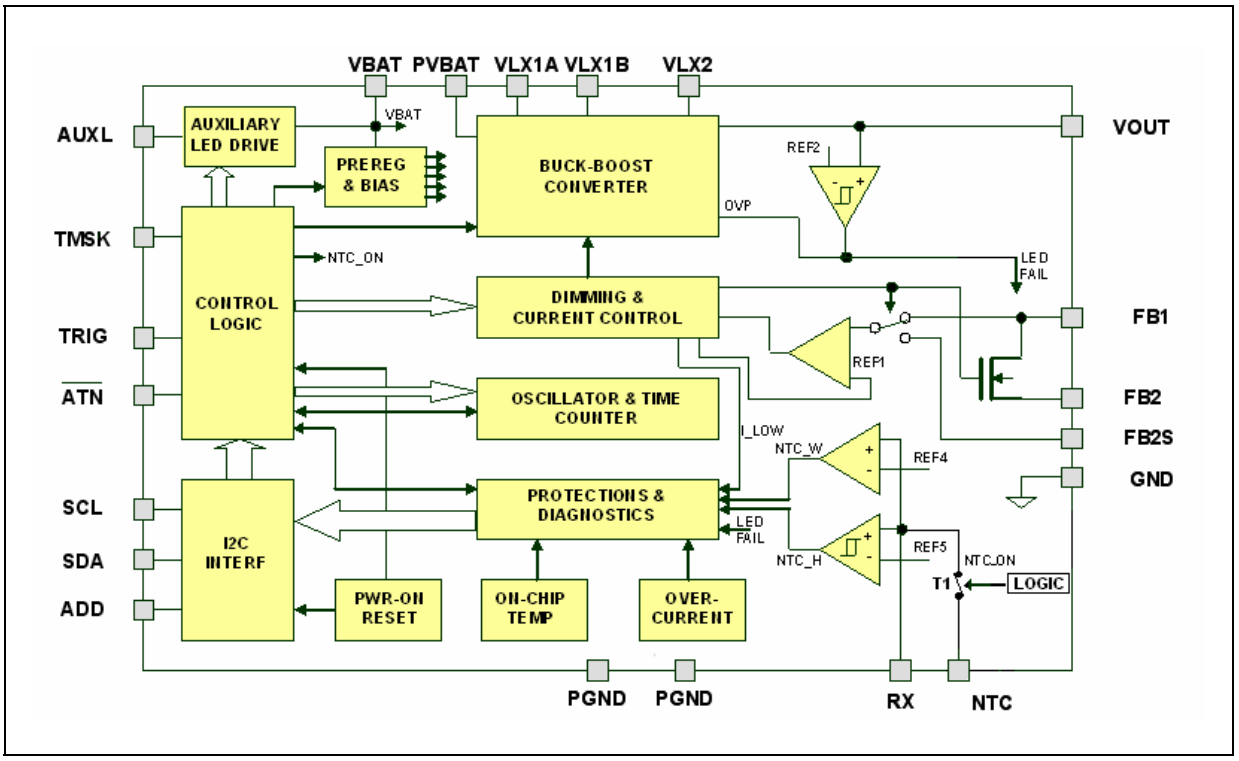
In mobile phone applications it is possible to reduce immediately the Flash LED current during the signal transmission using the TMSK pin. This saves battery life and gives more priority to supply RF transmission instead of flash function.

It is possible by I^2C to separately program the current intensity in FLASH and TORCH MODE using exponential steps. An auxiliary output can control an optional red LED to be used as a recording indicator.

The device is packaged in QFN 4x4 20L with a height less than 1 mm and in TFBGA25 3x3.

2 Diagram

Figure 1. Block diagram



3 Pin configuration

Figure 2. Pin connections (bottom view)

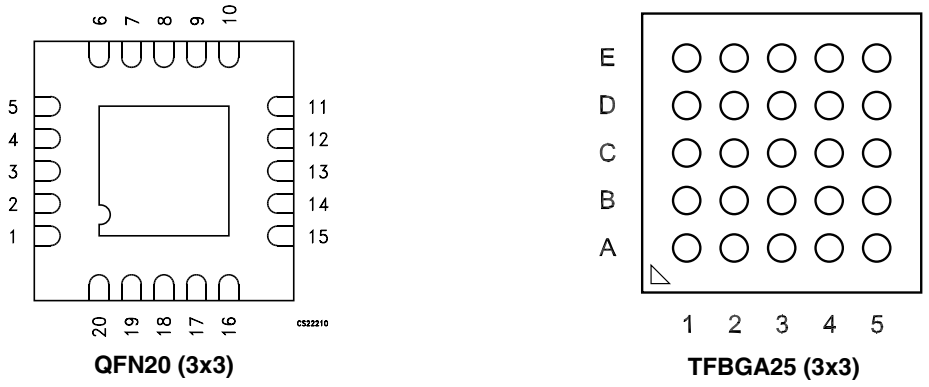


Table 2. Pin description

Pin n° for QFN20	Pin n° for TFBGA25	Symbol	Name and function
1	E1, D2	VLX2	Inductor connection
2	B3	RX	Rx resistor connection
3	A4	NTC	NTC resistor connection
4	D1, C2	VOUT	Output voltage
5	B5	FB1	Feedback pin [I_{LED}*(R_{FL}+R_{TR})]
6	A5	FB2	R_{TR} bypass
7	B4	FB2S	Feedback sensing pin [I_{LED}*R_{FL}]
8	E2	GND	Signal ground
9	D4	ADD	I^2C address selection
10	D5	AUXL	Auxiliary LED output
11	C5	TMSK	TX mask input.
12	B1, C1	PVBAT	Power supply voltage
13	A3	VBAT	Supply voltage
14	A2	VLX1A	Inductor connection
15	A1, B2	VLX1B	Inductor connection
16	E5	SCL	I^2C clock signal
17	E3	SDA	I^2C data
18	C3, D3	PGND	Power ground
19	E4	ATN	Attention (open drain output, active LOW)
20	C4	TRIG	Flash trigger input
Exposed pad		PGND	To be connected to the PCB ground plane for optimal electrical and thermal performance.

4 Maximum ratings

Table 3. Absolute maximum ratings (see note)

Symbol	Parameter	Value	Unit
VBAT	Signal supply voltage	-0.3 to 6	V
PVBAT	Power supply voltage	-0.3 to 6	V
VLX1A, VLX1B	Inductor connection 1	–0.3 to V_I+0.3	V
VLX2	Inductor connection 2	–0.3 to V_O+0.3	V
VOUT	Output voltage	-0.3 to 6	V
AUXL	Auxiliary LED	–0.3 to V_I+0.3	V
FB1, FB2, FB2S	Feedback and sense voltage	-0.3 to 3	V
SCL, SDA, TRIG, ATN, ADD TMSK	Logic Pin	-0.3 to V_I+0.3	V
R_X	Connection for reference resistor	-0.3 to 3	V
NTC	Connection for LED Temperature sensing	-0.3 to 3	V
ESD	Human body model	±2	kV
P_{TOT} (BGA) (1)	Continuous power dissipation (at T_A=70°C)	800	mW
T_{OP}	Operating junction temperature range	-40 to 85	°C
T_J	Junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C

1. Power dissipation is related parameter to used PCB. The recommended PCB design is included in the application note.

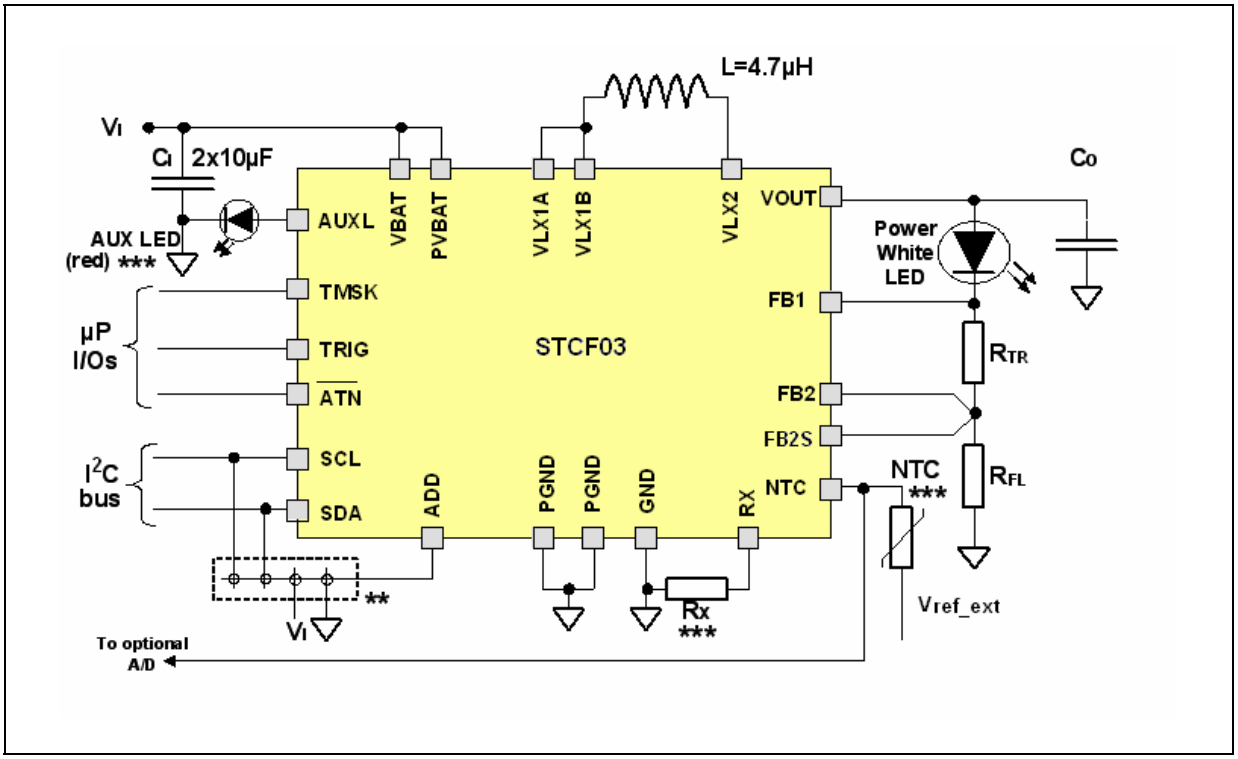
Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	QFN20	TFBGA25	Unit
R_{thJA}	Thermal resistance junction-ambient	59	150	°C/W

5 Application

Figure 3. Application schematic



**: Connect to V_I, or GND or SDA or SCL to choose one of the 4 different I^2C Slave Addresses.

***: Optional components to support auxiliary functions.

Table 5. List of external components

Component	Manufacturer	Part number	Value	Size
C_I	TDK	X5R0J106M	10 µF	0603
C_O	TDK	X5R0J105M	1 µF	0603
L (I_{FLASH} = 0.5A)	TDK	VLF3012ST-4R7MR91	4.7 µH	2.6 x 2.8 x 1.2mm
L (I_{FLASH} = 0.8A)	TDK	VLF4012AT-4R7M1R1	4.7 µH	3.7 x 3.5 x 1.2mm
NTC	Murata	NCP21WF104J03RA	100kΩ	0805
R_{FL}			0.27Ω	0603
R_{TR}			1.8Ω	0402
R_X			15kΩ	0402

Note: All of the above listed components refer to typical application. Operation of the STCF03 is not limited to the choice of these external components.

6 Electrical characteristics

Table 6. Electrical characteristics
(T_J = 25°C, V_I = 3.6 V, 2xC_I = 10 µF, C_O = 1 µF, L = 4.7 µH, R_{FL} = 0.27 Ω R_{TR} = 1.8 Ω, R_X = 15 KΩ, Typ. values @25°C, unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_I	Input operation supply voltage		2.7		5.5	V
$V_{PW\_ON\ RESET}$	Power ON reset threshold	V_I rising		2.3		V
I_O	Output current adjustment range I_{FLASH}	FLASH MODE for V_I = 2.7 V to 5.5 V (STCF03PNR)	60		800	mA
		FLASH MODE for V_I = 2.7 V to 3.3 V (STCF03TBR)	60		600	
		FLASH MODE for V_I=3.3 V to 5.5 V (STCF03TBR)	60		800	
	Output current adjustment range I_{TORCH}	Torch mode V_I = 2.7 V to 5.5 V	15		200	
	Auxiliary LED output current adjustment range I_{AUXLED}	Ready mode, V_I = 3.3 V to 5.5 V	0		20	
V_O	Regulated voltage range		2.5		5.3	V
FB1	Feedback voltage	Torch mode	30		250	mV
FB2	Feedback voltage	Flash mode	30		250	mV
ΔI_O	Output current tolerance	Flash mode, I_O = 160 mV/R_{FL}	-10		10	%
$R_{ON\_}$	FB1-FB2 ON resistance	Torch mode, I_O = 200 mA		90		mΩ
I_Q	Quiescent current in SHUTDOWN mode	NTC_ON=0		1		µA
		NTC_ON=1		1		
	Quiescent current in ready - mode			1.8		mA
f_s	Frequency	V_I = 2.7 V		1.8		MHz
ν	Efficiency of the chip itself	V_I = 3.2 to 4.2 V, Flash Mode, I_O = 800 mA		87		%
	Efficiency of the whole application	V_I = 3.2 to 4.2 V, Flash Mode, I_O = 800 mA, V_O=V_{fLED_max} + V_{FB2} = 5.02 V See the typical application schematic It is included losses of inductor and sensing resistor		76		
OVP	Output over voltage protection	V_I = 5.5 V, No Load	5.3			V
OV_{HYST}	Over voltage hysteresis	V_I = 5.5 V, No Load		0.3		V
OTP	Over temperature protection	V_I = 5.5 V		140		°C
OT_{HYST}	Over temperature hysteresis	V_I = 5.5 V		20		°C

Table 6. Electrical characteristics
(T_J = 25°C, V_I = 3.6 V, 2xC_I = 10 µF, C_O = 1 µF, L = 4.7 µH, R_{FL} = 0.27 Ω R_{TR} = 1.8 Ω, R_X = 15 KΩ, Typ. values @25°C, unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{ON}T1$	RX-NTC switch ON resistance	Ready mode		25		Ω
NTC_{LEAK}	RX-NTC switch OFF leakage	Shutdown mode, V_{NTC} = 2 V V_{RX} = GND			1	µA
V_{OL}	Output logic signal level low ATN	I_{OL} = 10 mA			0.2	V
I_{OZ}	Output logic leakage current ATN	V_{OZ} = 3.3 V			1	mA
V_{IL}	Input logic signal level SCL, SDA, TRIG, TEST, ADD	V_I = 2.7 V to 5.5 V	0		0.4	V
V_{IH}			1.4		3	
T_{ON}	LED current rise time I_{LED} = 0 to I_{LED} = max				2	ms

Note: Typical value, not production tested.

7 Introduction

The STCF03 is a buck-boost converter, dedicated to power and control the current of a Power White LED in a camera cell phone. The device operates at a constant switching frequency of 1.8 MHz typ. It provides an output voltage down to 2.5 V and up to 5.3 V, from a 2.7 V to 5.5 V supply voltage. This supply range allows operation from a single cell Lithium-Ion battery. The I^2C bus is used to control the device operation and for diagnostic purposes. The current in Torch mode is adjustable from 15 mA to 200 mA. Flash mode current is adjustable up to 800 mA, BGA version is able to deliver 600 mA at battery range 2.7 V to 3.3 V. The Aux LED current can be adjusted from 0 to 20 mA. The device uses an external NTC resistor to sense the temperature of the white LED. These two last functions may not be needed in all applications, and in these cases the relevant external components can be omitted.

7.1 Buck-Boost converter

The regulation of the PWM controller is done by sensing the current of the LED through external sensing resistors (R_{FL} and R_{TR}, see application schematic). Depending on the forward voltage of the Flash LED, the device automatically can change the operation mode between buck (step down) and boost (step up) mode.

Three cases can occur: Boost region ($V_O > V_{BAT}$): this configuration is used in most of the cases, as the output voltage $V_O = V_{fLED} + I_{LED}$ x RFL) is higher than V_{BAT}; Buck region ($V_O < V_{BAT}$); Buck / Boost region ($V_O \sim V_{BAT}$).

7.2 Logic pin description

7.2.1 SCL, SDA pins

These are the standard Clock and Data pins as defined in the I^2C bus specification. External pull-up is required according to I^2C bus specifications. The recommended maximum voltage of these signals should be 3.0 V.

7.2.2 TRIG pin

This input pin is internally AND-ed with the TRIG_EN bit to generate the internal signal that activates the flash operation. This gives to the user the possibility to accurately control the flash duration using a dedicated pin, avoiding the I^2C bus latencies (hard-triggering). No internal pull-up nor pull-down is provided.

7.2.3 ATN pin

This output pin (open-drain, active LOW) is provided to better manage the information transfer from the STCF03 to the µP. Because of the limitations of a Single Master I^2C bus configuration, the µP should regularly poll the STCF03 to verify if certain operations have been completed, or to check diagnostic information. Alternatively, the µP can use the ATN pin to be advised that new data are available in the STAT_REG, thus avoiding continuous polling. Then the information can be read in the STAT_REG by a read operation via I^2C that, besides, automatically resets the ATN pin. The STAT_REG bits affecting the ATN pin status are mapped in *Table 16*. No internal pull-up is provided.

7.2.4 ADD pin

With this pin it is possible to select one of the 4 possible I^2C slave addresses. No internal pull-up nor pull-down is provided. The pin has to be connected either GND, V_I, SCL or SDA to select the desired I^2C slave address (see *Table 6.*)

Table 7. Address table

ADD pin	A7	A6	A5	A4	A3	A2	A1	A0
GND	0	1	1	0	0	0	0	R/W
VBAT	0	1	1	0	0	0	1	R/W
SDAL	0	1	1	0	0	1	0	R/W
SCL	0	1	1	0	0	1	1	R/W

7.2.5 TMSK pin

This pin can be used to implement the TX masking function. This function has effect only for Flash current settings higher than 200 mA (bit FDIM_3=1). Under this condition, when this pin is pulled high by the P, the current flowing in the LED is forced at 200 mA typ. No internal pull-up nor pull-down is provided: to be externally wired to GND if TX masking function is not used.

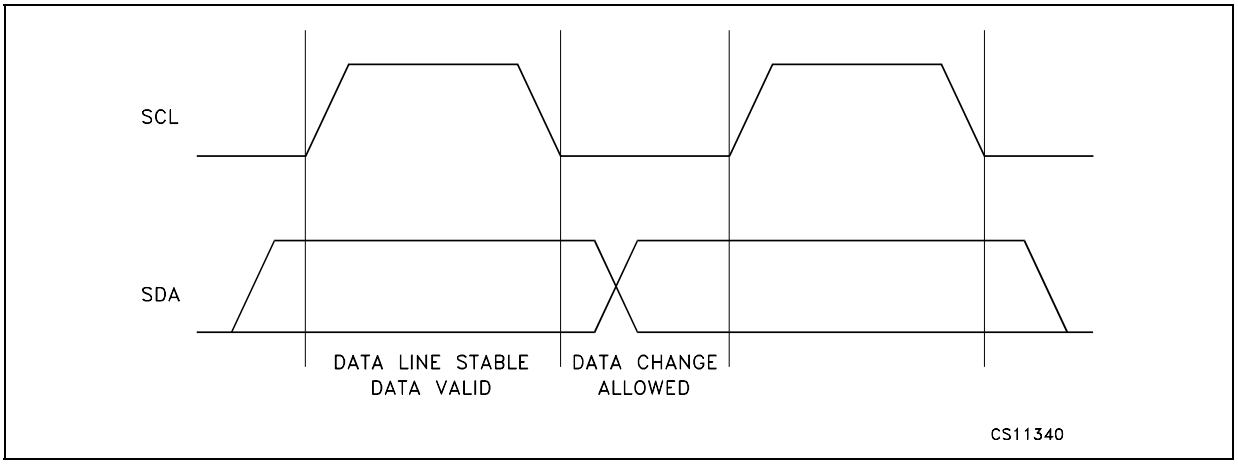
7.3 I^2C BUS interface

Data transmission from the main µP STCF03 and vice versa takes place through the 2 wires I^2C bus interface wires, consisting of the two lines SDA and SCL (pull-up resistors to a positive supply voltage must be externally connected). The recommended maximum voltage of these signals should be 3.0 V.

7.4 Data validity

As shown in *Figure 4*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

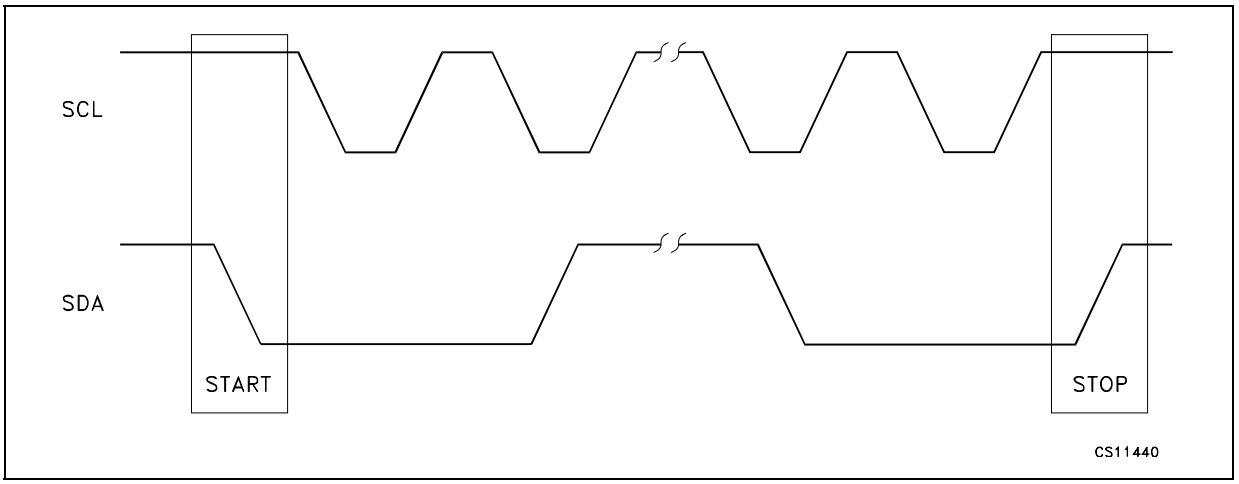
Figure 4. Data validity on the I^2C Bus



7.5 Start and stop conditions

Both DATA and CLOCK lines remain HIGH when the bus is not busy. As shown in *Figure 5* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition

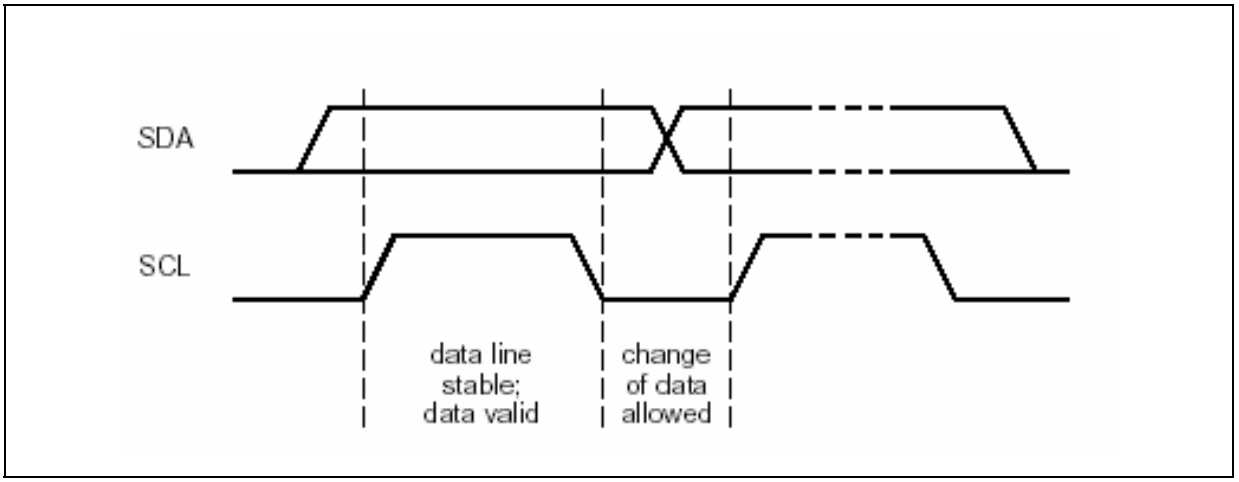
Figure 5. Timing diagram on I^2C Bus



7.6 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Any change in the SDA line at this time will be interpreted as a control signal.

Figure 6. Bit transfer



7.7 Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 7*). The peripheral (STCF03) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed has to generate an acknowledge pulse after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse duration. In this case the master transmitter can generate the STOP information in order to abort the transfer. The STCF03 won't generate the acknowledge if the V_I supply is below the undervoltage lockout threshold.

Figure 7. Acknowledge on I²C Bus

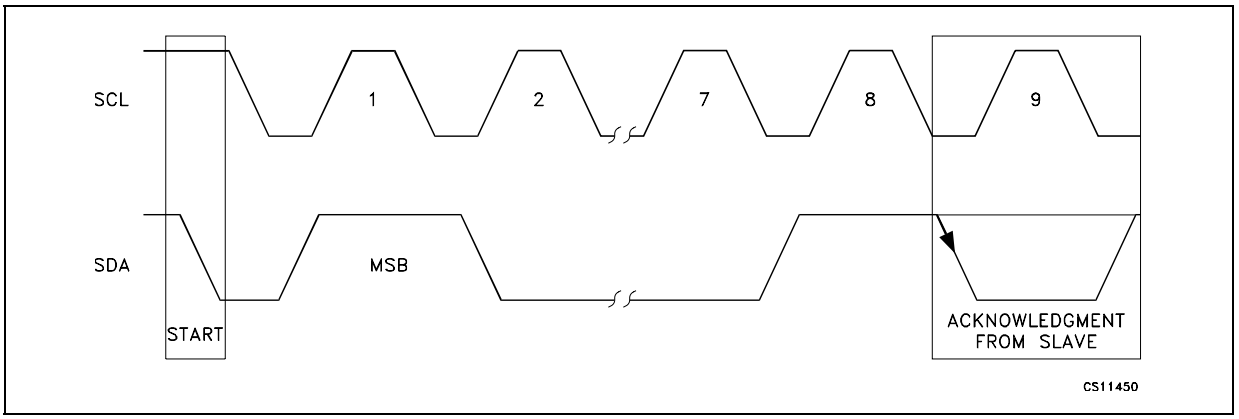


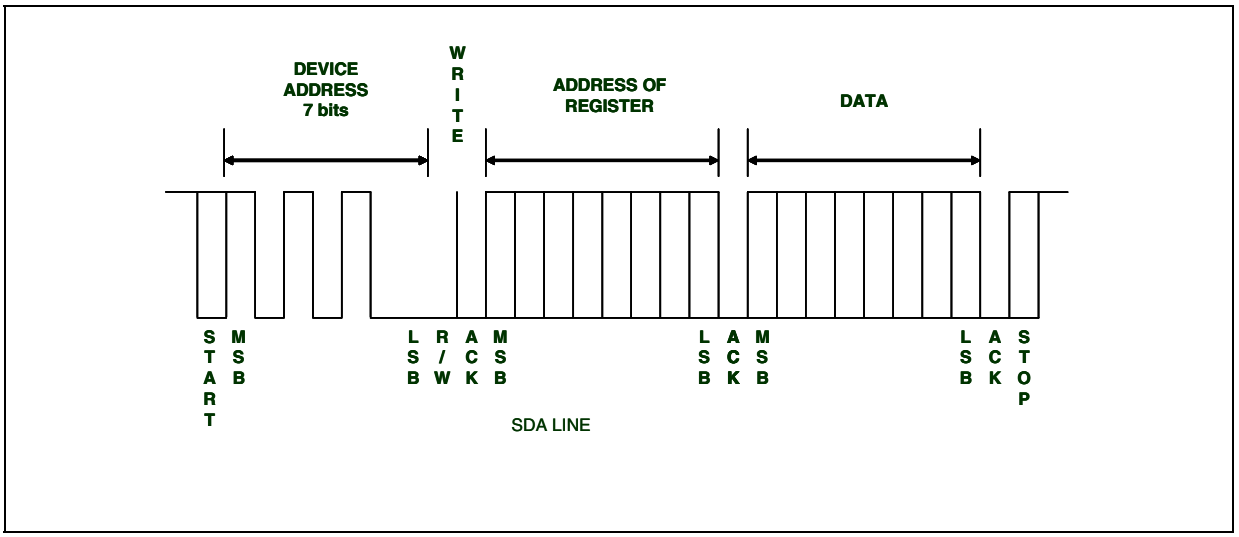
Table 8. Interface protocol

	Device address + R/W bit									Register address									Data									
	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0		
START	MSB						LSB	RW	ACK	MSB							LSB	ACK	MSB							LSB	ACK	STOP

7.8 Writing to a single register

Writing to a single register starts with a START bit followed by the 7 bit device address of STCF03. The 8th bit is the R/W bit, which is 0 in this case. R/W = 1 means a reading operation. Then the master waits for an acknowledge from STCF03. Then the 8 bit address of register is sent to STCF03. It is also followed by an acknowledge pulse. The last transmitted byte is the data that is going to be written to the register. It is again followed by an acknowledge pulse from STCF03. Then master generates a STOP bit and the communication is over. See *Figure 8* below.

Figure 8. Writing to a single register



7.9 Interface protocol

The interface protocol is composed:

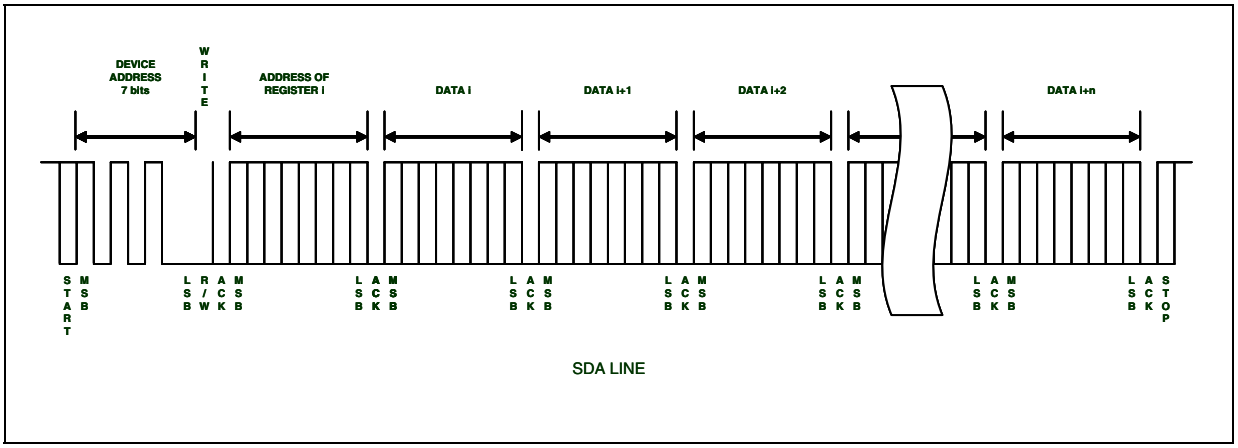
- A start condition (START)
- A Device address + R/W bit (read =1 / write =0)
- A Register address byte
- A sequence of data n* (1 byte + acknowledge)
- A stop condition (STOP)

The Register address byte determines the first register in which the read or write operation takes place. When the read or write operation is finished, the register address is automatically increased.

7.10 Writing to multiple registers with incremental addressing

It would be unpractical to send several times the device address and the address of the register when writing to multiple registers. STCF03 supports writing to multiple registers with incremental addressing. When the data is written to a register, the address register is automatically increased, so the next data can be sent without sending the device address and the register address again. See *Figure 9* below.

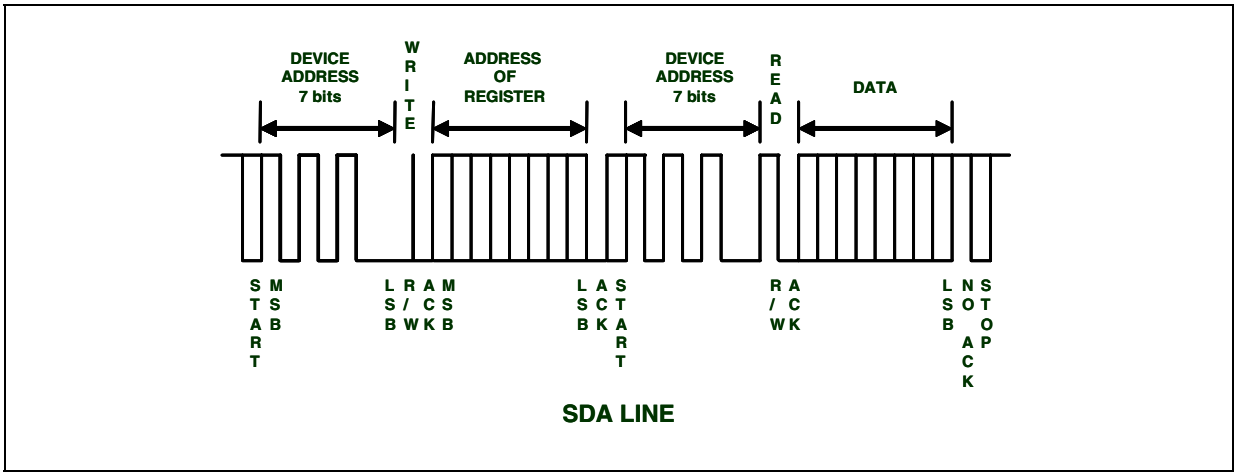
Figure 9. Writing to multiple register with incremental addressing



7.11 Reading from a single register

The reading operation starts with a START bit followed by the 7 bit device address of STCF03. The 8th bit is the R/W bit, which is 0 in this case. STCF03 confirms the receiving of the address + R/W bit by an acknowledge pulse. The address of the register which should be read is sent afterwards and confirmed again by an acknowledge pulse of STCF03 again. Then the master generates a START bit again and sends the device address followed by the R/W bit, which is 1 now. STCF03 confirms the receiving of the address + R/W bit by an acknowledge pulse and starts to send the data to the master. No acknowledge pulse from the master is required after receiving the data. Then the master generates a STOP bit to terminate the communication. See *Figure 10*

Figure 10. Reading from a single register

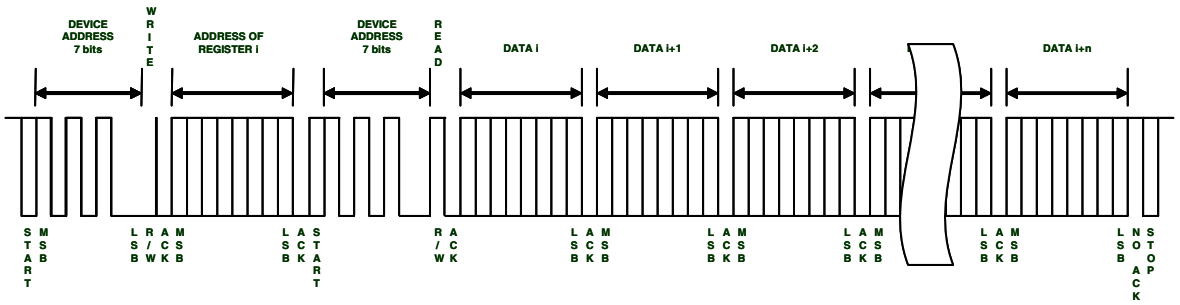


7.12 Reading from multiple registers with incremental addressing

Reading from multiple registers starts in the same way like reading from a single register. As soon as the first register is read, the register address is automatically increased. If the master generates an acknowledge pulse after receiving the data from the first register, then reading of the next register can start immediately without sending the device address and

the register address again. The last acknowledge pulse before the STOP bit is not required. See the *Figure 11*.

Figure 11. Reading from multiple registers



8 Description of internal registers

Table 9. I^2C Register mapping function

Register name	SUB ADDRESS (hex)	Operation
CMD_REG	00	R / W
DIM_REG	01	R / W
AUX_REG	02	R / W
STAT_REG	03	R only

Table 10. Command register

CMD_REG (write mode)	MSB							LSB
SUB ADD=00	PWR_ON	TRIG_EN	TCH_ON	NTC_ON	FTIM_3	FTIM_2	FTIM_1	FTIM_0
Power ON RESET Value	0	0	0	0	0	0	0	0

8.1 PWR_ON

When set, it activates all analog and power internal blocks including the NTC supporting circuit, and the device is ready to operate (Ready Mode). As long as PWR_ON=0, only the I^2C interface is active, minimizing Stand-by Mode power consumption.

8.2 TRIG_EN

This bit is AND-ed with the TRIG pin to generate the internal signal FL_ON that activates Flash Mode. By this way, both soft-triggering and hard-triggering of the Flash are made possible. If soft-triggering (through I^2C) is chosen, the TRIG pin is not used and must be kept HIGH (VI). If hard-triggering is chosen, then the TRIG pin has to be connected to a µP I/O devoted to Flash timing control, and the TRIG_EN bit must be set in advance. Both triggering modes can benefit of the internal Flash Time Counter, that uses the TRIG_EN bit and can work either as a safety shut-down timer or as a Flash duration timer. Flash mode can start only if PWR_ON=1. LED current is controlled by the value set by the FDIM_0~3 of the DIM_REG.

8.3 TCH_ON

When set from Ready Mode, the STCF03 enters the Torch mode. The LED current is controlled by the value set by the TDIM_0~3 of the DIM_REG.

8.4 NTC_ON

In ready mode, the comparators that monitor the LED temperature are activated if NTC_ON bit is set. NTC-related blocks are always active regardless of this bit in Torch mode and Flash mode.

8.5 FTIM_0~3

This 4bit register defines the maximum Flash duration. It is intended to limit the energy dissipated by the LED to a maximum safe value or to leave to the STCF03 the control of the Flash duration during normal operation. Values from 0~15 correspond to 0~1.5s (100ms steps). The timing accuracy is related to the internal oscillator frequency that clocks the Flash Time Counter (+/-20%). Entering Flash mode (either by soft or hard triggering) activates the Flash Time Counter, which begins counting down from the value loaded in the F_TIM register. When the counter reaches zero, Flash mode is stopped by resetting TRIG_EN bit, and simultaneously the ATN pin is set to true (LOW) to alert the µP that the maximum time has been reached. FTIM value remains unaltered at the end of the count.

Table 11. Dimming register

DIM_REG (write mode)	MSB							LSB
SUB ADD=01	TDIM_3	TDIM_2	TDIM_1	TDIM_0	FDIM_3	FDIM_2	FDIM_1	FDIM_0
Power ON, SHUTDOWN MODE RESET Value	0	0	0	0	0	0	0	0

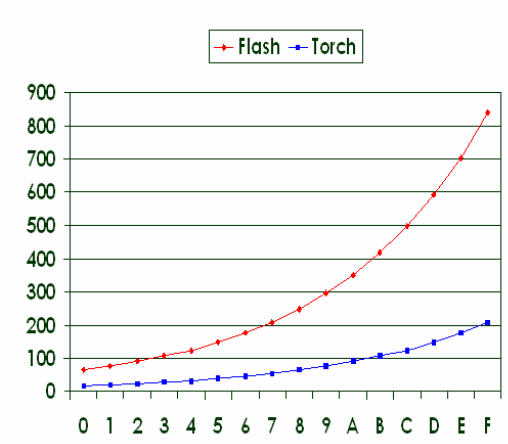
8.6 TDIM_0~3

These 4 bits define the LED current in Torch mode with 16 values fitting an exponential law. Max Torch current value is 25% of max Flash current. (*Figure 12*)

8.7 FDIM_0~3

These 4 bits define the LED current in Flash mode with 16 values fitting an exponential law. The Max value of the current is set by the external resistors R_{FL} and R_{TR}. (*Figure 12*)

Figure 12. Flash and Torch current vs. dimming value



Current Step Coefficient - 1.19

Note: LED current values refer to R_{FL}=0.27 Ω, R_{TR}=1.8 Ω

Table 12. Auxiliary register

AUX_REG (write mode)	MSB							LSB
SUB ADD=02	AUXI_3	AUXI_2	AUXI_1	AUXI_0	AUXT_3	AUXT_2	AUXT_1	AUXT_0
Power ON, SHUTDOWN MODE RESET Value	0	0	0	0	0	0	0	0

8.8 AUXI_0~3

This 4 bits register defines the AUX LED current from 0 to 20 mA. See AUX LED Dimming Table for reference. Loading any value between 1 and 15 also starts the AUX LED current source timer, if enabled. The AUX LED current source is active only in Ready Mode, and is deactivated in any other mode.

8.9 AUXT_0~3

This 4 bit register controls the timer that defines the ON-time of the AUX LED current source. ON-time starts when the AUXI register is loaded with any value other than zero, and stops after the time defined in the AUXT register. Values from 1 to 14 of the AUXT register correspond to an ON-time of the AUX LED ranging from 100 to 1400 ms in 100 ms steps. The value 15 puts the AUX LED to the continuous light mode. The activation/deactivation of the AUX LED current source is controlled using only the AUXI register.

Table 13. Auxiliary led dimming table (1)

AUXI (hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
AUX LED current [mA]	0.0	1.3	2.6	4.0	5.3	6.6	8.0	9.3	10.6	12.0	13.3	14.6	16.0	17.3	18.6	20.0

1. 20 mA output current is achievable only if the supply voltage is higher than 3.3 V.

Table 14. Torch Mode and Flash Mode dimming registers settings

T_DIM (hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F								
F_DIM (hex)									0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
LED current [mA]	16	19	23	27	32	39	46	55	65	77	92	109	124	147	175	209	248	296	352	418	498	592	705	840
Internal step	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
V_{REF1} [mV]	33	40	47	56	67	80	95	113	134	160	190	227	33	40	47	56	67	79	95	113	134	160	190	227
Sense Resist.	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL} + R_{TR}	R_{FL}	R_{FL}	R_{FL}	R_{FL}	R_{FL}	R_{FL}	R_{FL}	R_{FL}	R_{FL}	R_{FL}	R_{FL}	R_{FL}

Note: LED current values refer to R_{FL}=0.27 Ω, R_{TR}=1.8 Ω

Table 15. Status register

STAT_REG (read mode)	MSB							LSB
SUB ADD=03	N/A	F_RUN	LED_F	NTC_W	NTC_H	OT_F	N/A	VOUTOK_N
Power ON, SHUTDOWN MODE RESET Value	0	0	0	0	0	0	0	0

8.10 F_RUN

This bit is kept HIGH by the STCF03 during Flash mode. By checking this bit, the µP can verify if the Flash mode is running or has been terminated by the Time Counter.

8.11 LED_F

This bit is set by the STCF03 when the voltage seen on the LED pin is V_{REF2} >5.3 V during a Torch or Flash operation. This condition can be caused by an open LED, indicating a LED failure. The device automatically goes into Ready mode to avoid damage. Internal high frequency filtering avoids false detections. This bit is reset by the STCF03 following a read operation of the STAT_REG.

8.12 NTC_W

This bit is set HIGH by the STCF03 and the ATN pin is pulled down, when the voltage seen on the pin Rx exceeds V_{REF4} = 0.56 V. This threshold corresponds to a warning temperature value at the LED measured by the NTC. The device is still operating, but a warning is sent to the µP. This bit is reset by the STCF03 following a read operation of the STAT_REG.

8.13 NTC_H

This bit is set HIGH by the STCF03 and the ATN pin is pulled down, when the voltage seen on the pin Rx exceeds V_{REF5}. This threshold (1.2V) corresponds to an excess temperature value at the LED measured by the NTC. The device is put in Ready mode to avoid damaging the LED. This bit is reset by the STCF03 following a read operation of the STAT_REG.

8.14 OT_F

This bit is set HIGH by the STCF03 and the ATN pin is pulled down, when the chip over-temperature protection (~140°C) has put the device in Ready mode. This bit is reset by the STCF03 following a read operation of the STAT_REG.

8.15 VOUTOK_N

This bit is set by the STCF03. It is used to protect the device, if the output is shorted. The VOUTOK_N bit is set to HIGH at the start-up. Then a current generator of 20mA charges the output capacitor for 360 µs typ. and it detects when the output capacitor reaches 100 mV. If this threshold is reached the bit is set to LOW. If the output is shorted to ground or the LED is shorted this threshold is never reached: the bit stays HIGH, ATN pin is pulled down and the device will not start. This bit is reset following a read operation of the STAT_REG.

Figure 13. VOUTOK_N behavior

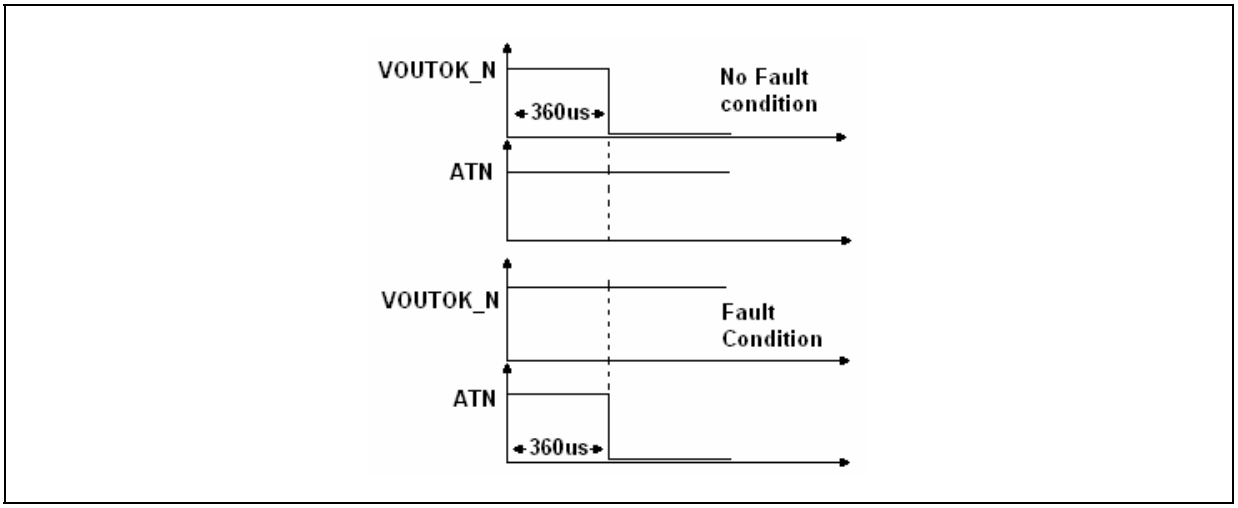


Table 16. Status register details

Bit Name	F_RUN (STAT_REG)	LED_F (STAT_REG)	NTC_W (STAT_REG)	NTC_H (STAT_REG)	OT_F (STAT_REG)	VOUTOK_N (STAT_REG)
Default value	0	0	0	0	0	0
Latched (1)	NO	YES	YES	YES	YES	YES
Forces Ready mode when set	NO	YES	NO	YES	YES	YES
Sets ATN LOW when set	NO	YES	YES	YES	YES	YES

1. YES means that the bit is set by internal signals and is reset to default by an I^2C read operation of STAT_REG NO means that the bit is set and reset by internal signals in real-time.

9 Detailed description

9.1 PowerON reset

This mode is initiated by applying a supply voltage above the $V_{PW\_ON\ RESET}$ threshold value. An internal timing (~1 µs) defines the duration of this status. The logic blocks are powered, but the device doesn't respond to any input. The registers are reset to their default values, the ATN and SDA pins are in high-Z, and the I^2C slave address is internally set by reading the ADD pin configuration. After the internally defined time has elapsed, the STCF03 automatically enters the Stand-by mode.

9.2 Shutdown, shutdown with NTC

In this mode only the I^2C interface is alive, accepting I^2C commands and register settings. The device enters this mode: automatically from Power ON Reset status; by resetting the PWR_ON bit from other operation modes. Power consumption is at the minimum (1 µA max) if NTC is not activated (NTC_ON=0). If PWR_ON and NTC_ON is set, the T1 is switched ON (see the block diagram), allowing the µP to measure the LED temperature through its A/D converter. When NTC circuits are active and the $V_{REF-EXT}$ is present, the typ. current consumption is increased to 1 µA, then it is recommended not to leave the STCF03 in this status if battery drain has to be minimized.

9.3 Ready mode

In this mode all internal blocks are turned ON, but the DC/DC converter is disabled and the White LED is disconnected. The NTC circuit can be activated to monitor the temperature of the LED and I^2C commands and register settings are allowed to be executed immediately. Only in this mode the Auxiliary LED is operational and can be turned ON and set at the desired brightness using the AUX REGISTER. The device enters this mode: from Stand-by by setting the PWR_ON bit; from Flash operation by resetting the TRIG pin or the TRIG_EN bit or automatically from Flash operation when the Time Counter reaches zero; from Torch operation by resetting the TCH_ON bit. The device automatically enters this mode also when an overload or an abnormal condition has been detected during Flash or Torch operation (*Table 16: Status register details*:).

9.4 Single or multiple Flash using external (µP) temporization

To avoid the I^2C bus time latency, it is recommended to use the dedicated TRIG pin to define the Flash duration (hard-triggering). The TRIG_EN bit of CMD_REG should be set before starting each flash operation, because it could have been reset automatically in the previous flash operation. Flash duration is determined by the pulse length that drives the TRIG pin. As soon as the Flash is activated, the system needs typically 1.2 ms to ramp up the output current on the Power LED. The internal Time Counter will Time-out flash operation and keep the LED dissipated energy within safe limits in case of Software deadlock; FTIM register has to be set first, either in Stand-by or in Ready Mode. Multiple flashes are possible by strobing the TRIG pin. Time out counter will cumulate every flash on-time until the defined time out is reached unless it is reloaded by updating the CMD_REG. If single or multiple Flash operation is timed-out, the device automatically goes in Ready mode by resetting the

TRIG_EN bit, and also resets the F_RUN bit. The ATN pin is pulled down to inform the µP that the STAT_REG has been updated.

9.5 External (µP) temporization using TRIG_EN bit

Even if it is possible, it is not recommended to use the TRIG_EN bit to start and stop the Flash operation, because of I^2C bus latencies: this would result in inaccurate Flash timing. Nevertheless, if this operation mode is chosen, the TRIG pin has to be kept High (logic level or wired to V_{BAT}), leaving the whole flash control to the I^2C bus. Also in this operation mode the Time Counter will Time-out Flash operation and keep the LED dissipated energy dissipated by the LED within safe limits in case of SW deadlock.

9.6 Single Flash using internal temporization

Flash triggering can be obtained either by TRIG pin (hard-triggering) or by I^2C commands (soft-triggering). The first solution is recommended for an accurate start time, while the second is less accurate because of the I^2C bus time latency. Stop time is defined by the STCF03 internal temporization and its accuracy is determined by the internal oscillator. For hard-triggering it is necessary to set the TRIG_EN bit in advance. For soft-triggering the TRIG pin has to be kept High (logic level or wired to V_{BAT}) and the Flash can be started by setting the FTIM and the TRIG_EN through I^2C (both are located in the CMD REG). There is a delay time between the moment the Flash is triggered and when it appears. This delay is caused by the time necessary to charge up the output capacitor, which is around 1.2 ms depending on battery voltage and output current value. Once triggered, the flash operation will be stopped when the Time Counter reaches zero. As soon as the Flash is finished, the F_RUN bit is reset, the ATN pin is pulled down for 11 µs to inform the µP that the STAT_REG has been updated and the device goes back to Ready mode. If it is necessary to make a Flash longer than the internal timer allows or a continuous Flash, then the FTIM must be reloaded through I^2C bus every time, before the internal timer reaches zero. For example: To get a continuous FLASH, set FTIM to 1.5 s and every 1 s reload the CMD_REG.

9.7 Multiple Flash using internal temporization

This operation has to be processed as a sequence of single flashes using internal temporization starting from hard or soft triggering. Since the TRIG_EN bit is reset at the end of each flash, it is necessary to reload the CMD_REG to start the next one.

10 Typical performance characteristics

Figure 14. Efficiency

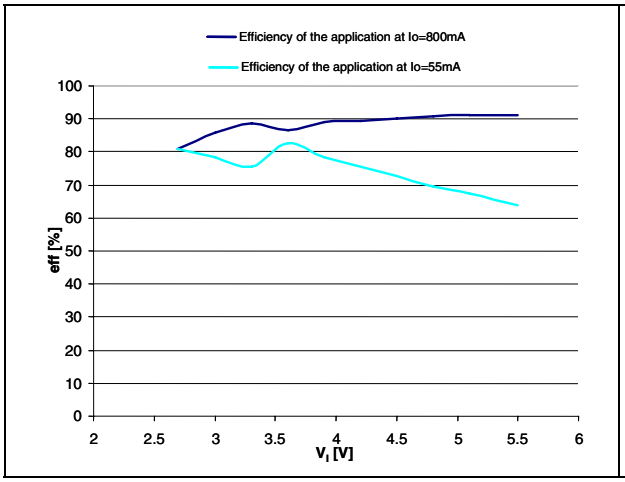


Figure 15. I_{OTORCH} vs T_DIMM

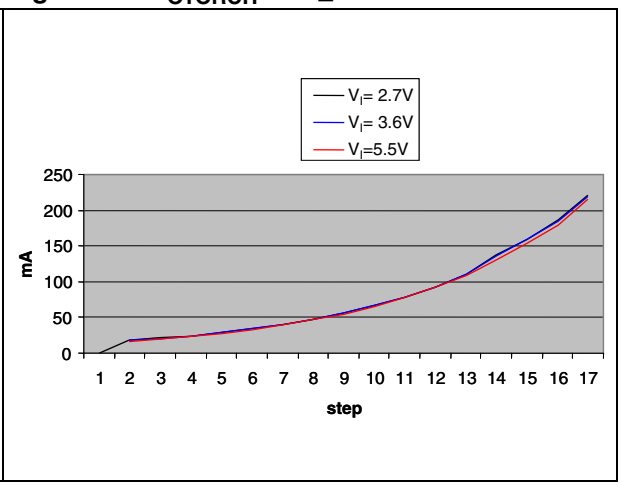


Figure 16. I_{OFLASH} vs F_DIMM

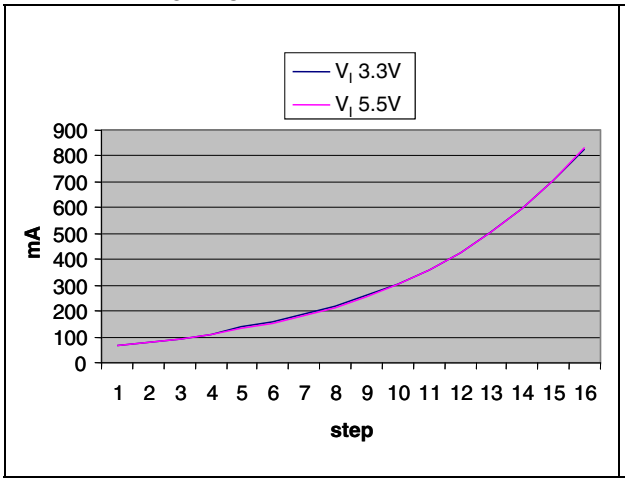


Figure 17. I_{OAUX} vs AUXI

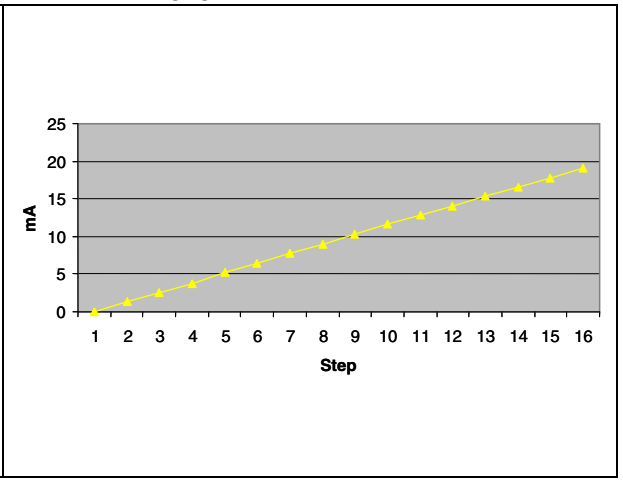


Figure 18. I_{OFLASH} vs Temp. V_I = 3.3V

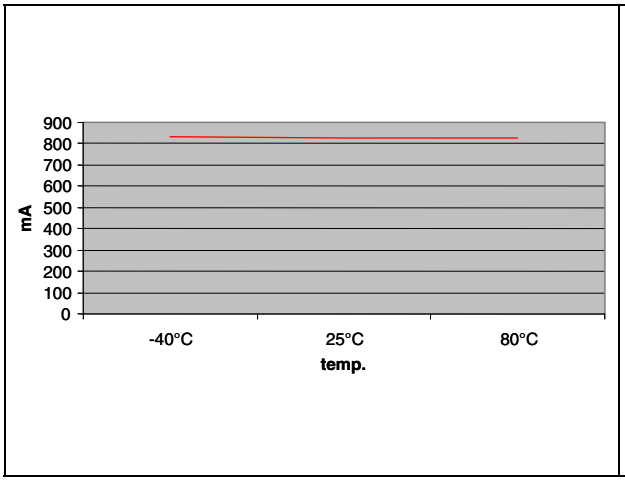


Figure 19. VFB2 vs Temp. at I_O = 800mA, V_I = 3.3V

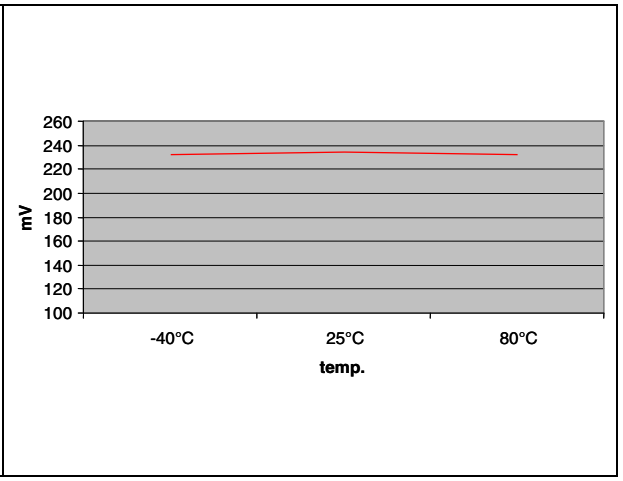


Figure 20. I_Q vs Temp. V_I = 5.5V Ready-Mode

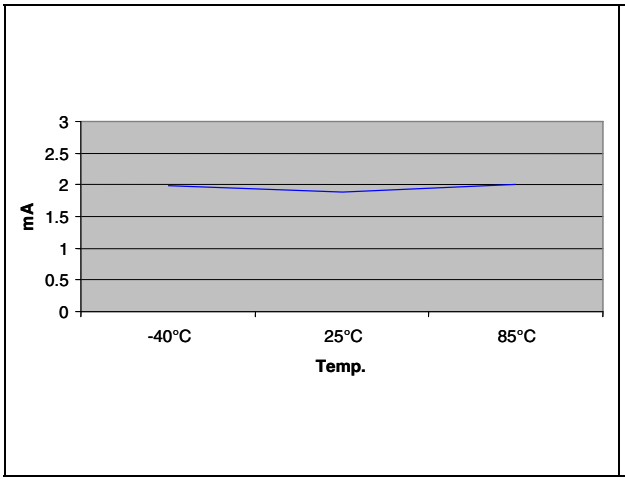


Figure 21. Start-Up in Flash Mode 800mA at V_I = 3.6V

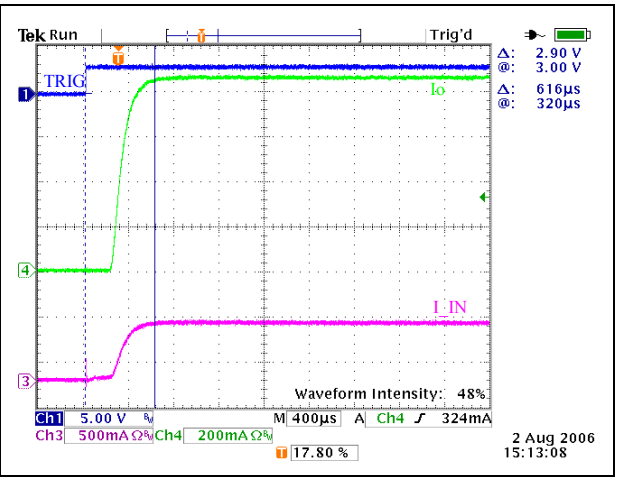
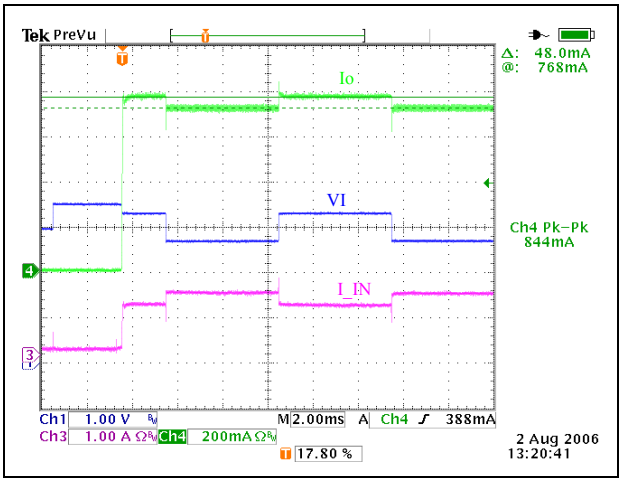


Figure 22. Line transient in Flash Mode 800mA, change of V_I from 2.7V to 3.3V in 10µs

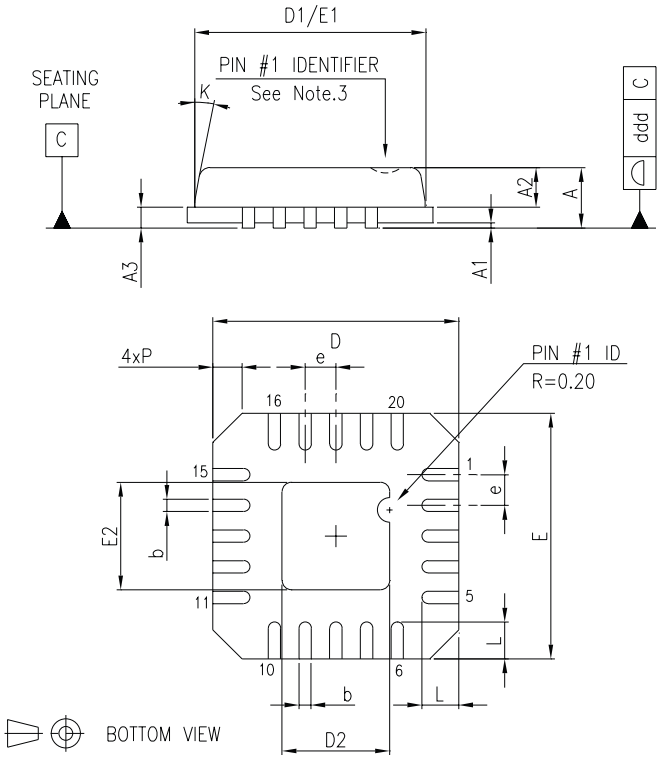


11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

QFN20 (4mm x 4mm) mechanical data

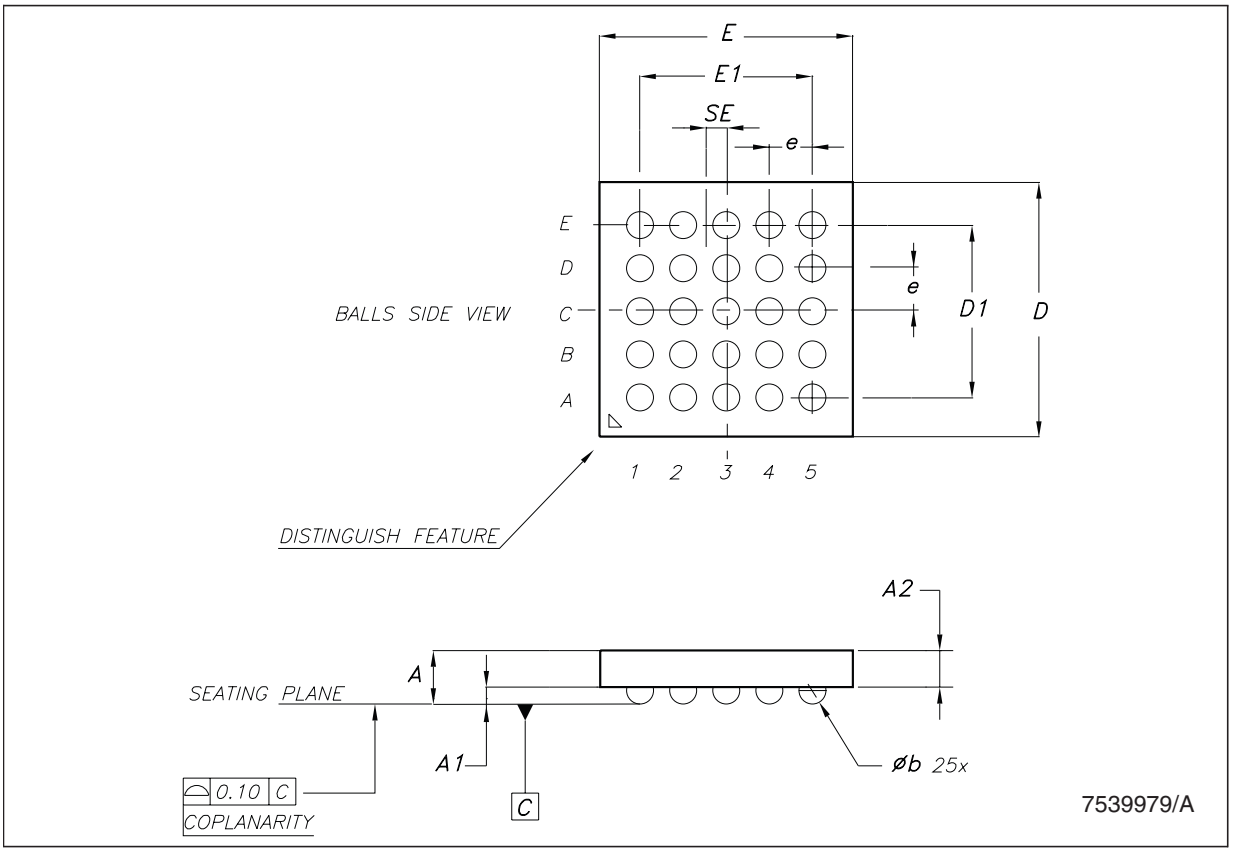
Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.65	1.00		25.6	39.4
A3		0.20			7.9	
b	0.18	0.25	0.30	7.1	9.8	11.8
D	3.85	4.00	4.15	151.6	157.5	163.4
D1		3.75			147.6	
D2 (A)	1.55	1.70	1.85	61.0	66.9	72.8
D2 (B)	1.95	2.10	2.25	76.8	82.7	88.6
D2 (C)	2.15	2.30	2.45	84.6	90.6	96.5
E	3.85	4.00	4.15	151.6	157.5	163.4
E1		3.75			147.6	
E2 (A)	1.55	1.70	1.85	61.0	66.9	72.8
E2 (B)	1.95	2.10	2.25	76.8	82.7	88.6
E2 (C)	2.15	2.30	2.45	84.6	90.6	96.5
e		0.50			19.7	
L	0.35	0.55	0.75	13.8	21.7	29.5
P			0.60			23.6
K			14			551.2
ddd			0.08			3.1



7366925A

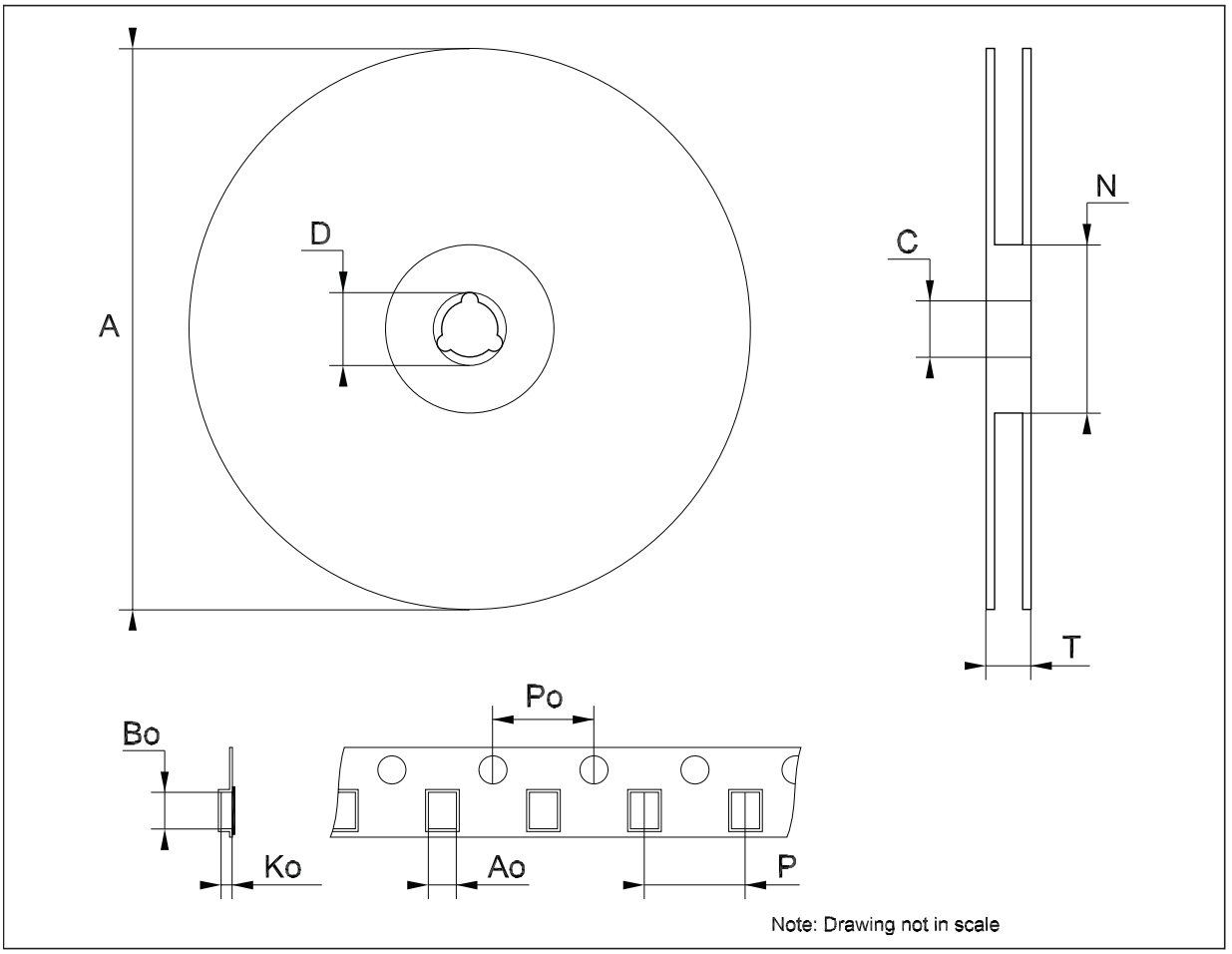
TFBGA25 mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.0	1.1	1.16	39.4	43.3	45.7
A1			0.25			9.8
A2	0.78		0.86	30.7		33.9
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.9	3.0	3.1	114.2	118.1	122.0
D1		2			78.8	
E	2.9	3.0	3.1	114.2	118.1	122.0
E1		2			78.8	
e		0.5			19.7	
SE		0.25			9.8	



Tape & reel QFNxx/DFNxx (4x4) mechanical data

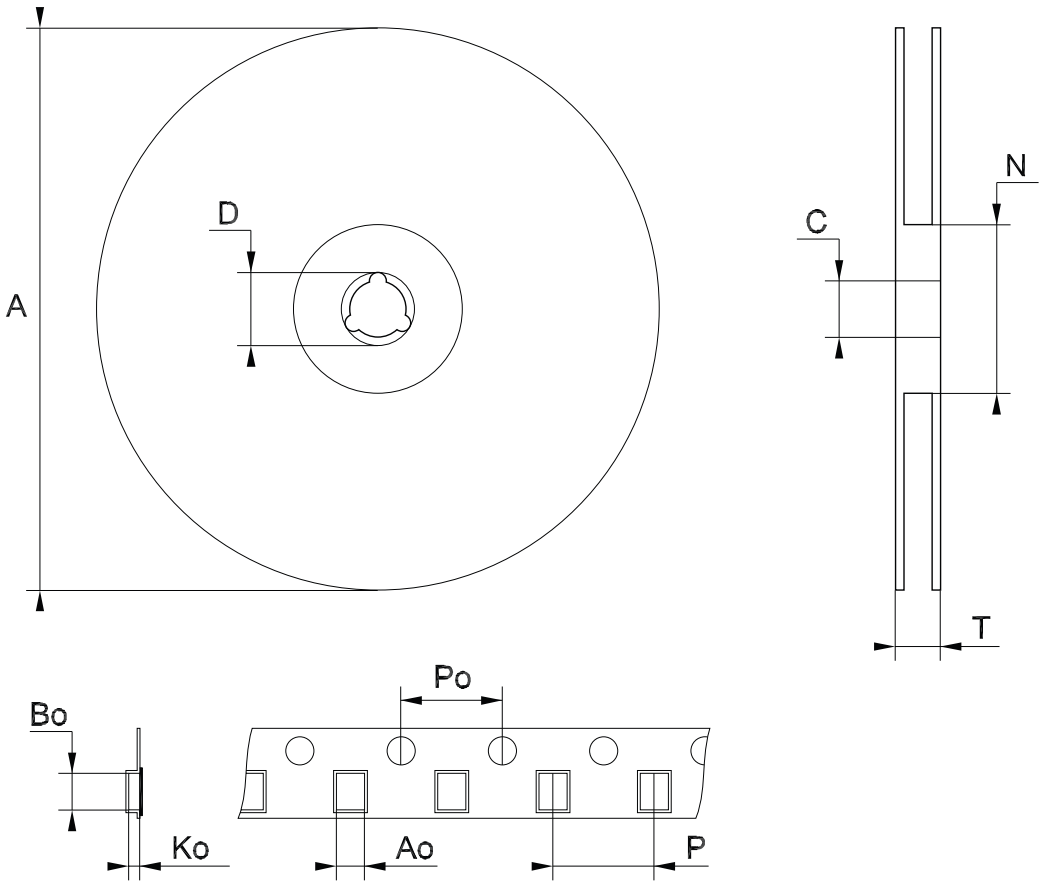
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Tape & reel TFBGA25 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.60			0.063	
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

12 Revision history

Table 17. Document revision history

Date	Revision	Changes
30-Jan-2007	1	First Release.
27-Mar-2007	2	The OVP min. value on table 5 is changed: 5.5 V ==> 5.3 V.
28-Aug-2007	3	*Table 5.* updated.
12-Sep-2007	4	*Figure 2.* title changed.

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