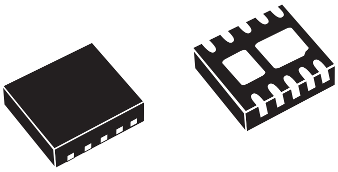
STBP120

Overvoltage protection device with thermal shutdown

Features

- Input overvoltage protection up to 28 V
- Integrated high voltage N-channel MOSFET switch
- Low $R_{DS(on)}$ of 90 mΩ
- Integrated charge pump
- Thermal shutdown protection
- Softstart feature to control the inrush current
- Enable input ($\overline{EN}$)
- Fault indication output ($\overline{FLT}$)
- IN input ESD withstand voltage up to ±15 kV (air discharge), up to ±8 kV (contact discharge) in typical application circuit with 1 µF input capacitor (±2 kV HBM for standalone device)
- Certain overvoltage options compliant with the China Communications Standard YD/T 1591-2006 (overvoltage protection only)
- Small, RoHS compliant 2.5 x 2 mm TDFN – 10-lead package.



TDFN – 10-lead (2.5 x 2 mm)

Applications

- Smart phones
- Digital cameras
- PDA and palmtop devices
- MP3 players
- Low-power handheld devices.

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1 Description

The STBP120 device provides overvoltage protection for input voltage up to +28 V. Its low $R_{DS(on)}$ N-channel MOSFET switch protects the systems connected to the OUT pin against failures of the DC power supplies in accordance with the China MII Communications Standard YD/T 1591-2006.

In the event of an input overvoltage condition, the device immediately disconnects the DC power supply by turning off an internal low $R_{DS(on)}$ N-channel MOSFET to prevent damage to protected systems.

In addition, the device also monitors its own junction temperature and switches off the internal MOSFET if the junction temperature exceeds the specified limit.

The device can be controlled by the microcontroller and can also provide status information about fault conditions.

The STBP120 is offered in a small, RoHS-compliant TDFN – 10-lead (2.5 mm x 2 mm) package.

Figure 1. Logic diagram

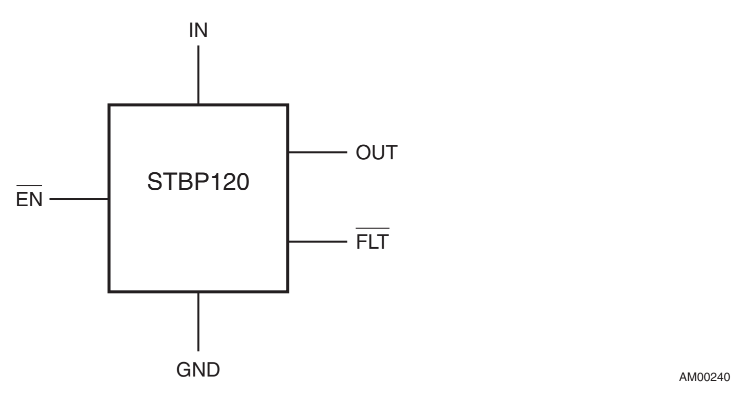
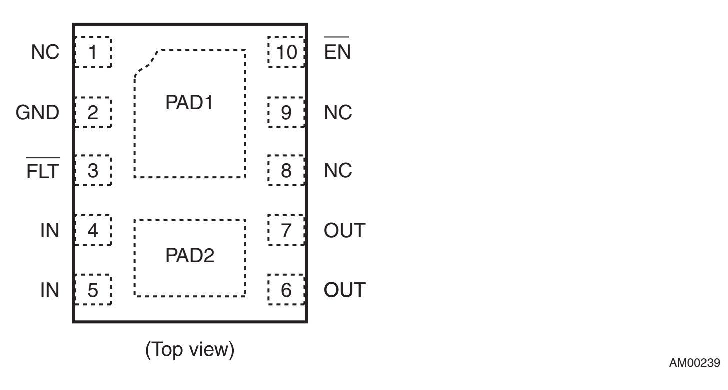


Figure 2. Pinout(1)



1. Pin 1, PAD1 and PAD2 are No Connect (NC) and may be tied to IN or GND.

2 Pin descriptions

2.1 Input (IN)

Input voltage pin. This pin is connected to the DC power supply. External low ESR ceramic capacitor of minimum value 1 µF must be connected between IN and GND. This capacitor is for decoupling and also protects the IC against dangerous voltage spikes and ESD events. This capacitor should be located as close to the IN pins as possible.

All IN pins (4, 5) must be hardwired to common supply.

2.2 Power output (OUT)

Output voltage pin. This pin is connected to the input through a low $R_{DS(on)}$ N-channel MOSFET switch.

If no fault is detected and the STBP120 is not disabled (controlled by the $\overline{\text{EN}}$ input), this switch is turned on and the output voltage follows the input voltage.

The output is disconnected from the input when the input voltage is under the UVLO threshold or above the OVLO threshold, when the chip temperature is above the thermal shutdown threshold or when the chip is disabled by the $\overline{\text{EN}}$ input.

There is a 50 ms delay, t_{on}, between input voltage or junction temperature returns to specified range and the power output is connected to the input (see *Figure 6*).

All OUT pins (6, 7) must be hardwired to common supply.

2.3 Fault indication output ($\overline{\text{FLT}}$)

The fault indication output (active-low - open-drain) provides information on the STBP120 state to the application controller. When $\overline{\text{FLT}}$ is active (i.e. driven low), this indicates the STBP120 is in the undervoltage or overvoltage condition or thermal shutdown mode is active. When the input voltage and junction temperature is in specified range, the $\overline{\text{FLT}}$ output is in high impedance (Hi-Z) state.

There is an additional 50 ms delay, t_{start}, between the power output is connected to the input and the $\overline{\text{FLT}}$ output is deactivated (i.e. in Hi-Z state) (see *Figure 6*).

Since the $\overline{\text{FLT}}$ output is of open-drain type, it may be pulled up by an external resistor R_P to the controller supply voltage. If there is no need to use this output, it may be left disconnected. The suitable R_P resistor value is in range of 10 kΩ to 1 MΩ.

To improve safety and to prevent damage to application circuits in the event of extreme voltage or current conditions, an optional protective resistor R_{FLT} can be connected between the $\overline{\text{FLT}}$ output and the controller input. The suitable R_{FLT} resistor value is in range of 22 kΩ to 100 kΩ.

The function of the $\overline{\text{FLT}}$ output is not affected by the $\overline{\text{EN}}$ input state (see *Figure 9*).

2.4 Enable input ($\overline{EN}$)

This logical input (active-low) can be used to enable or disable the device. When $\overline{EN}$ input is driven high, the STBP120 enters the standby mode and the power output is disconnected from the input. When $\overline{EN}$ input is driven low and all operating conditions are within specified limits, the power output is connected to the input.

Since the $\overline{EN}$ input has no internal pull-down resistor, its logical level must be defined by the controller or by an external resistor. If there is no need to use this input, it should be connected to the GND.

To improve safety and to prevent damage to application circuits in the event of extreme voltage or current conditions, an optional protective resistor R_{EN} can be connected between the $\overline{EN}$ input and the controller output. The suitable resistor value is in range of 22 kΩ to 100 kΩ.

The $\overline{EN}$ input level has no impact on the functionality of $\overline{FLT}$ output (see *Figure 8* and *Figure 9*).

2.5 No Connect (NC)

Pins 1, 8, 9 and exposed pads PAD1, PAD2 are No Connect. Pin 1 and exposed pads PAD1, PAD2 may be tied to IN or GND if necessary.

2.6 Ground (GND)

Ground. All voltages are referenced to GND.

Table 1. Pin description and signal names

Pin	Name	Type	Function
1, PAD1, PAD2	NC	—	No Connect. May be tied to IN or GND.
2	GND	Supply	Ground
3	$\overline{FLT}$	Output	Fault indication output (open-drain)
4, 5	IN	Input / supply	Input voltage
6, 7	OUT	Output	Output voltage
8, 9	NC	—	No Connect
10	$\overline{EN}$	Input	Enable input (no internal pull-down resistor)

Figure 3. Block diagram

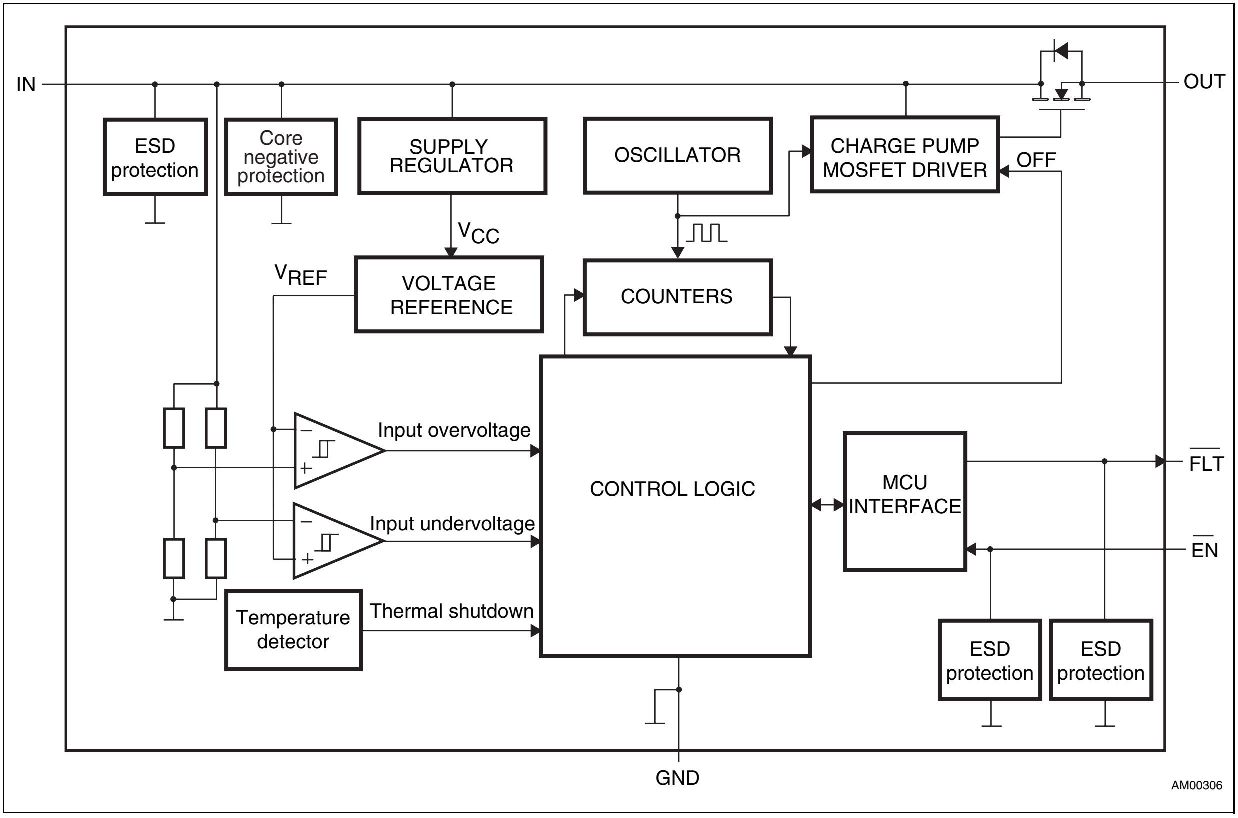
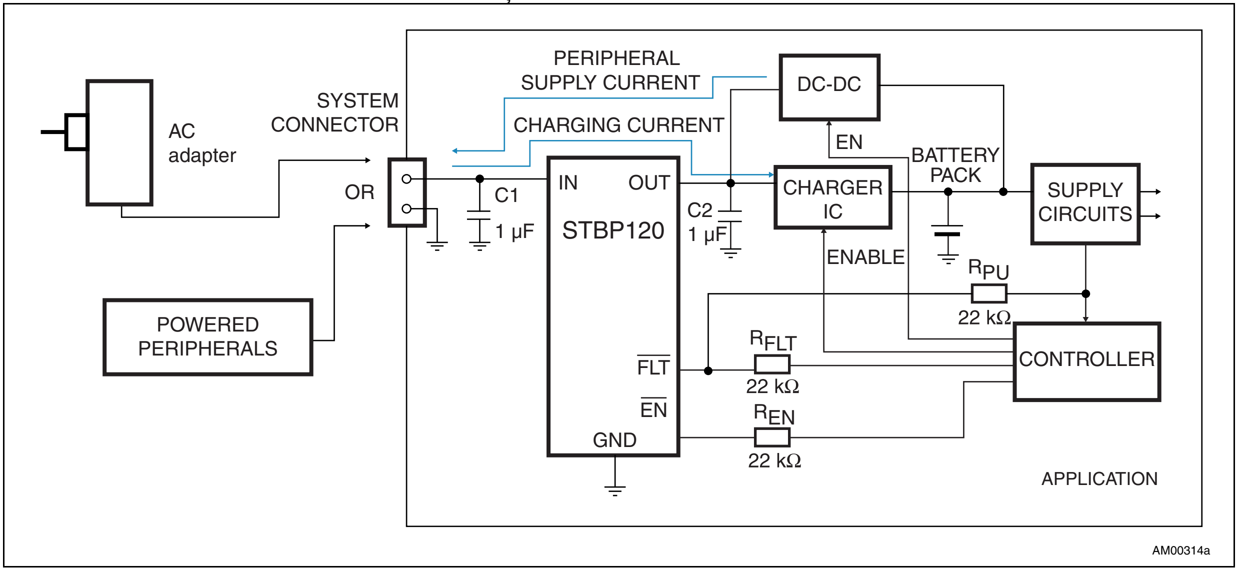


Figure 4. Typical application circuit(1), (2)



1. Optional resistors R_{EN}, R_{FLT} prevent damage to the controller under extreme voltage or current conditions and are not required. Low ESR ceramic capacitor C1 is necessary to ensure proper function of the STBP120. Capacitor C2 is not necessary for STBP120 but may be required by the charger IC.
2. The STBP120 MOSFET switch topology allows the current to also flow in the reverse direction, from OUT to IN, which can be useful for powering external peripherals from the system connector. The charger IC should not contain the reverse diode to prevent the battery pack voltage from appearing on the system connector. If the reverse current (supply current) is undesirable, it may be prevented by connecting a Schottky diode in series with the OUT pin. The voltage drop between IN and charger is increased by the voltage drop across the diode.

3 Operation

The STBP120 provides overvoltage protection for positive input voltage up to 28 V using a built-in low $R_{DS(on)}$ N-channel MOSFET switch.

3.1 Power-up

At power-up, with $\overline{\text{EN}}$ = low, the MOSFET switch is turned on after a 50 ms delay, t_{on}, after the input voltage exceeds the UVLO threshold to ensure the input voltage is stabilized. After an additional 50 ms delay, t_{start}, the $\overline{\text{FLT}}$ indication output is deactivated (see *Figure 6*).

The $\overline{\text{FLT}}$ output state is valid for V_{IN} input voltage 1.2 V or higher.

3.2 Normal operation

The device continuously monitors the input voltage and its own internal temperature so the output voltage is kept within the specified range. Internal MOSFET switch is turned on and the $\overline{\text{FLT}}$ output is not active.

The STBP120 enters normal operation state if the input voltage returns to the interval between V_{UVLO} and V_{OVLO} - $V_{HYS(OVLO)}$ and the junction temperature falls below T_{OFF} - $T_{HYS(OFF)}$. Internal MOSFET is turned on after the 50 ms delay t_{on} to ensure that the conditions have stabilized. Then, after an additional 50 ms delay, t_{start}, the $\overline{\text{FLT}}$ output is deactivated (i.e. driven high). This behavior is equivalent to the startup shown on *Figure 6*.

Note: *The STBP120 MOSFET switch topology allows the current to also flow in the reverse direction, i.e. from OUT to IN, which can be useful e.g. for powering external peripherals from the system connector (see the supply current in Figure 4). At first, the current flows through the MOSFET body diode. If the voltage that appears on the IN terminal is above the UVLO threshold, the MOSFET is (after the 50 ms startup delay) turned on so the voltage drop across STBP120 is significantly reduced. The charger IC should not contain the reverse diode to prevent the battery pack voltage from appearing on the system connector. If the reverse current is undesirable, it may be prevented by connecting a properly rated low drop Schottky diode in series with the OUT pin. The voltage drop between IN and charger is increased by the voltage drop across the diode.*
Due to the MOSFET body diode, thermal shutdown protection is not functional for the supply current.

3.3 Undervoltage lockout (UVLO)

To ensure proper operation under any conditions, the STBP120 has an undervoltage lockout (UVLO) threshold. For rising input voltage, the output remains disconnected from input until V_{IN} voltage exceeds the V_{UVLO} threshold (3.25 V typ). The $\overline{\text{FLT}}$ output is driven low as long as V_{IN} is below the UVLO threshold (assuming the input voltage is above 1.2 V). For falling input voltage, the UVLO circuit has a 50 mV hysteresis, $V_{HYS(UVLO)}$, to improve noise immunity under transient conditions.

3.4 Overvoltage lockout (OVLO)

If the input voltage V_{IN} rises above the threshold level V_{OVLO}, the MOSFET switch is immediately turned off (see *Figure 7*). At the same time, the fault indication output $\overline{FLT}$ is activated (i.e. driven low). This device is equipped with hysteresis, $V_{HYS(OVLO)}$, to improve noise immunity under transient conditions.

For available OVLO thresholds and hystereses, please see the *Table 5*.

3.5 Thermal shutdown

If the STBP120 internal junction temperature exceeds the T_{OFF} threshold, internal MOSFET switch is turned off and the fault indication output $\overline{FLT}$ is driven low.

To improve thermal stability, this circuit has a 20 °C hysteresis, $T_{HYS(OFF)}$.

4 Application information

4.1 Calculating the power dissipation

The maximum power dissipation of the STBP120 internal power MOSFET can be calculated using following formula:

$P_D = I^2 \times R_{DS(on)(max)}$,

Where I is current flowing through the MOSFET and $R_{DS(on)(max)}$ is maximum value of MOSFET resistance.

Example:

$R_{load} = 5\ \Omega$, $V_{IN} = 5$ V, $R_{DS(on)(max)} = 150$ mΩ

$I = V_{IN} / (R_{DS(on)(max)} + R_{load}) = 5 / (5 + 0.150) = 0.97$ A

$P_D = 0.97^2 \times 0.15 = 0.14$ W

The power dissipation of reverse diode (in powering peripherals mode) can be estimated as $P_D = (V_{OUT} - V_{IN}) \times I \approx 0.7 \times I$.

4.2 Calculating the junction temperature

The maximum junction temperature for given power dissipation, ambient temperature and thermal resistance junction - to - ambient can be calculated as

$T_J = T_A + 1.15 \times P_D \times R_{thJA} = T_A + 1.15 \times I^2 \times R_{DS(on)(max)} \times R_{thJA}$,

where T_J is junction temperature, T_A is given ambient temperature, 1.15 is a derating factor and R_{thJA} is thermal resistance junction - to - ambient, depending on shape, dimension and design of PCB. Two examples of PCB with appropriate thermal resistance are listed in *Table 3*. The junction temperature may not exceed 125 °C (see *Table 4*), due to T_{OFF} (thermal shutdown threshold temperature).

Maximum allowed MOSFET current for ambient temperature $T_A = 85$ °C and various R_{thJA} values are listed in *Figure 5*.

Example: For conditions listed in previous example, well designed PCB ($R_{thJA} = 82$ °C/W) and $T_A = 85$ °C, the maximum junction temperature is

$85 + 1.15 \times 0.14 \times 82 = 98.2$ °C.

4.3 PCB layout recommendations

- This device is intended as a protection device to the application from overvoltage. It must be ensured that the clearances between PCB tracks satisfy the high voltage design rules.
- Input capacitor, C1, should be located as close as possible to the STBP120 device. It should be a Low-ESR ceramic capacitor. Also the protective resistors R_{FLT}, R_{EN} (if used) should be located close to the STBP120.
- For good thermal performance, it is recommended to connect the STBP120 exposed thermal pads with the PCB ground plane. In most designs, this requires thermal vias between the copper pads on PCB and the ground plane.

5 Maximum rating

Stressing the device above the rating listed in the "absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{IN} off)	–55 to 150	C
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	C
T_J(2)	Operating junction temperature range	–40 to 150	C
T_A	Operating ambient temperature range	–40 to 85	C
V_{IN}	Input voltage (pins IN)	–0.3 to 30	V
$V_{IO(OUT)}$	Input / output voltage (pins OUT)	–0.3 to 12	V
V_{IO}	Input / output voltage (other pins)	–0.3 to 7	V
I_{IN}, $I_{OUT(MOSFET)}$	Input / output current through MOSFET (pins IN, OUT)	2000	mA
$I_{(\overline{FLT})}$	Output current (pin $\overline{FLT}$)	15	mA
V_{ESD}	ESD withstand voltage (IEC 61000-4-2, pins IN only)(3)	±15 (air), ±8 (contact)	kV
	Human body model (HBM), Model = 2(4)	2000	V
	Machine model (MM), Model = B(5)	200	V

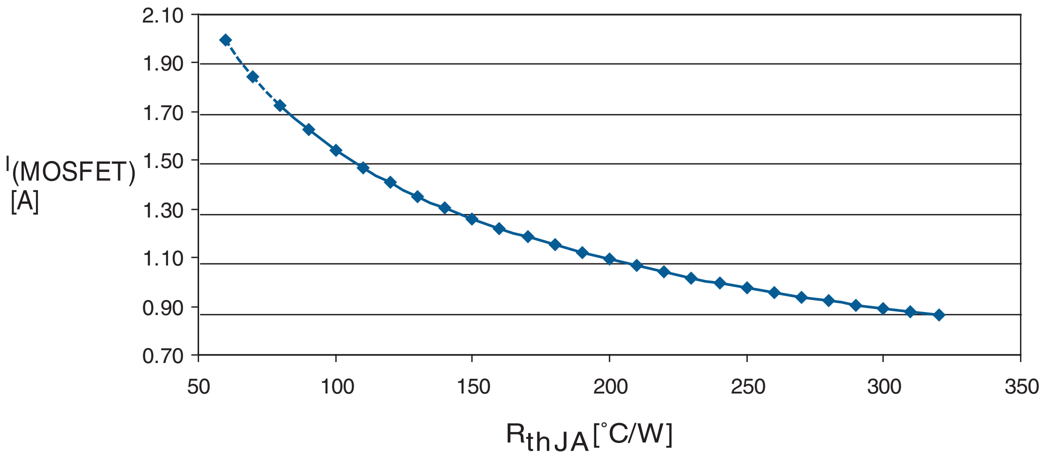
1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. Maximum junction temperature is internally limited by the thermal shutdown circuit (not valid for reverse current, see *Chapter 3.2*).
3. System-level value (see *Figure 4*, C1 ≥ 1 µF low ESR ceramic capacitor).
4. Human body model, 100 pF discharged through a 1.5kΩ resistor according the JESD22/A114 specification.
5. Machine model, 200 pF discharged through all pins according the JESD22/A115 specification.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance (junction to ambient)	204(1) 82(2)	°C/W
R_{thJC}	Thermal resistance (junction to case)	43	°C/W

1. The package is mounted on a 2-layers (1S) JEDEC board as per JESD51-7 without thermal vias underneath the exposed pads.
2. The package is mounted on a 4-layers (2S2P) JEDEC board as per JESD51-7 with 2 thermal vias (one underneath each exposed pad) as per JESD-51-5. Thermal vias connected from exposed pad to 1'st buried copper plane of PCB.

Figure 5. Maximum MOSFET current at T_A = 85 °C for various PCB thermal performance and T_J = 125 °C



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6 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in *Table 4*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Value	Unit
Input voltage (V_{IN})	5	V
Ambient operating temperature (T_A)	–40 to 85	°C
Junction operating temperature (T_J)	–40 to 125	°C
Output load resistance (R_{load})	5	Ω

Table 5. DC and AC characteristics

Symbol	Description	Test condition[1]	Min	Typ	Max	Unit
V_{IN}	Input voltage range		1.2		28	V
V_{UVLO}	Input undervoltage lockout threshold		3.1	3.25	3.4	V
$V_{HYS(UVLO)}$	Undervoltage lockout hysteresis		20	50	100	mV
V_{OVLO}	Overvoltage lockout threshold	V_{IN} rises up OVLO threshold, OVLO option A	5.25	5.375	5.50	V
		V_{IN} rises up OVLO threshold, OVLO option B	5.30	5.50	5.70	
		V_{IN} rises up OVLO threshold, OVLO option C	5.71	5.85	6.00	
		V_{IN} rises up OVLO threshold, OVLO option D	5.70	6.02	6.40	
$V_{HYS(OVLO)}$	Input overvoltage hysteresis		30	60	90	mV
$R_{DS(on)}$	IN to OUT resistance	$\overline{EN} = 0$ V, $V_{IN} = 5$ V, R_{load} connected to OUT		90	150	mΩ
I_{CC}	Operating current	$\overline{EN} = 0$ V, no load on OUT, $V_{IN} = 5$ V		170	250	µA
$I_{CC(STDBY)}$	Standby current	$\overline{EN} = 5$ V, no load on OUT, $V_{IN} = 5$ V		96	150	µA
$I_{CC(UVLO)}$	UVLO operating current	$V_{IN} = 2.9$ V		70	100	µA
$V_{OL(\overline{FLT})}$	$\overline{FLT}$ output low level voltage	1.2 V < $V_{IN} < V_{UVLO}$, $I_{SINK(\overline{FLT})} = 50$ µA		20	400	mV
		$V_{IN} > V_{OVLO}$, $I_{SINK(\overline{FLT})} = 1$ mA			400	mV
$I_{L(\overline{FLT})}$	$\overline{FLT}$ output leakage current	$V_{(\overline{FLT})} = 5$ V		5		nA
$V_{IL(\overline{EN})}$	$\overline{EN}$ low level input voltage				0.4	V
$V_{IH(\overline{EN})}$	$\overline{EN}$ high level input voltage		1.2			V
$I_{L(\overline{EN})}$	$\overline{EN}$ input leakage current	$V_{(\overline{EN})} = 0$ V or 5 V		5		nA

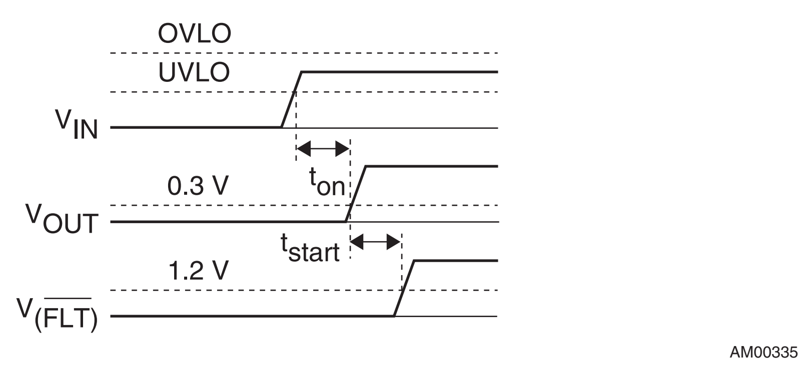
Table 5. DC and AC characteristics (continued)

Symbol	Description	Test condition[1]	Min	Typ	Max	Unit
Timing parameters						
t_{on}	Startup delay	Time measured from $V_{IN} > V_{UVLO}$ to V_{OUT} = 0.3 V (see *Figure 6*)	30	50	70	ms
t_{start}	$\overline{\text{FLT}}$ indication delay (OK)	Time measured from V_{OUT} = 0.3 V to $V_{(\overline{FLT})}$ = 1.2 V (see *Figure 6*)	30	50	70	ms
t_{off}[2]	Output turn-off time	Time measured from $V_{IN} > V_{OVLO}$ to $V_{OUT} \leq 0.3$ V. V_{IN} increasing from 5.0 V to 8.0 V at 3.0 V/µs, R_{load} connected to OUT. (see *Figure 7*)		1.5	5	µs
t_{stop}[2]	$\overline{\text{FLT}}$ indication delay (FAULT)	Time measured from $V_{IN} > V_{OVLO}$ to $V_{(\overline{FLT})} \leq 0.4$ V. V_{IN} increasing from 5.0 V to 8.0 V at 3.0 V/µs, R_{load} connected to OUT. (see *Figure 7*)		1		µs
t_{dis}[2]	Disable time	Time measured from $V_{(\overline{EN})} \geq 1.2$ V to $V_{OUT} < 0.3$ V. R_{load} connected to OUT. (see *Figure 8*)		1	5	µs
Thermal shutdown						
T_{OFF}	Thermal shutdown threshold temperature		130	145		°C
$T_{HYS(OFF)}$	Thermal shutdown hysteresis			20		°C

1. Test conditions described in *Table 4* (except where noted).
2. Guaranteed by design. Not tested in production.

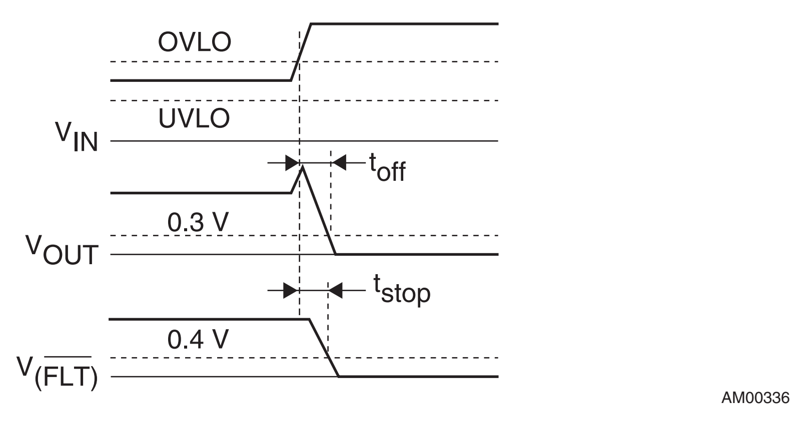
7 Timing diagrams

Figure 6. Startup(1)



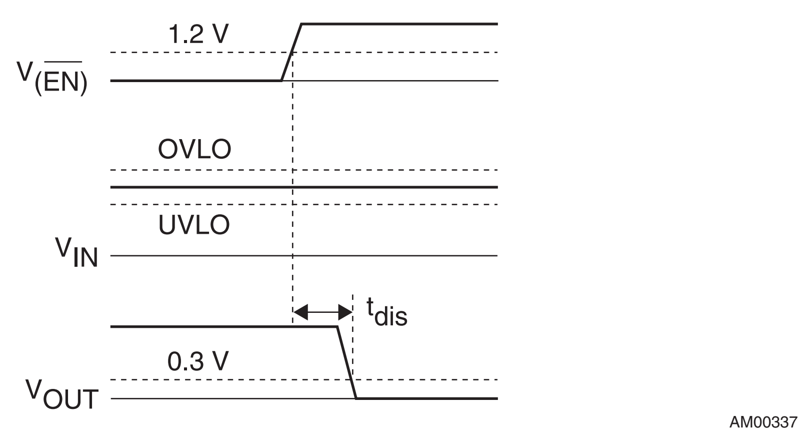
1. $\overline{EN}$ input is low.

Figure 7. Overvoltage protection(1)



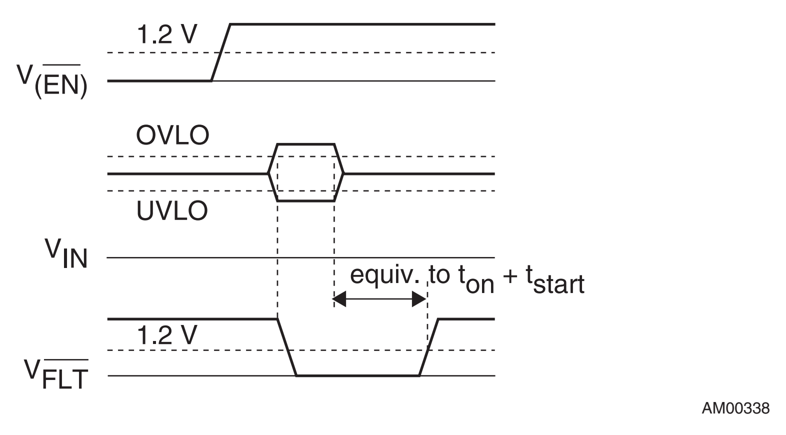
1. $\overline{EN}$ input is low.

Figure 8. Disable ($\overline{EN}$ = high)(1)



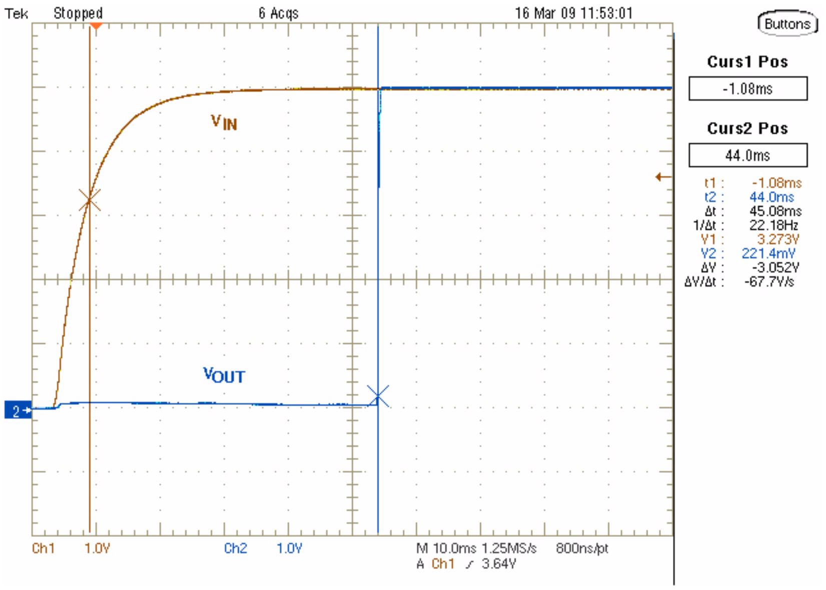
1. $\overline{FLT}$ output still indicates the V_{IN} status.

Figure 9. $\overline{FLT}$ behavior in disable ($\overline{EN}$ = high)



8 Typical application performance (STBP120DVDK6F)

Figure 10. Startup delay, t_{on}



1. The "leakage" on the V_{OUT} trace is a crosstalk caused mainly by the parasitic capacitances of the MOSFET switch.
2. No load on the output.

Figure 11. $\overline{FLT}$ indication delay (OK), t_{start}

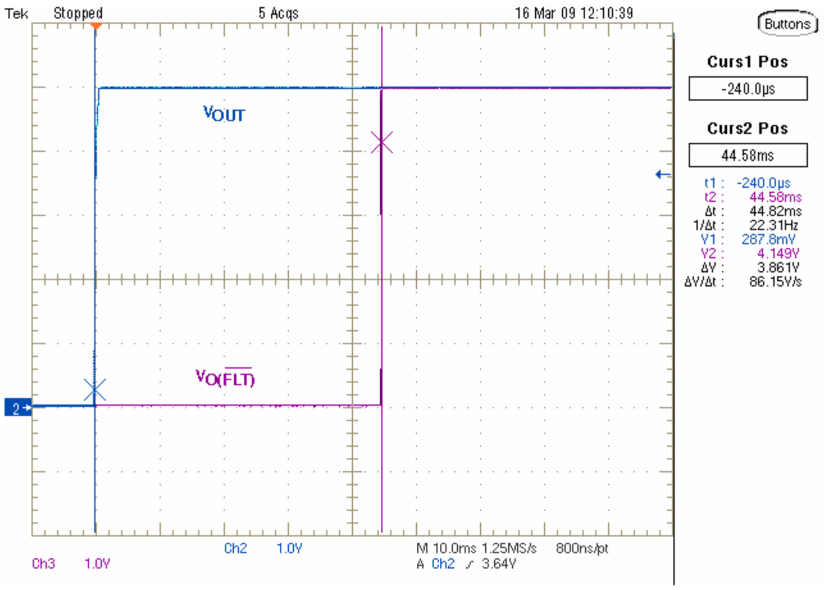
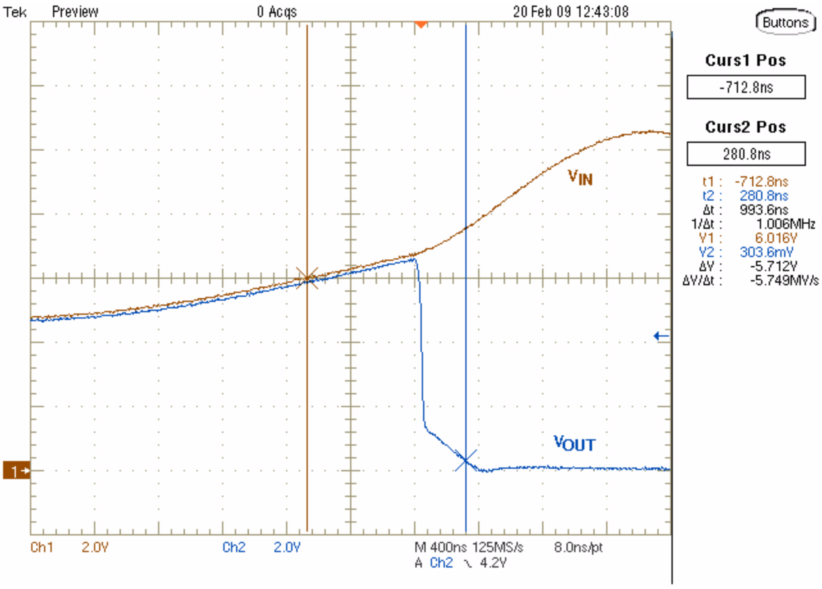
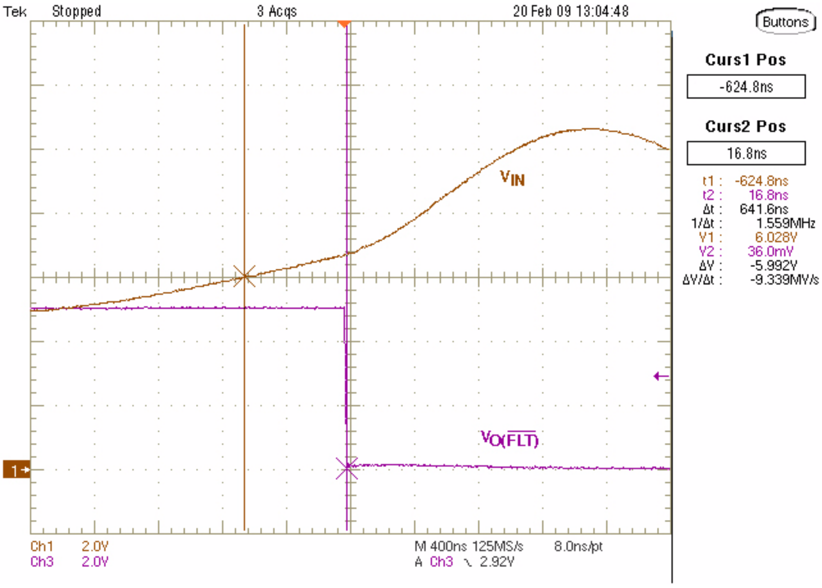


Figure 12. Output turn-off time, t_{off}



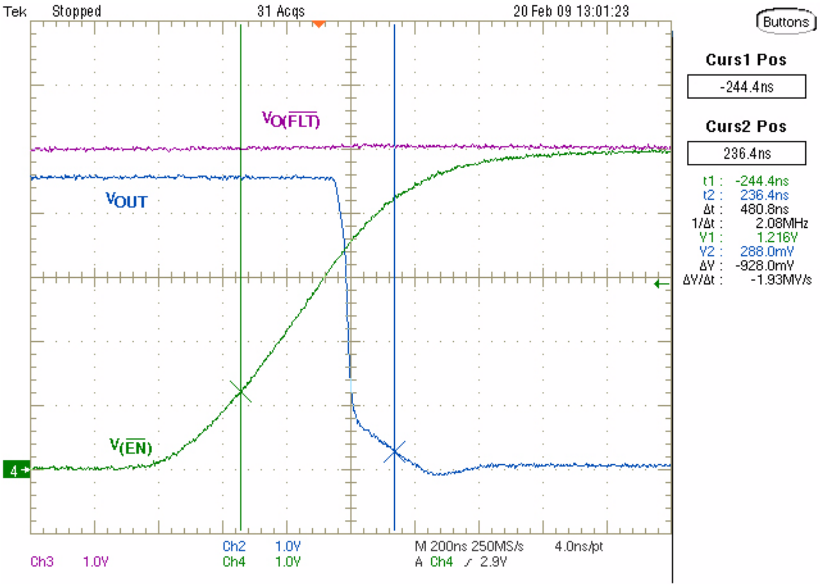
1. 5 Ω load on the output.

Figure 13. $\overline{\text{FLT}}$ indication delay (FAULT), t_{stop}



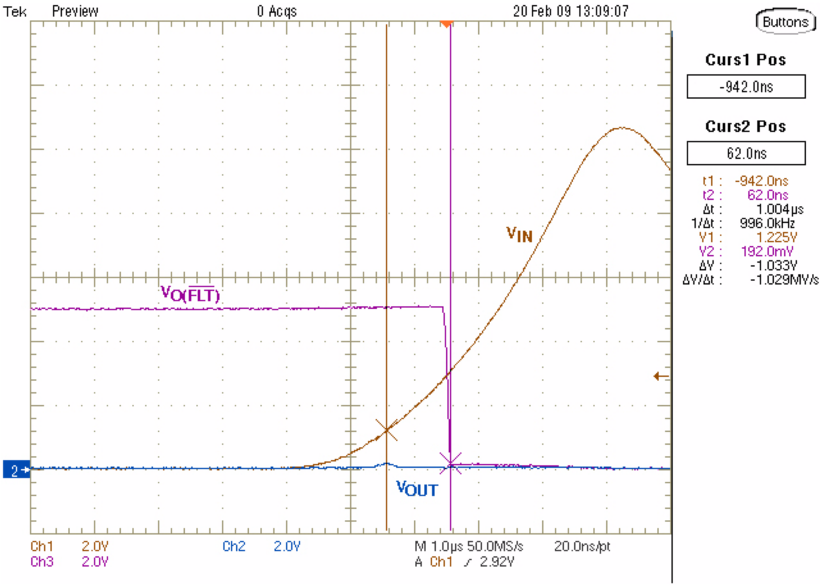
1. 5 Ω load on the output.

Figure 14. Disable time, t_{dis}



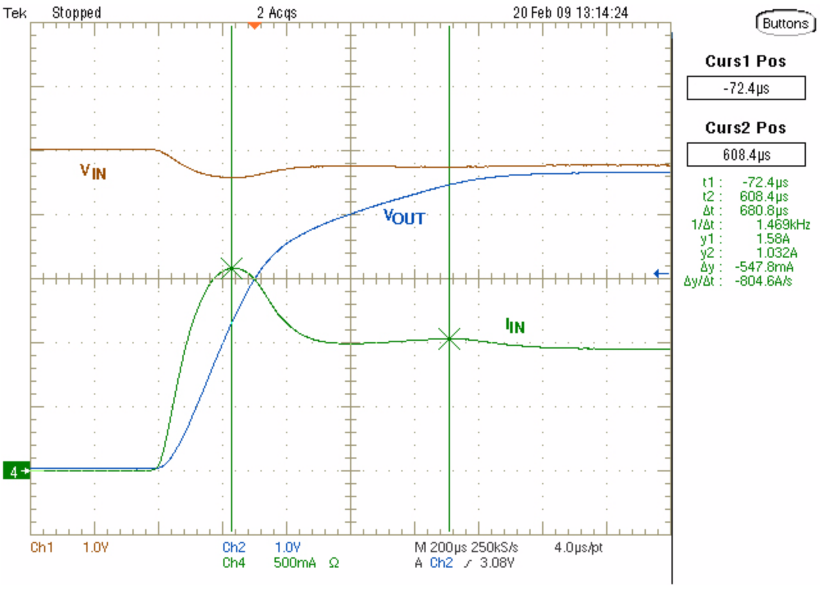
1. No change in $V_{O(\overline{FLT})}$ status during disable.
2. 5 Ω load on the output.

Figure 15. Startup to overvoltage and startup $V_{O(\overline{FLT})}$ delay



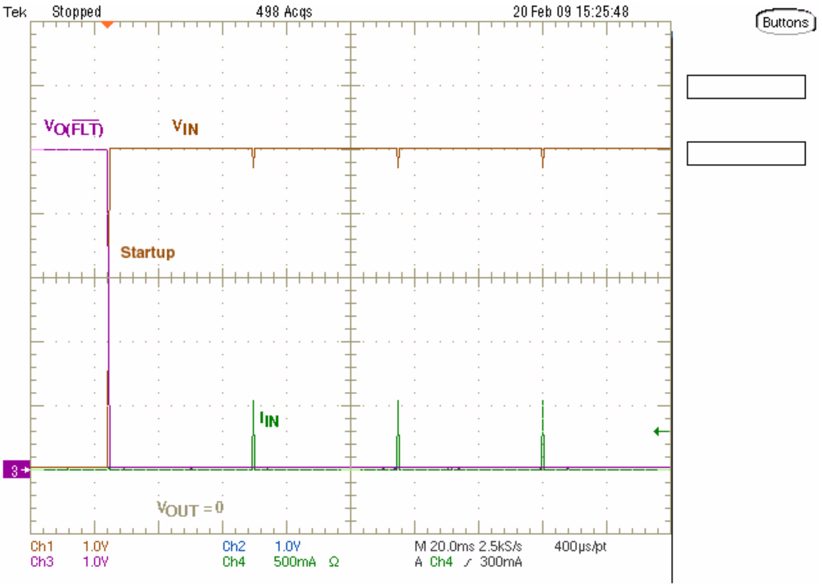
1. 5 Ω load on the output.

Figure 16. Startup inrush current



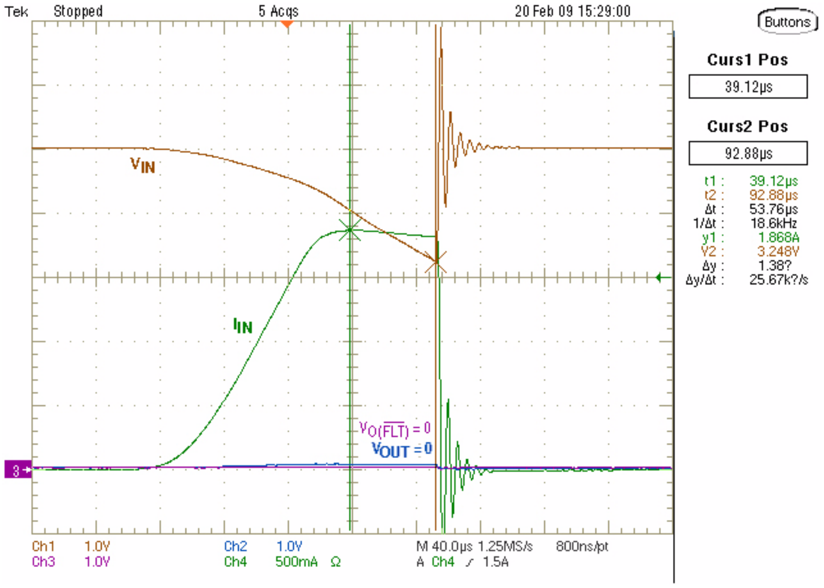
1. Output load 5 Ω in parallel with C = 100 µF, power supply cable inductance 1 µH, power supply cable resistance 0.3 Ω.

Figure 17. Output short-circuit



1. See also details on *Figure 18*.
2. Power supply cable inductance 1 µH, power supply cable resistance 0.3 Ω.

Figure 18. Output short-circuit detail



1. Due to power supply cable impedance, during the output short-circuit the input voltage falls below the V_{UVLO} threshold, resulting in turning off the power MOSFET and preventing any damage to the components.
2. Power supply cable inductance 1 µH, power supply cable resistance 0.3 Ω.

9 Typical thermal characteristics (STBP120DVDK6F)

Figure 19. I_{CC} vs. temperature

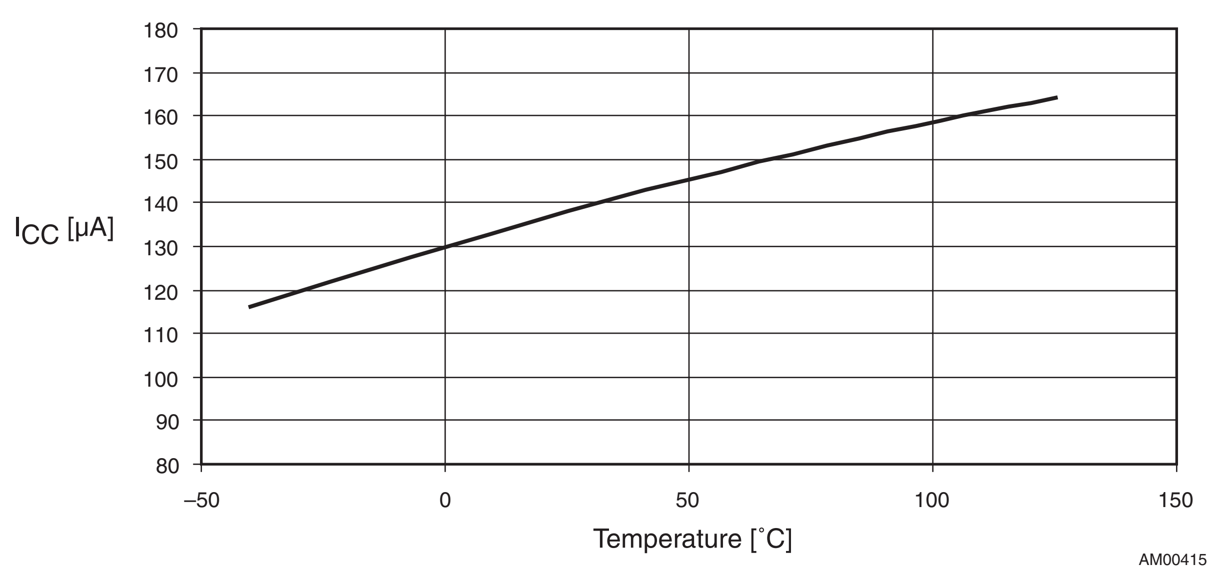


Figure 20. $I_{CC(STDBY)}$ vs. temperature

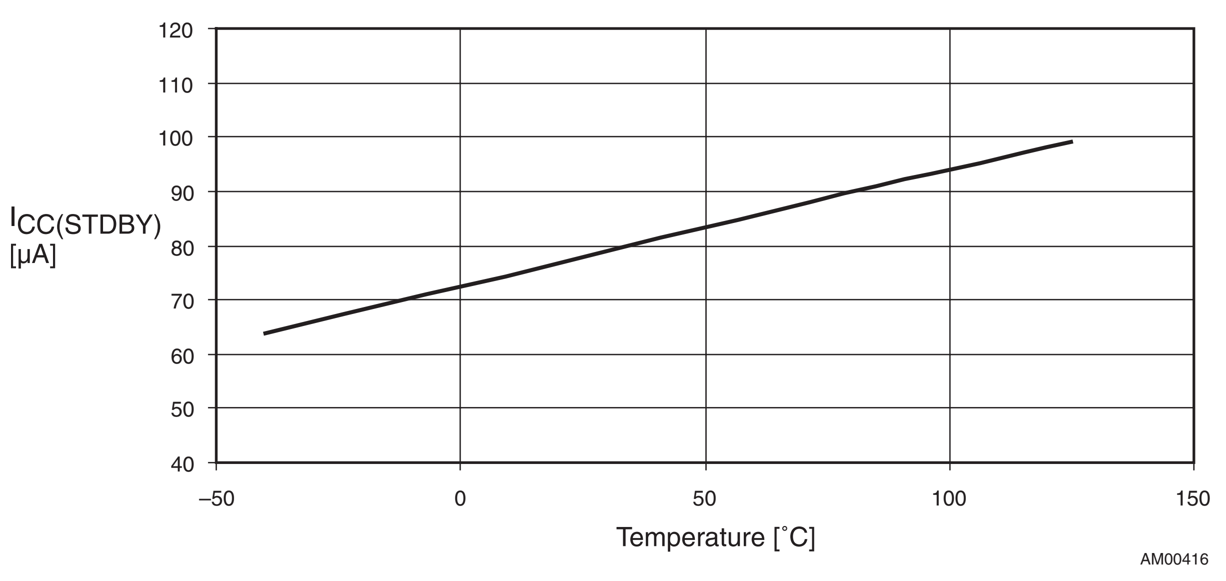


Figure 21. $I_{CC(UVLO)}$ at 2.9 V vs. temperature

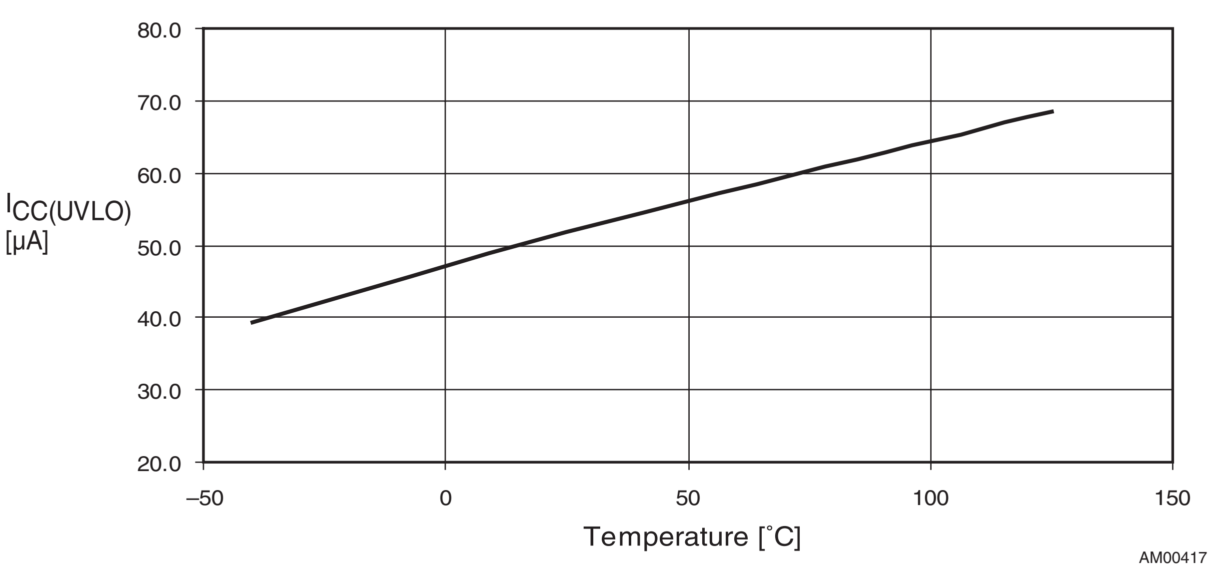


Figure 22. V_{OVLO} vs. temperature

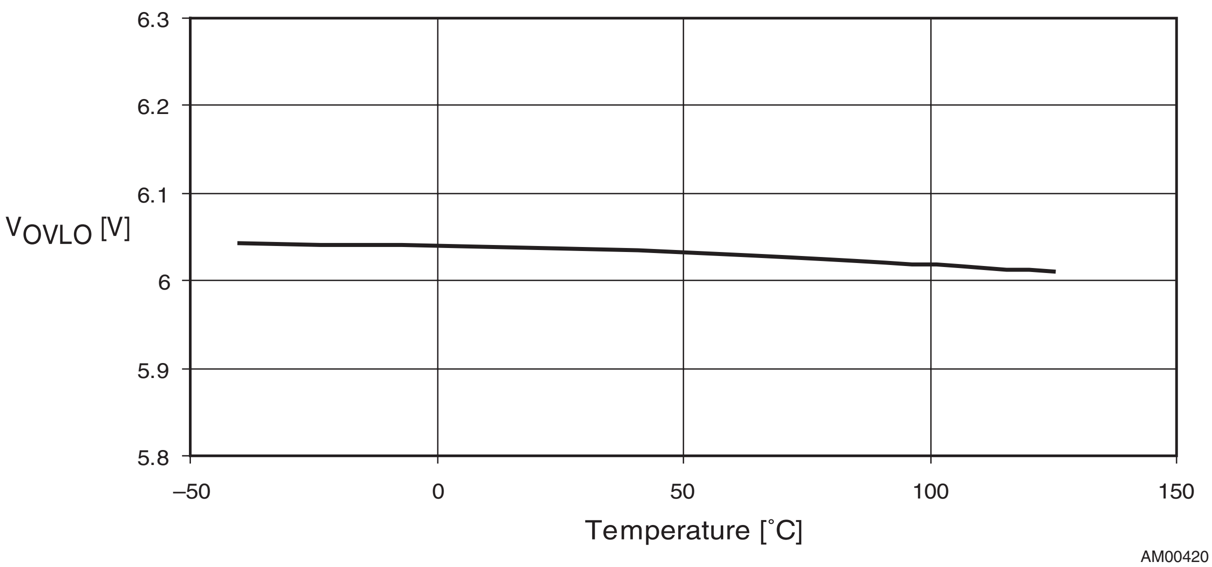


Figure 23. V_{UVLO} vs. temperature

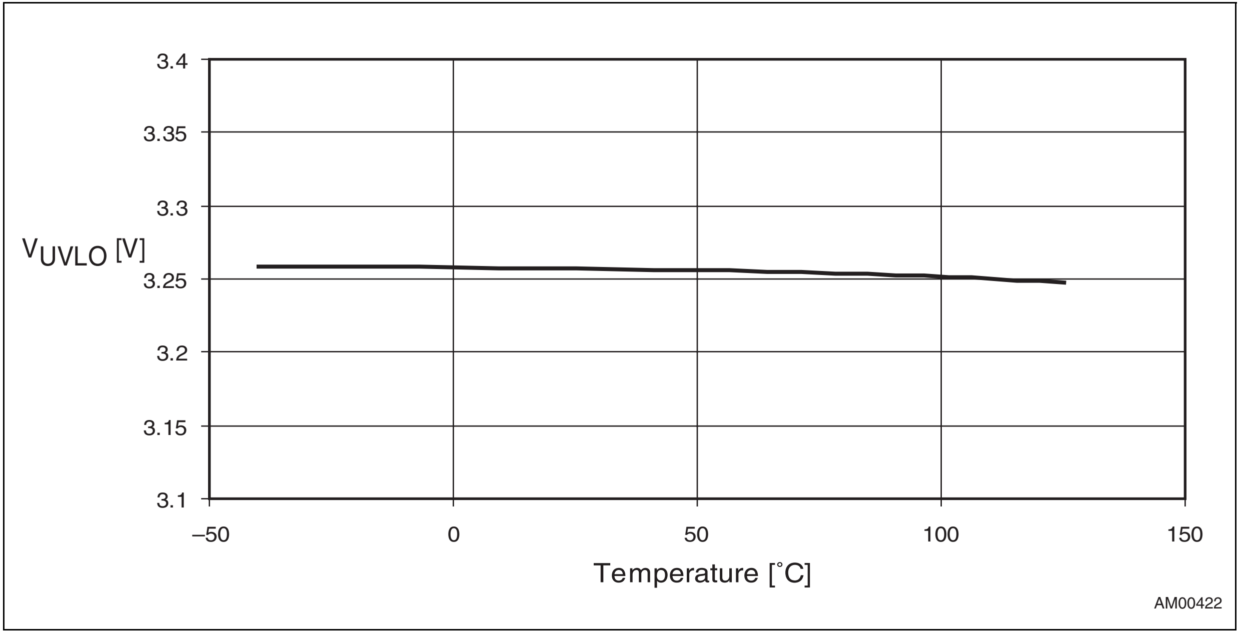


Figure 24. $V_{OL(\overline{FLT})}$ at 1 mA vs. temperature

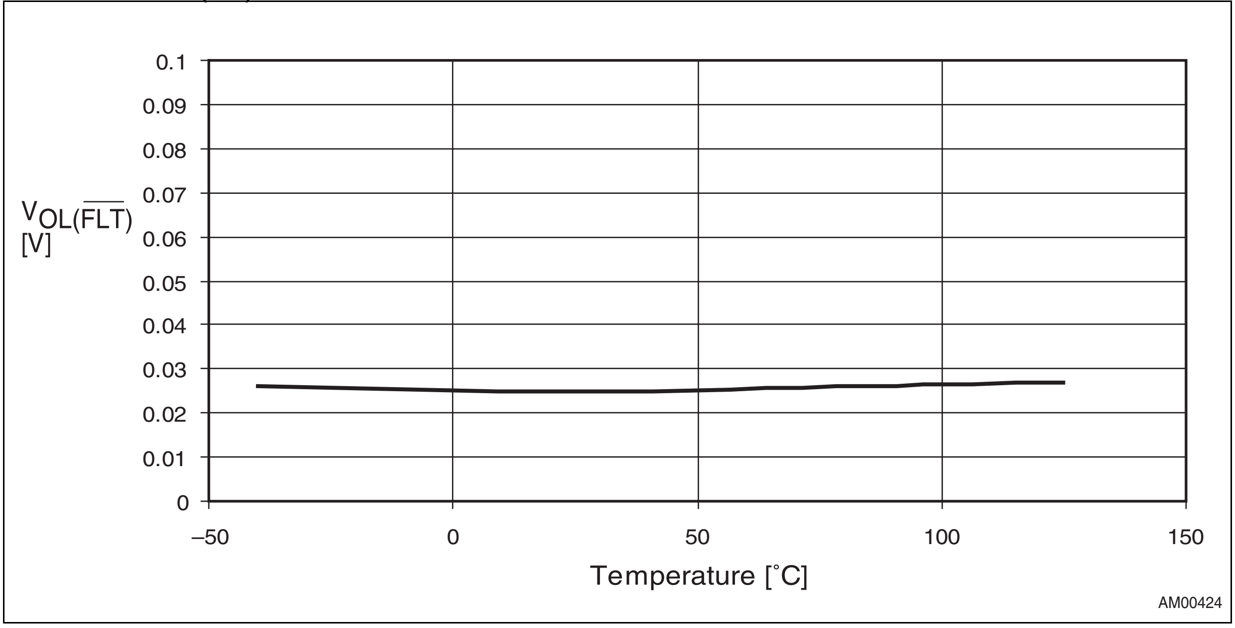
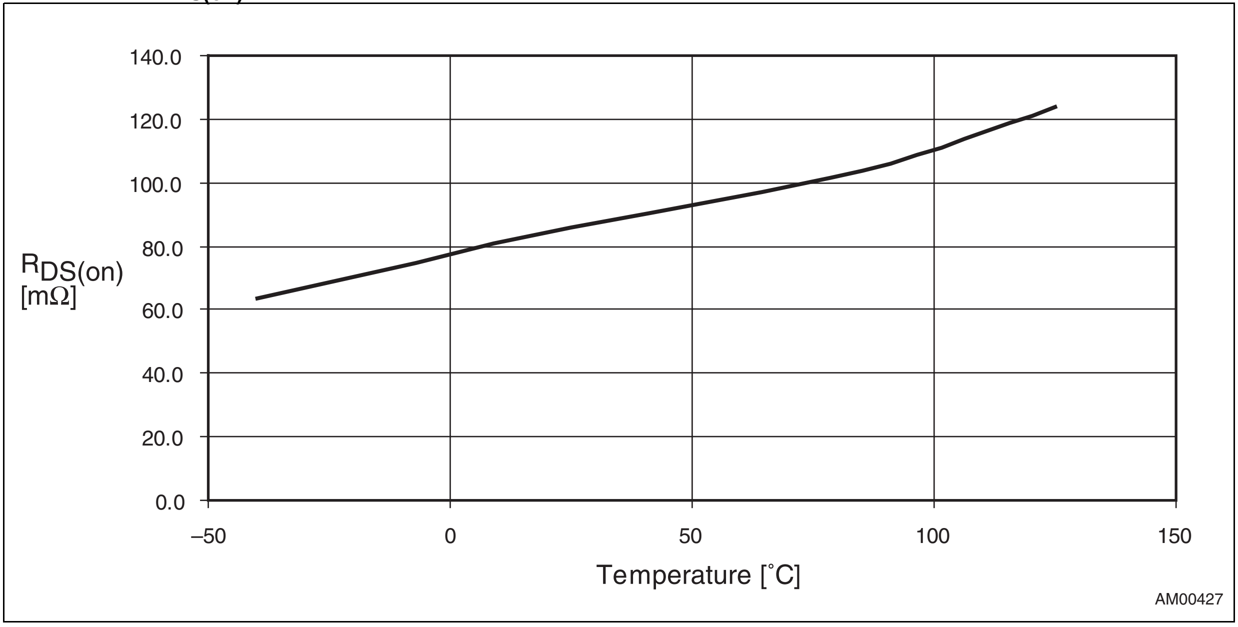


Figure 25. $R_{DS(on)}$ at 1 A vs. temperature



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 26. TDFN – 10-lead, 2.5 x 2.0 x 0.75 mm body, pitch 0.50 mm, package mechanical drawing

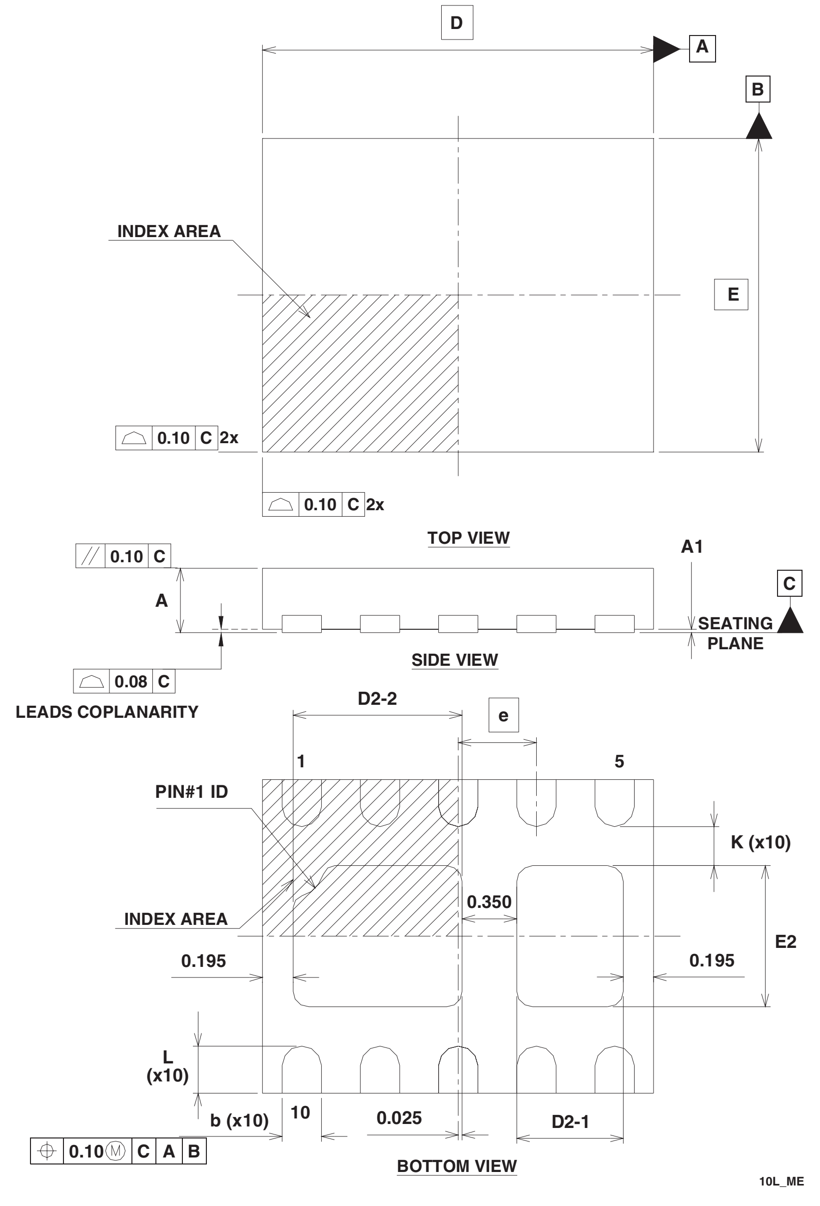


Table 6. TDFN – 10-lead, 2.5 x 2.0 x 0.75 mm body, pitch 0.50 mm, package mechanical data dimensions(1)

Symbol	(mm)			(inches)			Note
	Min.	Nom.	Max.	Min.	Nom.	Max.	
A	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00	0.02	0.05	0.000	0.001	0.002	
b	0.18	0.25	0.30	0.007	0.010	0.012	
D BSC		2.50			0.098		
D2-1	0.53	0.68	0.78	0.021	0.027	0.031	
D2-2	0.93	1.08	1.18	0.037	0.043	0.046	
E BSC		2.00			0.079		
E2	0.75	0.90	1.00	0.030	0.035	0.039	
e		0.50			0.020		
L	0.20	0.30	0.40	0.008	0.012	0.016	
K	0.20			0.008			
N	10			10			(2)

1. Controlling dimension: millimeters.
2. N is the total number of terminals.

11 Tape and reel specification

Figure 27. Tape and reel

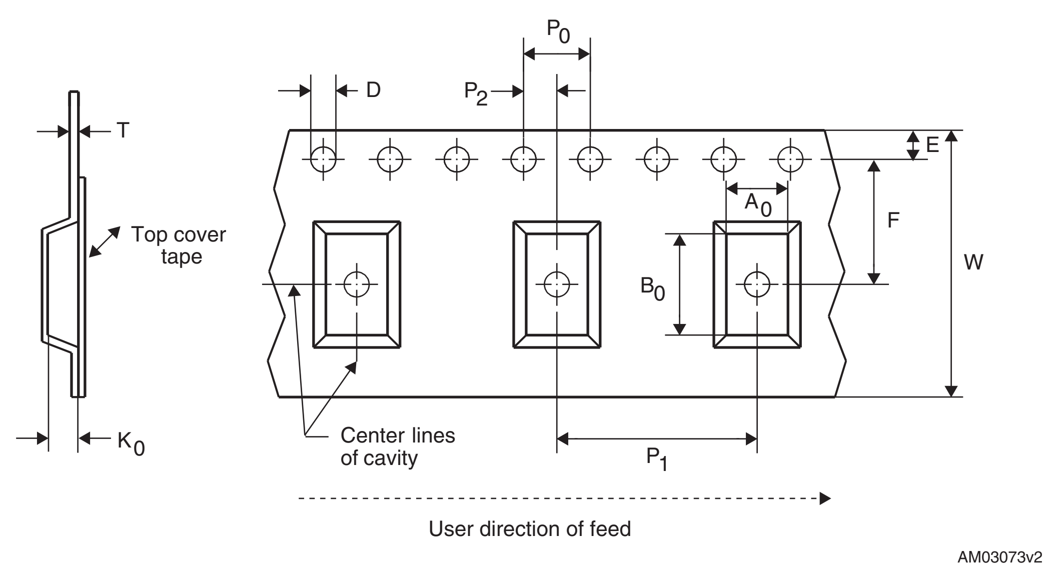


Table 7. Carrier tape dimensions

Tape size	W	D	E	Po	P2	F
12	12.00 ± 0.30	1.50 +0.10 / –0.00	1.75 ± 0.10	4.00 ± 0.10	2.00 ± 0.10	5.50 ± 0.05

Table 8. Further tape and reel information

Package code	W	Ao	Bo	Ko	P1	T	Bulk Qty.	Reel Diameter
2 x 2.5mm TDFN 10 lead	12	2.30 ± 0.10	2.80 ± 0.10	1.10 ± 0.01	4.00 ± 0.10	0.30 ± 0.05	3000	13

Figure 28. Reel dimensions

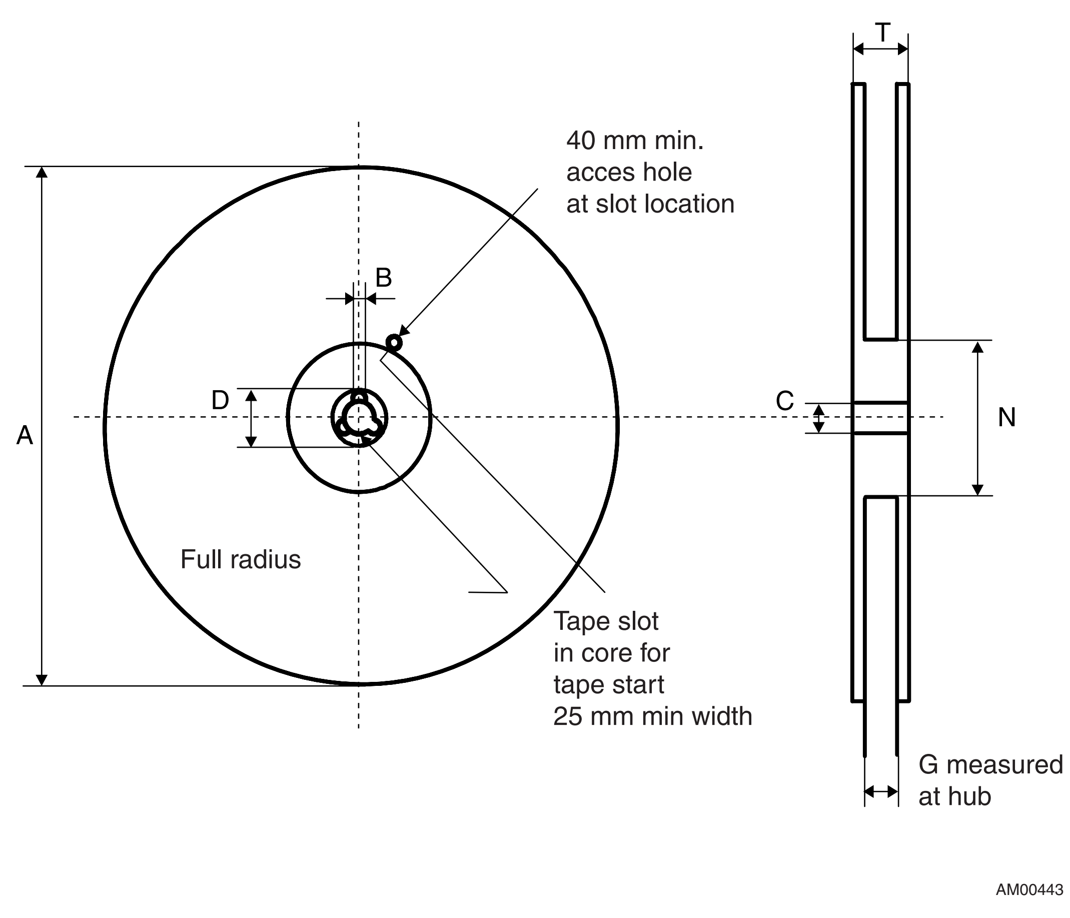


Table 9. Reel dimensions

Tape size	A max.	B min.	C	D min.	N min.	G	T max.
12 mm	330 (13 inch)	1.5	13 ± 0.2	20.2	60	12.4 + 2 / – 0	18.4

Figure 29. Tape trailer/leader

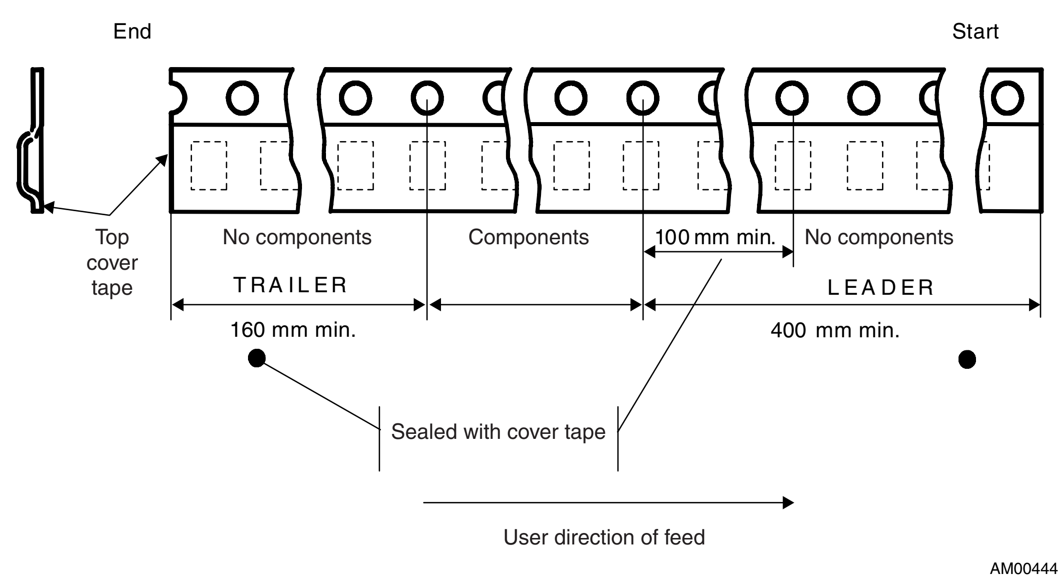
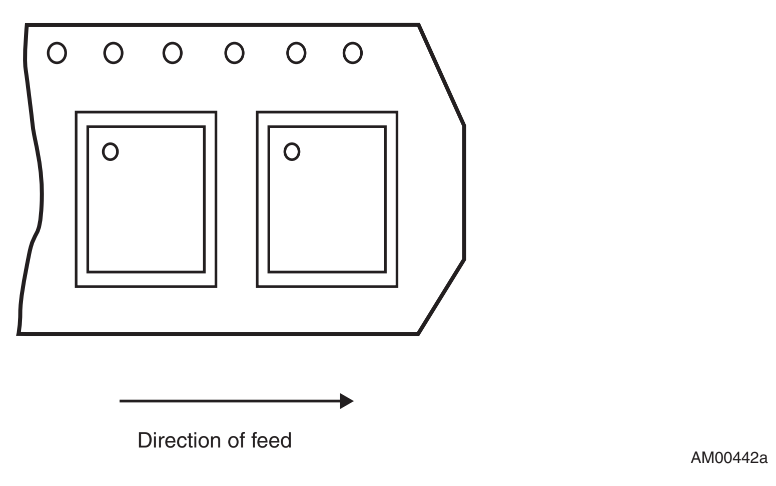


Figure 30. Pin 1 orientation



Note: 1 *Drawings are not to scale.*

2 *All dimensions are in mm, unless otherwise noted.*

12 Part numbering

Table 10. Ordering information scheme

STBP120 D V DK 6 F

Device type

STBP120

Overvoltage threshold

A = 5.375 V

B = 5.50 V

C = 5.85 V

D = 6.02 V

Undervoltage threshold

V = 3.25 V

Package

DK = TDFN – 10-lead, 2.5 x 2 mm

Temperature range

6 = –40 °C to +85 °C

Shipping method

F = ECOPACK® package, tape and reel

Note: *Other overvoltage thresholds are offered. Minimum order quantities may apply. Contact local sales office for availability.*

13 Package marking information

Table 11. Marking description

Part number(1)	Overvoltage threshold (V)	Topside marking
STBP120AVxxxx	5.375	P12A
STBP120BVxxxx	5.50	P12B
STBP120CVxxxx	5.85	P12C
STBP120DVxxxx	6.02	P12D

1. Other overvoltage thresholds are offered. Minimum order quantities may apply.
Contact local sales office for availability.

14 Revision history

Table 12. Document revision history

Date	Revision	Changes
20-Mar-2009	1	Initial release.
07-Apr-2009	2	Updated *Section 2*, *Section 3*, *Figure 5*, t_{on} and t_{start} in *Table 5* and shipping method in *Table 10*, added *Section 8* and *Section 9*.
29-Apr- 2009	3	Updated the revision history table - removed the draft revisions.
01-Jun-2009	4	Updated *Features*, *Section 4.3*, *Table 2*, *Figure 5*, *Table 5*, *Figure 10*, *Figure 12*, *Figure 13*, *Figure 14*, *Figure 15*, *Figure 16*, *Figure 17*, *Figure 18*, removed *Figure 22, Figure 23*, *Figure 25, Figure 27, Figure 29, Figure 30,* added *Section 11: Tape and reel specification*.

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