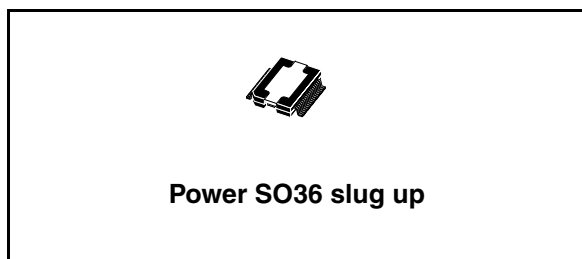


**60 V 6 A quad power half bridge****Features**

- Minimum input output pulse width distortion
- 200 m $\Omega$  R<sub>dsON</sub> complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- Thermal warning output
- Under voltage protection

**Description**

STA516B is a monolithic quad half bridge stage in Multipower BCD Technology. The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to V<sub>dd</sub> pin, as single bridge with double current capability, and as half bridge (Binary mode) with half current capability.

The device is particularly designed to make the output stage of a stereo all-digital high efficiency (DDX™) amplifier capable to deliver 160 + 160 W @ THD = 10 % at V<sub>cc</sub> 50 V output power on 8  $\Omega$  load and 320 W @ THD = 10 % at V<sub>cc</sub> 50V on 4  $\Omega$  load in single BTL configuration.

The input pins have threshold proportional to V<sub>L</sub> pin voltage.

**Table 1. Device summary**

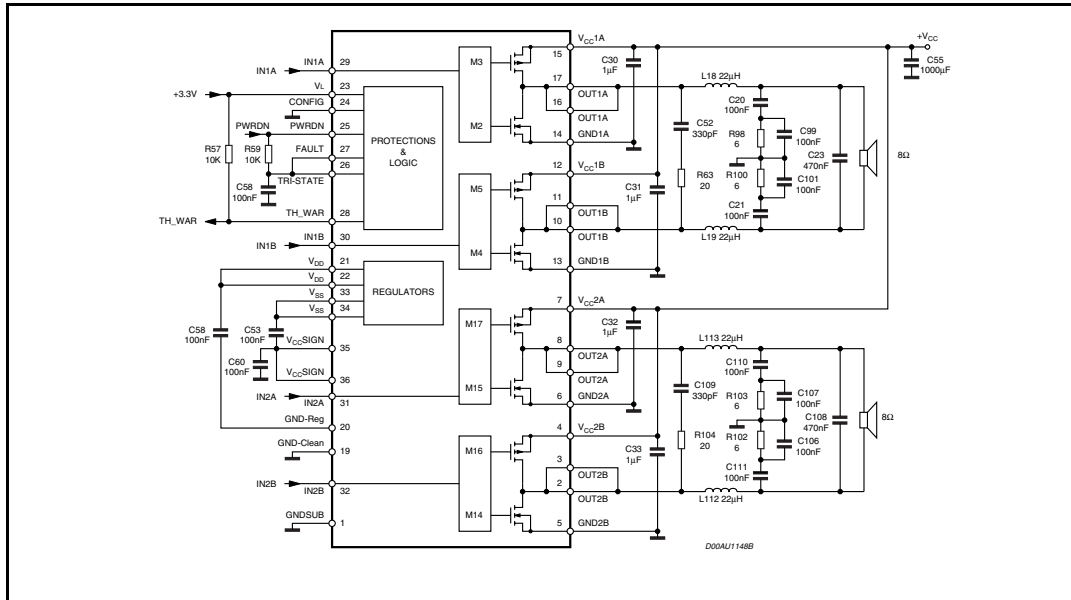
Part number	Package	Packaging
STA516B	Power SO36 slug up	Tube
STA516B13TR	Power SO36 slug up	Tape and reel

## Contents

1	Introduction .....	3
2	Pin lists .....	4
3	Electrical characteristics .....	6
4	Power supply and control sequencing .....	8
5	Test .....	9
6	Mechanical and package data .....	11
7	Revision history .....	12

# 1 Introduction

Figure 1. Application circuit (dual BTL)



## 2 Pin lists

**Table 2. Pin function**

Number	Pin	Description
1	GND-SUB	Substrate ground
2, 3	OUT2B	Output half bridge 2B
4	Vcc2B	Positive supply
5	GND2B	Negative supply
6	GND2A	Negative supply
7	Vcc2A	Positive supply
8, 9	OUT2A	Output half bridge 2A
10, 11	OUT1B	Output half bridge 1B
12	Vcc1B	Positive supply
13	GND1B	Negative supply
14	GND1A	Negative supply
15	Vcc1A	Positive supply
16, 17	OUT1A	Output half bridge 1A
18	NC	Not connected
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator Vdd
21, 22	Vdd	5 V regulator referred to ground
23	V <sub>L</sub>	High logical state setting voltage
24	CONFIG	Configuration pin
25	PWRDN	Stand-by pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
33, 34	Vss	5 V regulator referred to +Vcc
35, 36	Vcc sign	Signal positive supply

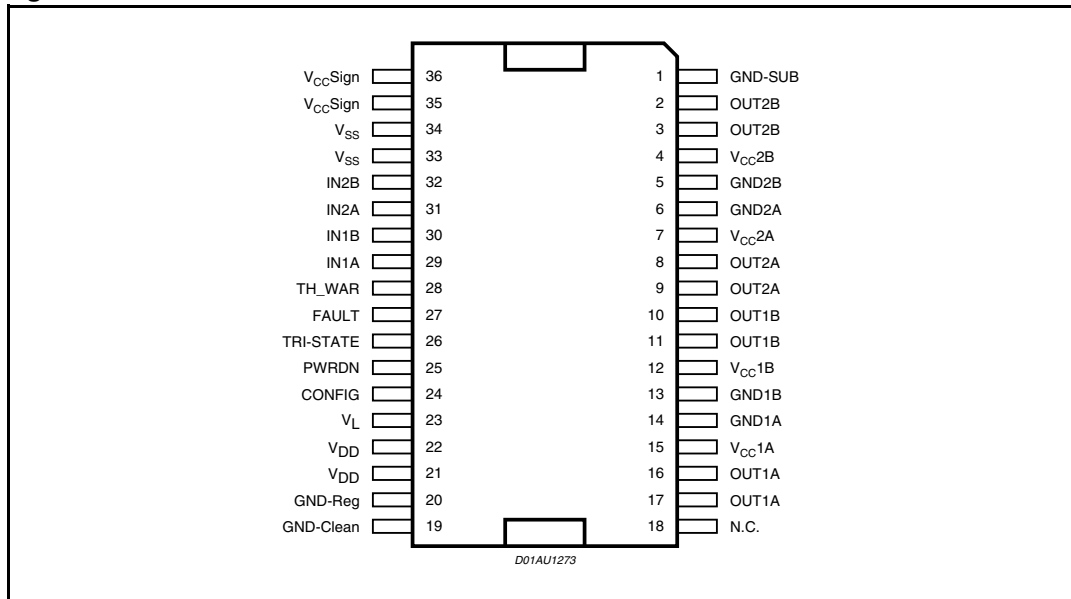
**Table 3. Functional pin status**

Pin name	Logical value	Status
FAULT	0	Fault detected (short circuit or thermal for example)
FAULT <sup>(1)</sup>	1	Normal operation
TRI-STATE	0	All powers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorption
PWRDN	1	Normal operation
THWAR	0	Temperature of the IC =130 °C
THWAR <sup>(1)</sup>	1	Normal operation
CONFIG	0	Normal operation
CONFIG <sup>(2)</sup>	1	OUT1A=OUT1B; OUT2A=OUT2B (IF IN1A = IN1B; IN2A = IN2B)

1. The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.

2. To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd)

**Figure 2. Pin connection**



### 3 Electrical characteristics

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage (Pins 4,7,12,15)	60	V
$V_{max}$	Maximum voltage on pins 23 to 32	5.5	V
$T_{op}$	Operating temperature range	0 to 70	°C
$T_{stg}, T_j$	Storage and junction temperature	-40 to 150	°C

**Table 5. Thermal data**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{j-case}$	Thermal resistance junction to case (thermal pad)		1	2.5	°C/W
$T_{jSD}$	Thermal shut-down junction temperature		150		°C
$T_{warn}$	Thermal warning temperature		130		°C
$t_{hSD}$	Thermal shut-down hysteresis		25		°C

**Table 6. Electrical characteristics**  
( $V_L = 3.3$  V;  $V_{CC} = 50$  V;  $T_{amb} = 25$  °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{dsON}$	Power Pchannel/Nchannel MOSFET $R_{dsON}$	$I_d = 1A$		200	240	mΩ
$I_{dss}$	Power Pchannel/Nchannel leakage $I_{dss}$				100	μA
$g_N$	Power Pchannel $R_{dsON}$ matching	$I_d = 1A$	95			%
$g_P$	Power Nchannel $R_{dsON}$ matching	$I_d = 1A$	95			%
$Dt_s$	Low current dead time (static)	see <a href="#">Figure 4</a>		10	20	ns
$Dt_d$	High current dead time (dynamic)	$L = 22\mu H, C = 470nF$ $R_I = 8\Omega, I_d = 4.5A$ see <a href="#">Figure 5</a>			50	ns
$t_{dON}$	Turn-on delay time	Resistive load			100	ns
$t_{dOFF}$	Turn-off delay time	Resistive load			100	ns
$t_r$	Rise time	Resistive load see <a href="#">Figure 4</a>			25	ns
$t_f$	Fall time	Resistive load see <a href="#">Figure 4</a>			25	ns
$V_{CC}$	Supply operating voltage		10		52	V
$V_{IN-High}$	High level input voltage				$V_L/2 + 300mV$	V
$V_{IN-Low}$	Low level input voltage		$V_L/2 - 300mV$			V
$I_{IN-H}$	High level Input current	Pin voltage = $V_L$		1		μA
$I_{IN-L}$	Low level input current	Pin voltage = 0.3 V		1		μA

**Table 6. Electrical characteristics (continued)**  
**(VL= 3.3 V; Vcc = 50 V; Tamb = 25 °C unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>PWRDN-H</sub>	High level PWRDN pin input current	V <sub>L</sub> = 3.3 V		35		μA
V <sub>Low</sub>	Low logical state voltage VL (pin PWRDN, TRISTATE)(see <a href="#">Table 7</a> )	V <sub>L</sub> = 3.3 V	0.8			V
V <sub>High</sub>	High logical state voltage VH (pin PWRDN, TRISTATE)(see <a href="#">Table 7</a> )	V <sub>L</sub> = 3.3 V			1.7	V
I <sub>VCC-PWRDN</sub>	Supply current from Vcc in power down	PWRDN = 0			3	mA
I <sub>FAULT</sub>	Output current pins FAULT -TH-WARN when FAULT CONDITIONS	V <sub>pin</sub> = 3.3 V		1		mA
I <sub>VCC-hiz</sub>	Supply current from Vcc in Tristate	Tristate = 0		22		mA
I <sub>VCC</sub>	Supply current from Vcc in operation both channel switching)	Input pulse width = 50 % duty Switching frequency = 384 KHz; No LC filters		70		mA
I <sub>OUT-SH</sub>	Over current protection threshold I <sub>sc</sub> (short circuit current limit) <sup>1</sup>		6	8	10	A
V <sub>UV</sub>	Under voltage protection threshold			7		V
V <sub>OV</sub>	Over voltage protection threshold		60		70	V
t <sub>pw_min</sub>	Output minimum pulse width	No load	25		40	ns

1. See specific application note number: AN1994.

**Table 7. VLow, VHigh variation with VL**

V <sub>L</sub>	V <sub>Low</sub> min	V <sub>High</sub> max	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

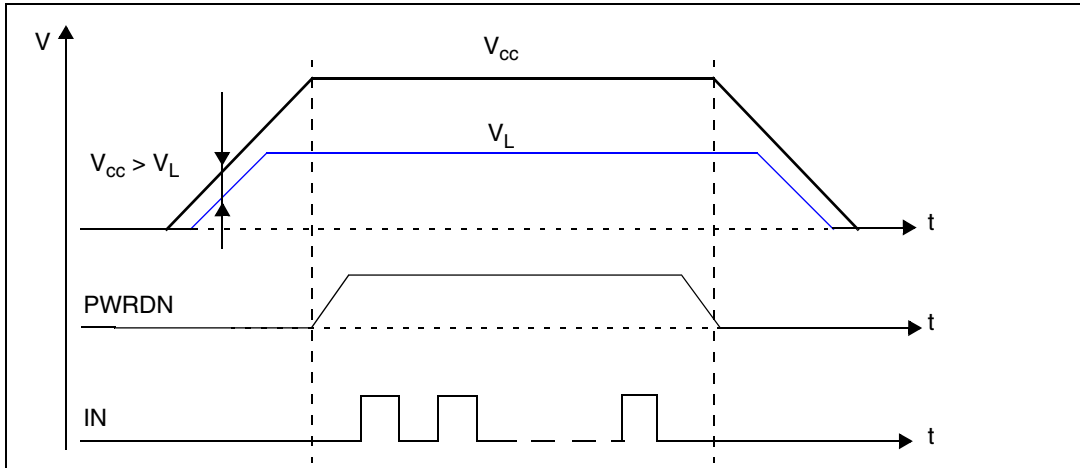
**Table 8. Logic truth table (see [Figure 2](#))**

Tristate	INxA	INxB	Q1	Q2	Q3	Q4	Output mode
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

## 4 Power supply and control sequencing

To guarantee correct operation and reliability, a correct turn on/off sequence must be followed. *Figure 3* shows the correct power on sequence.

**Figure 3. Correct power-on sequence**



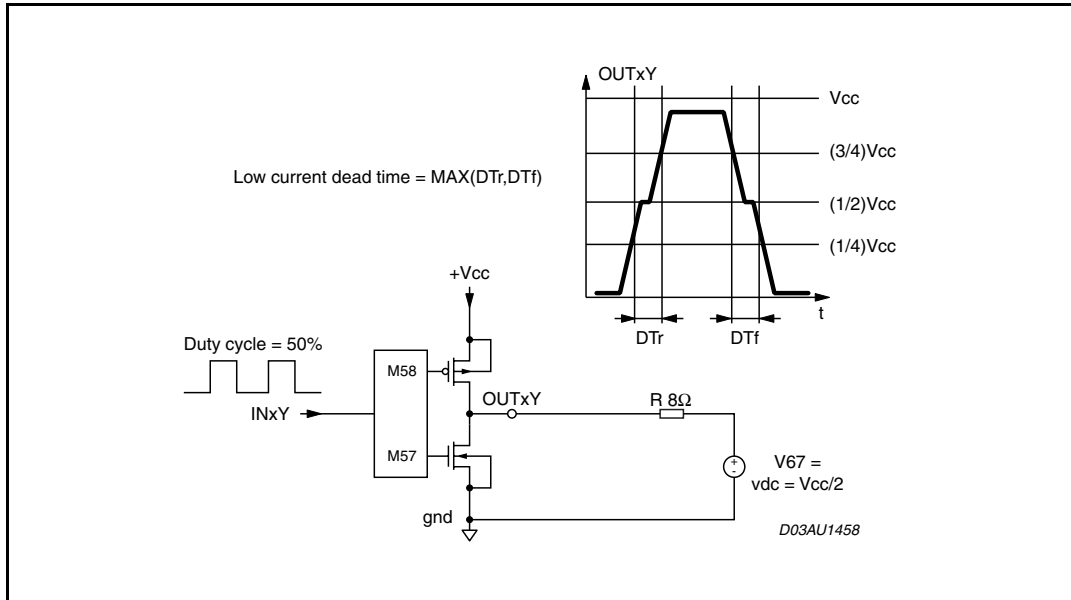
$V_{CC}$  must turn on before  $V_L$  in order to prevent uncontrolled current flowing through an internal protection diode connected between  $V_L$  (logic supply) and  $V_{CC}$  (high power supply). Failure to do so could result in damage to the device.

PWRDN must be released after  $V_L$  is switched on. An input signal can then be sent to the power stage.

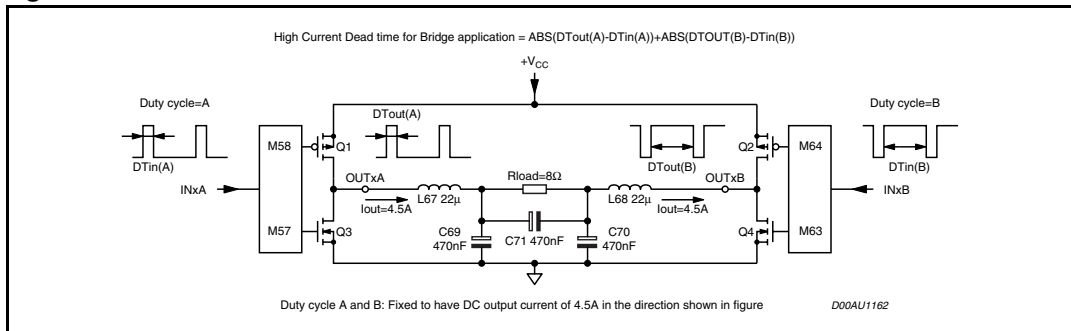


# 5 Test

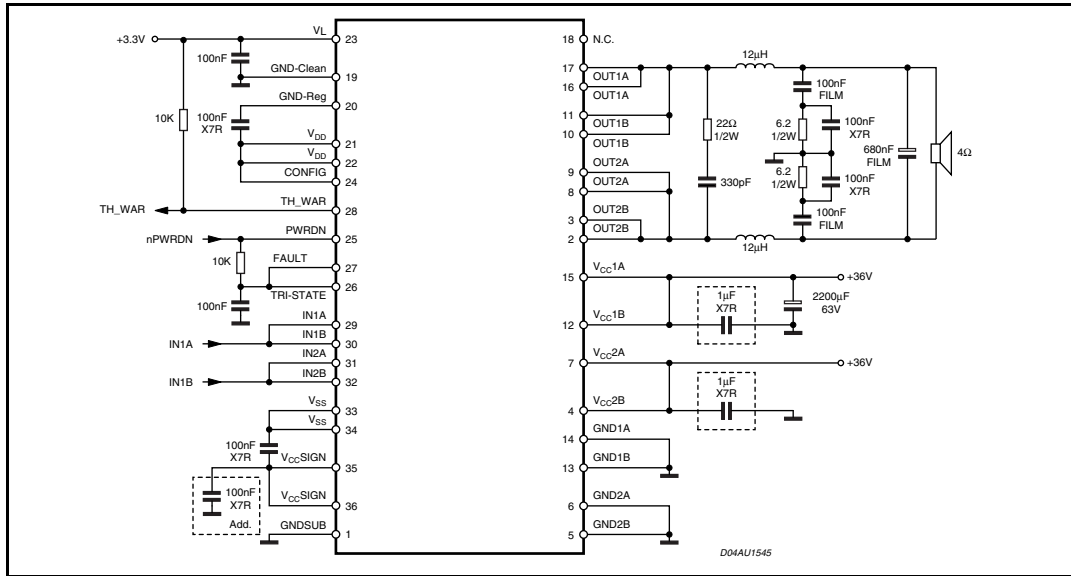
**Figure 4. Test circuit**



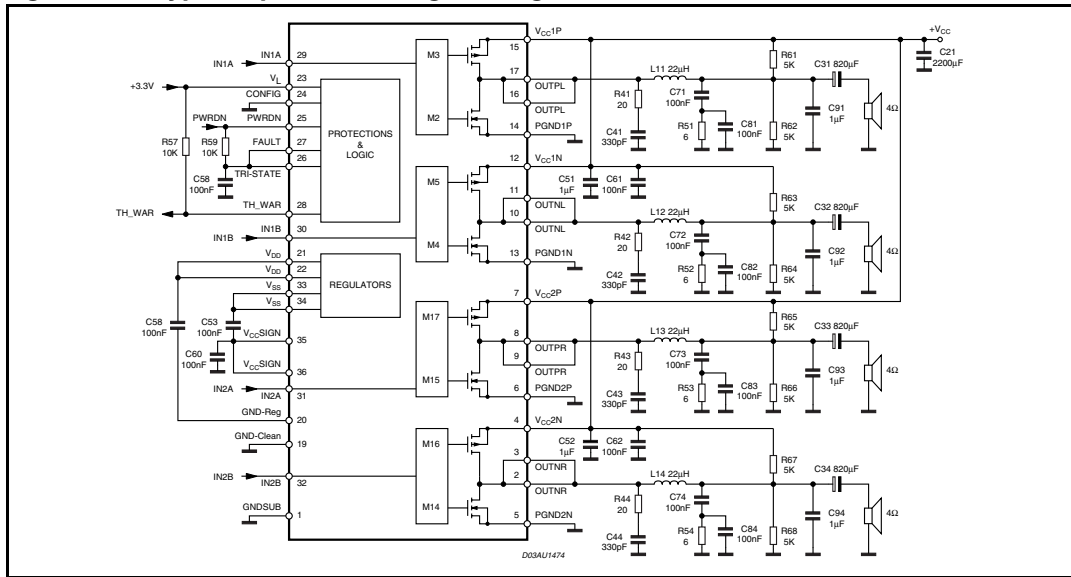
**Figure 5. Current dead time test circuit**



**Figure 6. Typical single BTL configuration to obtain 320 W @ THD 10 %,  $R_L = 4 \Omega$ ,  $V_{CC} = 50 \text{ V}$  (a)**



**Figure 7. Typical quad half bridge configuration**



For more information, refer to the application note “ST50X and STA51X digital power amplifiers”.

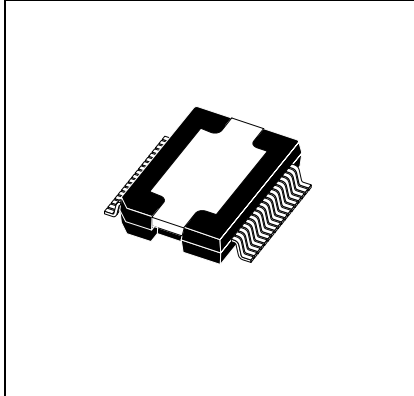
a. A PWM modulator as driver is required. This result was obtained using the STA30X+STA50X demo board.

# 6 Mechanical and package data

Figure 8. Power SO36 (slug up) mechanical data and package dimension

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.43	0.128		0.135
A2	3.1		3.2	0.122		0.126
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0.030		-0.040	0.0011		-0.0015
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N			10°			10°
s			8°			8°

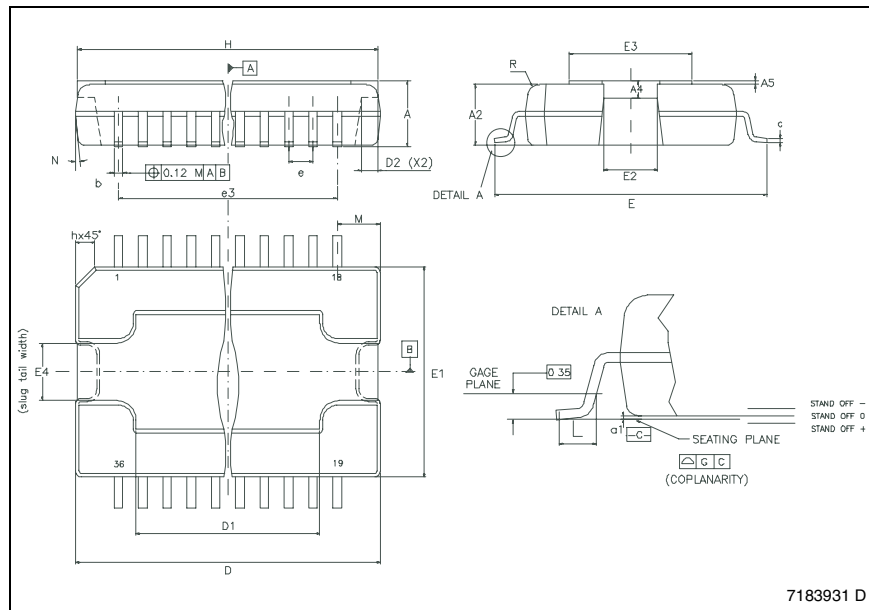
**OUTLINE AND MECHANICAL DATA**



**PowerSO36 (SLUG UP)**

(1) "D and E1" do not include mold flash or protrusions.  
Mold flash or protrusions shall not exceed 0.15mm (0.006")

(2) No intrusion allowed inwards the leads.



## 7 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
01-Feb-2007	1	Initial release
19-Mar-2007	2	Update to reflect product maturity.

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

