



STA333ML

Sound Terminal™

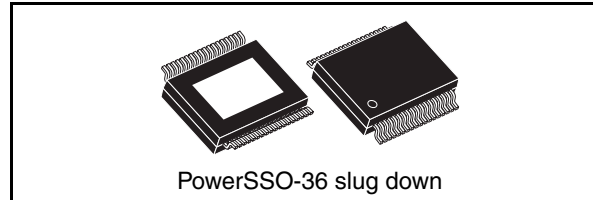
2-channel microless high-efficiency digital audio system

Features

- Wide supply voltage range (4.5 - 18 V)
- 2 x 20 W into 8 Ω at $V_{CC} = 18$ V
- 3 power output configurations; 2 channels of ternary PWM
- PowerSSO-36 exposed pad package
- 2 channels of 24-Bit DDX®
- 100-dB SNR and dynamic range
- 32 kHz to 48 kHz input sample rates
- Soft volume update
- Automatic zero-detect mute
- Automatic invalid input detect mute
- 2-channel I²S input data interface
- Selectable clock input ratio (256 or 364 x fs)
- Max power correction for lower full power
- 96 kHz internal processing sample rate, 24-bit precision
- Thermal overload and short-circuit protection embedded

Applications

- LCD
- DVD
- Cradle
- Digital speaker
- Wireless speaker cradle



Description

STA333ML is a single die embedding digital audio processing and high efficiency DDX® power amplification, capable of operating without the aid of an external micro controller.

The STA333ML is part of the Sound Terminal™ family that provides full digital audio streaming to the speaker offering cost effectiveness, low energy dissipation and sound enrichment.

The STA333ML combines a unique 24-bit DDX® digital class-D ternary modulator together with an extremely low $R_{DS(ON)}$ stereo power DMOS stage. It is capable of a total output power of 2 x 20 W with outstanding performance in terms of efficiency (>90 %), THD, SNR and EMI.

The microless feature allows the use in low-cost applications (cradle, digital speakers, audio terminals) where no micro controller is needed.

The serial audio data interface accepts the universally used I²S format. Basic features (like oversampling clock, gain and I2S format) can be set using a minimal number of selection pins.

The STA333ML is self-protected against thermal overload, overcurrent, short circuit and overvoltage conditions.

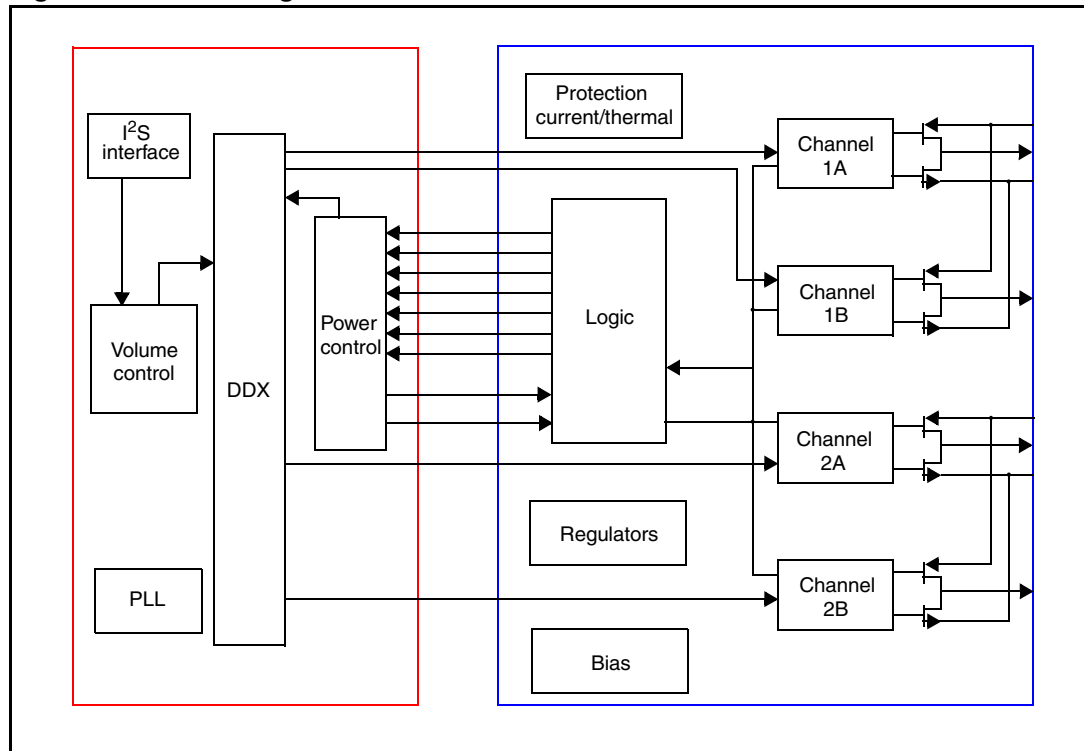
The fault condition is also exported to an external pin (INT_LINE) for specific requirements.

Table 1. Device summary

Order code	Package	Packaging
STA333ML	PowerSSO-36 (slug down)	Tube
STA333ML13TR	PowerSSO-36 (slug down)	Tape and reel

1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection (top view)

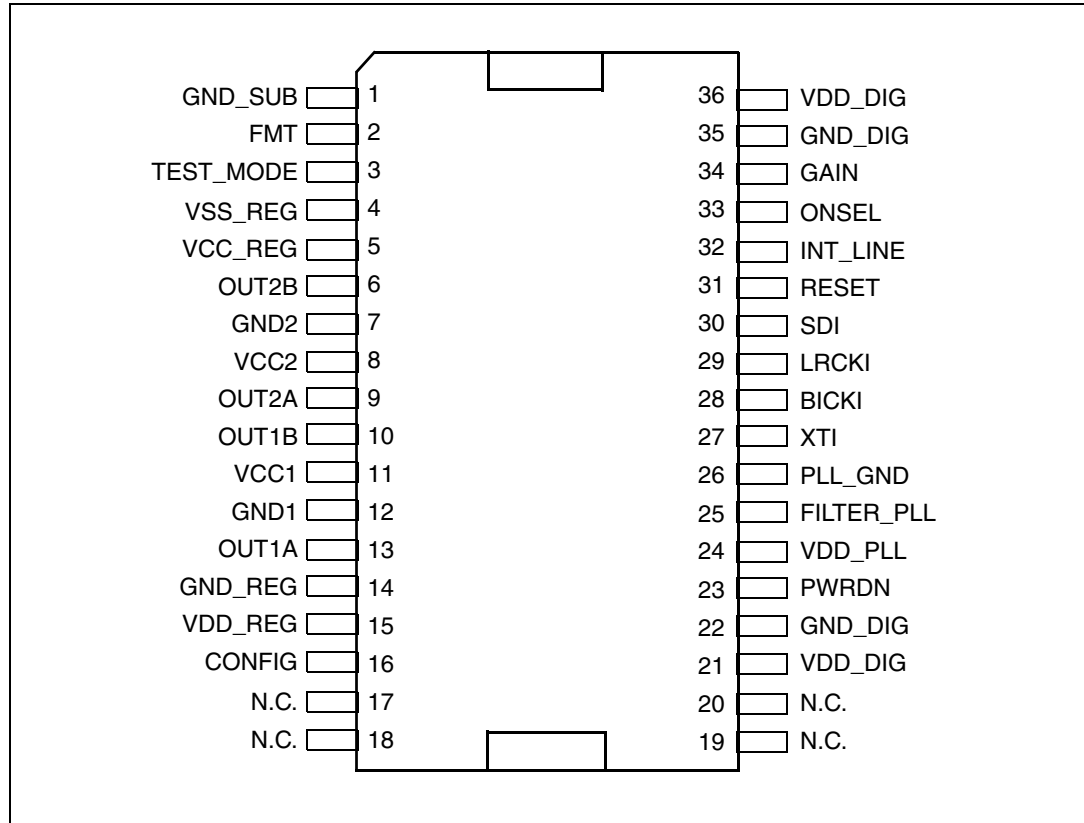


Table 2. Pin description

Pin	Type	Name	Description
1	Gnd	GND_SUB	Substrate ground
2	I	FMT	0: I ² S format 1: left justified
3	I	TEST_MODE	This pin must be connected to ground
4	I/O	VSS	Internal reference at Vcc-3.3 V
5	I/O	VSS_REG	Internal Vcc reference
6	O	OUT2B	Output half bridge 2B
7	Gnd	GND2	Power negative supply
8	Power	VCC2	Power positive supply
9	O	OUT2A	Output half bridge 2A
10	O	OUT1B	Output half bridge 1B
11	Power	VCC1	Power positive supply
12	Gnd	GND1	Power negative supply

Table 2. Pin description (continued)

Pin	Type	Name	Description
13	I/O	OUT1A	Output half bridge 1A
14	GND	GND_REG	Internal ground reference
15	Power	VDD_REG	Internal 3.3 V reference voltage
16	I	CONFIG	Paralleled mode command
17		N.C.	Not connected
18		N.C.	Not connected
19		N.C.	Not connected
20		N.C.	Not connected
21	Power	VDD_DIG	Positive supply digital
22	GND	GND_DIG	Digital ground
23	I	PWDN	Power down: 0: low-power mode 1: normal operation
24	Power	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	GND	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock, 256 x fs or 384 x fs
28	I	BICKI	I ² S serial clock
29	I	LRCKI	I ² S left/right clock
30	I	SDI	I ² S serial data channel
31	I	RESET	Reset
32	O	INT_LINE	Fault interrupt
33	I	ONSEL	Oversampling selector: 0: 256 fs 1: 384 fs
34	I	GAIN	Gain selector: 0: 0 dBFS 1: 24 dBFS
35	GND	GND_DIG	Digital ground
36	Power	VDD_DIG	Digital supply

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{Th(j-case)}$	Thermal resistance junction to case (thermal pad)		1.5	2	°C/W
T_{sd}	Thermal shut-down junction temperature		150		°C
T_w	Thermal warning temperature		130		°C
T_{hsd}	Thermal shut-down hysteresis		20		°C

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Power supply voltage (VCC1, VCC2)			20	V
V_L	Logic input interface	-0.3		4	V
VDD_DIG	Positive supply digital			4	V
T_{op}	Operating junction temperature	0		150	°C
T_{stg}	Storage temperature	-40		150	°C

3.3 Recommended operating condition

Table 5. Recommended operating condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power supply voltage (VCC1, VCC2)	4.5		18.0	V
V_L	Logic Input Interface	2.7	3.3	3.6	V
V_{DD_DIG}	Positive supply digital	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	0		70	°C

3.4 Electrical characteristics

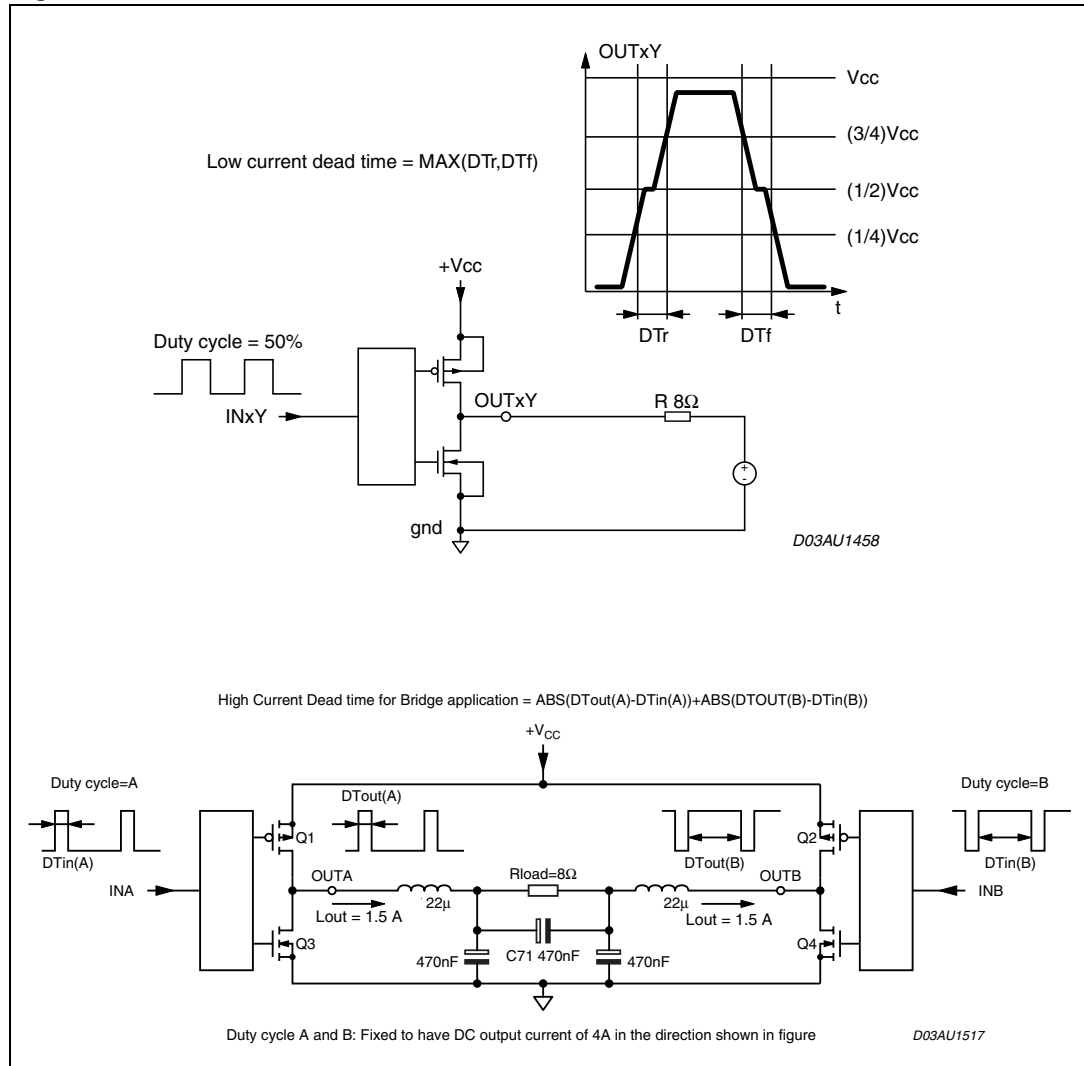
The specifications given here are with the operating conditions $V_{CC} = 18\text{ V}$, $V_{DD_DIG} = 3.3\text{ V}$, $f_{sw} = 384\text{ kHz}$, $T_{amb} = 25^\circ\text{ C}$ and $R_L = 8\ \Omega$, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Po	Output power BTL	THD = 1%		16		W
		THD = 10%		20		
R _{dsON}	Power Pchannel/Nchannel MOSFET (total bridge)	I _d = 1 A		180	250	mΩ
I _{dss}	Power Pchannel/Nchannel leakage	V _{cc} = 18 V			10	μA
gP	Power Pchannel RdsON matching	I _d = 1 A	95			%
gN	Power Nchannel RdsON matching	I _d = 1 A	95			%
I _{LDT}	Low current dead time (static)	Resistive load, see Figure 3		5	10	ns
I _{HDT}	High current dead time (dynamic)	I _{load} = 1.5 A, see Figure 3		10	20	ns
t _r	Rise time	Resistive load, see Figure 3		8	10	ns
t _f	Fall time	Resistive load, see Figure 3		8	10	ns
V _{CC}	Supply voltage (VCC1, VCC2)		4.5		18	V
I _{cc}	Supply current from V _{CC} in power down mode	PWRDN = 0		0.1		mA
	Supply current from V _{CC} in operation	PCM input signal = -60 dBFS. Switching frequency = 384 kHz No LC filters		30		mA
	Supply current DDX processing (reference only)	Internal clock = 49.152 MHz		80		mA
I _{lim}	Overcurrent limit	Nonlinear output	2.2	3.5	4.3	A
I _{sc}	Short circuit protection	Hi-Z output	2.7	3.8	5.0	A
UVL	Under voltage protection threshold			3.5	4.3	V
t _{min}	Output minimum pulse width	No load	20	30	60	ns
DR	Dynamic range			100		dB
SNR	Signal to noise ratio	A-weighted		94		dB
THD+N	Total harmonic distortion and noise	Po = 1 W, f = 1 kHz		0.05	0.2	%
PSRR	Power supply rejection ratio	DDX stereo, < 5 kHz Vripple = 1 V RMS Audio input = dither only		80		dB
X _{TALK}	Crosstalk	DDX stereo, < 5 kHz One channel driven at 1 W other channel measured		80		dB
η	Peak efficiency, DDX mode	Po = 2 x 20 W, 8 Ω		90		%

3.5 Testing

Figure 3. Test circuits



4 Functional description

4.1 Serial audio interface protocols

Figure 4. I²S

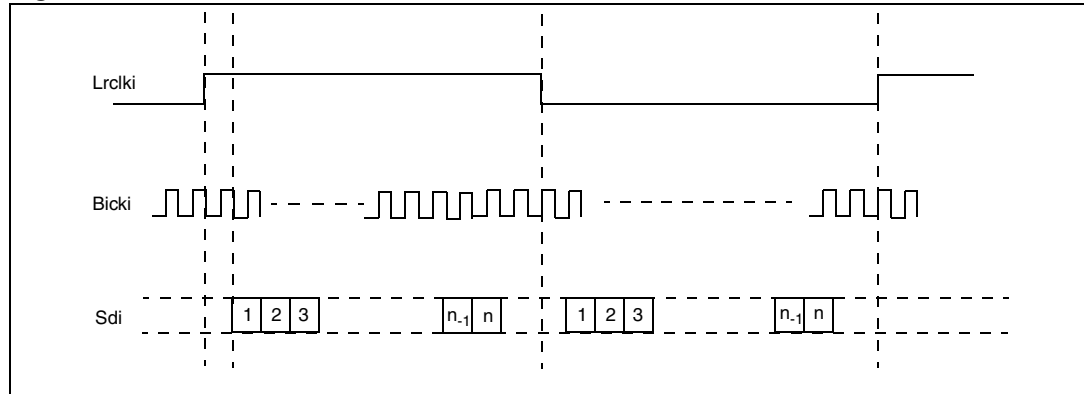
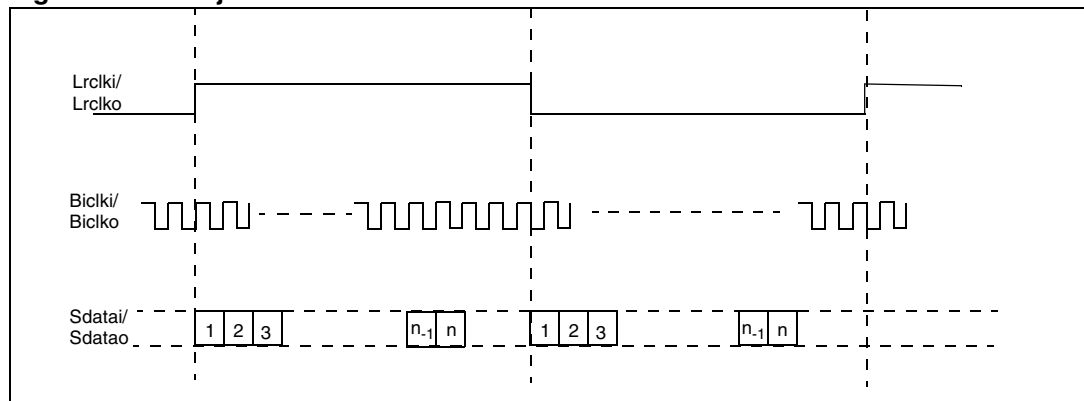


Figure 5. Left justified



4.2 Fault detect recovery bypass

The on-chip STA333ML power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either over-current or thermal). When FAULT is asserted (set to 0), the power control block attempts a recovery from the fault by asserting the tristate output (setting it to 0 which directs the power output block to begin recovery), holds it at 0 for 1 ms and then toggles it back to 1. This sequence is repeated for as long as the fault exists.

4.3 Zero-detect mute enable

If this function is enabled, the zero-detect circuit examines each processing channel to see if 2048 consecutive zero value samples (regardless of fs) are received. If so the channel is muted.

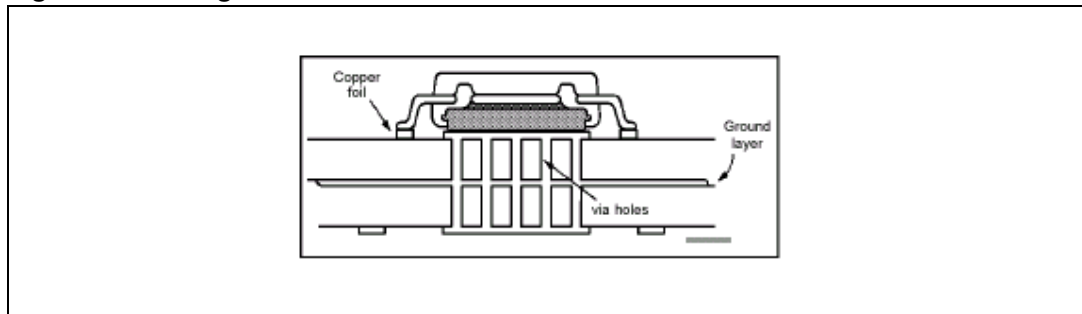
5 Package thermal characteristics

The amount of power dissipated within the device depends primarily on the supply voltage, load impedance and output modulation level. For the STA333ML the maximum dissipated power is approximately 3 W.

Thus, at an ambient temperature of 70 °C (the generally recommended maximum for consumer applications) the device can tolerate a further temperature rise of around 80° C before thermal shutdown is invoked (at $T_j = 150^\circ \text{C}$). A suitable heatsink must, therefore, be found.

Now, a thermal resistance of 25° C/W can be achieved using a ground copper area of 3 x 3 cm², and 16 vias, on the PCB as shown in [Figure 6](#). This gives a tiny margin of safety near to the upper recommended operating limits.

Figure 6. Using the PCB as heatsink



6 Package information

Figure 7 shows the 36-pin PowerSSO package drawing and Table 7 gives the dimensions.

Figure 7. PowerSSO-36 slug down outline drawing

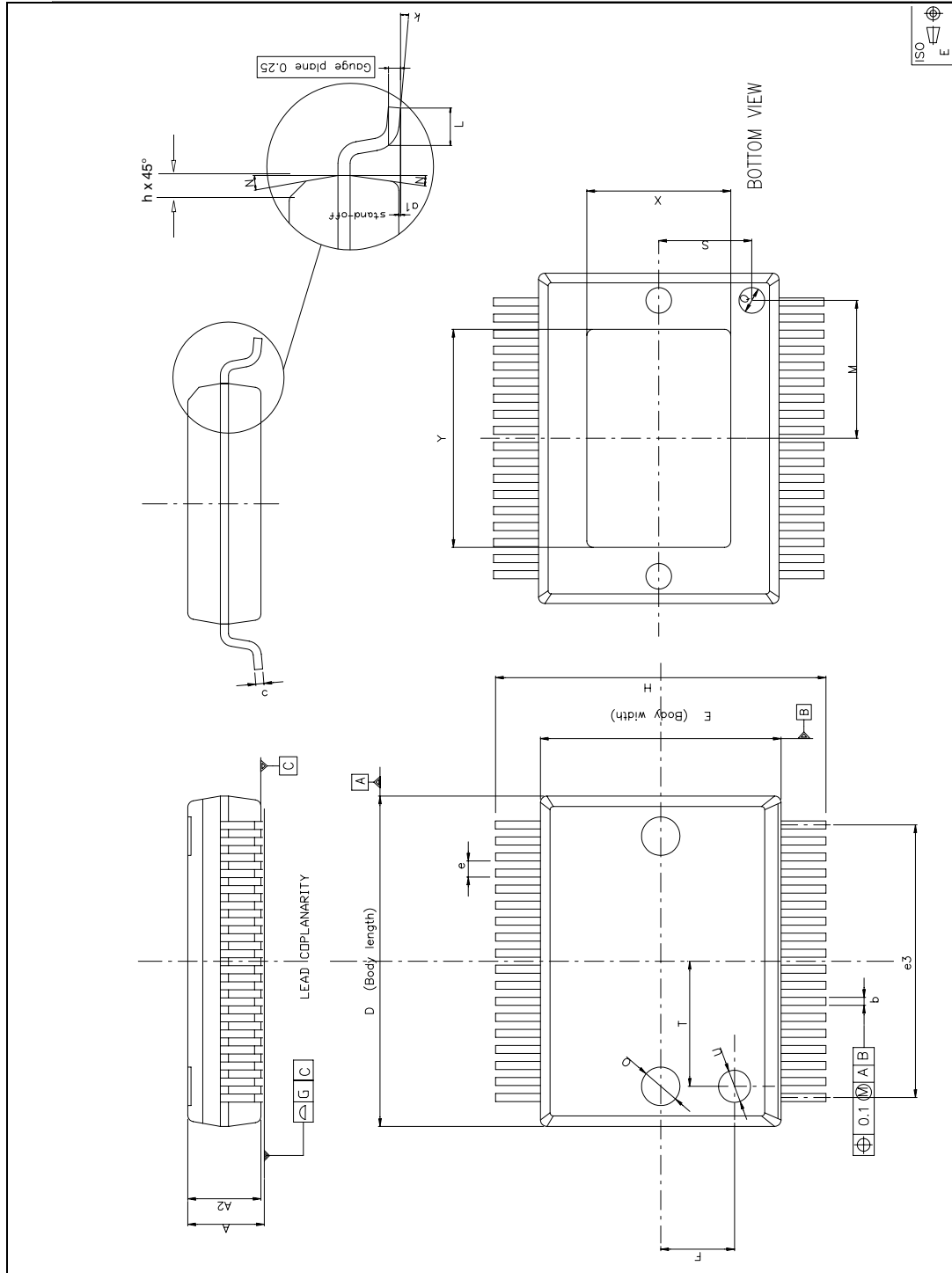


Table 7. PowerSSO-36 slug down dimensions

Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0	-	0.10	0	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	
e3	-	8.5	-	-	0.335	
F	-	2.3	-	-	0.091	
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398		0.413
h	-	-	0.40			0.016
k	0	-	8 degrees			8 degrees
L	0.60	-	1.00	0.024		0.039
M	-	4.30	-		0.169	
N	-	-	10 degrees			10 degrees
O	-	1.20	-		0.047	
Q	-	0.80	-		0.031	
S	-	2.90	-		0.114	
T	-	3.65	-		0.144	
U	-	1.00	-		0.039	
X	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.280

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

7 Trademarks and other acknowledgements

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ECOPACK is a registered trademark of STMicroelectronics.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
2-May-2008	2	Package information update
1-Feb-2007	1	Initial release.

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