Sitronix

ST7588T

81 x 132 Dot Matrix LCD Controller/Driver

n INTRODUCTION

ST7588T is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 132-segment, 80-common and 1-icon driver circuits. ST7588T can be connected directly to a microprocessor which accepts parallel interface (8-bit), serial peripheral interface (3-line or 4-line SPI), I^2C interface. Display data stores in an on-chip display data RAM (DDRAM) of 81 x 132 bits. It performs display data RAM read/write operation without external operating clock to minimize the power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

n FEATURES

Single-chip LCD controller & driver

Driver Output Circuits

- 132-segment / 81-common (1/81 duty)
- Optional display duty
  1/49, 1/65 and 1/81 (selected by MODE[1:0] pin)
- Partial display mode: 1/33 duty and 1/17 duty

On-chip Display Data RAM

- Capacity: 81X132=10,692 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MPU
- 4-line A mode SPI (write only)
- 4-line B mode SPI (write only)
- 3-line 8-bit A mode SPI (write only)
- 3-line 8-bit B mode SPI (write only)
- 3 line 9-bit SPI (write only)
- I^2C (Inter-Integrated Circuit) Interface (write only)

On-chip Low Power Analog Circuit

- Built-in Voltage Booster (x2, x3, x4, x5, x6)
- Support external booster supply (V_{OUT})
- Built-in Voltage Regulator
  With 255-step electronic contrast control
  (temperature gradient -0.12%/°C)
- Built-in Voltage Follower (with 1/4 ~ 1/11 bias)
- Supports external power supply circuits

External RESB (hardware reset) Pin

Built-in Oscillation Circuit

- Oscillator requires no external components

Wide Voltage Range

- V_{DD1}: 1.8V to 3.3V (typ.)
- V_{DD2}: 2.4V to 3.3V (typ.)
- Recommend LCD Vop: 9.5V ~ 10.5V
  (1/10 Bias, 1/81 Duty)

Temperature Range: -30 to +85 °C

ST7588T	**6800, 8080, 4-Line, 3-Line interface (without I^2C interface)**	
ST7588Ti	**I^2C interface**	

n PAD ARRANGEMENT (COG)

Chip Size: 7,708 μm × 980 μm

Bump Pitch: (minimum)

PAD NO 1~185, 248~276: 45μm (COM/SEG)

PAD NO 186~187, 188~189, 191~192, 193~194, 195~196, 197~198, 199~200, 201~202, 213~214,215~216: 119μm

PAD NO 187~188, 189~190, 192~193, 194~195, 196~197, 198~199, 200~201, 209~211, 212~213, 214~215, 216~217, 218~220: 73μm

PAD NO 190~191: 134μm; PAD NO 202~203: 77μm; PAD NO 204~205, 206~207: 75μm

PAD NO 203~204, 205~206: 175μm; PAD NO 207~208: 150μm; PAD NO 211~212, 217~218: 102μm

PAD NO 220~221: 93μm; PAD NO 208~209: 68μm; PAD NO 221~243, 244~247: 70μm PAD NO 243~244: 145μm

Bump Size:

PAD NO 1~156, 174~185, 248~259: 30(x) μm × 80(y) μm

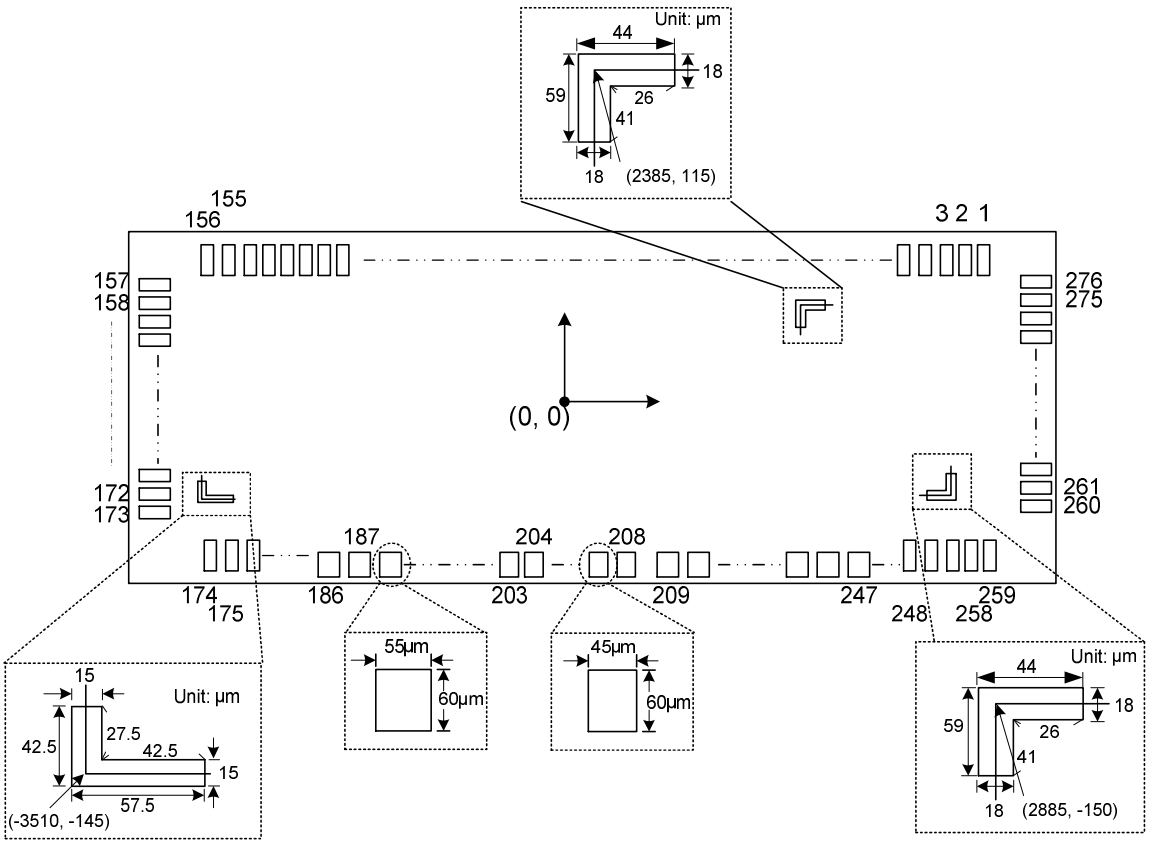
PAD NO 157~173, 260~276: 80(x) μm × 30(y) μm

PAD NO 186~202, 209~247: 55(x) μm × 60(y) μm

PAD NO 203~208: 45(x) μm × 60(y) μm

Bump Height: 17 μm

Chip Thickness: 480 μm



n PAD CENTER COORDINATES (49 duty)

Pad No.	Pin Name	X	Y
001	Reserved	3487	379
002	Reserved	3442	379
003	Reserved	3397	379
004	Reserved	3352	379
005	Reserved	3307	379
006	Reserved	3262	379
007	Reserved	3217	379
008	Reserved	3172	379
009	Reserved	3127	379
010	Reserved	3082	379
011	Reserved	3037	379
012	Reserved	2992	379
013	SEG[131]	2947	379
014	SEG[130]	2902	379
015	SEG[129]	2857	379
016	SEG[128]	2812	379
017	SEG[127]	2767	379
018	SEG[126]	2722	379
019	SEG[125]	2677	379
020	SEG[124]	2632	379
021	SEG[123]	2587	379
022	SEG[122]	2542	379
023	SEG[121]	2497	379
024	SEG[120]	2452	379
025	SEG[119]	2407	379
026	SEG[118]	2362	379
027	SEG[117]	2317	379
028	SEG[116]	2272	379
029	SEG[115]	2227	379
030	SEG[114]	2182	379
031	SEG[113]	2137	379
032	SEG[112]	2092	379
033	SEG[111]	2047	379
034	SEG[110]	2002	379
035	SEG[109]	1957	379

Pad No.	Pin Name	X	Y
036	SEG[108]	1912	379
037	SEG[107]	1867	379
038	SEG[106]	1822	379
039	SEG[105]	1777	379
040	SEG[104]	1732	379
041	SEG[103]	1687	379
042	SEG[102]	1642	379
043	SEG[101]	1597	379
044	SEG[100]	1552	379
045	SEG[99]	1507	379
046	SEG[98]	1462	379
047	SEG[97]	1417	379
048	SEG[96]	1372	379
049	SEG[95]	1327	379
050	SEG[94]	1282	379
051	SEG[93]	1237	379
052	SEG[92]	1192	379
053	SEG[91]	1147	379
054	SEG[90]	1102	379
055	SEG[89]	1057	379
056	SEG[88]	1012	379
057	SEG[87]	967	379
058	SEG[86]	922	379
059	SEG[85]	877	379
060	SEG[84]	832	379
061	SEG[83]	787	379
062	SEG[82]	742	379
063	SEG[81]	697	379
064	SEG[80]	652	379
065	SEG[79]	607	379
066	SEG[78]	562	379
067	SEG[77]	517	379
068	SEG[76]	472	379
069	SEG[75]	427	379
070	SEG[74]	382	379

Pad No.	Pin Name	X	Y
071	SEG[73]	337	379
072	SEG[72]	292	379
073	SEG[71]	247	379
074	SEG[70]	202	379
075	SEG[69]	157	379
076	SEG[68]	112	379
077	SEG[67]	67	379
078	SEG[66]	22	379
079	SEG[65]	-23	379
080	SEG[64]	-68	379
081	SEG[63]	-113	379
082	SEG[62]	-158	379
083	SEG[61]	-203	379
084	SEG[60]	-248	379
085	SEG[59]	-293	379
086	SEG[58]	-338	379
087	SEG[57]	-383	379
088	SEG[56]	-428	379
089	SEG[55]	-473	379
090	SEG[54]	-518	379
091	SEG[53]	-563	379
092	SEG[52]	-608	379
093	SEG[51]	-653	379
094	SEG[50]	-698	379
095	SEG[49]	-743	379
096	SEG[48]	-788	379
097	SEG[47]	-833	379
098	SEG[46]	-878	379
099	SEG[45]	-923	379
100	SEG[44]	-968	379
101	SEG[43]	-1013	379
102	SEG[42]	-1058	379
103	SEG[41]	-1103	379
104	SEG[40]	-1148	379
105	SEG[39]	-1193	379
106	SEG[38]	-1238	379

Pad No.	Pin Name	X	Y
107	SEG[37]	-1283	379
108	SEG[36]	-1328	379
109	SEG[35]	-1373	379
110	SEG[34]	-1418	379
111	SEG[33]	-1463	379
112	SEG[32]	-1508	379
113	SEG[31]	-1553	379
114	SEG[30]	-1598	379
115	SEG[29]	-1643	379
116	SEG[28]	-1688	379
117	SEG[27]	-1733	379
118	SEG[26]	-1778	379
119	SEG[25]	-1823	379
120	SEG[24]	-1868	379
121	SEG[23]	-1913	379
122	SEG[22]	-1958	379
123	SEG[21]	-2003	379
124	SEG[20]	-2048	379
125	SEG[19]	-2093	379
126	SEG[18]	-2138	379
127	SEG[17]	-2183	379
128	SEG[16]	-2228	379
129	SEG[15]	-2273	379
130	SEG[14]	-2318	379
131	SEG[13]	-2363	379
132	SEG[12]	-2408	379
133	SEG[11]	-2453	379
134	SEG[10]	-2498	379
135	SEG[9]	-2543	379
136	SEG[8]	-2588	379
137	SEG[7]	-2633	379
138	SEG[6]	-2678	379
139	SEG[5]	-2723	379
140	SEG[4]	-2768	379
141	SEG[3]	-2813	379
142	SEG[2]	-2858	379

Pad No.	Pin Name	X	Y
143	SEG[1]	-2903	379
144	SEG[0]	-2948	379
145	COMS1	-2993	379
146	COM[0]	-3038	379
147	COM[1]	-3083	379
148	COM[2]	-3128	379
149	COM[3]	-3173	379
150	COM[4]	-3218	379
151	COM[5]	-3263	379
152	COM[6]	-3308	379
153	COM[7]	-3353	379
154	COM[8]	-3398	379
155	COM[9]	-3443	379
156	COM[10]	-3488	379
157	COM[11]	-3743	358
158	COM[12]	-3743	313
159	COM[13]	-3743	268
160	COM[14]	-3743	223
161	COM[15]	-3743	178
162	COM[16]	-3743	133
163	COM[17]	-3743	88
164	COM[18]	-3743	43
165	COM[19]	-3743	-2
166	COM[20]	-3743	-47
167	COM[21]	-3743	-92
168	COM[22]	-3743	-137
169	COM[23]	-3743	-182
170	Reserved	-3743	-227
171	Reserved	-3743	-272
172	Reserved	-3743	-317
173	Reserved	-3743	-362
174	Reserved	-3488	-379
175	Reserved	-3443	-379
176	Reserved	-3398	-379
177	Reserved	-3353	-379
178	Reserved	-3308	-379

Pad No.	Pin Name	X	Y
179	Reserved	-3263	-379
180	Reserved	-3218	-379
181	Reserved	-3173	-379
182	Reserved	-3128	-379
183	Reserved	-3083	-379
184	Reserved	-3038	-379
185	Reserved	-2993	-379
186	SYNC	-2417	-389
187	CL	-2298	-389
188	DOF	-2225	-389
189	CSB	-2106	-389
190	VSS	-2033	-389
191	RESB	-1899	-389
192	A0	-1780	-389
193	/WR(R/W)	-1707	-389
194	/RD(E)	-1588	-389
195	D0	-1515	-389
196	D1	-1396	-389
197	D2	-1323	-389
198	D3	-1204	-389
199	D4	-1131	-389
200	D5	-1012	-389
201	D6	-939	-389
202	D7	-820	-389
203	T5	-743	-389
204	T4	-568	-389
205	T3	-493	-389
206	T2	-318	-389
207	T1	-243	-389
208	T0	-93	-389
209	VSS	-25	-389
210	VSS	48	-389
211	VSS	121	-389
212	MS	223	-389
213	MODE0	296	-389
214	MODE1	415	-389

Pad No.	Pin Name	X	Y
215	PS0	488	-389
216	PS1	607	-389
217	PS2	680	-389
218	V_{DD1}	782	-389
219	V_{DD1}	855	-389
220	V_{DD1}	928	-389
221	V_{DD2}	1021	-389
222	V_{DD2}	1091	-389
223	V_{OUT}	1161	-389
224	V_{OUT}	1231	-389
225	V_{OUT}	1301	-389
226	CAP3N	1371	-389
227	CAP3N	1441	-389
228	CAP3P	1511	-389
229	CAP3P	1581	-389
230	CAP5P	1651	-389
231	CAP5P	1721	-389
232	CAP1N	1791	-389
233	CAP1N	1861	-389
234	CAP1P	1931	-389
235	CAP1P	2001	-389
236	CAP2P	2071	-389
237	CAP2P	2141	-389
238	CAP2N	2211	-389
239	CAP2N	2281	-389
240	CAP4P	2351	-389
241	CAP4P	2421	-389
242	VRS	2491	-389
243	V0	2561	-389
244	V1	2706	-389
245	V2	2776	-389

Pad No.	Pin Name	X	Y
246	V3	2846	-389
247	V4	2916	-389
248	COMS2	2992	-379
249	COM[47]	3037	-379
250	COM[46]	3082	-379
251	COM[45]	3127	-379
252	COM[44]	3172	-379
253	COM[43]	3217	-379
254	COM[42]	3262	-379
255	COM[41]	3307	-379
256	COM[40]	3352	-379
257	COM[39]	3397	-379
258	COM[38]	3442	-379
259	COM[37]	3487	-379
260	COM[36]	3743	-362
261	COM[35]	3743	-317
262	COM[34]	3743	-272
263	COM[33]	3743	-227
264	COM[32]	3743	-182
265	COM[31]	3743	-137
266	COM[30]	3743	-92
267	COM[29]	3743	-47
268	COM[28]	3743	-2
269	COM[27]	3743	43
270	COM[26]	3743	88
271	COM[25]	3743	133
272	COM[24]	3743	178
273	Reserved	3743	223
274	Reserved	3743	268
275	Reserved	3743	313
276	Reserved	3743	358

n PAD CENTER COORDINATES (65 duty)

Pad No.	Pin Name	X	Y
001	COM[35]	3487	379
002	COM[34]	3442	379
003	COM[33]	3397	379
004	COM[32]	3352	379
005	Reserved	3307	379
006	Reserved	3262	379
007	Reserved	3217	379
008	Reserved	3172	379
009	Reserved	3127	379
010	Reserved	3082	379
011	Reserved	3037	379
012	Reserved	2992	379
013	SEG[131]	2947	379
014	SEG[130]	2902	379
015	SEG[129]	2857	379
016	SEG[128]	2812	379
017	SEG[127]	2767	379
018	SEG[126]	2722	379
019	SEG[125]	2677	379
020	SEG[124]	2632	379
021	SEG[123]	2587	379
022	SEG[122]	2542	379
023	SEG[121]	2497	379
024	SEG[120]	2452	379
025	SEG[119]	2407	379
026	SEG[118]	2362	379
027	SEG[117]	2317	379
028	SEG[116]	2272	379
029	SEG[115]	2227	379
030	SEG[114]	2182	379
031	SEG[113]	2137	379
032	SEG[112]	2092	379
033	SEG[111]	2047	379
034	SEG[110]	2002	379
035	SEG[109]	1957	379

Pad No.	Pin Name	X	Y
036	SEG[108]	1912	379
037	SEG[107]	1867	379
038	SEG[106]	1822	379
039	SEG[105]	1777	379
040	SEG[104]	1732	379
041	SEG[103]	1687	379
042	SEG[102]	1642	379
043	SEG[101]	1597	379
044	SEG[100]	1552	379
045	SEG[99]	1507	379
046	SEG[98]	1462	379
047	SEG[97]	1417	379
048	SEG[96]	1372	379
049	SEG[95]	1327	379
050	SEG[94]	1282	379
051	SEG[93]	1237	379
052	SEG[92]	1192	379
053	SEG[91]	1147	379
054	SEG[90]	1102	379
055	SEG[89]	1057	379
056	SEG[88]	1012	379
057	SEG[87]	967	379
058	SEG[86]	922	379
059	SEG[85]	877	379
060	SEG[84]	832	379
061	SEG[83]	787	379
062	SEG[82]	742	379
063	SEG[81]	697	379
064	SEG[80]	652	379
065	SEG[79]	607	379
066	SEG[78]	562	379
067	SEG[77]	517	379
068	SEG[76]	472	379
069	SEG[75]	427	379
070	SEG[74]	382	379

Pad No.	Pin Name	X	Y
071	SEG[73]	337	379
072	SEG[72]	292	379
073	SEG[71]	247	379
074	SEG[70]	202	379
075	SEG[69]	157	379
076	SEG[68]	112	379
077	SEG[67]	67	379
078	SEG[66]	22	379
079	SEG[65]	-23	379
080	SEG[64]	-68	379
081	SEG[63]	-113	379
082	SEG[62]	-158	379
083	SEG[61]	-203	379
084	SEG[60]	-248	379
085	SEG[59]	-293	379
086	SEG[58]	-338	379
087	SEG[57]	-383	379
088	SEG[56]	-428	379
089	SEG[55]	-473	379
090	SEG[54]	-518	379
091	SEG[53]	-563	379
092	SEG[52]	-608	379
093	SEG[51]	-653	379
094	SEG[50]	-698	379
095	SEG[49]	-743	379
096	SEG[48]	-788	379
097	SEG[47]	-833	379
098	SEG[46]	-878	379
099	SEG[45]	-923	379
100	SEG[44]	-968	379
101	SEG[43]	-1013	379
102	SEG[42]	-1058	379
103	SEG[41]	-1103	379
104	SEG[40]	-1148	379
105	SEG[39]	-1193	379
106	SEG[38]	-1238	379

Pad No.	Pin Name	X	Y
107	SEG[37]	-1283	379
108	SEG[36]	-1328	379
109	SEG[35]	-1373	379
110	SEG[34]	-1418	379
111	SEG[33]	-1463	379
112	SEG[32]	-1508	379
113	SEG[31]	-1553	379
114	SEG[30]	-1598	379
115	SEG[29]	-1643	379
116	SEG[28]	-1688	379
117	SEG[27]	-1733	379
118	SEG[26]	-1778	379
119	SEG[25]	-1823	379
120	SEG[24]	-1868	379
121	SEG[23]	-1913	379
122	SEG[22]	-1958	379
123	SEG[21]	-2003	379
124	SEG[20]	-2048	379
125	SEG[19]	-2093	379
126	SEG[18]	-2138	379
127	SEG[17]	-2183	379
128	SEG[16]	-2228	379
129	SEG[15]	-2273	379
130	SEG[14]	-2318	379
131	SEG[13]	-2363	379
132	SEG[12]	-2408	379
133	SEG[11]	-2453	379
134	SEG[10]	-2498	379
135	SEG[9]	-2543	379
136	SEG[8]	-2588	379
137	SEG[7]	-2633	379
138	SEG[6]	-2678	379
139	SEG[5]	-2723	379
140	SEG[4]	-2768	379
141	SEG[3]	-2813	379
142	SEG[2]	-2858	379

Pad No.	Pin Name	X	Y
143	SEG[1]	-2903	379
144	SEG[0]	-2948	379
145	COMS1	-2993	379
146	COM[0]	-3038	379
147	COM[1]	-3083	379
148	COM[2]	-3128	379
149	COM[3]	-3173	379
150	COM[4]	-3218	379
151	COM[5]	-3263	379
152	COM[6]	-3308	379
153	COM[7]	-3353	379
154	COM[8]	-3398	379
155	COM[9]	-3443	379
156	COM[10]	-3488	379
157	COM[11]	-3743	358
158	COM[12]	-3743	313
159	COM[13]	-3743	268
160	COM[14]	-3743	223
161	COM[15]	-3743	178
162	COM[16]	-3743	133
163	COM[17]	-3743	88
164	COM[18]	-3743	43
165	COM[19]	-3743	-2
166	COM[20]	-3743	-47
167	COM[21]	-3743	-92
168	COM[22]	-3743	-137
169	COM[23]	-3743	-182
170	COM[24]	-3743	-227
171	COM[25]	-3743	-272
172	COM[26]	-3743	-317
173	COM[27]	-3743	-362
174	COM[28]	-3488	-379
175	COM[29]	-3443	-379
176	COM[30]	-3398	-379
177	COM[31]	-3353	-379
178	Reserved	-3308	-379

Pad No.	Pin Name	X	Y
179	Reserved	-3263	-379
180	Reserved	-3218	-379
181	Reserved	-3173	-379
182	Reserved	-3128	-379
183	Reserved	-3083	-379
184	Reserved	-3038	-379
185	Reserved	-2993	-379
186	SYNC	-2417	-389
187	CL	-2298	-389
188	DOF	-2225	-389
189	CSB	-2106	-389
190	VSS	-2033	-389
191	RESB	-1899	-389
192	A0	-1780	-389
193	/WR(R/W)	-1707	-389
194	/RD(E)	-1588	-389
195	D0	-1515	-389
196	D1	-1396	-389
197	D2	-1323	-389
198	D3	-1204	-389
199	D4	-1131	-389
200	D5	-1012	-389
201	D6	-939	-389
202	D7	-820	-389
203	T5	-743	-389
204	T4	-568	-389
205	T3	-493	-389
206	T2	-318	-389
207	T1	-243	-389
208	T0	-93	-389
209	VSS	-25	-389
210	VSS	48	-389
211	VSS	121	-389
212	MS	223	-389
213	MODE0	296	-389
214	MODE1	415	-389

Pad No.	Pin Name	X	Y
215	PS0	488	-389
216	PS1	607	-389
217	PS2	680	-389
218	V_{DD1}	782	-389
219	V_{DD1}	855	-389
220	V_{DD1}	928	-389
221	V_{DD2}	1021	-389
222	V_{DD2}	1091	-389
223	V_{OUT}	1161	-389
224	V_{OUT}	1231	-389
225	V_{OUT}	1301	-389
226	CAP3N	1371	-389
227	CAP3N	1441	-389
228	CAP3P	1511	-389
229	CAP3P	1581	-389
230	CAP5P	1651	-389
231	CAP5P	1721	-389
232	CAP1N	1791	-389
233	CAP1N	1861	-389
234	CAP1P	1931	-389
235	CAP1P	2001	-389
236	CAP2P	2071	-389
237	CAP2P	2141	-389
238	CAP2N	2211	-389
239	CAP2N	2281	-389
240	CAP4P	2351	-389
241	CAP4P	2421	-389
242	VRS	2491	-389
243	V0	2561	-389
244	V1	2706	-389
245	V2	2776	-389

Pad No.	Pin Name	X	Y
246	V3	2846	-389
247	V4	2916	-389
248	COMS2	2992	-379
249	COM[63]	3037	-379
250	COM[62]	3082	-379
251	COM[61]	3127	-379
252	COM[60]	3172	-379
253	COM[59]	3217	-379
254	COM[58]	3262	-379
255	COM[57]	3307	-379
256	COM[56]	3352	-379
257	COM[55]	3397	-379
258	COM[54]	3442	-379
259	COM[53]	3487	-379
260	COM[52]	3743	-362
261	COM[51]	3743	-317
262	COM[50]	3743	-272
263	COM[49]	3743	-227
264	COM[48]	3743	-182
265	COM[47]	3743	-137
266	COM[46]	3743	-92
267	COM[45]	3743	-47
268	COM[44]	3743	-2
269	COM[43]	3743	43
270	COM[42]	3743	88
271	COM[41]	3743	133
272	COM[40]	3743	178
273	COM[39]	3743	223
274	COM[38]	3743	268
275	COM[37]	3743	313
276	COM[36]	3743	358

n PAD CENTER COORDINATES (81 duty)

Pad No.	Pin Name	X	Y
001	COM[51]	3487	379
002	COM[50]	3442	379
003	COM[49]	3397	379
004	COM[48]	3352	379
005	COM[47]	3307	379
006	COM[46]	3262	379
007	COM[45]	3217	379
008	COM[44]	3172	379
009	COM[43]	3127	379
010	COM[42]	3082	379
011	COM[41]	3037	379
012	COM[40]	2992	379
013	SEG[131]	2947	379
014	SEG[130]	2902	379
015	SEG[129]	2857	379
016	SEG[128]	2812	379
017	SEG[127]	2767	379
018	SEG[126]	2722	379
019	SEG[125]	2677	379
020	SEG[124]	2632	379
021	SEG[123]	2587	379
022	SEG[122]	2542	379
023	SEG[121]	2497	379
024	SEG[120]	2452	379
025	SEG[119]	2407	379
026	SEG[118]	2362	379
027	SEG[117]	2317	379
028	SEG[116]	2272	379
029	SEG[115]	2227	379
030	SEG[114]	2182	379
031	SEG[113]	2137	379
032	SEG[112]	2092	379
033	SEG[111]	2047	379
034	SEG[110]	2002	379
035	SEG[109]	1957	379

Pad No.	Pin Name	X	Y
036	SEG[108]	1912	379
037	SEG[107]	1867	379
038	SEG[106]	1822	379
039	SEG[105]	1777	379
040	SEG[104]	1732	379
041	SEG[103]	1687	379
042	SEG[102]	1642	379
043	SEG[101]	1597	379
044	SEG[100]	1552	379
045	SEG[99]	1507	379
046	SEG[98]	1462	379
047	SEG[97]	1417	379
048	SEG[96]	1372	379
049	SEG[95]	1327	379
050	SEG[94]	1282	379
051	SEG[93]	1237	379
052	SEG[92]	1192	379
053	SEG[91]	1147	379
054	SEG[90]	1102	379
055	SEG[89]	1057	379
056	SEG[88]	1012	379
057	SEG[87]	967	379
058	SEG[86]	922	379
059	SEG[85]	877	379
060	SEG[84]	832	379
061	SEG[83]	787	379
062	SEG[82]	742	379
063	SEG[81]	697	379
064	SEG[80]	652	379
065	SEG[79]	607	379
066	SEG[78]	562	379
067	SEG[77]	517	379
068	SEG[76]	472	379
069	SEG[75]	427	379
070	SEG[74]	382	379

Pad No.	Pin Name	X	Y
071	SEG[73]	337	379
072	SEG[72]	292	379
073	SEG[71]	247	379
074	SEG[70]	202	379
075	SEG[69]	157	379
076	SEG[68]	112	379
077	SEG[67]	67	379
078	SEG[66]	22	379
079	SEG[65]	-23	379
080	SEG[64]	-68	379
081	SEG[63]	-113	379
082	SEG[62]	-158	379
083	SEG[61]	-203	379
084	SEG[60]	-248	379
085	SEG[59]	-293	379
086	SEG[58]	-338	379
087	SEG[57]	-383	379
088	SEG[56]	-428	379
089	SEG[55]	-473	379
090	SEG[54]	-518	379
091	SEG[53]	-563	379
092	SEG[52]	-608	379
093	SEG[51]	-653	379
094	SEG[50]	-698	379
095	SEG[49]	-743	379
096	SEG[48]	-788	379
097	SEG[47]	-833	379
098	SEG[46]	-878	379
099	SEG[45]	-923	379
100	SEG[44]	-968	379
101	SEG[43]	-1013	379
102	SEG[42]	-1058	379
103	SEG[41]	-1103	379
104	SEG[40]	-1148	379
105	SEG[39]	-1193	379
106	SEG[38]	-1238	379

Pad No.	Pin Name	X	Y
107	SEG[37]	-1283	379
108	SEG[36]	-1328	379
109	SEG[35]	-1373	379
110	SEG[34]	-1418	379
111	SEG[33]	-1463	379
112	SEG[32]	-1508	379
113	SEG[31]	-1553	379
114	SEG[30]	-1598	379
115	SEG[29]	-1643	379
116	SEG[28]	-1688	379
117	SEG[27]	-1733	379
118	SEG[26]	-1778	379
119	SEG[25]	-1823	379
120	SEG[24]	-1868	379
121	SEG[23]	-1913	379
122	SEG[22]	-1958	379
123	SEG[21]	-2003	379
124	SEG[20]	-2048	379
125	SEG[19]	-2093	379
126	SEG[18]	-2138	379
127	SEG[17]	-2183	379
128	SEG[16]	-2228	379
129	SEG[15]	-2273	379
130	SEG[14]	-2318	379
131	SEG[13]	-2363	379
132	SEG[12]	-2408	379
133	SEG[11]	-2453	379
134	SEG[10]	-2498	379
135	SEG[9]	-2543	379
136	SEG[8]	-2588	379
137	SEG[7]	-2633	379
138	SEG[6]	-2678	379
139	SEG[5]	-2723	379
140	SEG[4]	-2768	379
141	SEG[3]	-2813	379
142	SEG[2]	-2858	379

Pad No.	Pin Name	X	Y
143	SEG[1]	-2903	379
144	SEG[0]	-2948	379
145	COMS1	-2993	379
146	COM[0]	-3038	379
147	COM[1]	-3083	379
148	COM[2]	-3128	379
149	COM[3]	-3173	379
150	COM[4]	-3218	379
151	COM[5]	-3263	379
152	COM[6]	-3308	379
153	COM[7]	-3353	379
154	COM[8]	-3398	379
155	COM[9]	-3443	379
156	COM[10]	-3488	379
157	COM[11]	-3743	358
158	COM[12]	-3743	313
159	COM[13]	-3743	268
160	COM[14]	-3743	223
161	COM[15]	-3743	178
162	COM[16]	-3743	133
163	COM[17]	-3743	88
164	COM[18]	-3743	43
165	COM[19]	-3743	-2
166	COM[20]	-3743	-47
167	COM[21]	-3743	-92
168	COM[22]	-3743	-137
169	COM[23]	-3743	-182
170	COM[24]	-3743	-227
171	COM[25]	-3743	-272
172	COM[26]	-3743	-317
173	COM[27]	-3743	-362
174	COM[28]	-3488	-379
175	COM[29]	-3443	-379
176	COM[30]	-3398	-379
177	COM[31]	-3353	-379
178	COM[32]	-3308	-379

Pad No.	Pin Name	X	Y
179	COM[33]	-3263	-379
180	COM[34]	-3218	-379
181	COM[35]	-3173	-379
182	COM[36]	-3128	-379
183	COM[37]	-3083	-379
184	COM[38]	-3038	-379
185	COM[39]	-2993	-379
186	SYNC	-2417	-389
187	CL	-2298	-389
188	DOF	-2225	-389
189	CSB	-2106	-389
190	VSS	-2033	-389
191	RESB	-1899	-389
192	A0	-1780	-389
193	/WR(R/W)	-1707	-389
194	/RD(E)	-1588	-389
195	D0	-1515	-389
196	D1	-1396	-389
197	D2	-1323	-389
198	D3	-1204	-389
199	D4	-1131	-389
200	D5	-1012	-389
201	D6	-939	-389
202	D7	-820	-389
203	T5	-743	-389
204	T4	-568	-389
205	T3	-493	-389
206	T2	-318	-389
207	T1	-243	-389
208	T0	-93	-389
209	VSS	-25	-389
210	VSS	48	-389
211	VSS	121	-389
212	MS	223	-389
213	MODE0	296	-389
214	MODE1	415	-389

Pad No.	Pin Name	X	Y
215	PS0	488	-389
216	PS1	607	-389
217	PS2	680	-389
218	V_{DD1}	782	-389
219	V_{DD1}	855	-389
220	V_{DD1}	928	-389
221	V_{DD2}	1021	-389
222	V_{DD2}	1091	-389
223	V_{OUT}	1161	-389
224	V_{OUT}	1231	-389
225	V_{OUT}	1301	-389
226	CAP3N	1371	-389
227	CAP3N	1441	-389
228	CAP3P	1511	-389
229	CAP3P	1581	-389
230	CAP5P	1651	-389
231	CAP5P	1721	-389
232	CAP1N	1791	-389
233	CAP1N	1861	-389
234	CAP1P	1931	-389
235	CAP1P	2001	-389
236	CAP2P	2071	-389
237	CAP2P	2141	-389
238	CAP2N	2211	-389
239	CAP2N	2281	-389
240	CAP4P	2351	-389
241	CAP4P	2421	-389
242	VRS	2491	-389
243	V0	2561	-389
244	V1	2706	-389
245	V2	2776	-389
246	V3	2846	-389
247	V4	2916	-389
248	COMS2	2992	-379
249	COM[79]	3037	-379
250	COM[78]	3082	-379

Pad No.	Pin Name	X	Y
251	COM[77]	3127	-379
252	COM[76]	3172	-379
253	COM[75]	3217	-379
254	COM[74]	3262	-379
255	COM[73]	3307	-379
256	COM[72]	3352	-379
257	COM[71]	3397	-379
258	COM[70]	3442	-379
259	COM[69]	3487	-379
260	COM[68]	3743	-362
261	COM[67]	3743	-317
262	COM[66]	3743	-272
263	COM[65]	3743	-227
264	COM[64]	3743	-182
265	COM[63]	3743	-137
266	COM[62]	3743	-92
267	COM[61]	3743	-47
268	COM[60]	3743	-2
269	COM[59]	3743	43
270	COM[58]	3743	88
271	COM[57]	3743	133
272	COM[56]	3743	178
273	COM[55]	3743	223
274	COM[54]	3743	268
275	COM[53]	3743	313
276	COM[52]	3743	358

n BLOCK DIAGRAM

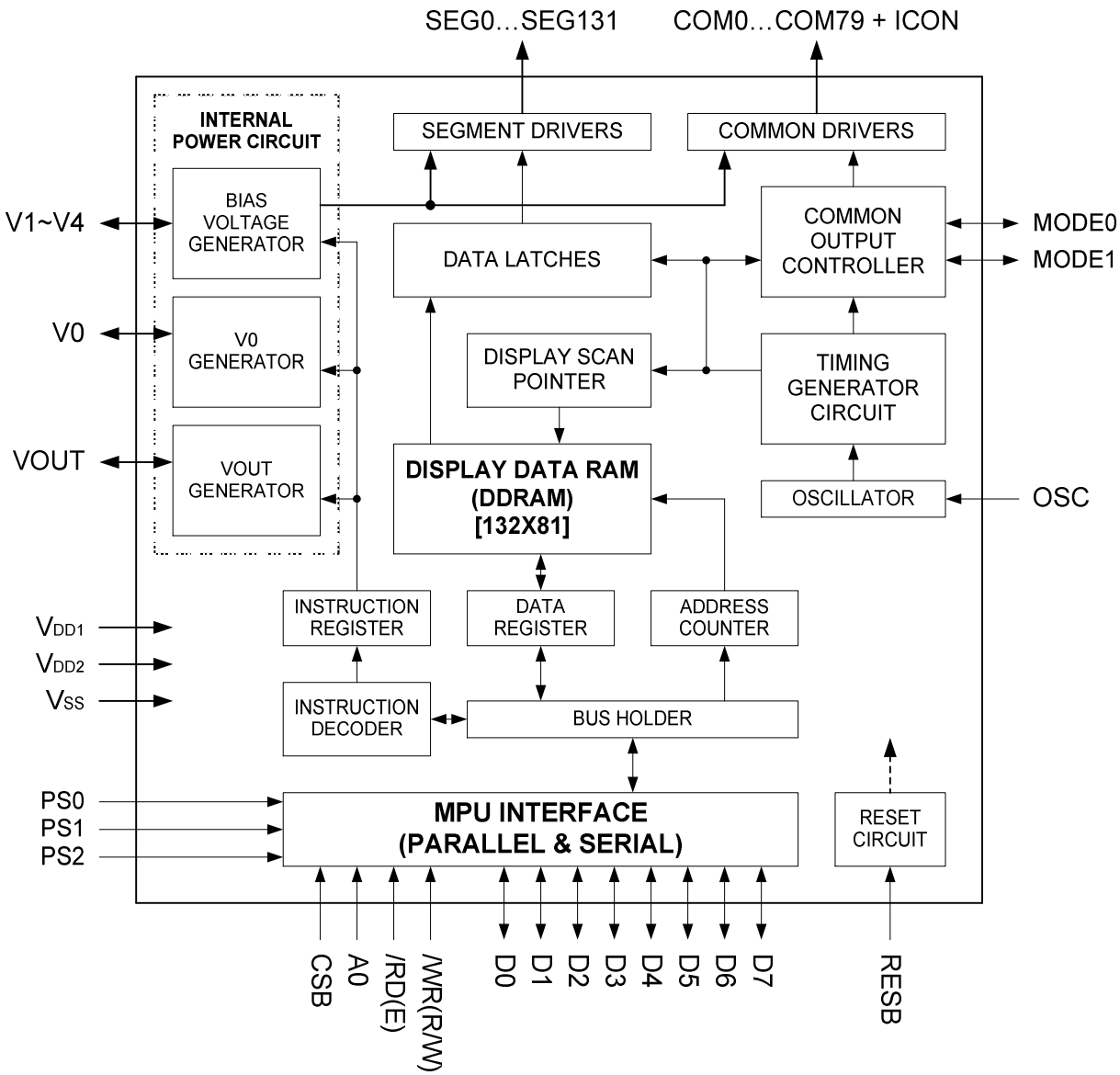


Figure 1 Block diagram

n PIN DESCRIPTIONS

<table>
<tr><td colspan="4">LCD driver outputs</td></tr>
<tr><td>Pin Name</td><td>Type</td><td>Description</td><td>No. of Pins</td></tr>
<tr><td>SEG0 to
SEG131</td><td>O</td><td>LCD segment driver outputs
The display data and frame signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">Frame</td><td colspan="2">Segment Driver Output</td></tr>
<tr><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>1</td><td>Negative</td><td>V0</td><td>V2</td></tr>
<tr><td>1</td><td>Positive</td><td>V_{SS}</td><td>V3</td></tr>
<tr><td>0</td><td>Negative</td><td>V2</td><td>V0</td></tr>
<tr><td>0</td><td>Positive</td><td>V3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Display OFF,
Power save mode</td><td>V_{SS}</td><td>V_{SS}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0 to
COM79</td><td>O</td><td>LCD column driver outputs
The scan signal and frame signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">Frame</td><td colspan="2">Common Driver Output</td></tr>
<tr><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>1</td><td>Negative</td><td colspan="2">V_{SS}</td></tr>
<tr><td>1</td><td>Positive</td><td colspan="2">V0</td></tr>
<tr><td>0</td><td>Negative</td><td colspan="2">V1</td></tr>
<tr><td>0</td><td>Positive</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Display OFF,
Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>80</td></tr>
<tr><td>COMS1
COMS2</td><td>O</td><td>Common output for the icons. COMS1 and COMS2 are identical.
The output signals of these pins are same. If not using, they should be left open.</td><td>2</td></tr>
<tr><td colspan="4">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>Pin Name</td><td>Type</td><td>Description</td><td>No. of Pins</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td>Microprocessor interface selection pins
<table>
<tr><td>PS2</td><td>PS1</td><td>PS0</td><td>Interface Mode</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8-bit 6800 parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4-line serial interface A mode</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4-line serial interface B mode</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>3-line (8 bit) serial interface A mode</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-line (8-bit) serial interface B mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3-line (9-bit) serial interface</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>I^2C serial interface</td></tr>
</table></td><td>3</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin
Microprocessor Interface is enabled only when CSB is "L".
When chip select is non-active (CSB=“H”), D[7:0] are high impedance.
CSB is not used in I^2C interface. Fix this pin to “H” by V_{DD1}.</td><td>1</td></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin
When RESB is “L”, initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the data bits are data or a command.
A0= “H” : Indicates that D[7:0] are display data.
A0= “L” : Indicates that D[7:0] are control data.
A0 is not used in 3-line SPI or I^2C interface. Fix this pin to “H” by V_{DD1}.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>/WR(R/W)</td><td>I</td><td>Read/Write execution control pin : (when PS[1:0]=L,L)
<table>
<tr><th>PS2</th><th>MPU type</th><th>/WR(R/W)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read
R/W=“L”: write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin.
The data on D0 to D7 are latched at the rising edge of the /WR signal.</td></tr>
</table>
This pin is not used in the serial interface. Fix to “H” by V_{DD1}.</td><td>1</td></tr>
<tr><td>/RD (E)</td><td>I</td><td>Read/Write execution control pin : (when PS[1:0]=L,L)
<table>
<tr><th>PS2</th><th>MPU Type</th><th>/RD (E)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Enable control input pin.
R/W=“H”: When E is “H”, D0 to D7 are in an output status.
R/W=“L”: The data on D0 to D7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, D0 to D7 are in an output status.</td></tr>
</table>
This pin is not used in the serial interface. Fix to “H” by V_{DD1}.</td><td>1</td></tr>
<tr><td>D[7:0]</td><td>I/O</td><td>When using parallel interface: 8-bit interface
This is an 8-bit bi-directional data bus that connected to the standard 8-bit microprocessor data bus.
When chip select pin (CSB) is not active, D7 to D0 are high impedance.

When using serial interface: 3-line or 4-line
D0: serial input clock (SCL).
D1 to D3: serial input data (SDA).
D4, D5, D6, D7: fix to “H” by V_{DD1}.
When chip select pin (CSB) is not active, D7 to D0 are high impedance.

When using I^2C interface (PS[2:0]="H")
D0: SCL, serial clock input.
D1: SDA_IN, serial input data.
D2 to D5: SDA_OUT, serial data acknowledge for the I^2C interface.
D6 and D7 are slave address bit 0 and 1 which can be set as 00 to 11.
<u>D1 to D5 must be connected together (SDA)</u>
Chip select pin (CSB) is not used and must be fixed to “H” by V_{DD1}.

By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^2C interface compatible. Separating acknowledge output from the serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledge-signal level and system cannot recognize this level as a valid logical “0” level. By splitting SDA_IN from SDA_OUT, the IC can be used in a mode which ignores the acknowledge-bit. For applications that check the acknowledge-bit, it is important to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level.</td><td>8</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>MODE[1:0]</td><td>I</td><td>Use this pin can select 1/49 duty, 1/65duty or 1/81 duty mode
<table>
<tr><td>Mode1</td><td>Mode0</td><td>Duty</td></tr>
<tr><td>0</td><td>0</td><td>1/49 duty</td></tr>
<tr><td>0</td><td>1</td><td>1/65 duty</td></tr>
<tr><td>1</td><td>0</td><td>---</td></tr>
<tr><td>1</td><td>1</td><td>1/81 duty</td></tr>
</table></td><td>1</td></tr>
<tr><td colspan="4">Power Supply Pins</td></tr>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>V_{SS}</td><td>Power</td><td>Ground.</td><td>9</td></tr>
<tr><td>V_{DD1}</td><td>Power</td><td>Digital Supply Voltage.
The 2 supply rails V_{DD1} and V_{DD2} could be connected together.
<u>If Digital Option pin is high, must be this level.</u></td><td>5</td></tr>
<tr><td>V_{DD2}</td><td>Power</td><td>Analog Supply Voltage.
The 2 supply rails V_{DD1} and V_{DD2} could be connected together.</td><td>4</td></tr>
<tr><td>V_{OUT}</td><td>Power</td><td>If using external voltage generator, the external supply voltage should connect to V_{OUT} pad as an external voltage input.
V_{OUT} must series one capacitor to V_{DD2}.</td><td>3</td></tr>
<tr><td>V0,
V1, V2, V3, V4</td><td>Power</td><td>This is a multi-level power supply for the liquid crystal operation.
$V_{OUT} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$</td><td>5</td></tr>
<tr><td>VRS</td><td>Power</td><td>Voltage Regulator reference level.
This pin must be left open.</td><td>1</td></tr>
<tr><td colspan="4">Test Pin</td></tr>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>T0~T5</td><td>Test</td><td>These pins are reserved for test only.</td><td>6</td></tr>
<tr><td>MS</td><td>I</td><td>Please fix this pin to “H” by VDD1.</td><td>1</td></tr>
<tr><td>SYNC
/DOF
CL</td><td>O</td><td>Please let these pads floating.</td><td>1
1
1</td></tr>
</table>

ITO Limitations

PIN Name	ITO Resistance
T0~5, SYNC, /DOF, CL	Floating
V_{DD1}, V_{DD2}, V_{SS}, V_{OUT}	<100Ω
V0, V1, V2, V3, V4, CAP1P, CAP1N, CAP2P, CAP2N , CAP3P, CAP3N, CAP4P, CAP5P	<200Ω
D[5:1] (if using I^2C interface mode)	<300Ω
CSB, E, R/W, A0, D[7:0]	<1KΩ
PS[2:0], MODE[1:0], MS	< 5KΩ
RESB	<10KΩ

Note:

1. The option setting to be “H” should connect to VDD1.
2. The option setting to be “L” should connect to VSS1.

n FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

CSB pin is used as chip-select input. ST7588T can interface with an MPU when CSB is "L". When CSB is “H”, the pins of A0, /RD (E), and /WR(R/W) with any combination will be ignored and D[7:0] are high impedance. In 3-line and 4-line serial interfaces, the internal shift-register and bit-counter are reset when CSB is “H”.

Interface Selection

ST7588T has eight types of interface for all kinds of MPU (6 kinds of serial interface and 2 kinds of parallel interface). The selection among these interfaces uses PS[2:0] pins as shown in Table 1.

Table 1 Parallel / Serial Interface Mode

Type	PS2	PS1	PS0	Interface mode
Parallel	0	0	0	8bit 8080-series MPU mode
	1	0	0	8 bit 6800-series MPU mode
Serial	0	1	0	4-line serial interface A mode
	1	1	0	4-line serial interface B mode
	0	0	1	3-line (8 bit) serial interface A mode
	1	0	1	3-line (8-bit) serial interface B mode
	0	1	1	3-line (9-bit) serial interface
	1	1	1	I^2C serial interface

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS0 as shown in Table 2. The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

PS2	CSB	A0	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CSB	A0	E	RW	DB0 to DB7	6800-series
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: In 6800-series interface mode, fixing E_RD pin at “H” can use CSB as enable signal instead. In this case, the interface data is latched at the rising edge of CSB and the access type of this transfer is determined by signals at A0 and RW_WR as defined in 6800-series mode.

Serial Interface

4-Line SPI

When the ST7588T is active (CSB=”L”), serial data (DB1~3) and serial clock (DB0) inputs are enabled. While not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either by software or the Register Select (A0) Pin. When the A0 pin is used, data is display data when A0 is high and is command data when A0 is low. When A0 is not used, the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data Direction command (11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sent, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

(1) 4-Line SPI A Mode (PS0 = "L", PS1 = "H", PS2 = "L")

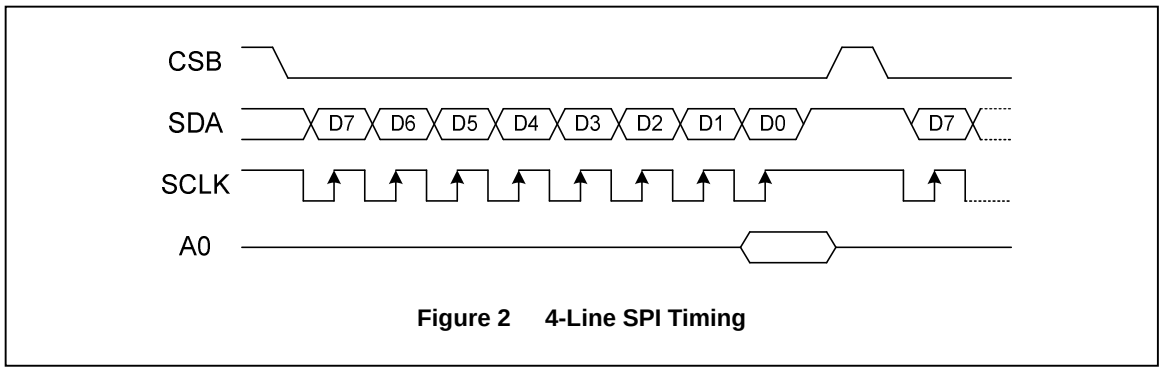


Figure 2 4-Line SPI Timing

(2) 4-Line SPI B Mode (PS0 = "L", PS1 = "H", PS2 = "H")

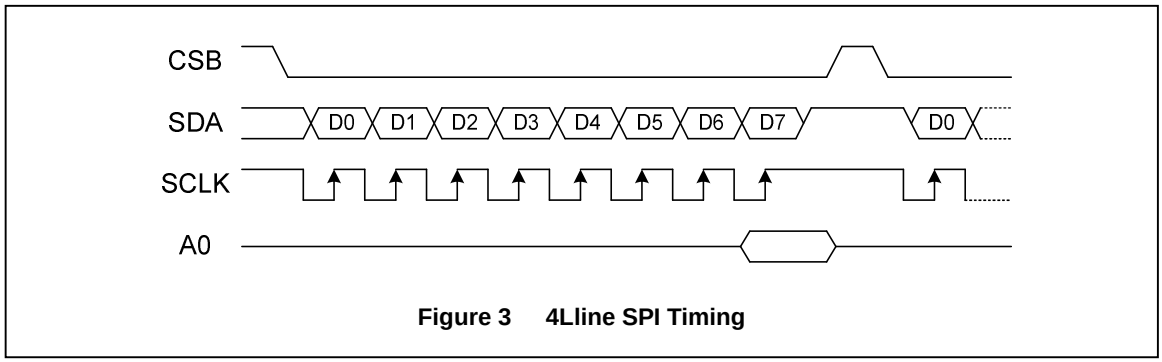
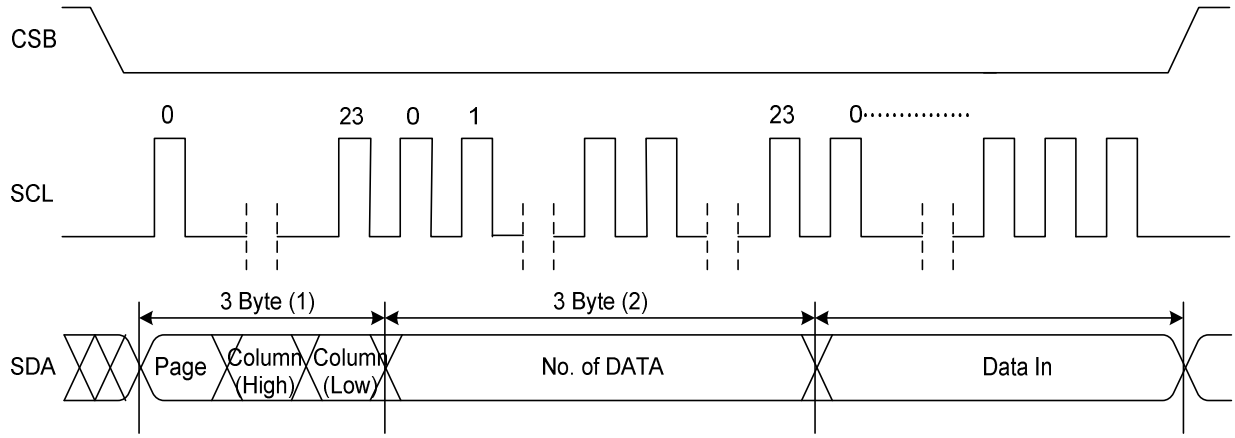


Figure 3 4Lline SPI Timing

3-Line SPI

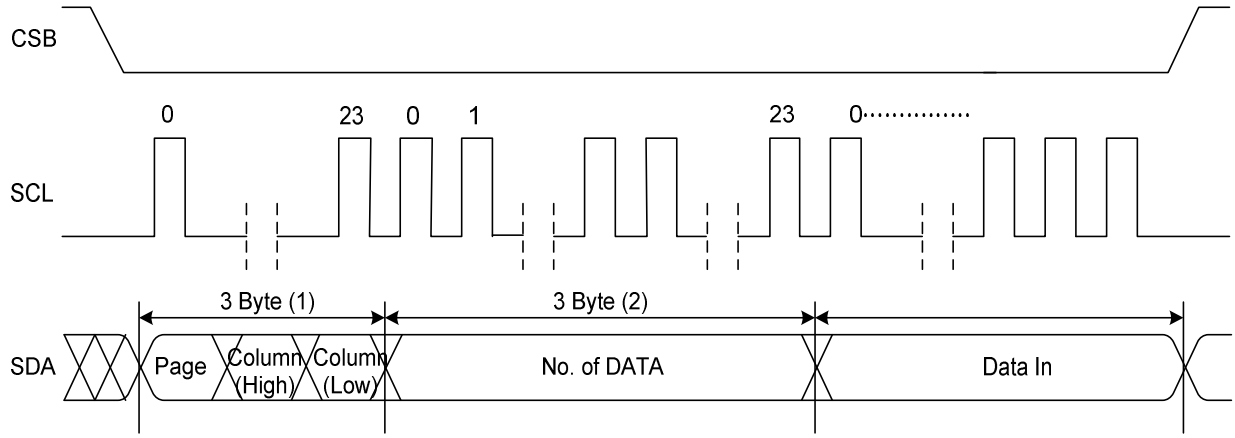
(1) 3-Line (8 bit) SPI

In this mode, the default transfer type is command. Two kinds of parameters must be set before write data: start addresses and data length. The flow to write data is: (1) Set start addresses, (2) Set data length and (3) Transfer data. Each bit is latched at the rising edge of SCL. The column address pointer is automatically increased by 1 after receiving 1 byte data.



Flow	Instruction	Bit Order (Left --> Right)							
1	Set Page Address	0	1	0	0	Y3	Y2	Y1	Y0
	Set Column Address (H)	1	1	1	1	X7	X6	X5	X4
	Set Column Address (L)	1	1	1	0	X3	X2	X1	X0
2	Set No. of Data Bytes (H)	0	1	1	1	0	DA10	DA9	DA8
	Set No. of Data Bytes (M)	0	1	1	0	DA7	DA6	DA5	DA4
	Set No. of Data Bytes (L) & Start	0	1	0	1	DA3	DA2	DA1	DA0
3	Transfer Data bytes								

Figure 4 3-line (8 bit) SPI A mode Timing (A0 is not used)



Flow	Instruction	Bit Order (Left --> Right)							
1	Set Page Address	Y0	Y1	Y2	Y3	0	0	1	0
	Set Column Address (H)	X4	X5	X6	X7	1	1	1	1
	Set Column Address (L)	X0	X1	X2	X3	0	1	1	1
2	Set No. of Data Bytes (H)	DA8	DA9	DA10	0	1	1	1	0
	Set No. of Data Bytes (M)	DA4	DA5	DA6	DA7	0	1	1	0
	Set No. of Data Bytes (L) & Start	DA0	DA1	DA2	DA3	1	0	1	0
3	Transfer Data bytes								

Figure 5 3-line (8 bit) SPI B mode Timing (A0 is not used)

"Set No. of Data Bytes" is used in this mode only. It must be 3 continuous instructions with valid data length which informs ST7588T the following n-bytes transfers are display data. After receiving these 3 instructions, the following transfers will be treated as display data until the data length counter is cleared. If data is halted during transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

NOTE: In spite of transmission of data, if CSB is disabled, state stops abnormally. Next state is initialized.

(2) 3-Line (9-bit) SPI

This mode uses the first bit to indicate the following 8 bits are data or instruction.

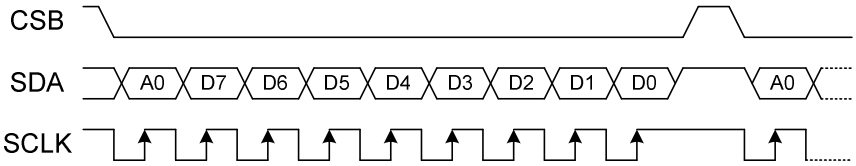


Figure 6 3-line SPI (9-bit) Timing

I²C Interface

The I²C interface receives and executes the commands sent via the I²C Interface. It also receives display data and sends it to the DDRAM. The I²C Interface uses two-line to communicate between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCLK to high when the bus is not busy. Data transfer may be initiated only when the bus is not busy. The I²C interface of ST7588T supports write access and checking acknowledge-bit.

(1) BIT TRANSFER

One data bit is transferred during each clock pulse. Data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on SDA at this moment will be interpreted as START or STOP. Please refer to Figure 8.

(2) START AND STOP CONDITIONS

Both SDA and SCLK lines remain HIGH when the bus is ready. A HIGH-to-LOW transition on SDA, while SCLK is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition on SDA, while SCLK is HIGH, is defined as the STOP condition (P). Please refer to Figure 9.

(3) SYSTEM CONFIGURATION

The system configuration is illustrated in Figure 10. A short glossary is listed below:

- Ø Transmitter: the device that sends the data to the bus.
- Ø Receiver: the device that receives the data from the bus.
- Ø Master: the device which initiates a transfer, generates clock signals and terminates the transfer.
- Ø Slave: the device which is addressed by a master.
- Ø Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Ø Arbitration: procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Ø Synchronization: procedure to synchronize the clock signals of two or more devices.

(4) ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge-bit. The transmitter generates an extra acknowledge-related clock pulse to check the acknowledge-bit. To receive the acknowledge-bit, the transmitter set the SCLK at LOW and put a HIGH signal on SDA. The device that acknowledges must pull-down SDA (acknowledgement) during the acknowledgement clock pulse. The transmitter will check SDA for the acknowledgement. Acknowledge-bit on SDA must be stable LOW during the HIGH period of the acknowledgement clock pulse (set-up and hold times must be taken into consideration). A slave receiver

which is addressed must generate an acknowledge-bit after the reception of each byte. Acknowledgement on the I²C Interface is illustrated in Figure 7.

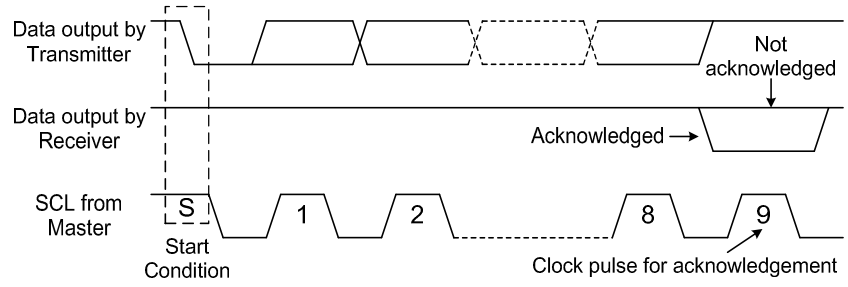


Figure 7 Acknowledgement of the I²C Interface

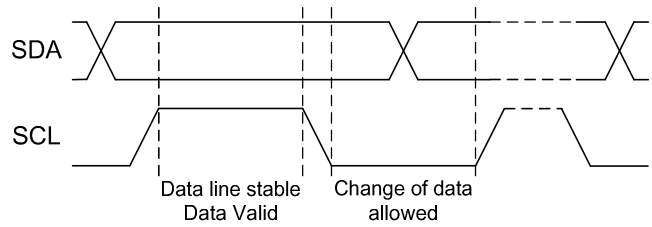


Figure 8 Bit transfer

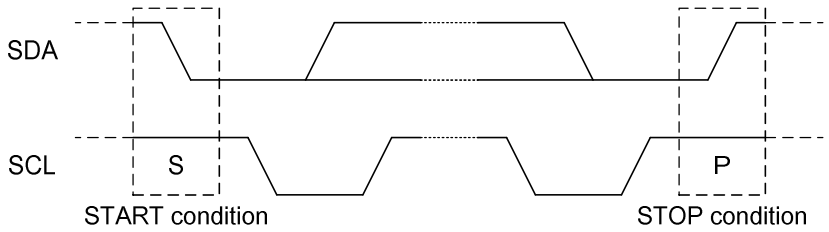


Figure 9 Definition of START and STOP conditions

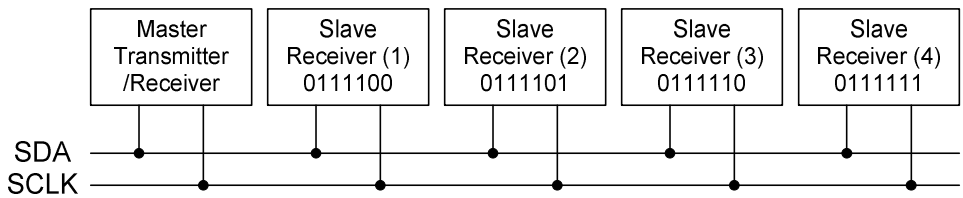


Figure 10 System configuration

(5) I^2C Interface protocol

The ST7588T supports command/data write addressed slaves on the bus. Before any data is transmitted on the I^2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111**00**, 0111**01**, 0111**10**, and 0111**11**) are reserved for the ST7588T. The least significant 2 bits of the slave address is set by connecting SA1 and SA0 to either logic 0 (V_{SS}) or logic 1 (V_{DD1}). The I^2C Interface protocol is illustrated in Figure 11.

A transfer is initiated with a START condition (S) set by the master and followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore this transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co=0). After a control byte with a cleared Co bit, only data bytes will follow. The A0 bit indicates the following data byte is a command or a display data. All addressed slaves on the bus also acknowledge the control and data bytes. The last control byte is followed by either series data bytes with display data or series data bytes with commands (depends on A0 bit). If A0 bit in the last control byte is set to logic 1, these data bytes are display data bytes and will be stored in DDRAM. The data pointer is automatically updated after each display data byte. If A0 bit in the last control byte is set to logic 0, these data bytes are commands and will be decoded to execute the receiving instructions. The master issues a STOP condition (P) at the end of the transmission.

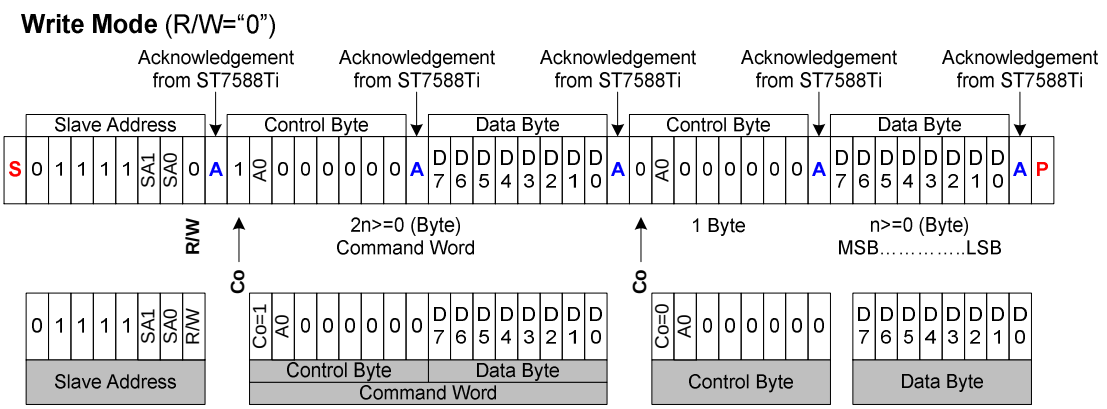


Figure 11 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Data Transfer

The ST7588T uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 12. Moreover, when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 13. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

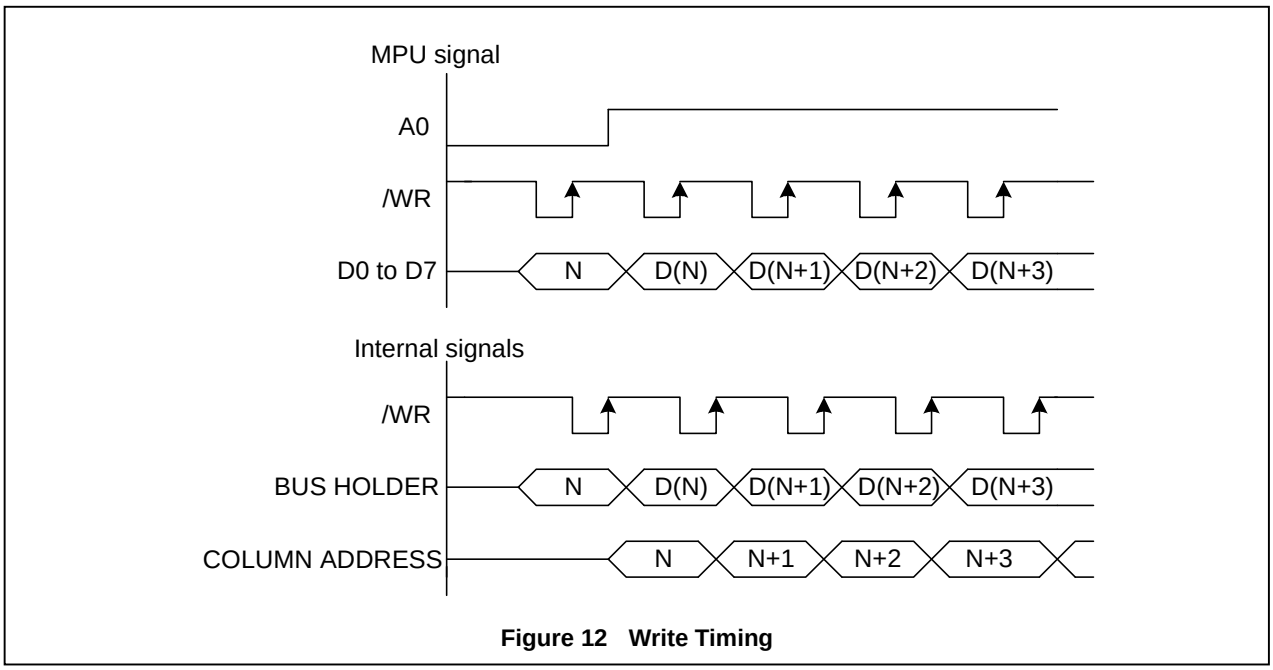


Figure 12 Write Timing

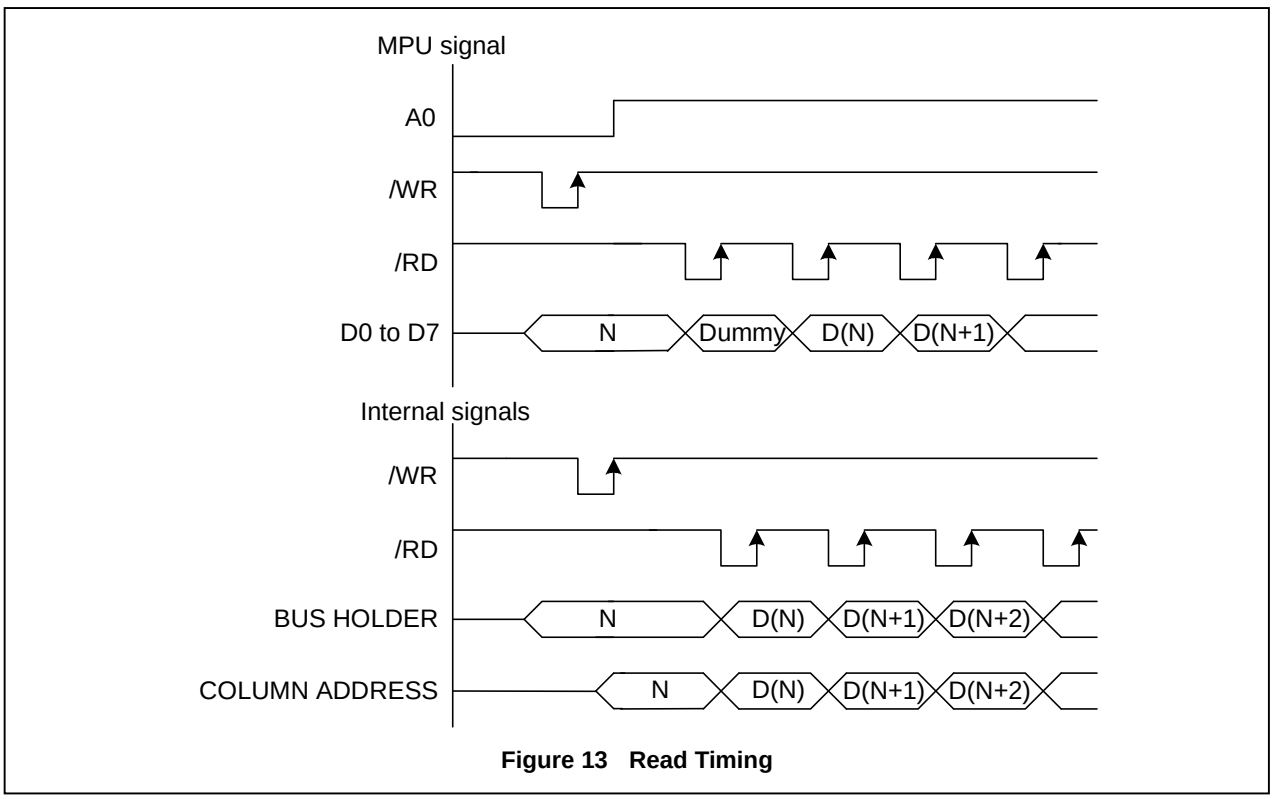


Figure 13 Read Timing

DISPLAY DATA RAM (DDRAM)

The ST7588T contains an 81X132 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has an 81(10 pageX8 bit +1 pageX1 bit) X 132. There is a direct correspondence between X-address and column output number. It is 81-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 11 is a special RAM area for the icons and display data D0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 132-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in Figure 14. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

Register MX and MY selection instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing MX select instruction. Refer to the following Figure 15.

SEG Output

MX	Segment Pads	
	SEG0	**SEG131**
“0”	Seg0 **à** Segment Address **à**	Seg131
“1”	Seg131 **ß** Segment Address **ß**	Seg0

COM Output

MY	Common Pads		
	COM0	**COM79**	**COMS**
“0”	Com0 **à** Common Address **à**	Com79 **à**	COMS
“1”	Com79 **ß** Common Address **ß**	Com0 **à**	COMS

Data is downloaded in bytes into the RAM matrix of ST7588T as indicated in Figs.14, 15, 16. The display RAM has a matrix of 81 by 132 bits. The address pointer addresses the columns. The address range is: X=0~131 (10000011); Y=0~10 (1010). Addresses out of this range are not allowed.

In horizontal addressing mode, the X address increments after each access (see Figure 16). After reaching the last X address (X = 131), X address wraps around to 0 and Y address increases to address the next row.

After the very last address (X = 131, Y = 10) the address pointers wrap around to address (X = 0, Y =0)

Figure 14 RAM format and addressing, if DO=0

Figure 15 RAM format and addressing, if DO=1

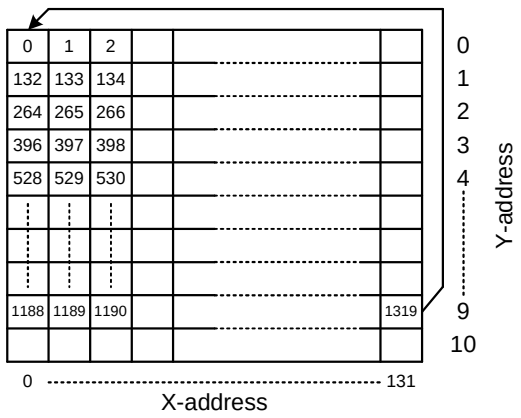


Figure 16 Sequence of writing data bytes into RAM with horizontal addressing

LCD DRIVER CIRCUIT

This driver circuit is configured by 81-channel common drivers and 132-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M (Frame Indicator) signal.

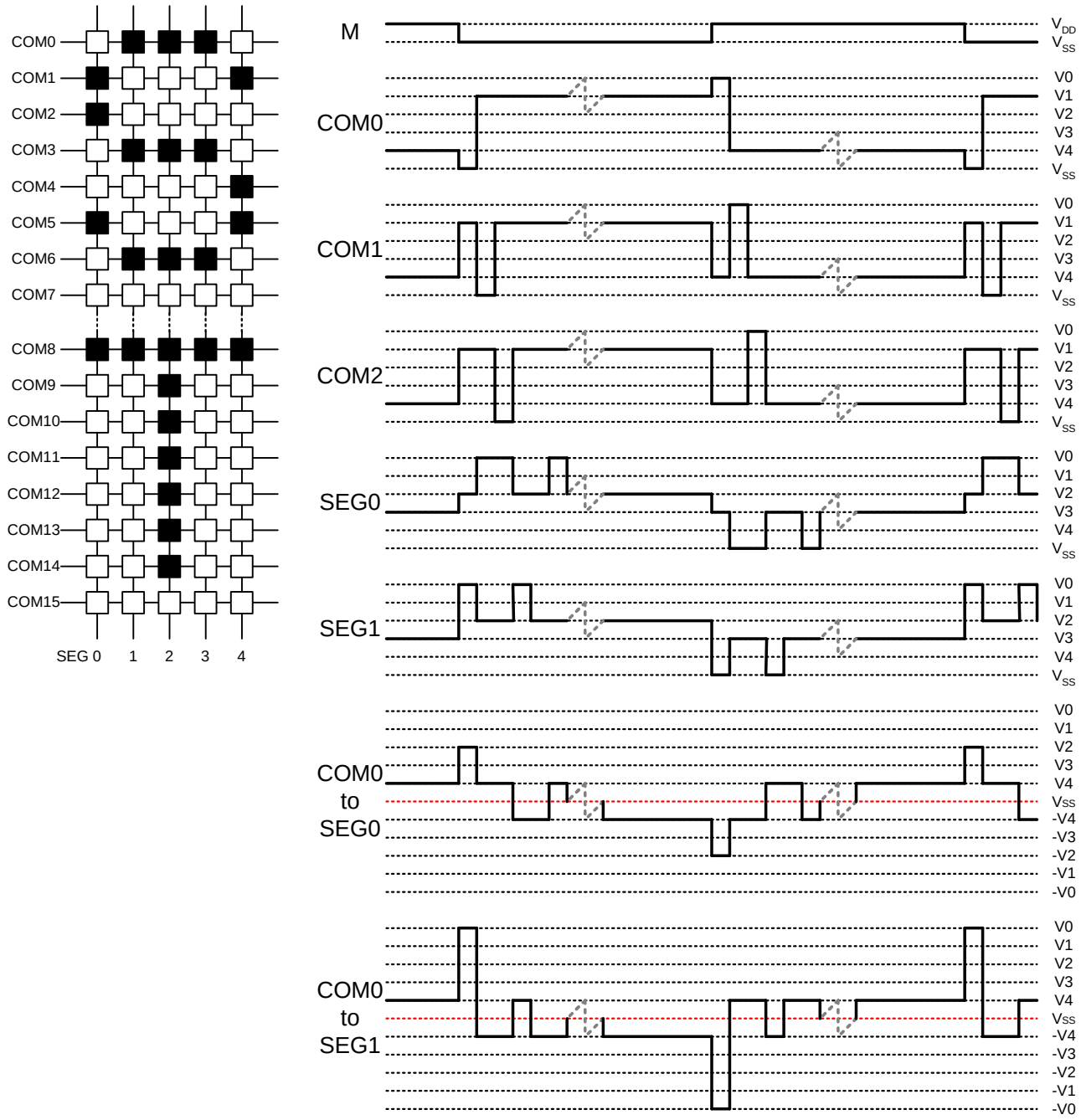


Figure 17 LCD Driver output waveform

REFERENCE BOOSTER CIRCUIT EXAMPLE

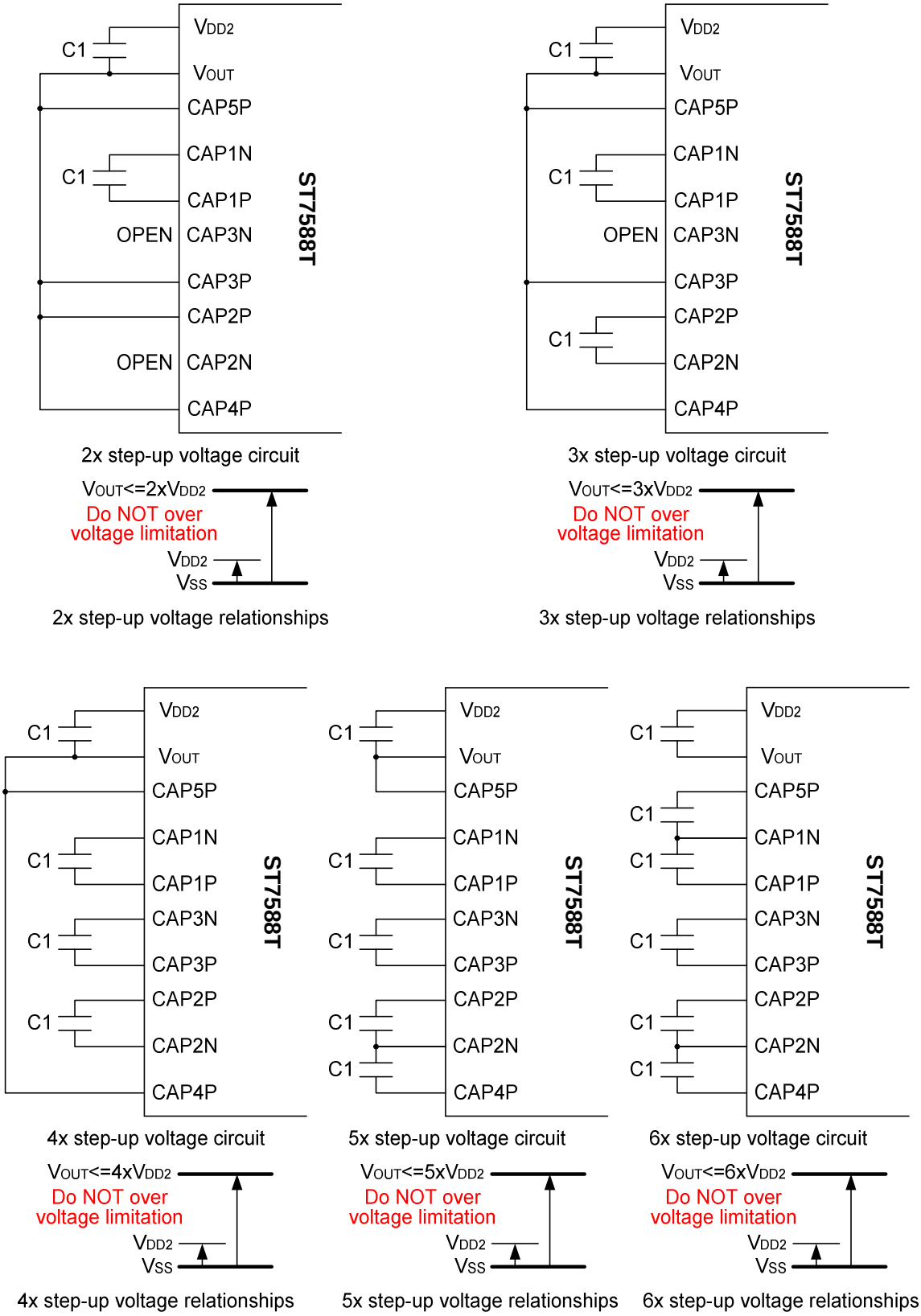


Figure 18 Booster Configuration

Notes:

1. C1 = 1uF ~ 4.7uF. Please take care about the “Voltage Rating” of the capacitor.
2. V_{OUT} should not exceed the Absolutely Maximum Rating.

RESET CIRCUIT

Setting RESB to “L” or Reset instruction can initialize internal function.

When RESB becomes “L”, the following procedure is entered.

Page address: 0

Column address: 0

Display control: Display blank

COM Scan Direction MY: 0

SEG Select Direction MX: 0

DO=0

Oscillator: OFF

N-line inversion register: 0 (disable)

Power down mode (PD = 1)

Normal instruction set (H[1:0] = 00)

Display blank (E = D = 0)

Address counter X [7:0] = 0, Y [3:0] = 0

Bias system (BS [2:0] = 010)

V0 is equal to 0; the HV generator is switched off (V_{OP} [6:0] = 0)

After power-on, RAM data are undefined

While RESB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB0. After DB0 becoming “L”, any instruction can be accepted. RESB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESB is essential before used.

Partial Display on LCD

The ST7588T realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. Moreover, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

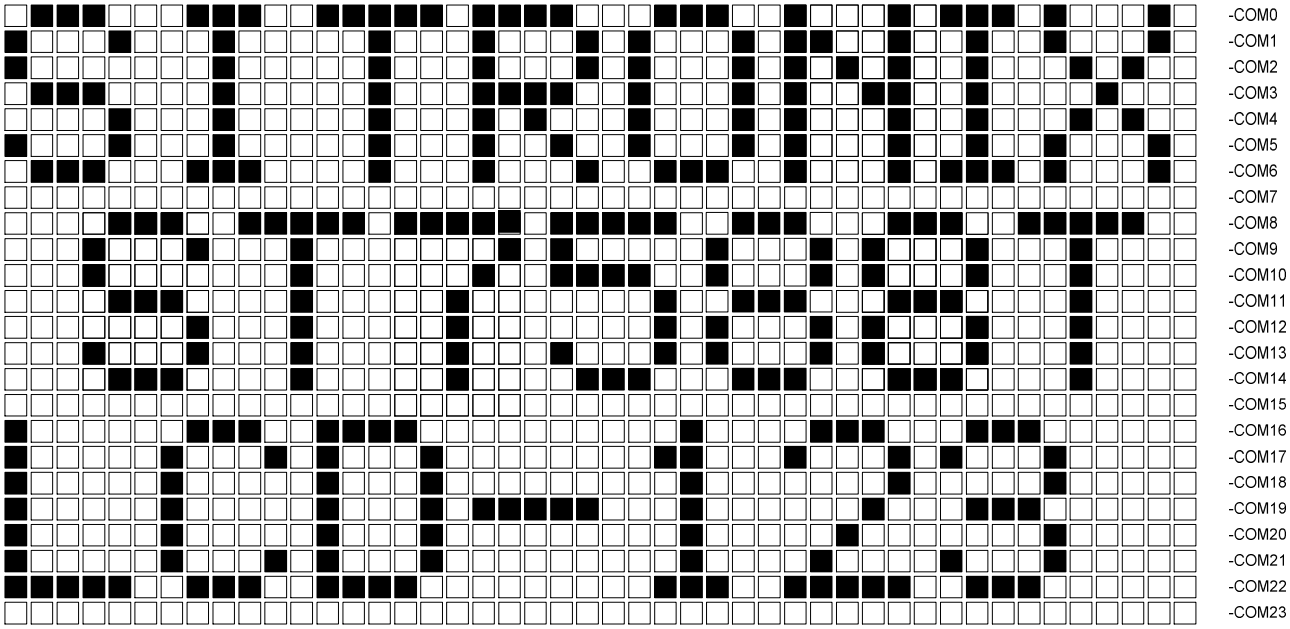


Figure 20 Reference Example for Partial Display

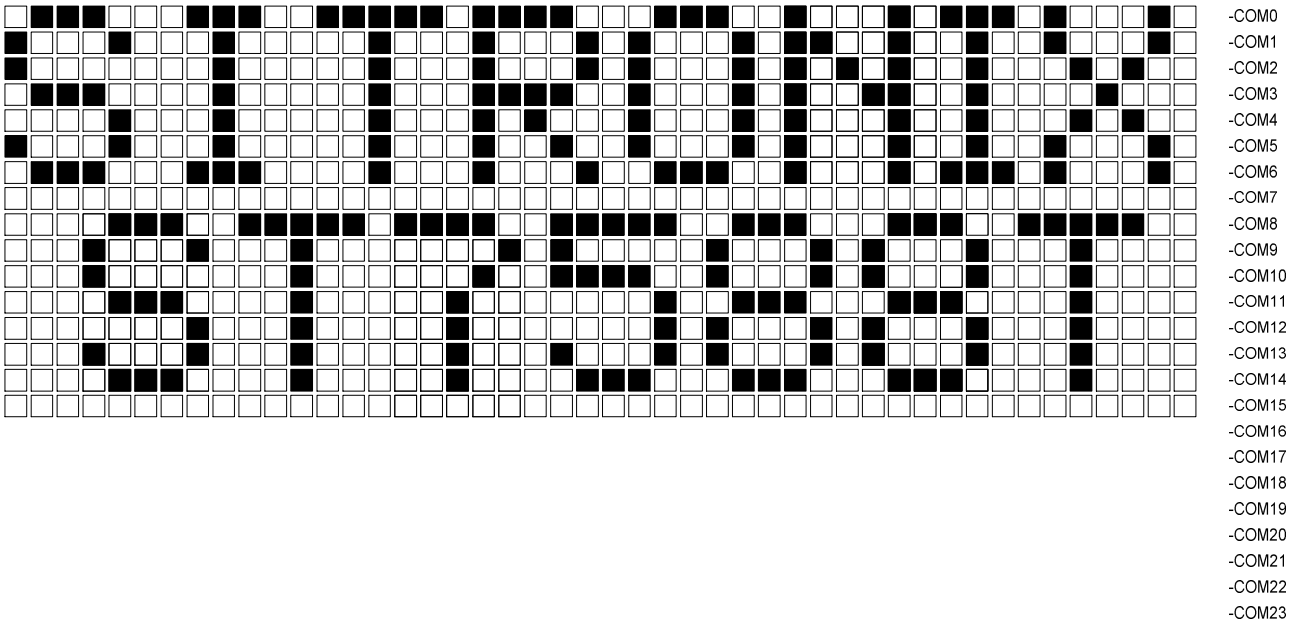


Figure 21 Partial Display (Partial Display Duty=16, initial COM0=0)

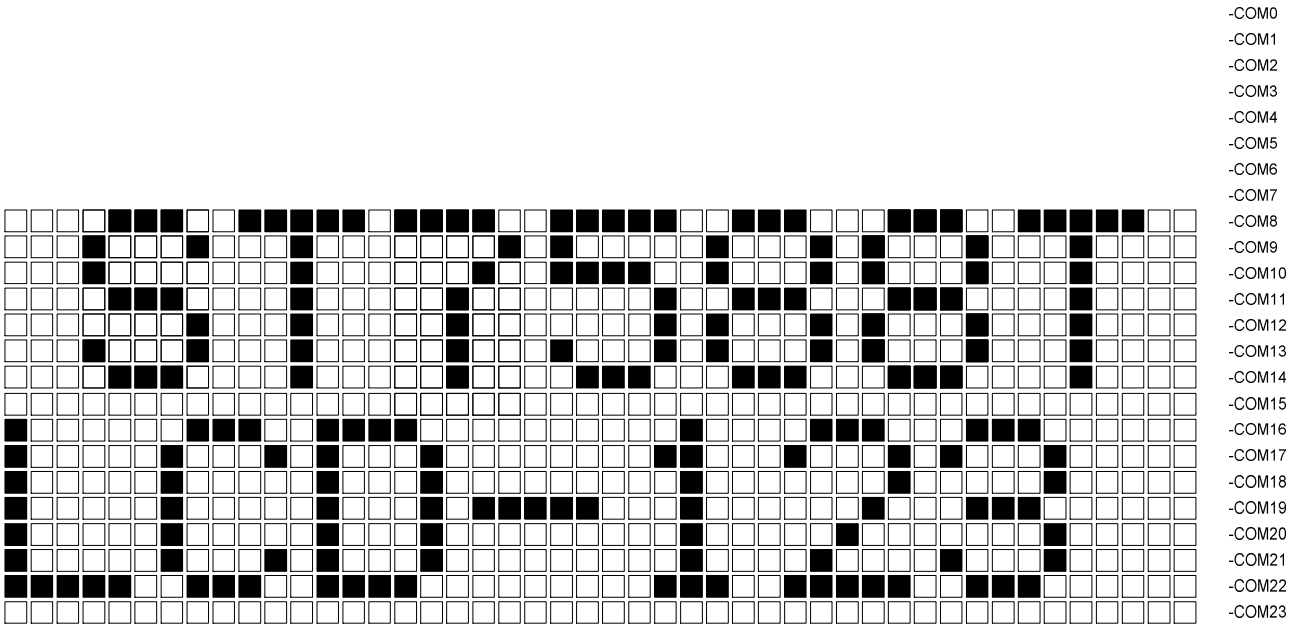


Figure 22 Moving Display (Partial Display Duty=16, Initial COM0=8)

n INSTRUCTION TABLE

INSTRUCTION	A0	R/W (WR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H independent instruction											
Write data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to RAM
Read data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data to RAM
Read status byte	0	1	PD	0	V	D	E	MX	MY	DO	Read status byte
Function Set	0	0	0	0	1	MX	MY	PD	H1	H0	Mirror X, Mirror Y, Power Down, Extended table

INSTRUCTION	A0	R/W (WR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H[1:0]=[0:0]											
Set V0 (V_{OP}) range	0	0	0	0	0	0	0	1	0	PRS	V0 (V_{OP}) range L/H select
END	0	0	0	0	0	0	0	1	1	0	Release read/modify/write
Read/modify/write	0	0	0	0	0	0	0	1	1	1	RAM address at R:+0 , W:+1
Display control	0	0	0	0	0	0	1	D	0	E	Sets display configuration
SI3-8bit data (L)&start	0	0	0	1	0	1	DA3	DA2	DA1	DA0	Set the number of data bytes, Low-bit (8 bit 3-line SPI)
SI3-8bit data (M)	0	0	0	1	1	0	DA7	DA6	DA5	DA4	Set the number of data bytes, Middle-bit (8 bit 3-line SPI)
SI3-8bit data (H)	0	0	0	1	1	1	0	DA10	DA9	DA8	Set the number of data bytes, High-bit (8 bit 3-line SPI)
Set Y address	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set Y address of RAM $0 \leqq Y \leqq 9$
Set X Address (L)	0	0	1	1	1	0	X3	X2	X1	X0	Set X address of RAM, Low-bit. $0 \leqq X \leqq 131$
Set X Address (H)	0	0	1	1	1	1	X7	X6	X5	X4	Set X address of RAM, High-bit. $0 \leqq X \leqq 131$
H[1:0]=[0:1]											
Display configuration	0	0	0	0	0	0	1	DO	0	V	Top/bottom row mode set data order
Bias system	0	0	0	0	0	1	0	BS2	BS1	BS0	Sets bias system (BSx)
Set V0 (V_{OP})	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Write V0 (V_{OP}) to register

INSTRUCTION	A0	R/W (WR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H[1:0]=[1:0]											
Set Partial screen mode	0	0	0	0	0	0	0	1	0	PS	PS=1: Enable Partial screen mode.
Partial Display	0	0	0	0	0	0	1	0	0	WS	Set partial screen size
Set Partial Display part	0	0	0	0	0	1	DP3	DP2	DP1	DP0	Set display area for partial screen mode
Set Start line	0	0	1	S6	S5	S4	S3	S2	S1	S0	Specify the initial display line to realize vertical scrolling
H[1:0]=[1:1]											
RESET	0	0	0	0	0	0	0	0	1	1	Software reset
High Power Mode	0	0	1	0	1	1	0	HP	0	0	High Power Mode SET
Frame	0	0	0	0	0	0	1	FR2	FR1	FR0	Frame rate control
N line inversion	0	0	0	1	0	NL4	NL3	NL2	NL1	NL0	Sets N line inversion

n INSTRUCTION DESCRIPTION

H[1:0] independent

Write data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	Write data							

Read data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read data							

Read status byte

Indicates the internal status of the ST7588T

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	0	V	D	E	MX	MY	DO

Flag			Description
PD	PD=0:chip is active PD=1:chip is in power down mode		
V	When V = 0, the horizontal addressing is selected. When V = 1, the vertical addressing is selected.		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display OFF
	0	1	All display segments on
	1	0	Normal mode
	1	1	Inverse video mode
MX	SEG bi-direction selection MY=0:normal direction (SEG0(SEG131) MY=1:reverse direction (SEG131(SEG0)		
MY	COM bi-direction selection MY=0:normal direction (COM0(COM79) MY=1:reverse direction (COM79(COM0)		
DO	DO=0:MSB is on top DO=1:LSB is on top		

Function Set

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	MX	MY	PD	H1	H0

Flag	Description
MX	SEG bi-direction selection MY=0:normal direction (SEG0 **à** SEG131); MY=1:reverse direction (SEG131 **à** SEG0)
MY	COM bi-direction selection MY=0:normal direction (COM0 **à** COM79); MY=1:reverse direction (COM79 **à** COM0)
PD	PD=0:chip is active; PD=1:chip is in power down mode All LCD outputs at VSS (display off), bias generator and V_{OUT} generator off, V0 can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written.
H0, H1	Selection of Extended Command Table

H[1:0]=[0:0]

Set V0 (V_{OP}) range

V0 (V_{OP}) range L/H select

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PRS

PRS=0: V0 (V_{OP}) programming range LOW

PRS=1: V0 (V_{OP}) programming range HIGH

END

This command releases the read/modify/write mode, and returns the column and row address to the address it was at when the mode was entered.

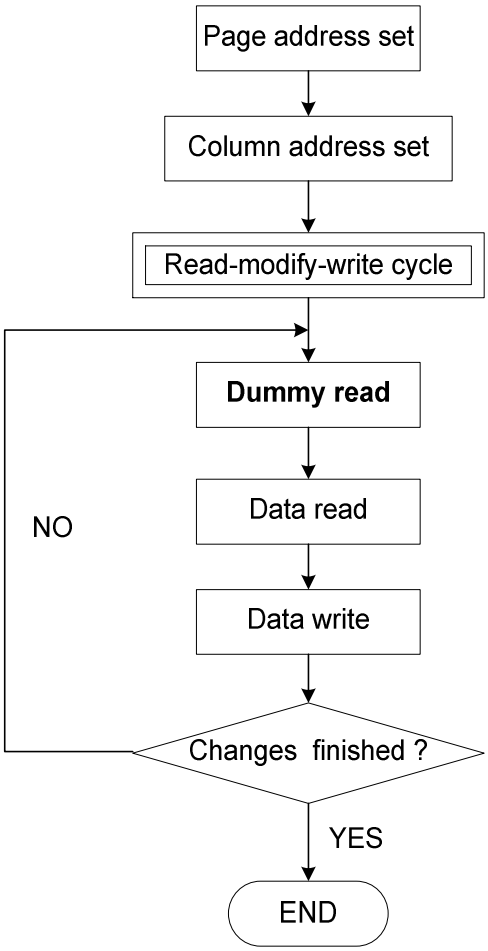
A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	0

Read/modify/write

This command is used coupled with the “END” command. Once this command has been input, the display data read command does not change the column and row address, but only the display data write command increments (+1) the address depend on V register setting. This mode is kept until the END command is input. When the END command is input, the address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	1

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.



Display Control

This bits D and E selects the display mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display OFF
	1	0	Normal display
	0	1	All display segments on
	1	1	Inverse video mode

Set SI3-8 bit Data

Display Data Length resister

This command is used in 8-bit 3-line SPI only. When A0 is not used, the Display Data Length instruction is used to indicate the specified number of display data byte to be transmitted. The next byte after the display data string is handled as data.

A0	WR (R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	DA3	DA2	DA1	DA0	SPI3-8bit Data(L) & Start
0	0	0	1	1	0	DA7	DA6	DA5	DA4	SPI3-8bit Data(M)
0	0	0	1	1	1	0	DA10	DA9	DA8	SPI3-8bit Data(H)

DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Display Data Length
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:	:	:	:
1	0	1	0	0	1	0	0	1	0	1	1317
1	0	1	0	0	1	0	0	1	1	0	1318
1	0	1	0	0	1	0	0	1	1	1	1319
1	0	1	0	0	1	0	1	0	0	0	1320

Set Y address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y3	Y2	Y1	Y0

Y3	Y2	Y1	Y0	CONTENT	ALLOWED X-RANGE
0	0	0	0	Page0 (display RAM)	0 to 131
0	0	0	1	Page1 (display RAM)	0 to 131
0	0	1	0	Page2 (display RAM)	0 to 131
0	0	1	1	Page3 (display RAM)	0 to 131
0	1	0	0	Page4 (display RAM)	0 to 131
0	1	0	1	Page5 (display RAM)	0 to 131
0	1	1	0	Page6 (display RAM)	0 to 131
0	1	1	1	Page7 (display RAM)	0 to 131
1	0	0	0	Page8 (display RAM)	0 to 131
1	0	0	1	Page9 (display RAM)	0 to 131

Set X address of RAM

The X address points to the columns. The range of X is 0…131.

	A0	WR (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
Set X Address (Low)	0	0	1	1	1	0	X3	X2	X1	X0
Set X address (High)	0	0	1	1	1	1	X7	X6	X5	X4

X7	X6	X5	X4	X3	X2	X1	X0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

H[1:0]=[0:1]

Display configuration

Top/bottom row mode set data order and the direction of Address.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	DO	0	V

Flag	Description
DO	DO=0:MSB is on top DO=1:LSB is on top
V	When V = 0, the horizontal addressing is selected. When V = 1, the vertical addressing is selected.

System Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS2	BS1	BS0

BS2	BS1	BS0	Bias
0	0	0	11
0	0	1	10
0	1	0	9
0	1	1	8
1	0	0	7
1	0	1	6
1	1	0	5
1	1	1	4

LCD bias voltage

Symbol	Bias voltage for 1/9 bias	Symbol	Bias voltage for 1/9 bias
V0	V0	V3	2/9 X V0
V1	8/9 X V0	V4	1/9 X V0
V2	7/9 X V0	V_{SS}	V_{SS}

Set V0 (V_{OP}) value:

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}

The operation voltage V0 (V_{OP}) can be set by software.

$$V0 = V_{OP} = (a + V_{OP} \times b) \quad (1)$$

The parameters are described in table 4.The maximum voltage that can be generated is depending on the V_{DD1} voltage and the display load current. Two overlapping V0 (V_{OP}) ranges are selectable via the command “Booster control”. For the LOW (PRS=0) range a=a1 and for the HIGH (PRS=1) range a=a2 with steps equal to “b” in both ranges. **Note that the charge pump is turned off if V_{OP} [6;0] and the bit PRS are all set to zero.**

SYMBOL	VALUE	UNIT
a1	3.528(PRS=0)	V
a2	8.862(PRS=1)	V
b	0.042	V

Table 4 Typical values for parameter for the HV-Generator programming

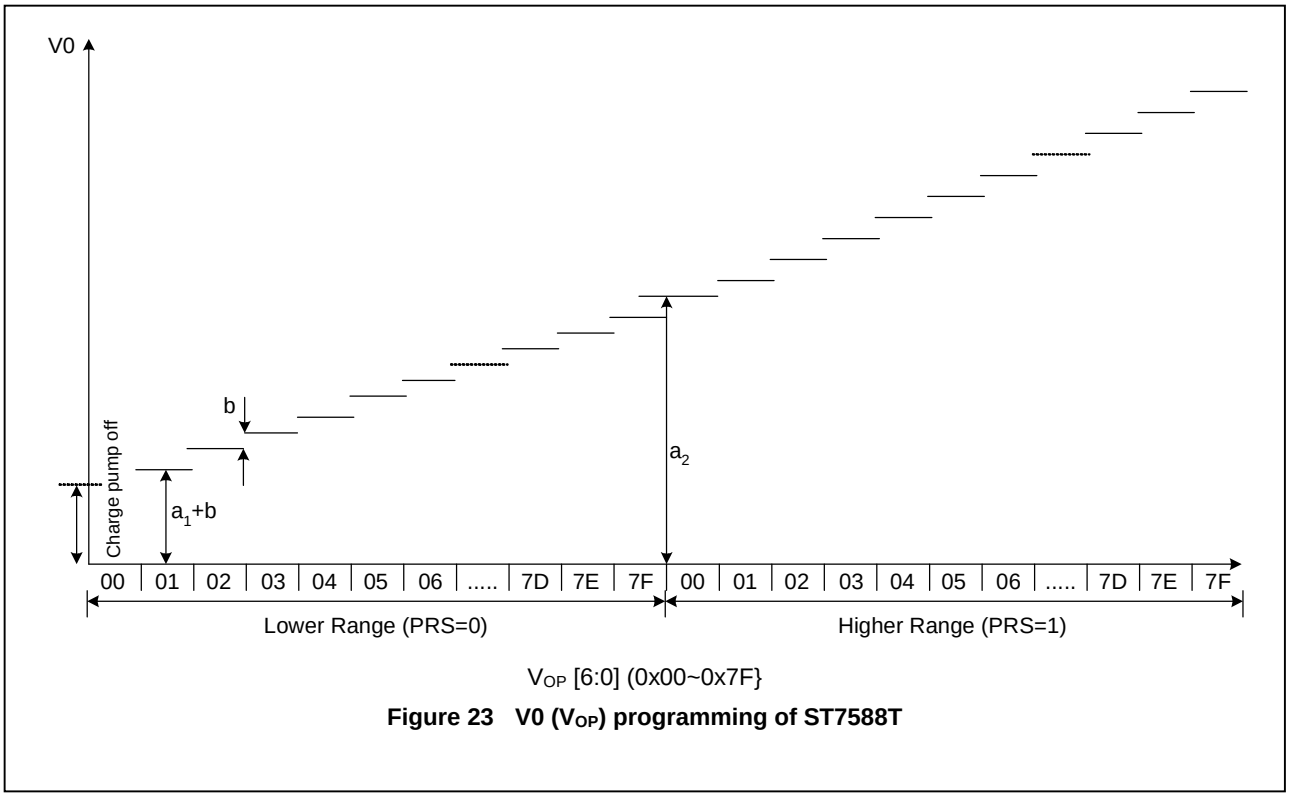


Figure 23 V0 (V_{OP}) programming of ST7588T

*** Recommended LCD V_{OP} voltage is 9.5V~10.5V (1/10 Bias).**

H[1:0]=[1:0]

Partial screen mode

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PS

Flag	Description
PS	Full display mode or partial screen mode selection. PS=0:Full display mode with MUX 1:80. PS=1:Partial screen mode with MUX 1:16 or MUX 1:32.

Partial screen size

This instruction controls partial screen size, partial screen 16 rows when WS is low and partial screen 32 rows when WS is high.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	0	WS

Display part

This instruction can select partial screen display area.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	DP3	DP2	DP1	DP0

(1) 1/16 Duty

Flag	Status				Description
DP3 DP2 DP1 DP0	0	0	0	0	RAM bank 0 to 1 (row0~row15)
	0	0	0	1	RAM bank 1 to 2 (row8~row23)
	0	0	1	0	RAM bank 2 to 3 (row16~row31)
	0	0	1	1	RAM bank 3 to 4 (row24~row39)
	0	1	0	0	RAM bank 4 to 5 (row32~row47)
	0	1	0	1	RAM bank 5 to 6 (row40~row55)
	0	1	1	0	RAM bank 6 to 7 (row48~row63)
	0	1	1	1	RAM bank 7 to 8 (row56~row71)
	1	0	0	0	RAM bank 8 to 9 (row64~row79)
	1	0	0	1	RAM bank 9 (row72~row79)

(2) 1/32 Duty

Flag	Status				Description
DP3 DP2 DP1 DP0	0	0	0	0	RAM bank 0 to 3 (row0~row31)
	0	0	0	1	RAM bank 1 to 4 (row8~row39)
	0	0	1	0	RAM bank 2 to 5 (row16~row47)
	0	0	1	1	RAM bank 3 to 6 (row24~row55)
	0	1	0	0	RAM bank 4 to 7 (row32~row63)
	0	1	0	1	RAM bank 5 to 8 (row40~row71)
	0	1	1	0	RAM bank 6 to 9 (row48~row79)
	0	1	1	1	RAM bank 7 to 9 (row56~row79)
	1	0	0	0	RAM bank 8 to 9 (row64~row79)
	1	0	0	1	RAM bank 9 (row72~row79)

Set start line

Sets the line address of display RAM to determine the initial display line instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	0	0	1	1	0	1	77
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79

Note: when 81 duty is selected, 4f (1001111) is MAX;
when 65 duty is selected, 3f (0111111) is MAX;
when 49 duty is selected, 2f (0101111) is MAX

H[1:0]=[1:1]

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status .This instruction cannot initialize the LCD power supply, which is initialized by the RESB pin.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1

High Power Mode

This command is to enter the high power mode. HP=1: high power mode, HP=0: normal mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	HP	0	0

Frame frequency

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	FR2	FR1	FR0

This command is used to set the frame frequency.

FR2	FR1	FR0	Frame frequency
0	0	0	50 Hz
0	0	1	68 Hz
0	1	0	70 Hz
0	1	1	73 Hz
1	0	0	75 Hz
1	0	1	78 Hz
1	1	0	81 Hz
1	1	1	150 Hz

Set N-line inversion

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M)

Note: The N-line inversion mode will be disabled when partial display mode enter. After the partial display mode end, the N-line inversion mode will return as it was.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	NL4	NL3	NL2	NL1	NL0

NL4	NL3	NL2	NL1	NL0	Selected n-line inversion
0	0	0	0	0	Frame inversion
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

n COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

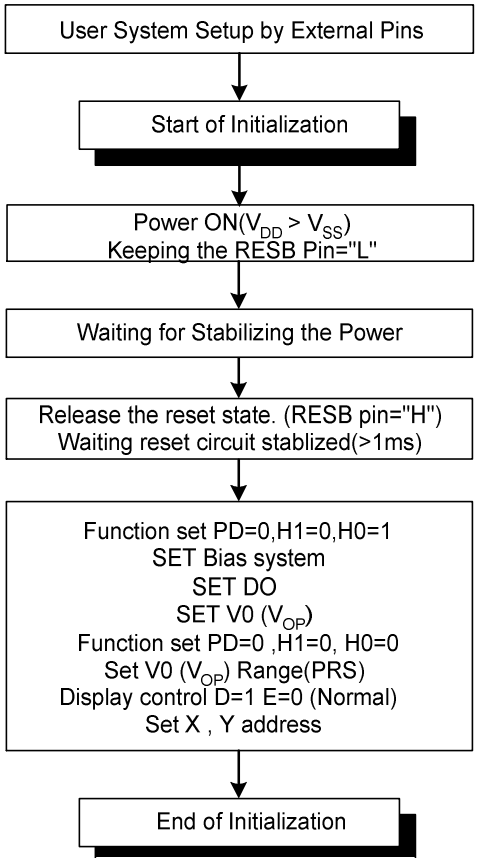


Figure 24 Initializing with the Built-in Power Supply Circuits

Referential Instruction Flow for Power Down:

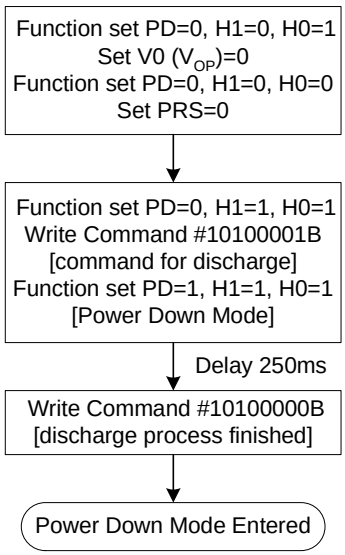
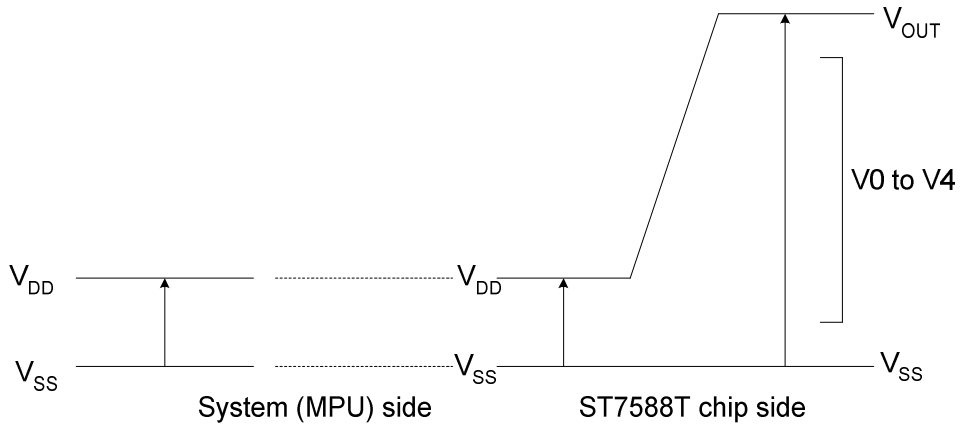


Figure 25 Instruction Flow for Power Down

n ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	V_{DD1}	–0.3 ~ 3.6	V
Analog Power supply voltage	V_{DD2}	–0.3 ~ 3.6	V
LCD Operation Power supply voltage	V_{OUT}, V0	–0.5 ~ +13.5	V
LCD Driving Power supply voltage	V1, V2, V3, V4	0.3 to V0	V
Input voltage	V_{IN}	–0.5 to V_{DD}+0.5	V
Output voltage	V_O	–0.5 to V_{DD}+0.5	V
Operating temperature	T_{OPR}	–30 to +85	°C
Storage temperature	T_{STR}	–65 to +150	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that
   $V_{OUT} \geqq V0 \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq Vss$
4. Recommended LCD V_{OP} voltage is 9.5V~10.5V (1/10 Bias).

n DC CHARACTERISTICS

V_{SS} = 0V; T_{amb} = -30℃ to +85℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		V_{DD1}			1.8	--	3.3	V	V_{DD1}
Operating Voltage (2)		V_{DD2}			2.4	--	3.3	V	V_{DD2}
High-level Input Voltage		V_{IHC}			0.7 x V_{DD1}	--	V_{DD1}	V	
Low-level Input Voltage		V_{ILC}			V_{SS}	--	0.3 x V_{DD1}	V	
High-level Output Voltage		V_{OHC}	I_{OH}=1mA		0.8 x V_{DD1}	--	V_{DD1}	V	
Low-level Output Voltage		V_{OLC}	I_{OL}=1mA		V_{SS}	--	0.2 x V_{DD1}	V	
Input leakage current		I_{LI}	V_{IN} = V_{DD1} or V_{SS}		-1.0	--	1.0	μA	
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (relative to V_{SS})	V0 = 11.0 V	--	0.8	1.1	kΩ	SEGn COMn
Oscillator Frequency	Internal Oscillator	f_{OSC}	1/81 duty		--	50	--	kHz	*1
	Frame Frequency	f_{FRAME}			--	75	--	Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Voltage Step-up Circuit output	V_{OUT}	(Relative To VSS)	--	--	13.5	V	V_{SS}, *2

*** Recommended LCD V_{OP} voltage is 9.5V~10.5V (1/10 Bias).**

Dynamic Consumption Current: During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	I_{SS}	V_{DD} = 3.0 V, V0 – V_{SS} = 10.0 V	--	120	--	μA	*3
Power Down	I_{SS}	Ta = 25°C	--	0.05	2	μA	*4

Notes to the DC characteristics:

1. Internal clock
2. The maximum possible V_{OUT} voltage that may be generated is dependent on voltage, temperature and (display) load.
3. If external V0 used, the display load current is not transmitted to I_{DD}.
4. Power-down mode. During power down, all static currents are switched off.

n TIMING CHARACTERISTICS

System Bus Read/Write Characteristics (For the 8080 Series MPU)

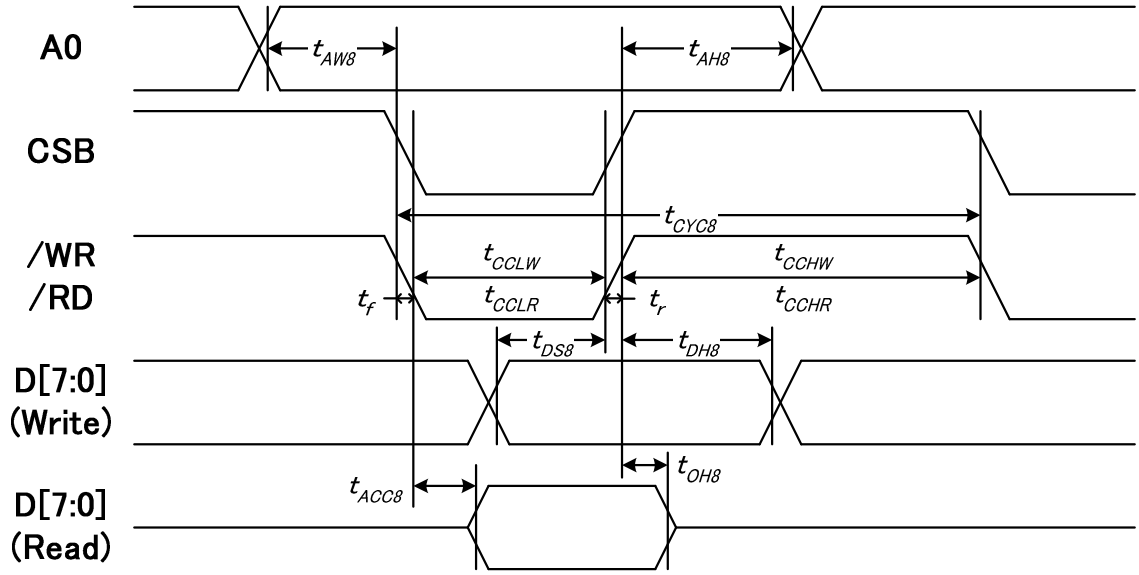


Figure 26

(V_{DD} = 3.3V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		20	--	ns
Address setup time		t_{AW8}		20	--	
System cycle time		t_{CYC8}		80	--	
Write L pulse width	/WR	t_{CCLW}		70	--	
Write H pulse width		t_{CCHW}		30	--	
Read L pulse width	/RD	t_{CCLR}		90	--	
Read H pulse width		t_{CCHR}		30	--	
Data setup time (Write)	D[7:0]	t_{DS6}		80	--	
Data hold time (Write)		t_{DH6}		20	--	
Data access time (Read)		t_{ACC6}	C_L = 100 pF	--	50	
Output disable time (Read)		t_{OH6}	C_L = 100 pF	10	30	

(V_{DD} = 2.7V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		20	--	ns
Address setup time		t_{AW8}		20	--	
System cycle time		t_{CYC8}		90	--	
Write L pulse width	/WR	t_{CCLW}		80	--	
Write H pulse width		t_{CCHW}		30	--	
Read L pulse width	/RD	t_{CCLR}		110	--	
Read H pulse width		t_{CCHR}		30	--	
Data setup time (Write)	D[7:0]	t_{DS6}		90	--	
Data hold time (Write)		t_{DH6}		20	--	
Data access time (Read)		t_{ACC6}	C_L = 100 pF	--	60	
Output disable time (Read)		t_{OH6}	C_L = 100 pF	10	40	

(V_{DD} = 1.8V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		20	--	ns
Address setup time		t_{AW8}		20	--	
System cycle time		t_{CYC8}		220	--	
Write L pulse width	/WR	t_{CCLW}		200	--	
Write H pulse width		t_{CCHW}		30	--	
Read L pulse width	/RD	t_{CCLR}		220	--	
Read H pulse width		t_{CCHR}		30	--	
Data setup time (Write)	D[7:0]	t_{DS6}		220	--	
Data hold time (Write)		t_{DH6}		20	--	
Data access time (Read)		t_{ACC6}	C_L = 100 pF	--	100	
Output disable time (Read)		t_{OH6}	C_L = 100 pF	10	30	

1. The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC8} – t_{CCLW} – t_{CCHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC8} – t_{CCLR} – t_{CCHR}$) are specified.
2. All timing is specified using 20% and 80% of V_{DD} as the reference.
3. t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics (For the 6800 Series MPU)

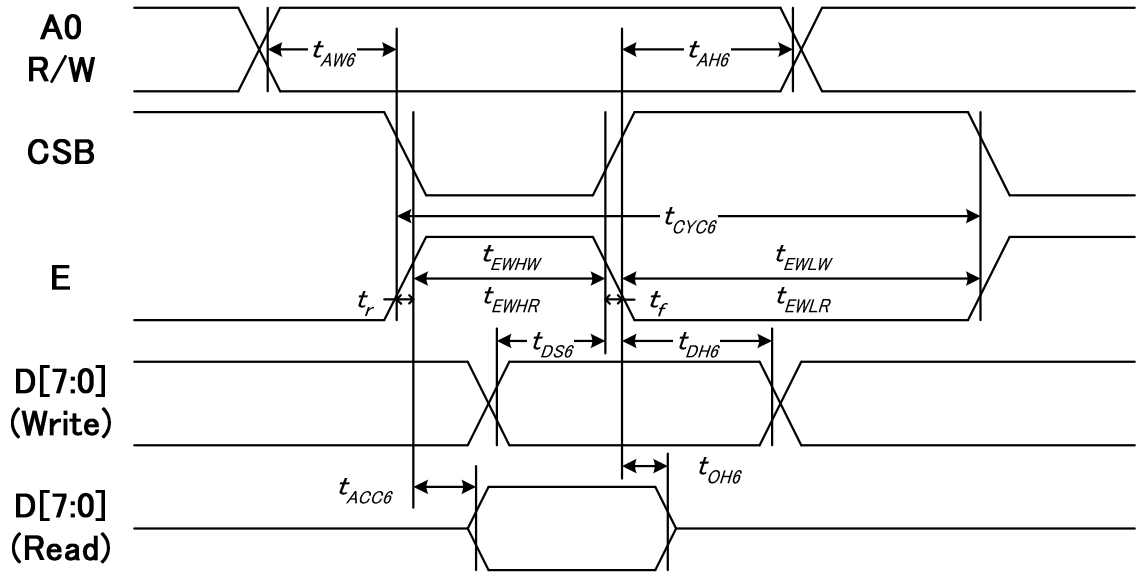


Figure 27

(V_{DD} = 3.3V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		20	--	ns
Address setup time		t_{AW6}		60	--	
System cycle time		t_{CYC6}		100	--	
Enable L pulse width (WRITE)	WR	t_{EWLW}		30	--	
Enable H pulse width (WRITE)		t_{EWHW}		40	--	
Enable L pulse width (READ)	RD	t_{EWLR}		30	--	
Enable H pulse width (READ)		t_{EWHR}		40	--	
WRITE Data setup time	D0 to D7	t_{DS6}		70	--	
WRITE Data hold time		t_{DH6}		20	--	
READ access time		t_{ACC6}	C_L = 100 pF	--	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	40	

(V_{DD} = 2.7V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		20	--	ns
Address setup time		t_{AW6}		70	--	
System cycle time		t_{CYC6}		140	--	
Enable L pulse width (WRITE)	WR	t_{EWLW}		30	--	
Enable H pulse width (WRITE)		t_{EWHW}		40	--	
Enable L pulse width (READ)	RD	t_{EWLR}		30	--	
Enable H pulse width (READ)		t_{EWHR}		40	--	
WRITE Data setup time	D0 to D7	t_{DS6}		90	--	
WRITE Data hold time		t_{DH6}		20	--	
READ access time		t_{ACC6}	C_L = 100 pF	--	80	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	40	

(V_{DD} = 1.8V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		20	--	ns
Address setup time		t_{AW6}		80	--	
System cycle time		t_{CYC6}		270	--	
Enable L pulse width (WRITE)	WR	t_{EWLW}		40	--	
Enable H pulse width (WRITE)		t_{EWHW}		60	--	
Enable L pulse width (READ)	RD	t_{EWLR}		40	--	
Enable H pulse width (READ)		t_{EWHR}		70	--	
WRITE Data setup time	D0 to D7	t_{DS6}		210	--	
WRITE Data hold time		t_{DH6}		20	--	
READ access time		t_{ACC6}	C_L = 100 pF	--	80	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	40	

1. The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
2. All timing is specified using 20% and 80% of V_{DD} as the reference.
3. t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

SERIAL INTERFACE (I²C Interface)

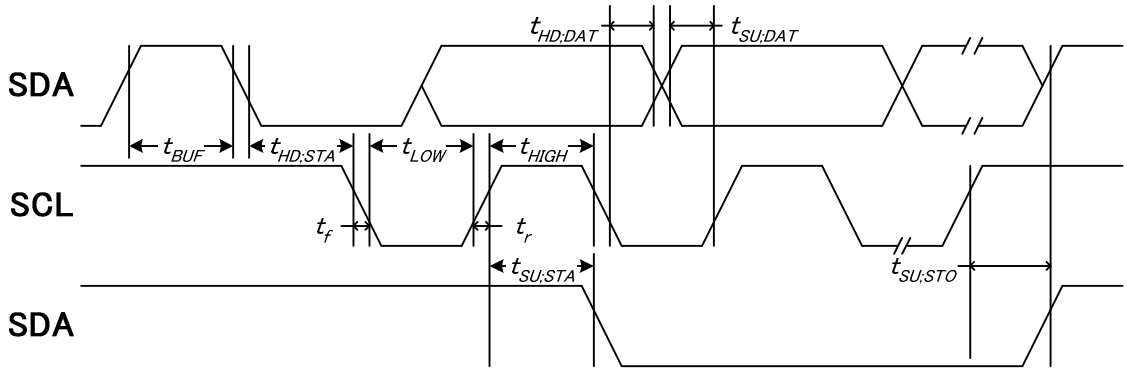


Figure 28

(V_{DD} = 3.3V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}		DC	400	kHz
SCL clock low period	SCL	t_{LOW}		150	--	ns
SCL clock high period	SCL	t_{HIGH}		100	--	
Data set-up time	SDA	$t_{SU;Dat}$		90	--	
Data hold time	SDA	$t_{HD;Dat}$		40	--	
Setup time for a repeated START condition	SDA	$t_{SU;STA}$		70	--	
Start condition hold time	SDA	$t_{HD;STA}$		170	--	
Setup time for STOP condition		$t_{SU;STO}$		90	--	
BUS free time between a STOP and START condition	SCL	t_{BUF}		70	--	

(V_{DD} = 2.7V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}		DC	400	kHz
SCL clock low period	SCL	t_{LOW}		190	--	ns
SCL clock high period	SCL	t_{HIGH}		110	--	
Data set-up time	SDA	$t_{SU;Dat}$		110	--	
Data hold time	SDA	$t_{HD;Dat}$		30	--	
Setup time for a repeated START condition	SDA	$t_{SU;STA}$		90	--	
Start condition hold time	SDA	$t_{HD;STA}$		220	--	
Setup time for STOP condition		$t_{SU;STO}$		110	--	
BUS free time between a STOP and START condition	SCL	t_{BUF}		90	--	

SERIAL INTERFACE (4-Line Interface)

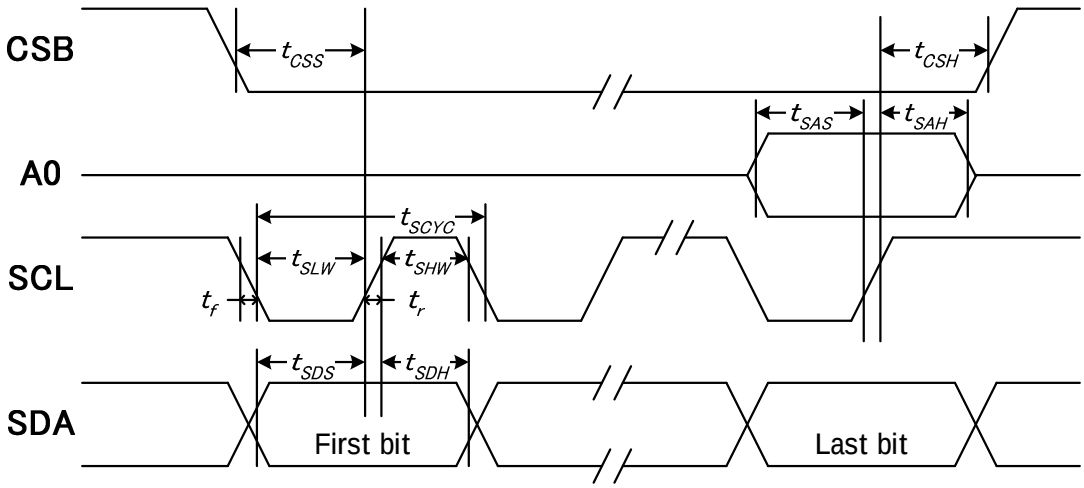


Figure 29

(V_{DD} = 3.3V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		100	--	ns
SCL “H” pulse width		t_{SHW}		60	--	
SCL “L” pulse width		t_{SLW}		60	--	
Address setup time	A0	t_{SAS}		20	--	
Address hold time		t_{SAH}		80	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		20	--	
CS-SCL time	CSB	t_{CSS}		30	--	
CS-SCL time		t_{CSH}		120	--	

(V_{DD} = 2.7V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		120	--	ns
SCL “H” pulse width		t_{SHW}		70	--	
SCL “L” pulse width		t_{SLW}		70	--	
Address setup time	A0	t_{SAS}		20	--	
Address hold time		t_{SAH}		100	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		20	--	
CS-SCL time	CSB	t_{CSS}		30	--	
CS-SCL time		t_{CSH}		150	--	

(V_{DD} = 1.8V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		330	--	ns
SCL “H” pulse width		t_{SHW}		150	--	
SCL “L” pulse width		t_{SLW}		150	--	
Address setup time	A0	t_{SAS}		20	--	
Address hold time		t_{SAH}		160	--	
Data setup time	SDA	t_{SDS}		40	--	
Data hold time		t_{SDH}		40	--	
CS-SCL time	CSB	t_{CSS}		40	--	
CS-SCL time		t_{CSH}		370	--	

1. The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of V_{DD} as the standard.

SERIAL INTERFACE (3-Line Interface)

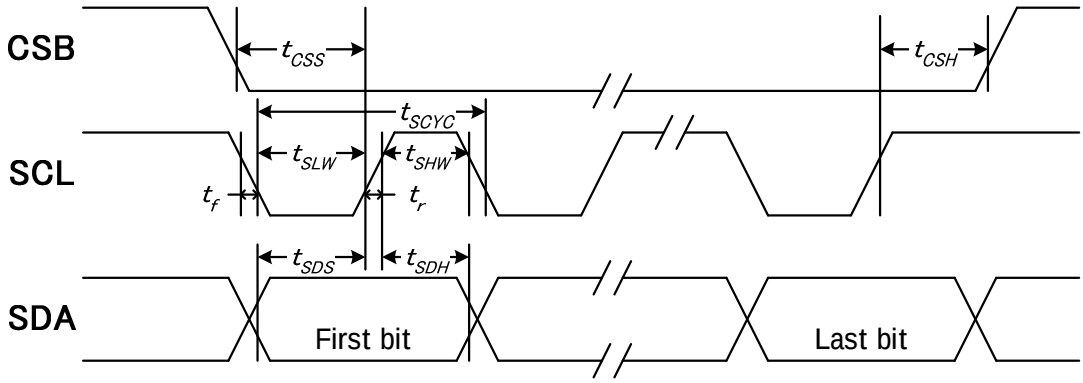


Figure 30

(V_{DD} = 3.3V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		100	--	ns
SCL “H” pulse width		t_{SHW}		60	--	
SCL “L” pulse width		t_{SLW}		60	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		20	--	
CS-SCL time	CSB	t_{CSS}		30	--	
CS-SCL time		t_{CSH}		120	--	

(V_{DD} = 2.7V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		120	--	ns
SCL “H” pulse width		t_{SHW}		70	--	
SCL “L” pulse width		t_{SLW}		70	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		20	--	
CS-SCL time	CSB	t_{CSS}		30	--	
CS-SCL time		t_{CSH}		150	--	

(V_{DD} = 1.8V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		330	--	ns
SCL “H” pulse width		t_{SHW}		150	--	
SCL “L” pulse width		t_{SLW}		150	--	
Data setup time	SDA	t_{SDS}		40	--	
Data hold time		t_{SDH}		40	--	
CS-SCL time	CSB	t_{CSS}		40	--	
CS-SCL time		t_{CSH}		370	--	

1. The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of V_{DD} as the standard.

n RESET TIMING

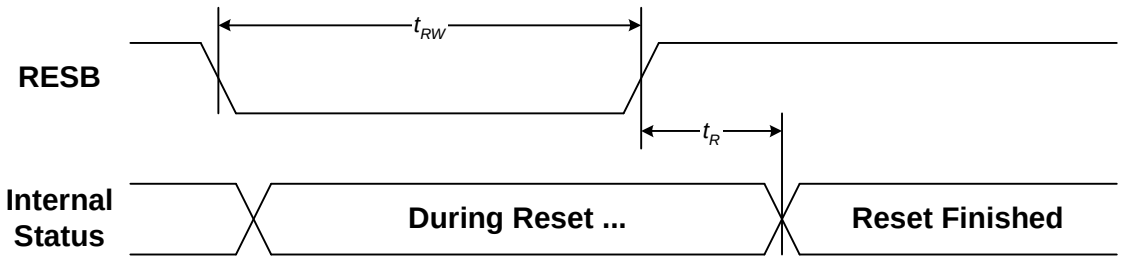


Figure 31

(V_{DD} = 3.3V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		--	--	400	ns
Reset “L” pulse width	/RES	t_{RW}		1200	--	--	

(V_{DD} = 2.7V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		--	--	350	ns
Reset “L” pulse width	/RES	t_{RW}		1600	--	--	

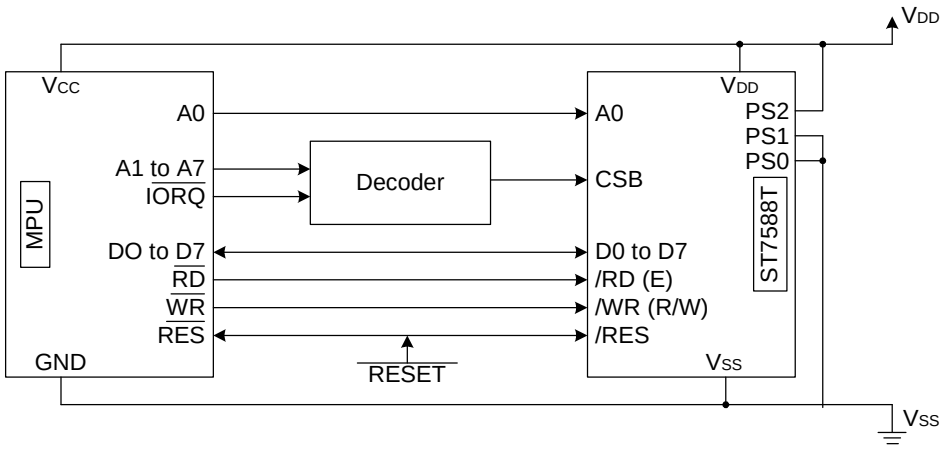
(V_{DD} = 1.8V, Ta = –30 to 85 °C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		--	--	140	ns
Reset “L” pulse width	/RES	t_{RW}		4500	--	--	

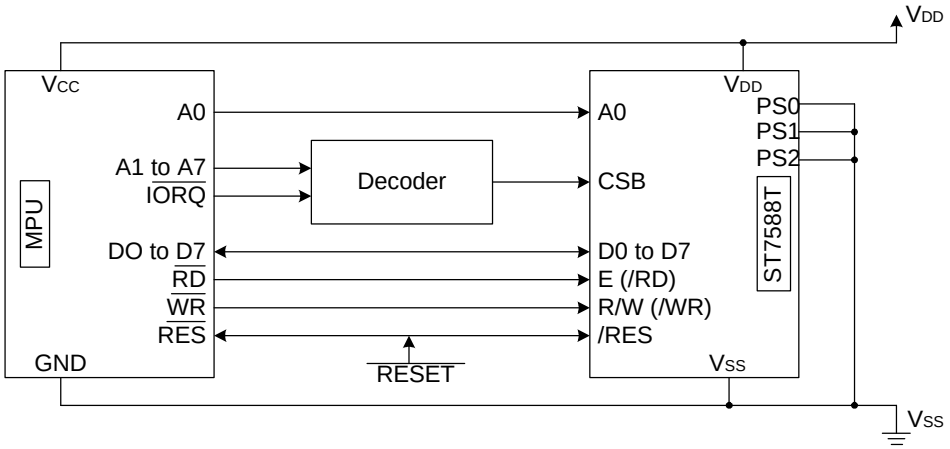
n THE MPU INTERFACE (REFERENCE EXAMPLES)

ST7588T can be connected to either 80X86 Series MPU or to 6800 Series MPU.

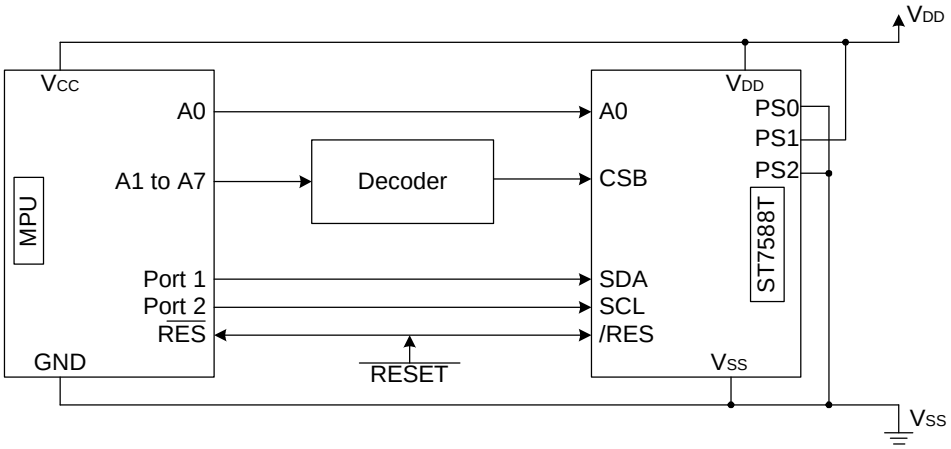
(1) 8080 Series MPU



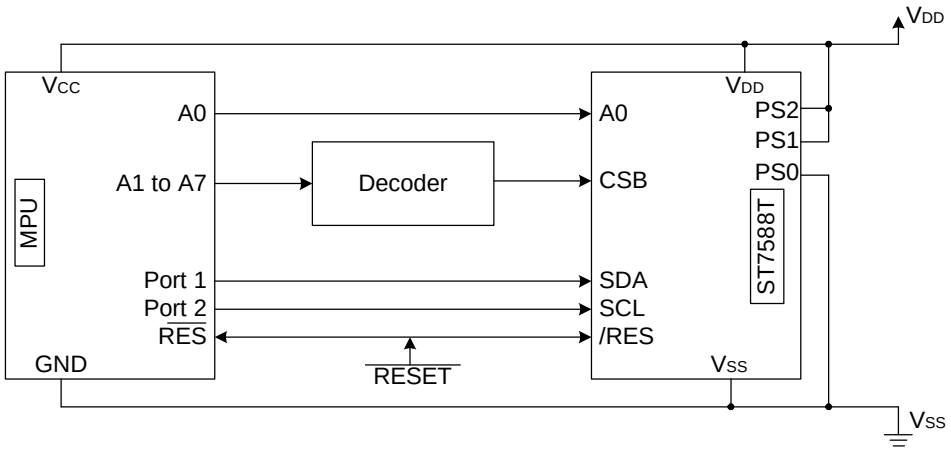
(2) 6800 Series MPU



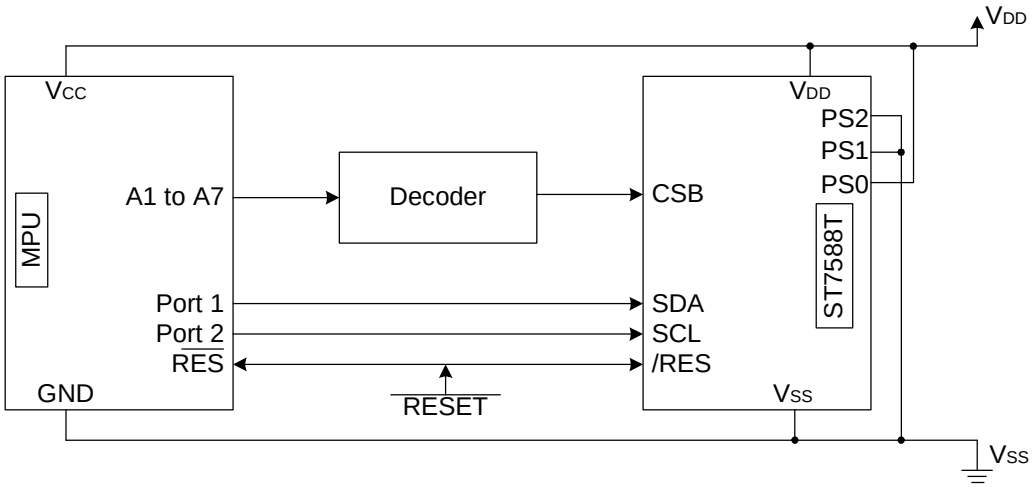
(3) Using the Serial Interface (4-line interface A mode)



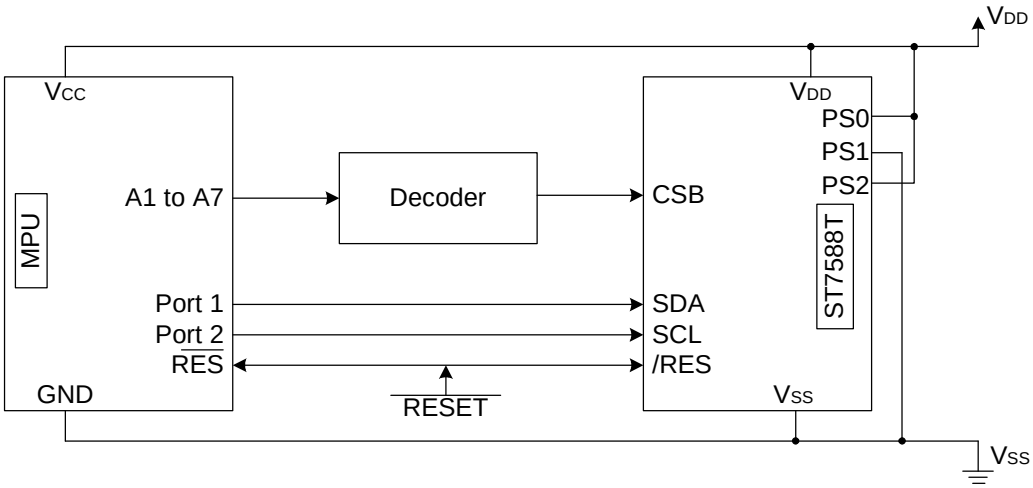
(4) Using the Serial Interface (4-line interface B mode)



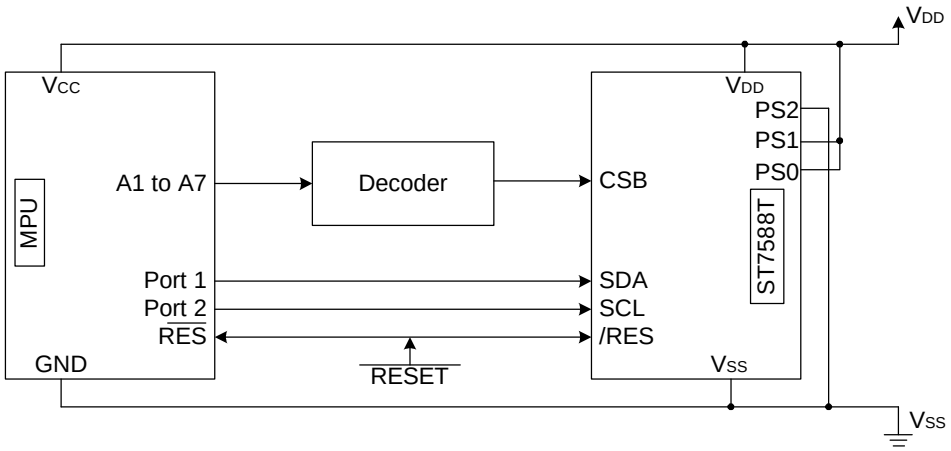
(5) Using the Serial Interface (3-line interface 8 bit A mode)



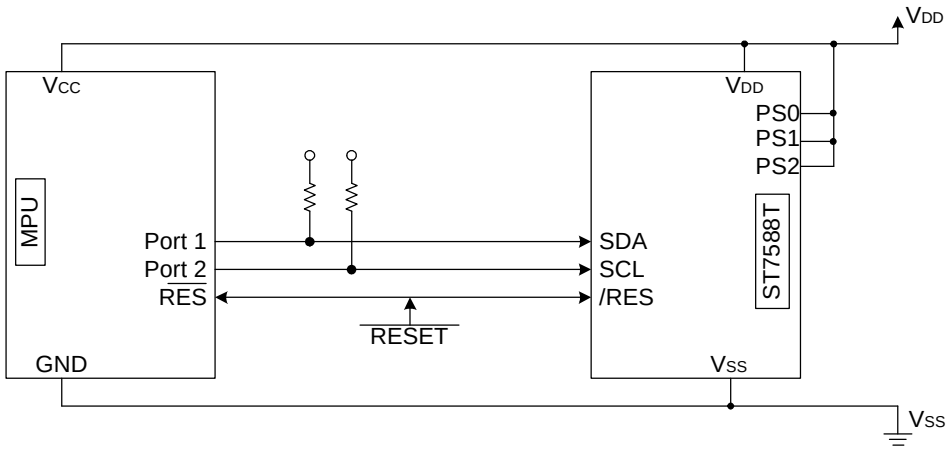
(6) Using the Serial Interface (3-line interface 8 bit B mode)



(7) Using the Serial Interface (3-line interface 9 bit)

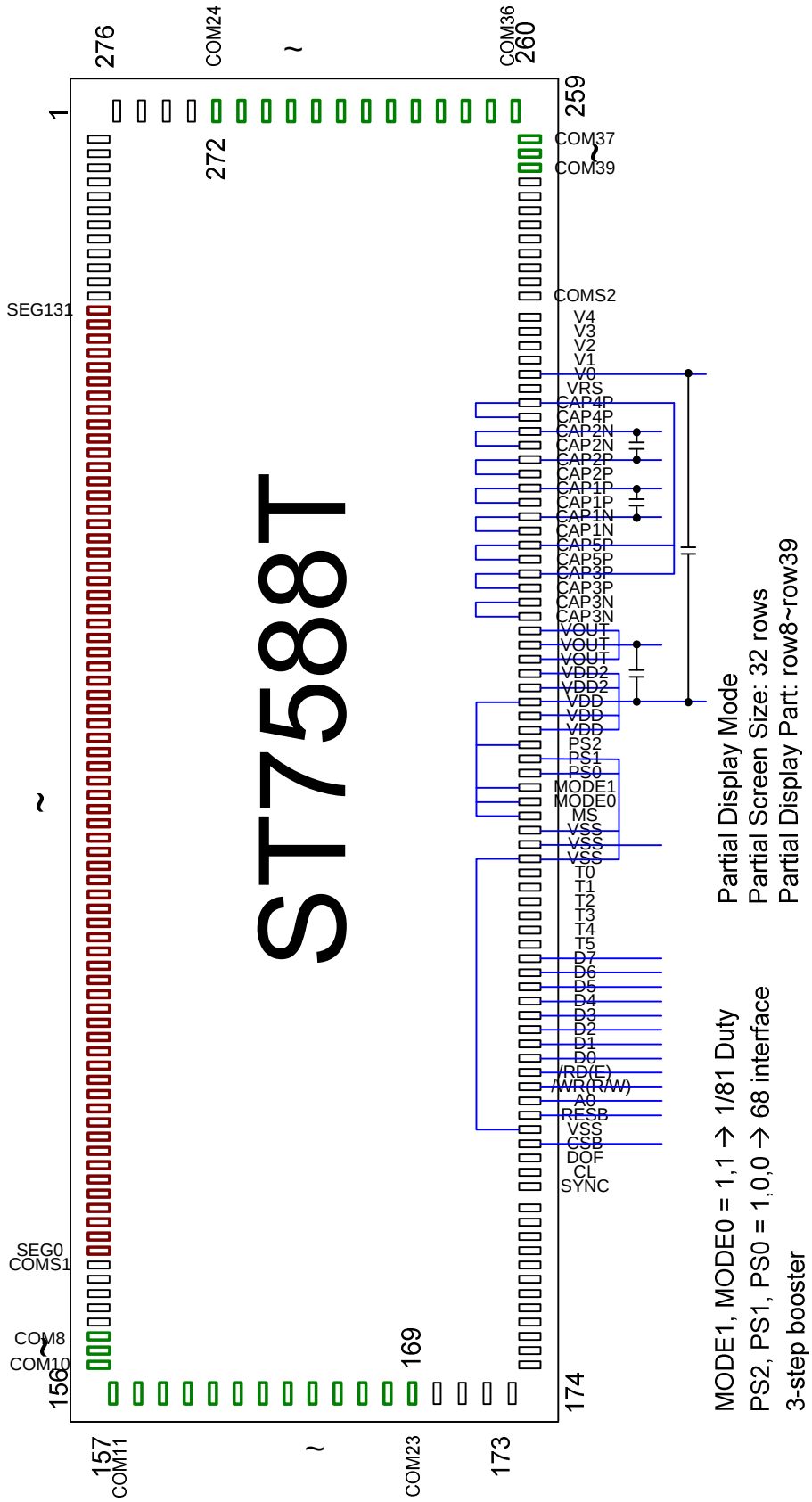


(8) Using the Serial Interface (I^2C interface)

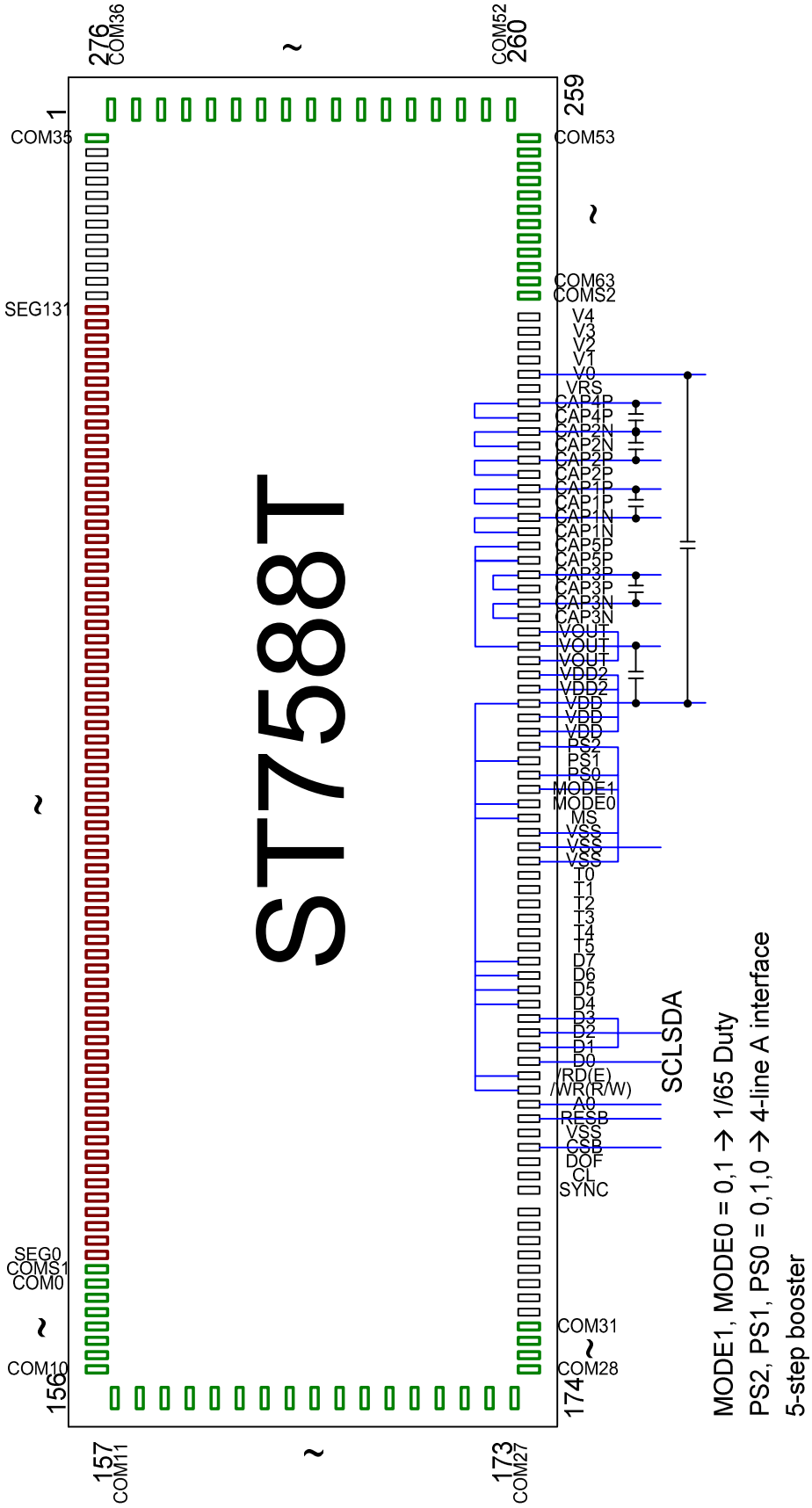


n APPLICATION CIRCUITS

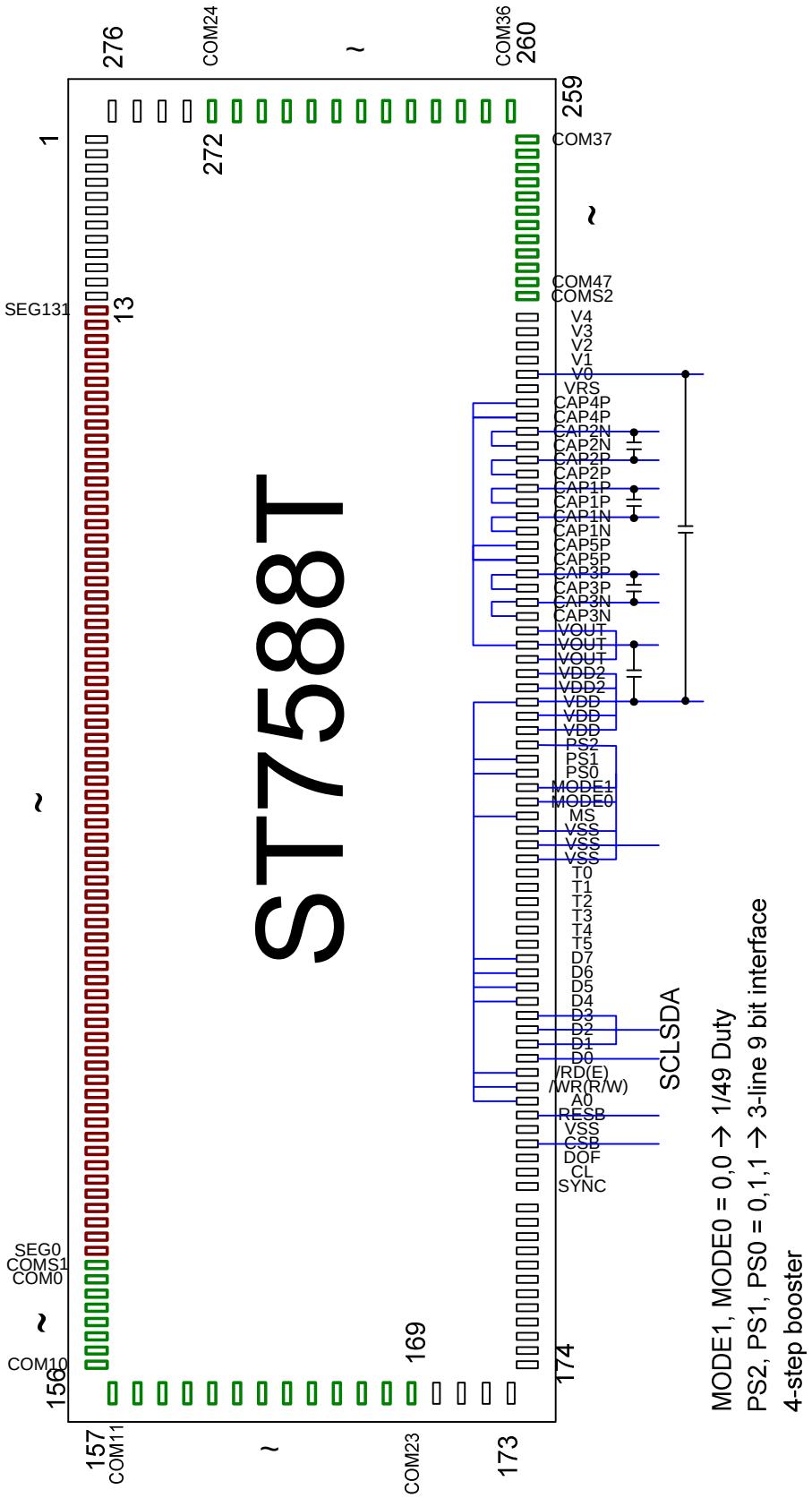
For the 6800 interface & 32 duty (partial display)



For the 4-line A interface & 65 duty

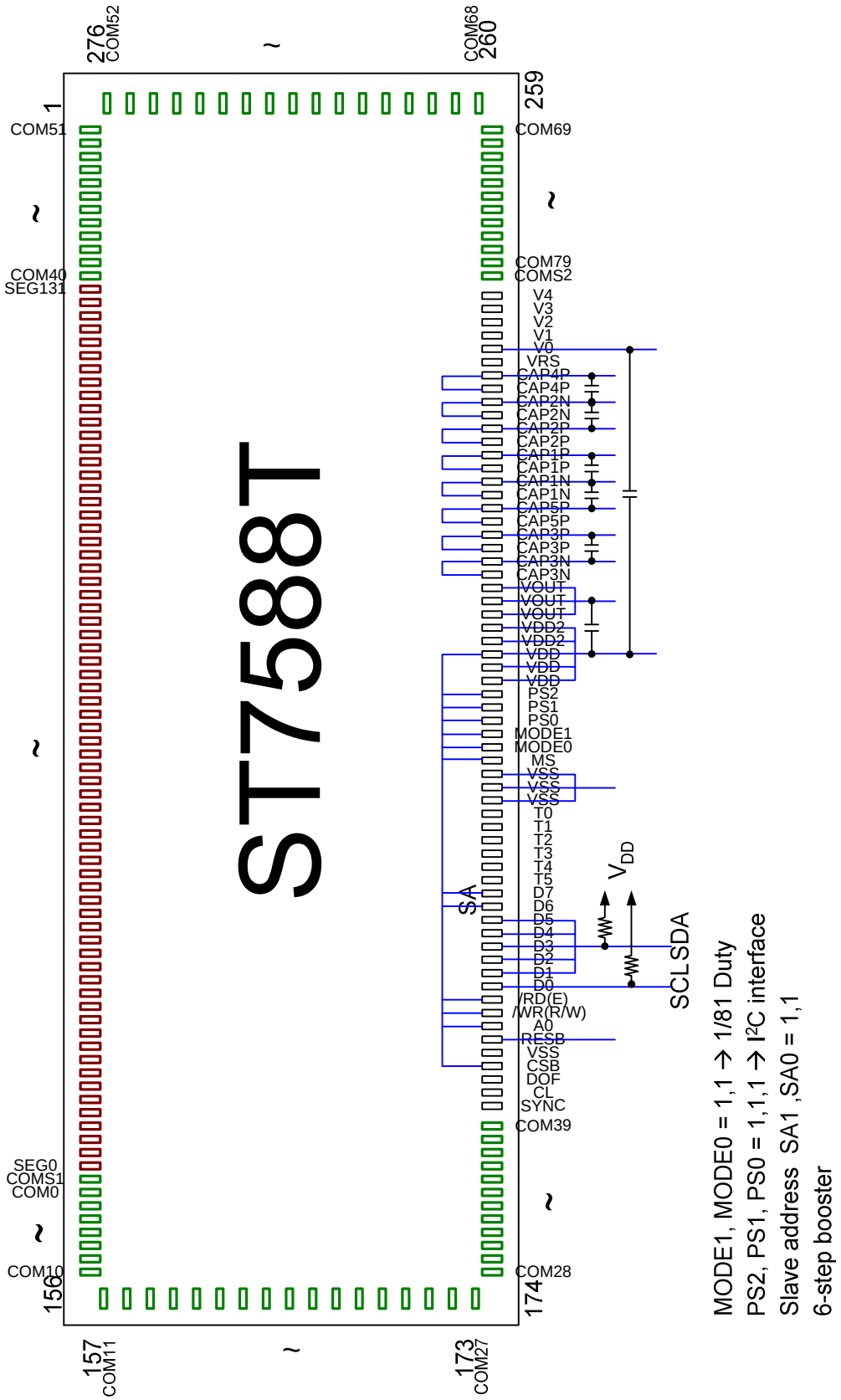


For the 3-line 9 bit interface & 49 duty



For the I²C interface & 81 duty

In I²C application, be awarded that the impedance of SDAs and GNDs should be treated as the POWER PIN.



n REVERSION HISTORY

Version	Data	Description
1.0	2005/08/01	1. Remove “Preliminary”. 2. Update I^2C SCL clock frequency.
1.1	2005/11/11	1. Chip thickness. 2. Redraw some figures. 3. Bias default value BS[2:0]=010. 4. Update V_{DD2} range.
1.2	2005/12/22	1. Remove History before V1.0.
1.2a	2005/12/29	1. Add voltage endurance warning to Booster Connection.
1.3	2007/09/20	1. Fix description mistake. 2. Remove Master-Slave related sections. Master-Slave function is reserved for special specification by customer. 3. Redraw timing figures. 4. Remove I^2C timing at 1.8V. 5. Fix Power Save flow mistake.