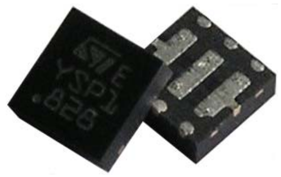
SPT01-335DEE

Automation sensor transient and overvoltage protection

Datasheet − production data



QFN 3x3 6+3 lead
SPT01-235DEE

Figure 1. SPT01-335 configuration diagram

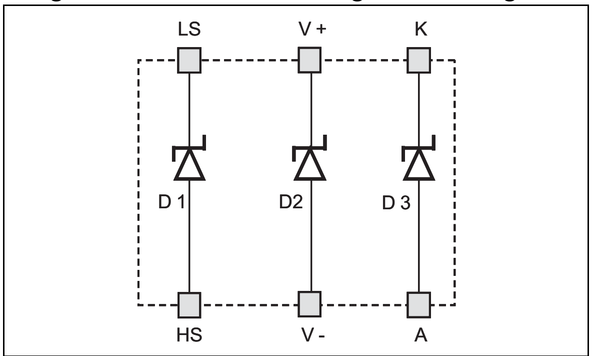
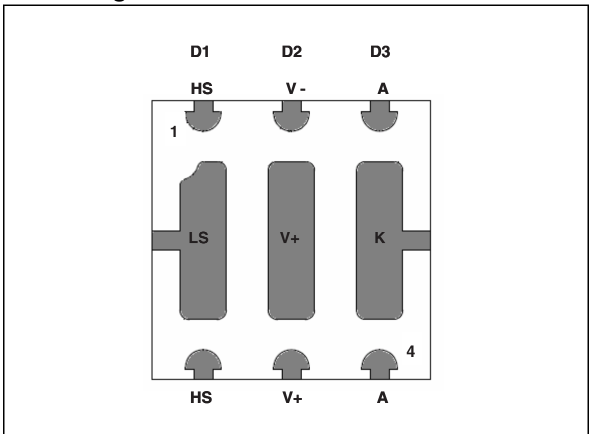


Figure 2. SPT01-335 bottom view



Features

- Triple diode array for power bus protection, switch protection and reverse blocking protection
- Flexible connection for NPN low side or PNP high side sensor configuration
- 6 V to 36 V supply voltage range
- Stand-off voltage: 36 V
- Minimum breakdown voltage V_{BR}: 38 V
- 8/20 µs 2A maximum clamping voltage: 46 V
- Direct sensor switch current: 300 mA
- Blocking diode drop forward voltage V_F: 1 V at 300 mA
- Blocking diode maximum 10 ms square pulse current I_{FSM}: 1 A
- Ambient temperature: -40 °C to +100 °C
- QFN3x3-6L 1 mm flat package: 3x3 mm
- Voltage surge: EN 60947-5-2 or IEC 61000-4-5 with R_{CC} = 500 Ω: ±1 kV
- Electrostatic discharge ESD, IEC 61000-4-2: ± 8 kV in contact, ± 15 kV in air
- Electrical transient immunity, IEC 61000-4-4: ±2 kV

Benefits

- Compliant for interface with logic input type 1, 2 and 3 IEC 61131-2 standard
- Recommended to protect any 3-wire sensor compliant with EN 60947-5-2 standard
- Highly compact with integrated power solution in SMD version

Applications

- Factory automation sensor application
- Proximity sensor interface protection
- Transient and surge voltage protection
- Compliant with sensor standard, EN60947-5-2

1 Description

The SPT01-335 is specifically designed for the protection of 24 V proximity sensors. It implements the reverse polarity and the overvoltage protection of the sensor power supply and the power switch overvoltage protection.

It provides a very compact and flexible solution offering two connections for PNP or NPN sensors as shown in *Figure 8* and *Figure 9*.

Thanks to high performance ST technology, the SPT01-335 protects the proximity sensor to the highest level compliant with IEC 61000-4-2, IEC 61000-4-4 and IEC 60947-5-2 / IEC 61000-4-5 standards.

2 Characteristics

Table 1. Pinout connections (see *Figure 2*)

Pin #	Name	Description
Exposed pad aligned with pins 1 and 6	LS	D1 Power bus protection diode cathode
1, 6	HS	D1 Power bus protection diode anode
5, Exposed pad aligned with pins 2 and 5	V+	D2 sensor switch protection diode cathode; pin 5 internally connected to mid pad
2	V-	D2 sensor switch protection diode anode
Exposed pad aligned with pins 3 and 4	K	D3 reverse blocking protection diode cathode
3, 4	A	D3 reverse blocking protection diode anode

Table 2. Absolute ratings (T_{amb} = 25 °C)

Symbol	Diode	Parameter	Value	Unit
V_{PP}	All	ESD protection, IEC 61000-4-2, per diode, in air (1)	15	kV
		ESD protection, IEC 61000-4-2, per diode, in contact (1)	8	kV
V_{PP}	All	Peak Surge Voltage, IEC 61000-4-5, per diode, R_{CC} = 500 Ω, (1)	1	kV
I_{PP}	All	Peak pulse forward and reverse current, t_p = 8/20 µs	2	A
P_{PP}	All	Peak pulse power dissipation, $T_J = T_{amb}$ = 100 °C, t_P = 8/20 µs	100	W
I_{FSM}	All	Maximum forward surge current, t_P = 10 ms square	1	A
E_{AR}	D1	Maximum repetitive avalanche energy L = 1 H, I_{RAS} = 0.3 A, R_S = 100 Ω, V_{CC} = 30 V,T_{amb} = 85 °C(1)	60	mJ
T_J	All	Storage junction temperature range	- 40 to 175	°C

1. See system oriented test circuits in *Figure 11* (ESD) and *Figure 10* (Surge as also described in
IEC 60947-5-2).

Table 3. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Operating power bus supply voltage	-30 to 36	V
	Pulse repetitive voltage t_P = 0.5 s, R_{CC} = 500 Ω	-30 to 35	V
I_F	D3 forward peak current T_j = 150 °C duty cycle = 50%	300	mA
T_{amb}	Operating ambient temperature range	-40 to 100	°C
T_J	Operating junction temperature range(1)	-40 to 175	°C

1. Extended from DC operating at 150 °C up to peak repetitive value during the inductive load demagnetization

Table 4. Electrical characteristics (T_J = 25 °C, unless otherwise specified)

Symbol	Diode	Name	Test conditions		Value	Unit
V_{RM}	All	Reverse stand off voltage[(1)]	I_R = 0.2 µA	Min	33	V
			I_R = 1 µA	Min	36	V
I_{RM}	All	Leakage reverse current	V_{RM} = 33 V	Max	0.2	µA
			V_{RM} = 33 V, T_J = 150 °C	Max	1	µA
V_{BR}	All	Reverse breakdown voltage	I_R = 1 mA	Min	38	V
				Typ	41.4	V
V_{CL}	All	Peak clamping voltage	I_{PP} = 2 A, t_P = 8 /20 µs	Max	46	V
				Typ	44	V
R_D	All	8/20µs dynamic resistance		Typ	0.5	Ω
αT	All	V_{BR} Temperature sensitivity		Max	10	10^{-4} /°C
V_{CL}	D1	Peak clamping voltage	I_R = 0.3 A, L = 1 H, t_P = 8 /20 µs, V_{CC} = 30 V	Max	46	V
V_F	D3	Forward drop voltage	I_F = 300 mA	Max	1	V

1. Reverse stand-off voltage is valid for ambient temperature within the operating temperature range.

Table 5. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	SMD thermal resistance junction to ambient, per diode FR4 board, copper thickness = 35 µm, S_{Cu} = 0.85 mm²	330	°C/W
$Z_{th(j-a)}$	SMD thermal transient impedance junction to ambient, per diode t_p = 15 ms, T_{amb} = 85 °C, S_{Cu} = 0.85 mm²	20	°C/W

Figure 3. Relative variation of peak pulse power versus initial junction temperature

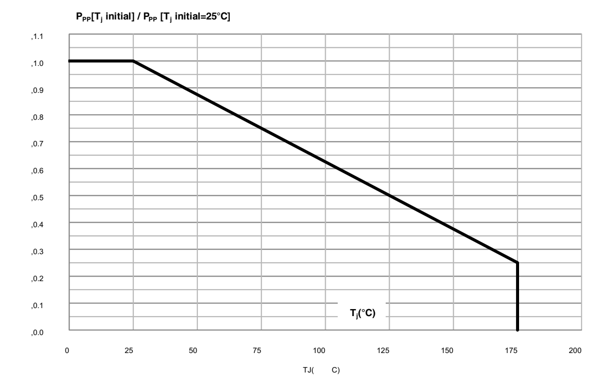


Figure 4. Peak pulse power versus exponential pulse duration (typical values)

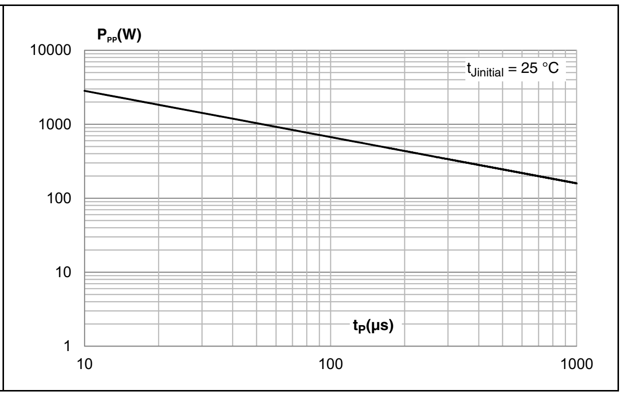


Figure 5. Clamping voltage versus peak pulse current (typical values)

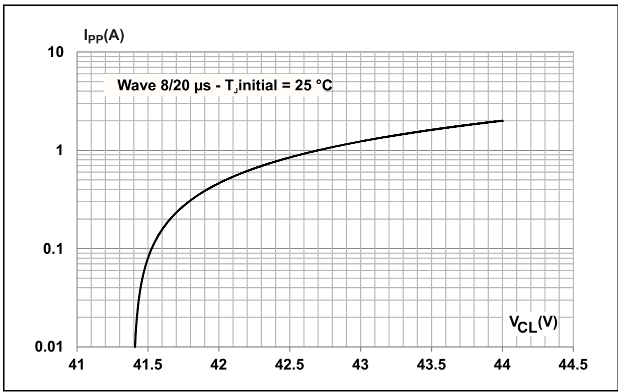


Figure 6. Forward voltage drop versus peak forward current (typical values)

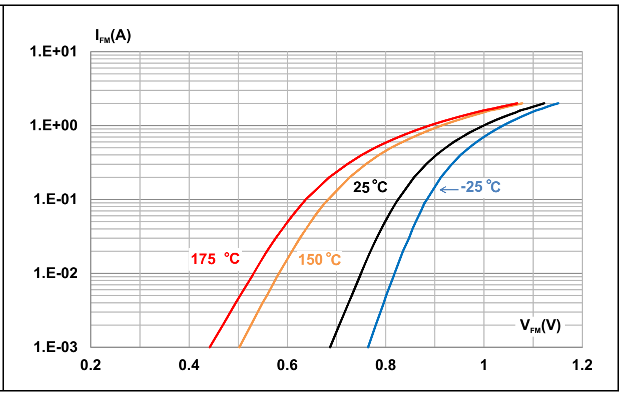
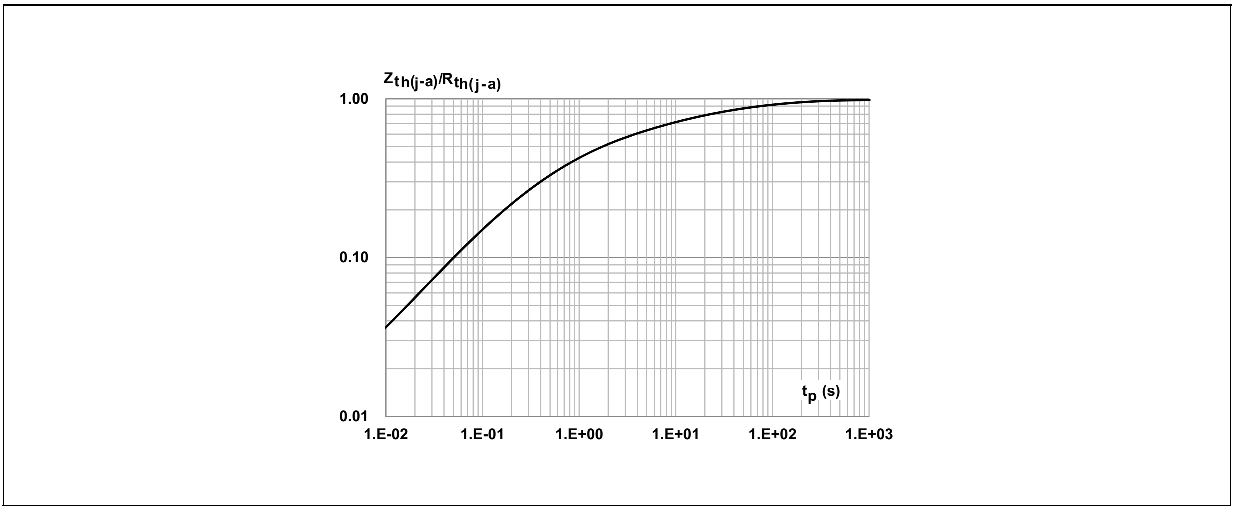


Figure 7. Relative variation of thermal impedance junction to ambient versus pulse duration (printed circuit board)



3 SPT01-335 basic application

Figure 8. PNP high side sensor configuration

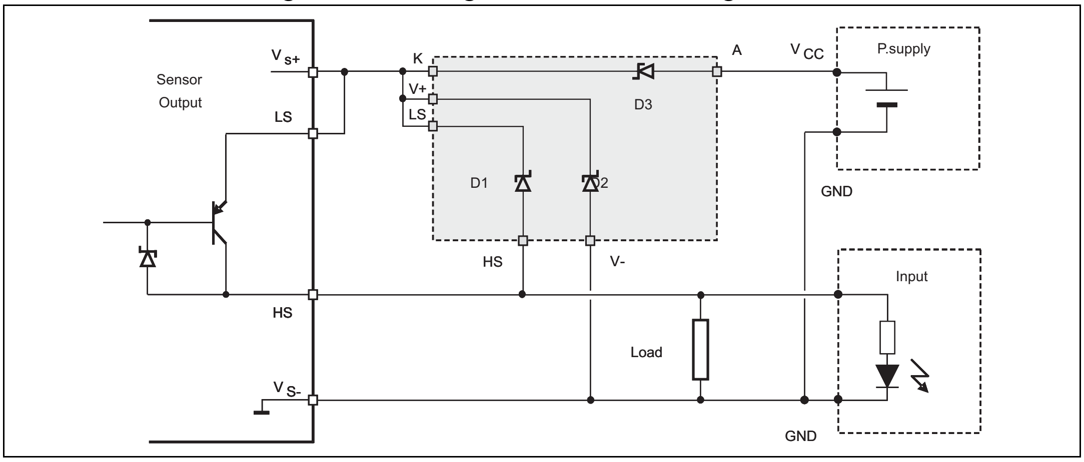


Figure 9. NPN low side sensor configuration

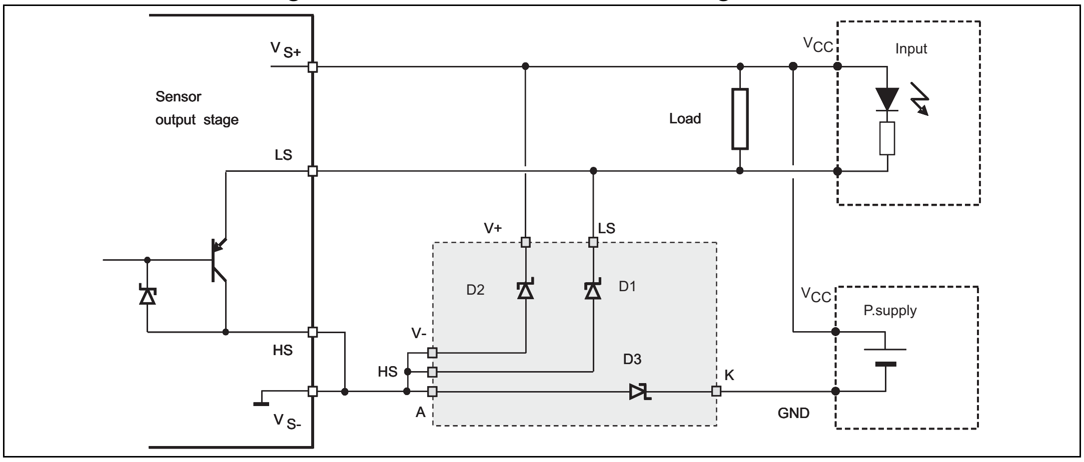


Table 6. SPT01-335 pin connection versus sensor output stage configuration as shown on *Figure 8.* and *Figure 9*

Sensor type	SPT01-335 terminal connection					
	LS	**HS**	**A**	**K**	**V+**	**V-**
PNP	To V_{S+}	Sensor HS	V_{CC}	To V_{S+}	Sensor V_{S+}	Sensor V_{S-}
NPN	Sensor LS	To V_{S-}	To V_{S-}	To GND		

Note: *It is advised to use diodes D1 and D3, which are the external devices in the package, as switch overvoltage protection and power supply reverse polarity protection since they allow better cooling design with PCB pad implementation. D2, the middle diode, can be dedicated to the power supply overvoltage protection because it would run only in pulse mode with basic PCB pad footprint.*

4 System related electromagnetic compatibility ratings

Refer to *Table 3* for test performance.

Figure 10. Surge Voltage test circuit according to IEC 61000-4-5 with 500 Ω serial resistor

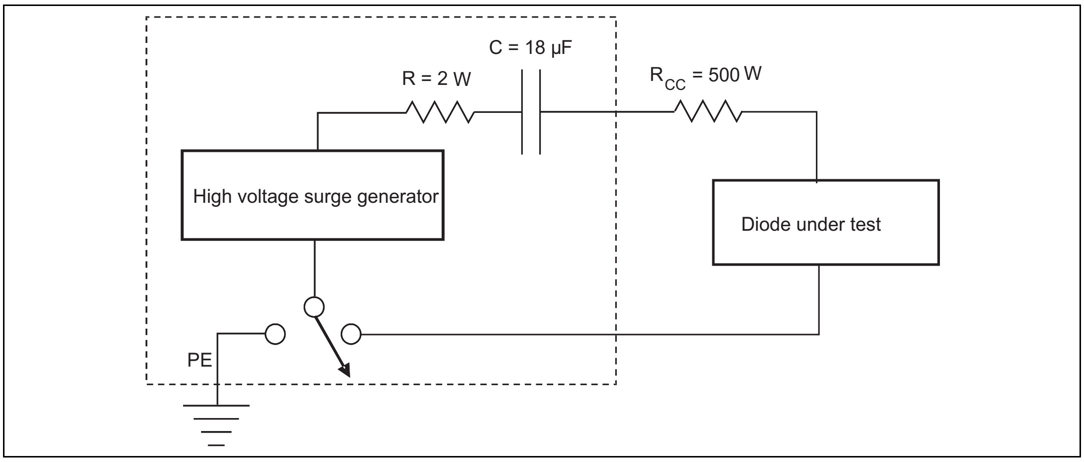
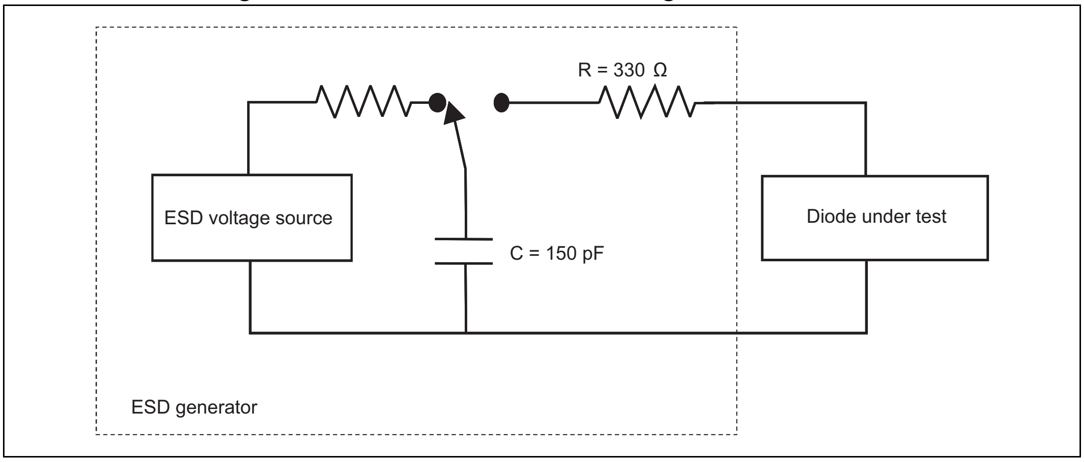


Figure 11. ESD test circuit according to IE 61000-4-2



5 Evaluation of the clamping voltage

V_{BR} $(T_J) = V_{BR}$ (25) x (1+ αT (T_J – 25))

$V_{CL\ MAX}$ (8/20 µs) = $V_{BR\ MAX}$ + R_D x I_{PP}

5.1 Application considerations

5.1.1 Demagnetization of an inductive load driven by the switch protection diode

The turn off energy E_{OFF} that could be dissipated in the D_1 diode is calculated as shown in AN587 and AN1351 application notes:

$E_{OFF} = V_{BR}$ x L x [V_{CC} + (V_{CC} - V_{BR}) x ln (V_{BR} / (V_{BR} - V_{CC}))] / $(R_S)^2$

t_{OFF} = L x ln (V_{BR} / (V_{BR} - V_{CC})) / R_S

$P_{OFF} = E_{OFF} / t_{OFF}$

With L = 1 H; I = 0.3 A; V_{BR} = 39 V; V_{CC} = 30 V, R_S = 100 Ω the stress withstood by D_1 becomes:

E_{OFF} = 65 mJ; t_{OFF} = 15 ms; P_{OFF} = 4.3 W

In a single pulse mode operation, the junction temperature can be fairly estimated:

$T_J = T_{amb}$ + [Z_{th} (t_{OFF}) x P_{OFF}]

In a repetitive operation with an F repetitive rate,

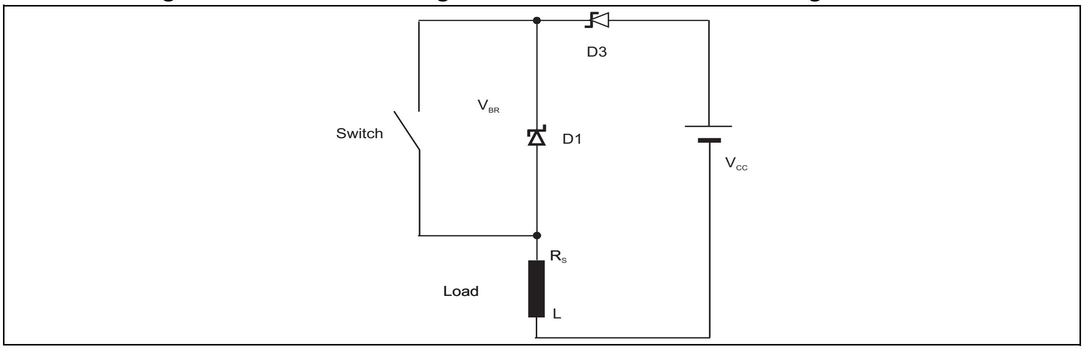
$P_{AV} = E_{OFF}$ x F

$T_{(J\_AV)} = T_{amb} + P_{AV}$ x $R_{th(j-a)}$

And during the demagnetization t_{OFF}, $T_{J\_PK} < T_{J\_AV} + P_{OFF}$ x Z_{th} (t_{OFF})

Z_{TH} is the transient thermal impedance of each diode for a pulse having a duration t_{OFF}.

Figure 12. Electrical diagram for inductive load demagnetization



5.1.2 Life time considerations

Life time of the product is calculated to exceed 10 years. The key parameters to consider are the ambient temperature (T_{amb} < 100 °C), the power supply voltage (V_{CC} < 30 V), and the current in the reverse blocking diode (I_F = 0.1 A switching at 0.5 Hz with 50% duty cycle, the stand-by current being less than 1.5 mA).

For higher current or higher switching frequency operation, the life time should be calculated considering the peak and average junction temperature.

This junction temperature can be reduced by reducing the thermal resistance of the clamping diode, D_1 normally. This can be done by increasing its PCB copper tab surface S_{Cu}.

6 Package information

- Epoxy meets UL94,V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 13. QFN 3x3 package dimension definitions

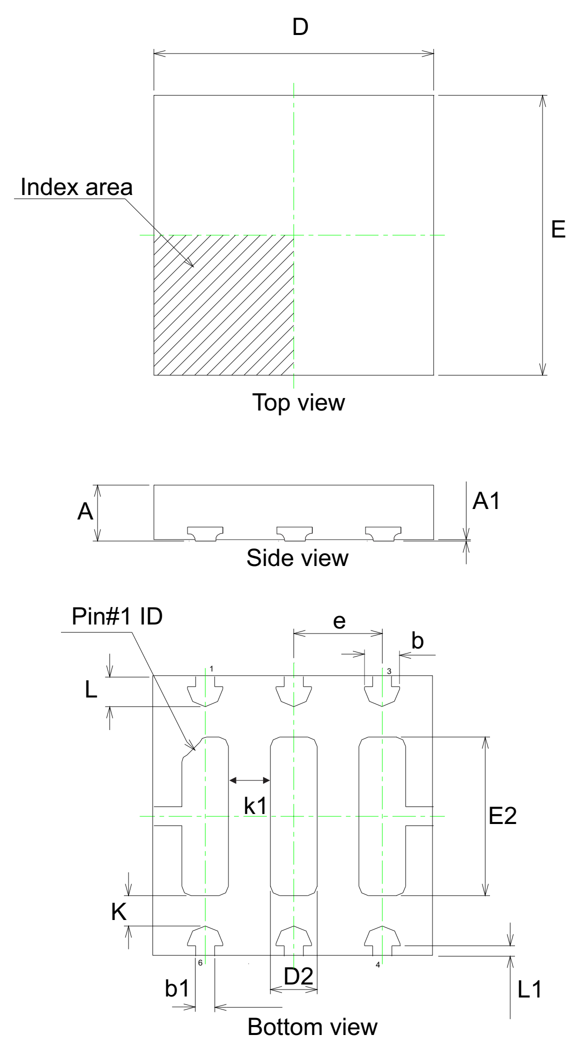
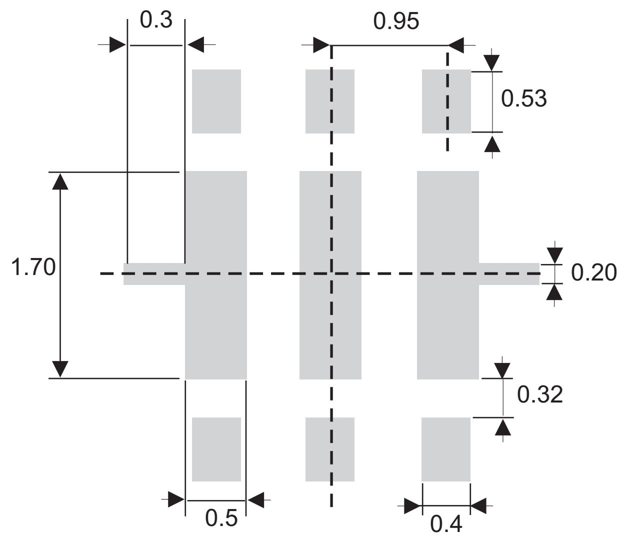


Table 7. QFN 3x3 package dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05		0.0007	
b	0.35	0.40	0.45	0.013	0.015	0.017
b1		0.2			0.007	
D	2.95	3.00	3.05	0.116	0.118	0.12
D2	0.35	0.50	0.60	0.013	0.019	0.023
E	2.95	3.00	3.05	0.116	0.118	0.12
E2	1.55	1.70	1.80	0.06	0.066	0.07
e		0.95			0.037	
k	0.20			0.007		
k1		0.45			0.017	
L	0.22	0.33	0.43	0.008	0.012	0.016
L1		0.11			0.004	

Figure 14. QFN 3x3 footprint (mm)

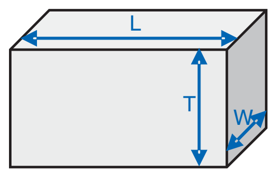


7 Recommendation on PCB assembly

7.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 15. Stencil opening dimensions



   b) General design rule

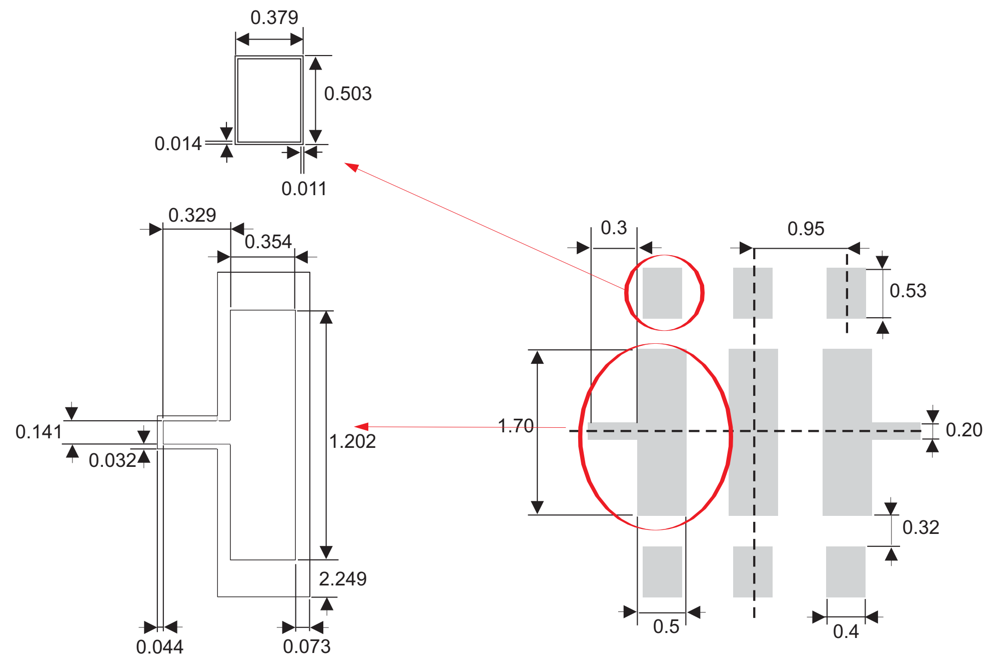
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1{,}5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0{,}66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 16. Recommended stencil window position



7.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

7.3 Placement

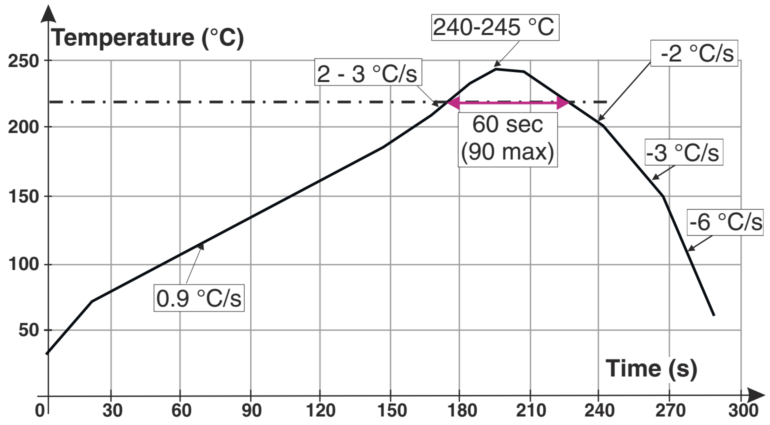
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

7.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

7.5 Reflow profile

Figure 17. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

8 Ordering information

Figure 18. Ordering information scheme

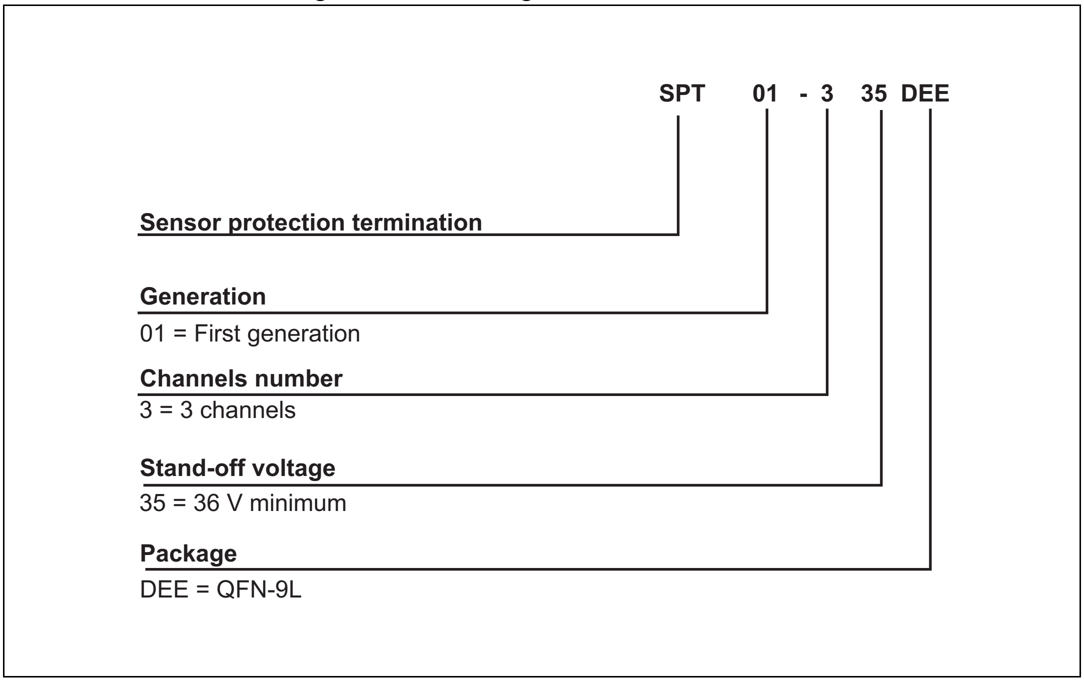


Table 8. Ordering information

Order code	Marking	Package	Weight	Packing
SPT01-335DEE	SP1	QFN 3x3	22.71 mg	Tape and reel

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Nov-2008	1	First issue
19-Mar-2012	2	Added UL statement in *Chapter 6*
03-May-2013	3	Updated features, *Table 3*, *Table 4*, *Figure 17* and *Figure 18*.