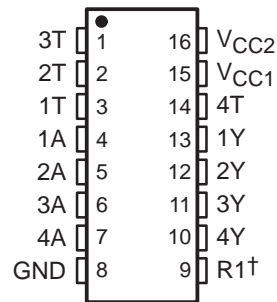


SN75154 QUADRUPLE LINE RECEIVER

SLLS083B – NOVEMBER 1970 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-232-E and ITU Recommendation V.28
- Input Resistance . . . 3 k Ω to 7 k Ω Over Full EIA/TIA-232-E Voltage Range
- Input Threshold Adjustable to Meet Fail-Safe Requirements Without Using External Components
- Built-In Hysteresis for Increased Noise Immunity
- Inverting Output Compatible With TTL
- Output With Active Pullup for Symmetrical Switching Speeds
- Standard Supply Voltages . . . 5 V or 12 V

D OR N PACKAGE
(TOP VIEW)



† For function of R1, see schematic

description

The SN75154 is a monolithic low-power Schottky line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI Standard EIA/TIA-232-E. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5-V supply; however, a built-in option allows operation from a 12-V supply without the use of additional components. The output is compatible with most TTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, even if power is being supplied via the alternate V_{CC2} terminal. This provides a wide hysteresis loop, which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

The SN75154 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

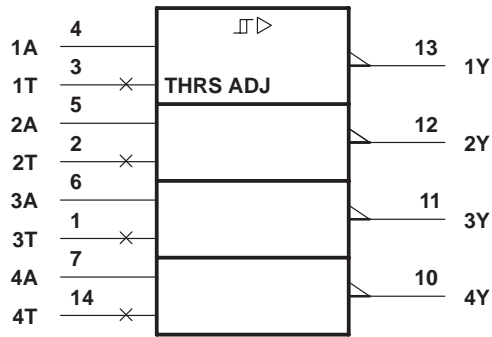
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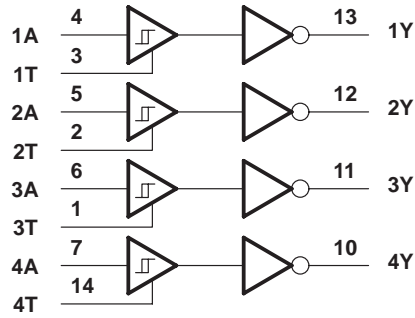
SN75154 QUADRUPLE LINE RECEIVER

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logic symbol†

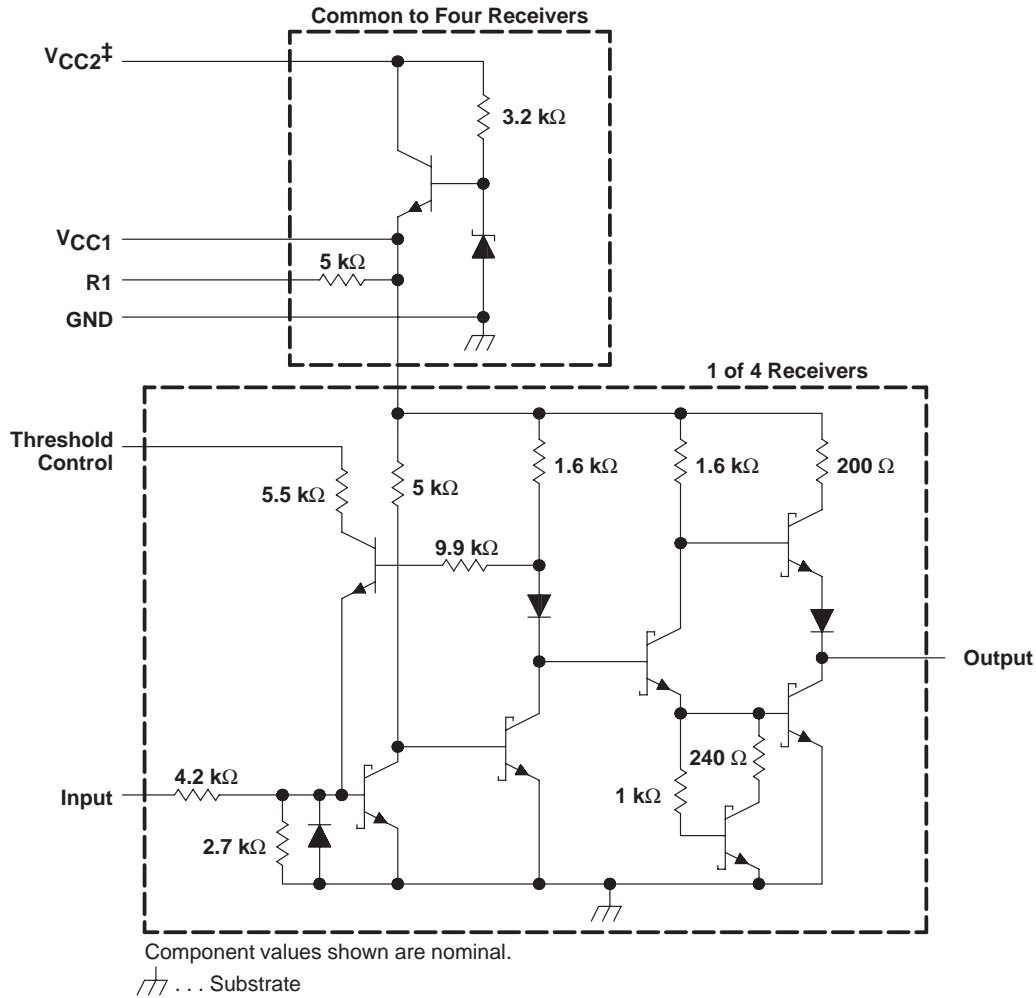


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic



‡ When V_{CC1} is used, V_{CC2} may be left open or shorted to V_{CC1} . When V_{CC2} is used, V_{CC1} must be left open or connected to the threshold control pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Normal supply voltage, V_{CC1} (see Note 1)	7 V
Alternate supply voltage, V_{CC2}	14 V
Input voltage, V_I	± 25 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage, V_{CC1}	4.5	5	5.5	V
Alternate supply voltage, V_{CC2}	10.8	12	13.2	V
High-level input voltage, V_{IH} (see Note 2)	3		15	V
Low-level input voltage, V_{IL} (see Note 2)	–15		–3	V
High-level output current, I_{OH}			–400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	1	Normal operation	0.8	2.2	3	V
			Fail-safe operation	0.8	2.2	3	
V _{IT-}	Negative-going input threshold voltage	1	Normal operation	-3	-1.1	0	V
			Fail-safe operation	0.8	1.4	3	
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})	1	Normal operation	0.8	3.3	6	V
			Fail-safe operation	0	0.8	2.2	
V _{OH}	High-level output voltage	1	I _{OH} = -400 μA	2.4	3.5		V
V _{OL}	Low-level output voltage	1	I _{OL} = 16 mA		0.29	0.4	V
r _i	Input resistance	2	ΔV _I = -25 V to -14 V	3	5	7	kΩ
			ΔV _I = -14 V to -3 V	3	5	7	
			ΔV _I = -3 V to 3 V	3	6	8	
			ΔV _I = 3 V to 14 V	3	5	7	
			ΔV _I = 14 V to 25 V	3	5	7	
V _{I(open)}	Open-circuit input voltage	3	I _I = 0	0	0.2	2	V
I _{OS}	Short-circuit output current‡	4	V _{CC1} = 5.5 V, V _I = -5 V	-10	-20	-40	mA
I _{CC1}	Supply current from V _{CC1}	5	V _{CC1} = 5.5 V, T _A = 25°C		20	35	mA
I _{CC2}	Supply current from V _{CC2}		V _{CC2} = 13.2 V, T _A = 25°C		23	40	

† All typical values are at V_{CC1} = 5 V, T_A = 25°C.

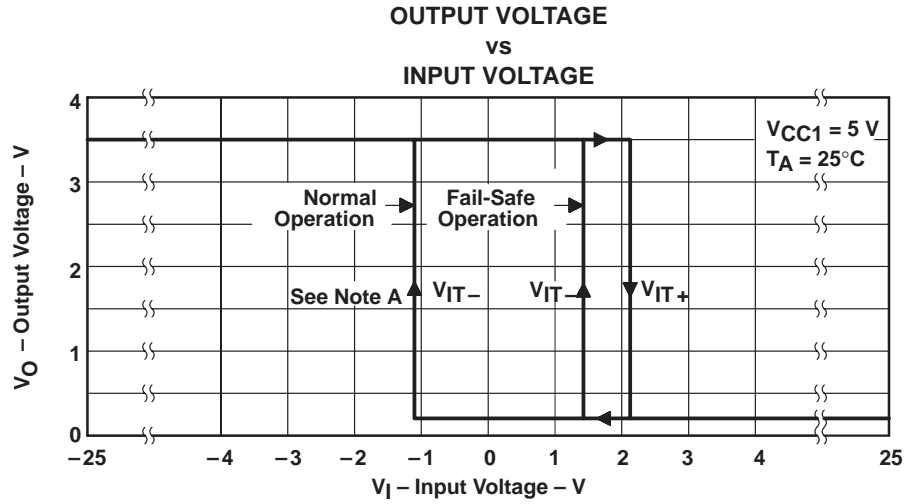
‡ Not more than one output should be shorted at a time.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	6	C _L = 50 pF, R _L = 390 Ω		11		ns
t _{PHL}	Propagation delay time, high- to low-level output				8		ns
t _{TLH}	Transition time, low- to high-level output				7		ns
t _{THL}	Transition time, high- to low-level output				2.2		ns



TYPICAL CHARACTERISTICS



NOTE A: For normal operation, the threshold controls are connected to V_{CC1} . For fail-safe operation, the threshold controls are open.

Figure 1

SN75154 QUADRUPLE LINE RECEIVER

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PARAMETER MEASUREMENT INFORMATION

dc test circuits†

TEST TABLE

TEST	MEASURE	A	T	Y	V _{CC1}	V _{CC2}
Open-circuit input (fail safe)	V _{OH}	Open	Open	I _{OH}	4.5 V	Open
	V _{OH}	Open	Open	I _{OH}	Open	10.8 V
V _{IT+} min, V _{IT-} min (fail safe)	V _{OH}	0.8 V	Open	I _{OH}	5.5 V	Open
	V _{OH}	0.8 V	Open	I _{OH}	Open	13.2 V
V _{IT+} min (normal)	V _{OH}	Note A	V _{CC1}	I _{OH}	5.5 V and T	Open
	V _{OH}	Note A	V _{CC1}	I _{OH}	T	13.2 V
V _{IL} max, V _{IT+} min (normal)	V _{OH}	-3 V	V _{CC1}	I _{OH}	5.5 V and T	Open
	V _{OH}	-3 V	V _{CC1}	I _{OH}	T	13.2 V
V _{IH} min, V _{IT+} max, V _{IT-} max (fail safe)	V _{OL}	3 V	Open	I _{OL}	4.5 V	Open
	V _{OL}	3 V	Open	I _{OL}	Open	10.8 V
V _{IH} min, V _{IT+} max (normal)	V _{OL}	3 V	V _{CC1}	I _{OL}	4.5 V and T	Open
	V _{OL}	3 V	V _{CC1}	I _{OL}	T	10.8 V
V _{IT-} max (normal)	V _{OL}	Note B	V _{CC1}	I _{OL}	5.5 V and T	Open
	V _{OL}	Note B	V _{CC1}	I _{OL}	T	13.2 V

NOTES: A. Momentarily apply -5 V, then 0.8 V.
B. Momentarily apply 5 V, then GND.

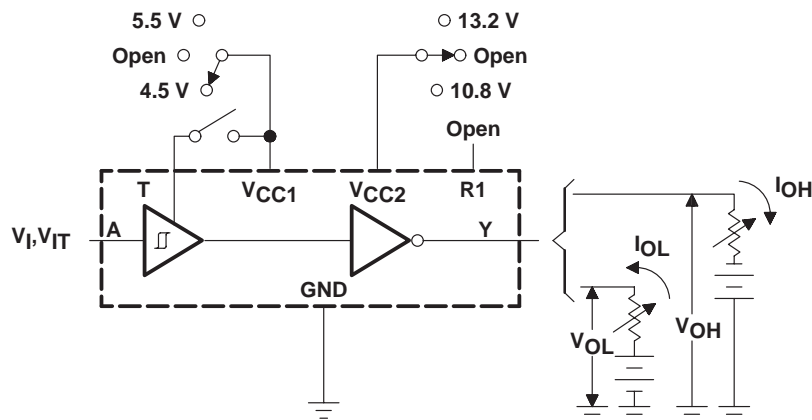
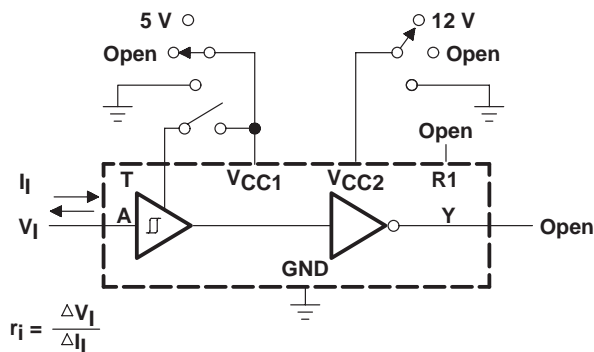


Figure 2. V_{IH}, V_{IL}, V_{IT+}, V_{IT-}, V_{OH}, V_{OL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

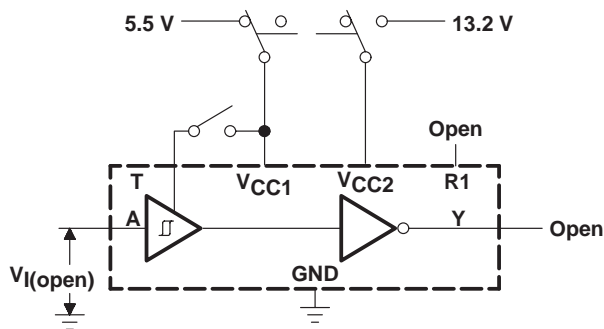
PARAMETER MEASUREMENT INFORMATION

dc test circuits† (continued)



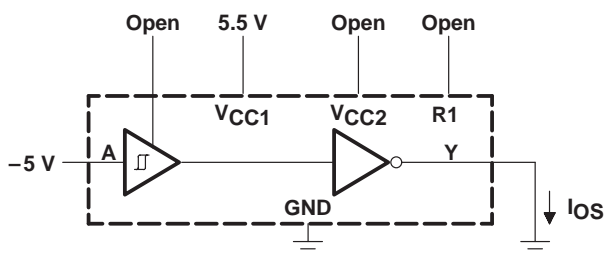
TEST TABLE		
T	V _{CC1}	V _{CC2}
Open	5 V	Open
Open	GND	Open
Open	Open	Open
V _{CC1}	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
V _{CC1}	T	12 V
V _{CC1}	T	GND
V _{CC1}	T	Open

Figure 3. Input Resistance



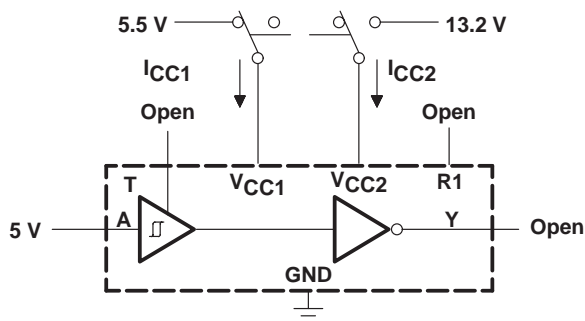
TEST TABLE		
T	V _{CC1}	V _{CC2}
Open	5.5 V	Open
V _{CC1}	5.5 V	Open
Open	Open	13.2 V
V _{CC1}	T	13.2 V

Figure 4. Input Voltage (Open)



Each output is tested separately.

Figure 5. Output Short-Circuit Current



All four line receivers are tested simultaneously.

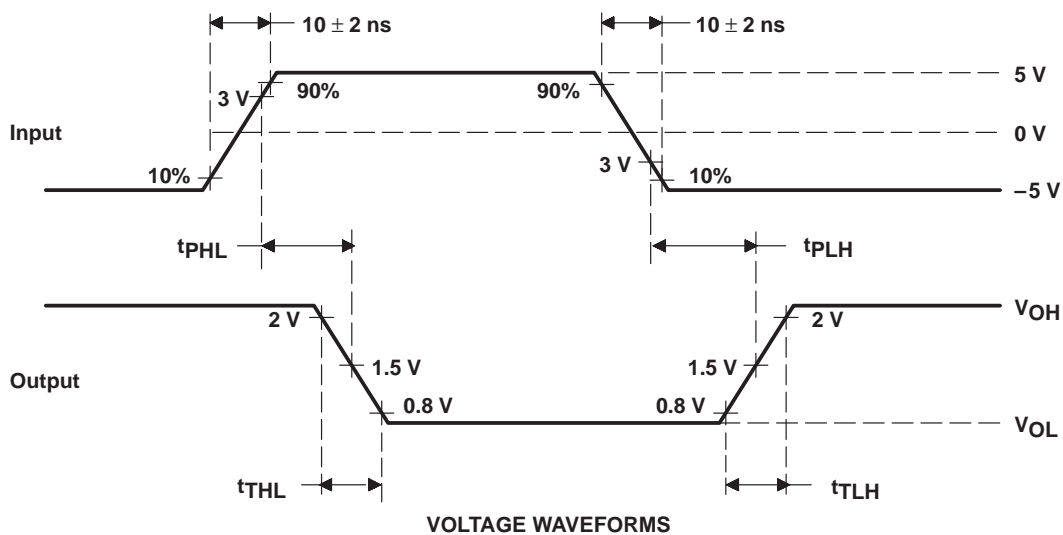
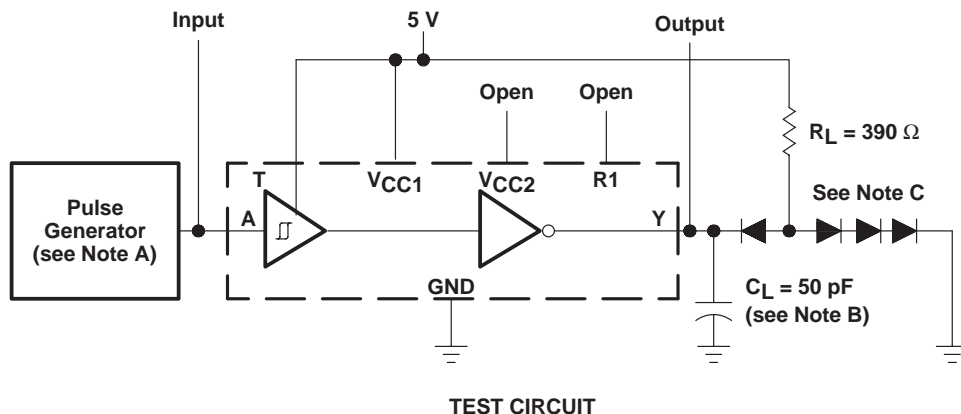
Figure 6. Supply Current

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

SN75154 QUADRUPLE LINE RECEIVER

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, $t_w \leq 200 \text{ ns}$, duty cycle $\leq 20\%$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064.

Figure 6. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75154D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75154	Samples
SN75154DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75154	Samples
SN75154DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75154	Samples
SN75154DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75154	Samples
SN75154N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75154N	Samples
SN75154NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75154N	Samples
SN75154NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75154	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75154DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75154NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75154DR	SOIC	D	16	2500	333.2	345.9	28.6
SN75154NSR	SO	NS	16	2000	367.0	367.0	38.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.



4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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