- **Member of the Texas Instruments** Widebus™ Family
- **UBT™ Transceiver Combines D-Type** Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or **Clocked Modes**
- **OEC™** Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference (EMI)
- Compliant With VME64, 2eVME, and 2eSST **Protocols**
- **Bus Transceiver Split LVTTL Port Provides** Feedback Path for Control and Diagnostics Monitorina
- I/O Interfaces Are 5-V Tolerant
- B-Port Outputs (-48 mA/64 mA)
- Y and A-Port Outputs (-12 mA/12 mA)
- I_{off}, Power-Up 3-State, and BIAS V_{CC} **Support Live Insertion**
- **Bus Hold on 3A-Port Data Inputs**
- 26- Ω Equivalent Series Resistor on 3A Ports and Y Outputs
- Flow-Through Architecture Facilitates **Printed Circuit Board Layout**
- Distributed V_{CC} and GND Pins Minimize **High-Speed Switching Noise**
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGG OR DGV PACKAGE (TOP VIEW) 1OEBY 48**∏** 10EAB 47 🛮 V_{CC} 1A 🛮 2 1Y 🛮 3 46 1B GND 4 45 GND 2A ∏ 5 44 BIAS V_{CC} 2Y | 6 43 2B V_{CC} L 42 V_{CC} 2OEBY 41 20EAB 40**[**] 3B1 3A1 [] GND 10 39 GND LE ∏ 11 38 V_{CC} 37 3B2 3A2 🛮 12 3A3 🛮 13 36 3B3 <u>OF</u> Π 14 35 V_{CC} **GND** 15 34 GND 3A4 🛮 16 33**∏** 3B4 CLKBA 17 32 CLKAB 31 V_{CC} V_{CC} 🛚 18 30 3B5 3A5 🛮 19 3A6 **∏** 20 29 **∏** 3B6 GND [] 21 28 GND 3A7 🛮 22 27**∏** 3B7 3A8 **1**23 26 ¶ 3B8 25 V_{CC} DIR **1** 24

description/ordering information

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	TSSOP – DGG	Tape and reel	SN74VMEH22501ADGGR	VMEH22501A
-40°C to 85°C	TVSOP - DGV	Tape and reel	SN74VMEH22501ADGVR	VK501A
	VFBGA – GQL	Tape and reel	SN74VMEH22501AGQLR	VK501A

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Motorola is a trademark of Motorola, Inc.

OEC, UBT, and Widebus are trademarks of Texas Instruments



description/ordering information (continued)

The SN74VMEH22501A 8-bit universal bus transceiver has two integral 1-bit three-wire bus transceivers and is designed for 3.3-V V_{CC} operation with 5-V tolerant inputs. The UBT™ transceiver allows transparent, latched, and flip-flop modes of data transfer, and the separate LVTTL input and outputs on the bus transceivers provide a feedback path for control and diagnostics monitoring. This device provides a high-speed interface between cards operating at LVTTL logic levels and VME64, VME64x, or VME320[†] backplane topologies.

The SN74VMEH22501A is pin-for-pin capatible to the VMEH22501, but operates at a wider operating temperature (-40°C to 85°C) range.

High-speed backplane operation is a direct result of the improved OEC™ circuitry and high drive that has been designed and tested into the VME64x backplane model. The B-port I/Os are optimized for driving large capacitive loads and include pseudo-ETL input thresholds (1/2 V_{CC} ±50 mV) for increased noise immunity. These specifications support the 2eVME protocols in VME64x (ANSI/VITA 1.1) and 2eSST protocols in VITA 1.5. With proper design of a 21-slot VME system, a designer can achieve 320-Mbyte transfer rates on linear backplanes and, possibly, 1-Gbyte transfer rates on the VME320 backplane.

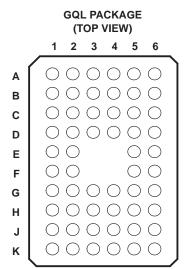
All inputs and outputs are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.

Active bus-hold circuitry holds unused or undriven 3A-port inputs at a valid logic state. Bus-hold circuitry is not provided on 1A or 2A inputs, any B-port input, or any control input. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for live-insertion applications using Ioff, power-up 3-state, and BIAS VCC. The Ioff circuitry prevents damaging current to backflow through the device when it is powered off/on. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, output-enable (OE and OEBY) inputs should be tied to V_{CC} through a pullup resistor and output-enable (OEAB) inputs should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the drive capability of the device connected to this input.

[†] VME320 is a patented backplane construction by Arizona Digital, Inc.



terminal assignments

	1	2	3	4	5	6
Α	1OEBY	NC	NC	NC	NC	10EAB
В	1Y	1A	GND	GND	Vcc	1B
С	2Y	2A	Vcc	Vcc	BIAS V _{CC}	2B
D	3A1	2OEBY	GND	GND	20EAB	3B1
Е	3A2	LE			Vcc	3B2
F	3A3	OE			VCC	3B3
G	3A4	CLKBA	GND	GND	CLKAB	3B4
Н	3A5	3A6	Vcc	Vcc	3B6	3B5
J	3A7	3A8	GND	GND	3B8	3B7
K	DIR	NC	NC	NC	NC	Vcc

NC - No internal connection



SCES620 - DECEMBER 2004

functional description

The SN74VMEH22501A is a high-drive (–48/64 mA), 8-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or flip-flop modes. Data transmission is true logic. The device is uniquely partitioned as 8-bit UBT transceivers with two integrated 1-bit three-wire bus transceivers.

functional description for two 1-bit bus transceivers

The OEAB inputs control the activity of the 1B or 2B port. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are disabled.

Separate 1A and 2A inputs and 1Y and 2Y outputs provide a feedback path for control and diagnostics monitoring. The OEBY inputs control the 1Y or 2Y outputs. When OEBY is low, the Y outputs are active. When OEBY is high, the Y outputs are disabled.

The OEBY and OEAB inputs can be tied together to form a simple direction control where an input high yields A data to B bus and an input low yields B data to Y bus.

1-BIT BUS TRANSCEIVER FUNCTION TABLE

INPUTS		OUTPUT	MODE	
OEAB	OEBY	OUTPUT	MODE	
L	Н	Z	Isolation	
Н	Н	A data to B bus	Torre delicer	
L	L	B data to Y bus	True driver	
Н	L	A data to B bus, B data to Y bus	True driver with feedback path	



functional description for 8-bit UBT transceiver

The 3A and 3B data flow in each direction is controlled by the \overline{OE} and direction-control (DIR) inputs. When \overline{OE} is low, all 3A- or 3B-port outputs are active. When \overline{OE} is high, all 3A- or 3B-port outputs are in the high-impedance state.

FUNCTION TABLE

INP	UTS	OUTDUT		
OE	DIR	ОИТРИТ		
Н	Χ	Z		
L	Н	3A data to 3B bus		
L	L	3B data to 3A bus		

The UBT transceiver functions are controlled by latch-enable (LE) and clock (CLKAB and CLKBA) inputs. For 3A-to-3B data flow, the UBT operates in the transparent mode when LE is high. When LE is low, the 3A data is latched if CLKAB is held at a high or low logic level. If LE is low, the 3A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB.

The UBT transceiver data flow for 3B to 3A is similar to that of 3A to 3B, but uses CLKBA.

UBT TRANSCEIVER FUNCTION TABLE[†]

	INPUTS				Mane		
OE	LE	CLKAB	3A	3B	MODE		
Н	Х	Χ	Χ	Z	Isolation		
L	L	Н	Х	в ₀ ‡			
L	L	L	Χ	В ₀ ‡ В ₀ §	Latched storage of 3A data		
L	Н	Х	L	L	Tour tour and		
L	Н	Χ	Н	Н	True transparent		
L	L	1	L	L	Ole also de terre no est OA de te		
L	L	\uparrow	Н	Н	Clocked storage of 3A data		

^{† 3}A-to-3B data flow is shown; 3B-to-3A data flow is similar, but uses CLKBA.

The UBT transceiver can replace any of the functions shown in Table 1.

Table 1. SN74VMEH22501A UBT Transceiver Replacement Functions

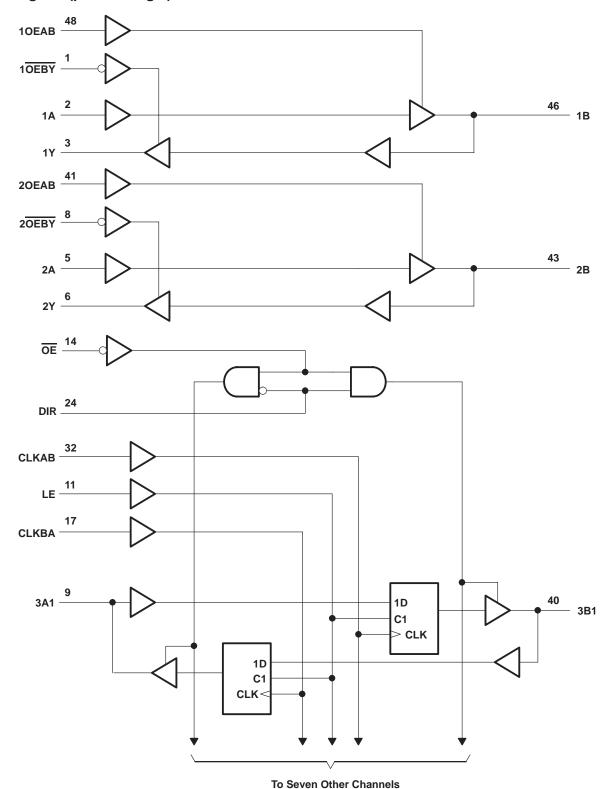
FUNCTION	8 BIT		
Transceiver	'245, '623, '645		
Buffer/driver	'241, '244, '541		
Latched transceiver	'543		
Latch	'373, '573		
Registered transceiver	'646, '652		
Flip-flop	'374, '574		
SN74VMEH22501A UBT transceiver replaces all above functions			



[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LE went low

Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.



SCES620 - DECEMBER 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} and BIAS V _{CC}	
Voltage range applied to any output in the high-impedance or power-off state, V _O (see Note 1)	
Voltage range applied to any output in the high or low state, V _O	
(see Note 1): 3A port or Y output	
B port	–0.5 V to 4.6 V
Output current in the low state, I _O : 3A port or Y output	
B port	
Output current in the high state, IO: 3A port or Y output	
B port	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$): B port	
Package thermal impedance, θ _{JA} (see Note 2): DGG package	
DGV package	
GQL package	
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 3 and 4)

			MIN	TYP	MAX	UNIT	
V _{CC} , BIAS V _{CC}	Supply voltage		3.15	3.3	3.45	V	
V	Langet well-and	Control inputs or A port		Vcc	5.5	.,	
VI	Input voltage	B port		Vcc	3 3.45	V	
V	Library Company and the man	Control inputs or A port	2				
V_{IH}	High-level input voltage	B port	0.5 V _{CC} + 50 mV			V	
V	Lave laved format wellings	Control inputs or A port			0.8	V	
VIL	Low-level input voltage	B port			0.5 V _{CC} – 50 mV	\ \	
lık	Input clamp current				-18	mA	
		3A port and Y output			-12		
IOH	High-level output current	B port			-48	mA	
		3A port and Y output			12		
loL	Low-level output current	B port			64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled			10	ns/V	
Δt/ΔV _{CC}	Power-up ramp rate		20			μs/V	
TA	Operating free-air temperature		-40		85	°C	

NOTES: 3. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.



SCES620 - DECEMBER 200-

electrical characteristics over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

PARAMETER		TEST CO	ONDITIONS	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 3.15 V,	I _I = -18 mA			-1.2	V
	3A port, any B ports, and Y outputs	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V},$	I _{OH} = -100 μA	V _{CC} -0.2			
.,	2A mant and Varitorita	V 245V	$I_{OH} = -6 \text{ mA}$	2.4			.,
VOH	3A port and Y outputs	V _{CC} = 3.15 V	$I_{OH} = -12 \text{ mA}$	2			V
	Any D nort	V 245V	$I_{OH} = -24 \text{ mA}$	2.4			
	Any B port	V _{CC} = 3.15 V	$I_{OH} = -48 \text{ mA}$	2			
	3A port, any B ports, and Y outputs	V _{CC} = 3.15 V to 3.45 V,	I _{OL} = 100 μA			0.2	
	OA mant and Wandards	V 0.45.V	I _{OL} = 6 mA			0.55	
V_{OL}	3A port and Y outputs	$V_{CC} = 3.15 \text{ V}$	I _{OL} = 12 mA			8.0	V
	Any B port		I _{OL} = 24 mA			0.4	
		V _{CC} = 3.15 V	$I_{OL} = 48 \text{ mA}$			0.55	
			$I_{OL} = 64 \text{ mA}$			0.6	
1.	Control inputs, 1A and 2A	$V_{CC} = 3.45 \text{ V},$	$V_I = V_{CC}$ or GND			±1	
l _l		$V_{CC} = 0 \text{ or } 3.45 \text{ V},$	V _I = 5.5 V			5	μΑ
I _{OZH} ‡	3A port, any B port, and Y outputs	V _{CC} = 3.45 V,	$V_O = V_{CC}$ or 5.5 V			5	μΑ
	3A port and Y outputs					-5	
lozl‡	Any B port	$V_{CC} = 3.45 \text{ V},$	$V_O = GND$			-20	μΑ
l _{off}		$V_{CC} = 0$, BIAS $V_{CC} = 0$,	V_{1} or $V_{0} = 0$ to 5.5 V			±10	μΑ
IBHL§	3A port	V _{CC} = 3.15 V,	V _I = 0.8 V	75			μΑ
I _{BHH} ¶	3A port	$V_{CC} = 3.15 \text{ V},$	V _I = 2 V	-75			μΑ
I _{BHLO} #	3A port	$V_{CC} = 3.45 \text{ V},$	$V_I = 0$ to V_{CC}	500			μΑ
_{IBHHO}	3A port	V _{CC} = 3.45 V,	$V_I = 0$ to V_{CC}	-500			μΑ
I _{OZ(PU/F}	סי,	$V_{CC} \le 1.3 \text{ V}, V_{O} = \underline{0.5} \text{ V to}$ $V_{I} = \text{GND or } V_{CC}, \overline{OE} = \text{dor}$	V _{CC} , n't care			±10	μΑ

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[‡] For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.

[§] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND, then raising it to V_{IL} max.

The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC}, then lowering it to V_{IH} min.

[#] An external driver must source at least IBHLO to switch this node from low to high.

An external driver must sink at least IBHHO to switch this node from high to low.

^{*}High-impedance state during power up or power down

electrical characteristics over recommended operating free-air temperature range for A and B ports (unless otherwise noted) (continued)

	PARAMETER	TEST CO	NDITIONS	MIN TYPT	MAX	UNIT
			Outputs high		30	
ICC		$V_{CC} = 3.45 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		30	mA
		1 = 100 01 QMD	Outputs disabled		30	
		$V_{CC} = 3.45 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND},$	Outputs enabled	76		μΑ/ clock
ICCD	One data input switch one-half clock frequer 50% duty cycle		Outputs disabled	19		MHz/ input
Δlcc]	V_{CC} = 3.15 V to 3.45 V, One Other inputs at V_{CC} or GND	input at V _{CC} – 0.6 V,		750	μΑ
_	1A and 2A inputs	V 0.45 V 0		2.8		
Ci	Control inputs	V _I = 3.15 V or 0		2.6		pF
Со	1Y or 2Y outputs	V _O = 3.15 V or 0		5.6		pF
C.	3A port	Va = - 2 2 V	\/a = 2.2 \/ or 0	7.9		, F
C _{io}	Any B port	$V_{CC} = 3.3 \text{ V},$	$V_{O} = 3.3 \text{ V or } 0$	11	12.5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

live-insertion specifications over recommended operating free-air temperature range for B port

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
1 (DIAC)/)	$V_{CC} = 0 \text{ to } 3.15 \text{ V},$	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$,	$I_{O(DC)} = 0$			5	mA
I _{CC} (BIAS V _{CC})	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}^{\ddagger},$	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$,	$I_{O(DC)} = 0$			10	μΑ
VO	$V_{CC} = 0$,	BIAS V _{CC} = 3.15 V to 3.45 V		1.3	1.5	1.7	V
lo		$V_{O} = 0,$	BIAS V _{CC} = 3.15 V	-20		-100	
	ACC = 0	V _O = 3 V,	BIAS V _{CC} = 3.15 V	20		100	μΑ

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



This is the increase in supply current for each input that is at the specified TTL voltage level, rather than VCC or GND.

[‡] VCC - 0.5 V < BIAS VCC

SCES620 - DECEMBER 2004

timing requirements over recommended operating conditions for UBT transceiver (unless otherwise noted) (see Figures 1 and 2)

				MIN	MAX	UNIT
fclock	Clock frequency	LE high CLK high or low 3A before CLK↑ 3A before LE↓ CLK high CLK low 3B before CLK↑ Data high CLK low Data high CLK low			120	MHz
	Polar donatar	LE high		2.5		
ιW	Pulse duration	CLK high or low	CLK high or low 3A before CLK↑ Data high Data low CLK high CLK low Data high CLK low Data high	3		ns
		0.0 h a farra 01.160	Data high	2.1		
		3A before CLK	Data low	2.2		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	CLK high	2				
	2					
	2.5		ns			
	3B before CLK	Data low	2.7			
	0D h - (E	CLK high	2			
		3B before LE↓	LE high 2.5 CLK high or low 3 3A before CLK↑ Data high 2.1 Data low 2.2 CLK high 2 CLK low 2 Data high 2.5 Data low 2.7 CLK high 2 CLK low 2 Data low 0 Data low 0 CLK high 1 CLK low 1 Data high 0 Data high 0 Data high 0 Data low 0 CLK low 1 Data low 0 CLK high 1 Data low 0 CLK high 1			
			Data high	0		
		3A after CLKT	Data low	0		
	Clock Clock frequency fre	1				
Setup time Se	1					
t _h	Hold time		Data high	0		ns
		3B after CLK1	Data low	0		
		,	CLK high	1		
		3B after LE↓		1		

switching characteristics over recommended operating conditions for bus transceiver function (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t _{PLH}	40.00.20	4D av 0D	4.8		8.9	
t _{PHL}	1A or 2A	1B or 2B	4.5		7.8	ns
t _{PLH}	1A or 2A	4\/ a= 0\/	6.2		14.5	
^t PHL	TA OI ZA	1Y or 2Y	6.1		13	ns
^t PZH	OEAB	4D av 0D	3.9		8.1	
tPZL	OEAB	1B or 2B	3.7		7.4	ns
^t PHZ	OEAB	1B or 2B	3.3		9.7	20
t _{PLZ}	OEAB	10 01 20	1.8		4.8	ns
t _r	Transition time, B port (10%–90%)		4.3		ns	
t _f	Transition time, B	port (90%-10%)		4.3		ns
^t PLH	4D of 0D	4)/ 0)/	1.6		5.6	
^t PHL	1B of 2B	1Y or 2Y	1.6		5.6	ns
^t PZH	OEBY	4\/ a= 0\/	1.2		5.6	
tPZL	OEBY	1Y or 2Y	1.8		4.9	ns
^t PHZ	OEBY	1Y or 2Y	0.9		5.4	20
^t PLZ	OLBI	IT UI ZT	1.4		4.5	ns

SCES620 - DECEMBER 2004

switching characteristics over recommended operating conditions for UBT transceiver (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP MAX	UNIT
fmax			120		MHz
t _{PLH}	0.4	0.5	5.1	9.3	
^t PHL	3A	3B	4.7	8.3	ns
t _{PLH}		0.5	5.5	10.6	
^t PHL	LE	3B	4.9	8.7	ns
^t PLH	OLKAD	0.0	5.8	10.1	
^t PHL	CLKAB	CLKAB 3B	4.2	8.4	ns
^t PZH	ŌĒ	0.0	4.2	9.3	
^t PZL	OE .	3B	3.2	8.5	ns
^t PHZ	ŌĒ	0.0	4.2	9.3	
^t PLZ	OE .	3B	2.4	5.7	ns
t _r	Transition time, B	port (10%–90%)		4.3	ns
tf	Transition time, B	port (90%-10%)		4.3	
^t PLH	0.0	0.4	1.5	5.9	
^t PHL	3B	3A	1.7	5.9	ns
^t PLH		0.4	1.7	5.9	
^t PHL	LE	3A	1.7	5.9	ns
^t PLH	CLKDA	0.4	1.1	5.5	
t _{PHL}	CLKBA	3A	1.4	5.5	ns
^t PZH	ŌĒ	0.4	1.5	6.2	
tPZL	OE	3A	2.1	5.5	ns
^t PHZ	ŌĒ	3A	0.8	6.2	
tPLZ	OE	3A	2.3	5.6	ns

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
tsk(LH)	44.04.24	4D or 2D	0.8	
tsk(HL)	TA OI ZA	1A or 2A 1B or 2B		ns
tsk(LH)	1B or 2B	1Y or 2Y	0.7	
tsk(HL)	16 01 26	11 01 21	0.7	ns
4. ot	1A or 2A	1B or 2B	3.9	200
t _{sk(t)} †	1B or 2B	1Y or 2Y	1.5	ns
+ + / >	1A or 2A	1B or 2B	3.6	20
^t sk(pp)	1B or 2B	1Y or 2Y	1.4	ns

[†] t_{sk(t)} – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].



CES620 - DECEMBER 2004

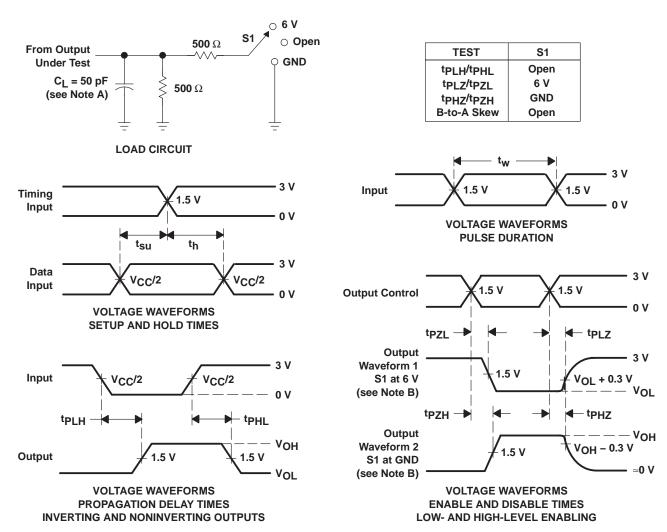
skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
^t sk(LH)	- 3A	3B	1.4	20
^t sk(HL)	- SA	JD	1.1	ns
^t sk(LH)	CLKAB	3B	0.8	20
^t sk(HL)	CLNAB	JD	0.8	ns
^t sk(LH)	- 3B	3A	0.7	
^t sk(HL)	ЭБ	3A	0.6	ns
t _{sk(LH)}	CLKBA	24	0.7	
t _{sk(HL)}	- CLKBA	3A	0.6	ns
	3A	3B	3.9	
+ +	CLKAB	3B	3.9	20
t _{sk(t)} †	3B	3A	1.6	ns
	CLKBA	3A	1.2	
	3A	3B	3.6	
• • • •	CLKAB	3B	3.5	
t _{sk} (pp)	3B	3A	1.3	ns
	CLKBA	3A	1.2	

[†] t_{Sk(t)} – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{Sk(t)}].



PARAMETER MEASUREMENT INFORMATION **A PORT**



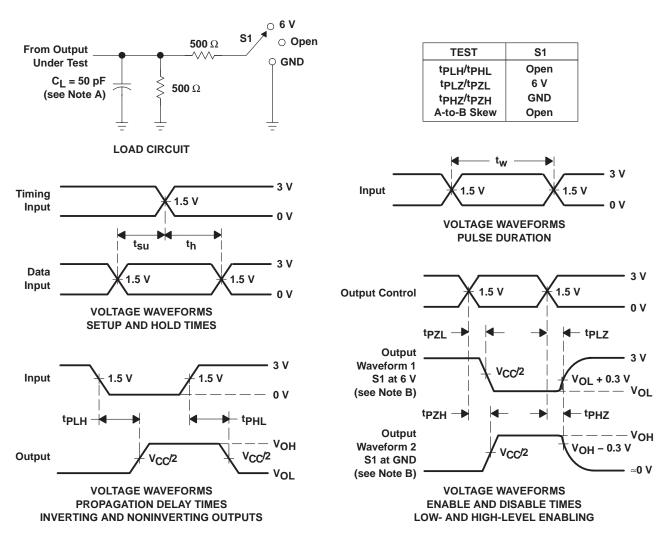
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, Z_{O} = 50 Ω , t_{f} \approx 2 ns, t_{f} \approx 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION B PORT



NOTES: A. C_L includes probe and jig capacitance.

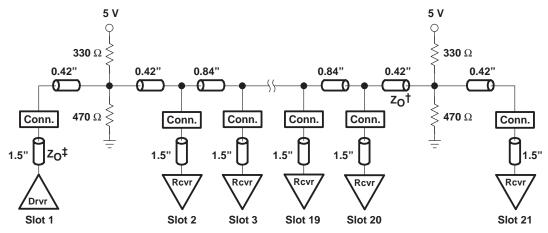
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, Z_O = 50 Ω , $t_f \approx$ 2 ns. $t_f \approx$ 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SCES620 - DECEMBER 2004

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics tables show the switching characteristics of the device into the lumped load shown in the parameter measurement information (PMI) (see Figures 1 and 2). All logic devices currently are tested into this type of load. However, the designer's backplane application probably is a distributed load. For this reason, this device has been designed for optimum performance in the VME64x backplane as shown in Figure 3.



[†] Unloaded backplane trace natural impedence (Z_{Ω}) is 45 Ω to 60 Ω is allowed, with 50 Ω being ideal.

Figure 3. VME64x Backplane

The following switching characteristics tables derived from TI-SPICE models show the switching characteristics of the device into the backplane under full and minimum loading conditions, to help the designer better understand the performance of the VME device in this typical backplane. See www.ti.com/sc/etl for more information.

driver in slot 11, with receiver cards in all other slots (full load)

switching characteristics over recommended operating conditions for bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
^t PLH	44 24	4D av 2D	5.9		8.5	
^t PHL	1A or 2A	1B or 2B	5.5		8.7	ns
t _r ¶	Transition time, B	Transition time, B port (10%–90%)		8.6	11.4	ns
t _f ¶	Transition time, B	port (90%-10%)	8.9	9	10.8	ns

[§] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. All values are derived from TI-SPICE models.



[‡] Card stub natural impedence (Z_{Ω}) is 60 Ω .

[¶] All t_r and t_f times are taken at the first receiver.

driver in slot 11, with receiver cards in all other slots (full load) (continued)

switching characteristics over recommended operating conditions for UBT (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
^t PLH	24	an.	6.2		8.9	
^t PHL	3A	3B	5.6		9	ns
tPLH	LE	ap.	6.1		9.1	20
t _{PHL}	LE	3B	5.6		9	ns
^t PLH	CLKAB	ap.	6.2		9.1	
^t PHL	CLKAB	3B	5.7		9	ns
t _r ‡	Transition time, B	Transition time, B port (10%–90%)		8.6	11.4	ns
t _f ‡	Transition time, B	port (90%–10%)	8.9	9	10.8	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYPT	MAX	UNIT
tsk(LH)	1A or 2A	1B or 2B		2.5	20
tsk(HL)	TA OF ZA	1B 01 2B		3	ns
t _{sk(t)} §	1A or 2A	1B or 2B		1	ns
tsk(pp)	1A or 2A	1B or 2B	0.5	3.4	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYPT MAX	UNIT
^t sk(LH)	24	ap.	2.4	
tsk(HL)	3A	3B	3.4	ns
^t sk(LH)	OLIVA D	ap.	2.7	
t _{sk(HL)}	CLKAB	3B	3.4	ns
. 8	3A	3B	1	
$t_{Sk(t)}$ §	CLKAB	3B	1	ns
*	3A	3B	0.5 3.4	
^t sk(pp)	CLKAB	3B	0.6 3.5	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

[§] t_{sk(t)} – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].



[‡] All t_r and t_f times are taken at the first receiver.

[§] t_{sk(t)} – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].

SCES620 - DECEMBER 2004

driver in slot 1, with one receiver in slot 21 (minimum load)

switching characteristics over recommended operating conditions for bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t _{PLH}	44 24	4D on 2D	5.5		7.4	
t _{PHL}	1A or 2A	1B or 2B	5.3		7.4	ns
t _r ‡	Transition time, B	Transition time, B port (10%–90%)		3.4	4.4	ns
t _f ‡	Transition time, B	port (90%–10%)	3.7	3.4	4.8	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

switching characteristics over recommended operating conditions for UBT (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
^t PLH	24	an.	5.8		7.9	
^t PHL	3A	3B	5.5		7.7	ns
t _{PLH}	LE	20	5.9		8	
^t PHL	LE	3B	5.5		7.8	ns
^t PLH	CLYAB	an.	5.9		8.1	
^t PHL	CLKAB	3B	5.5		7.7	ns
t _r ‡	Transition time, B	Transition time, B port (10%–90%)		3.4	4.4	ns
t _f ‡	Transition time, B	port (90%–10%)	3.7	3.4	4.8	ns

 $^{^\}dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYPT	MAX	UNIT
^t sk(LH)	1A or 2A	1B or 2B		1.7	
^t sk(HL)	TA OF ZA	16 01 26		2.1	ns
t _{sk(t)} §	1A or 2A	1B or 2B		1	ns
tsk(pp)	1A or 2A	1B or 2B	0.2	2.1	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.



[‡] All t_r and t_f times are taken at the first receiver.

[‡] All t_r and t_f times are taken at the first receiver.

[§] tsk(t) - Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case VCC and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].

driver in slot 1, with one receiver in slot 21 (minimum load) (continued)

skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYPT MA	X UNIT
^t sk(LH)	24	an.		2
t _{sk(HL)}	3A	3B	2	ns 3
t _{sk(LH)}	OLIKAR	o.D.	2	
t _{sk(HL)}	CLKAB	3B	2	ns 4
. +	3A	3B		1
t _{sk(t)} ‡	CLKAB	3B		ns 1
• • • •	3A	3B	0.2 2	
^t sk(pp)	CLKAB	3B	0.2 2	9 ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

By simulating the performance of the device using the VME64x backplane (see Figure 3), the maximum peak current in or out of the B-port output, as the devices switch from one logic state to another, was found to be equivalent to driving the lumped load shown in Figure 4.

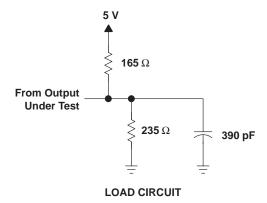


Figure 4. Equivalent AC Peak Output-Current Lumped Load

[‡]t_{sk(t)} – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [t_{sk(t)}].

driver in slot 1, with one receiver in slot 21 (minimum load) (continued)

In general, the rise- and fall-time distribution is shown in Figure 5. Since VME devices were designed for use into distributed loads like the VME64x backplane (B/P), there are significant differences between low-to-high (LH) and high-to-low (HL) values in the lumped load shown in the PMI (see Figures 1 and 2).

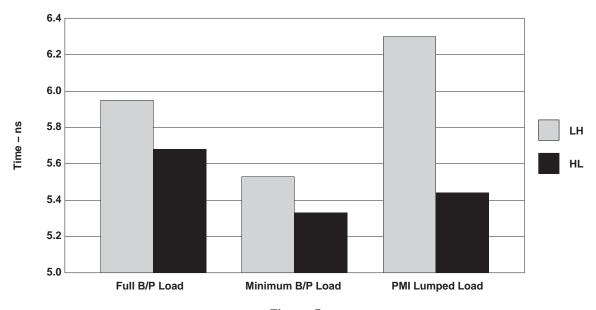
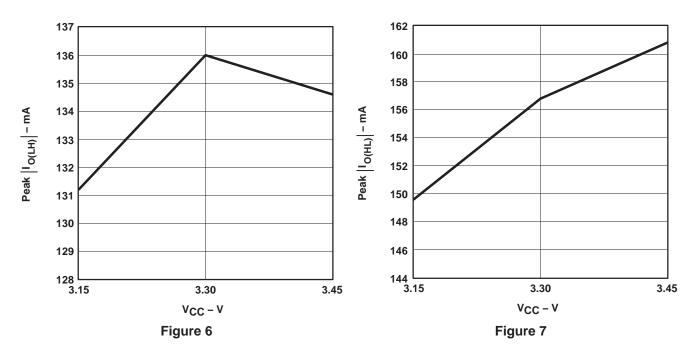
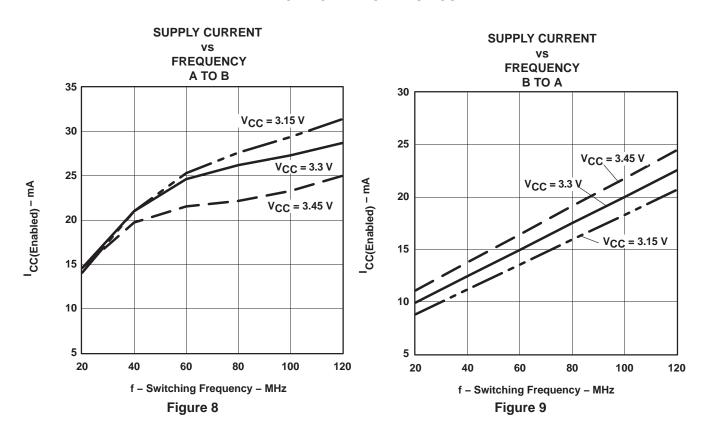


Figure 5

Characterization-laboratory data in Figures 6 and 7 show the absolute ac peak output current, with different supply voltages, as the devices change output logic state. A typical nominal process is shown to demonstrate the devices' peak ac output drive capability.



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE HIGH-LEVEL OUTPUT CURRENT

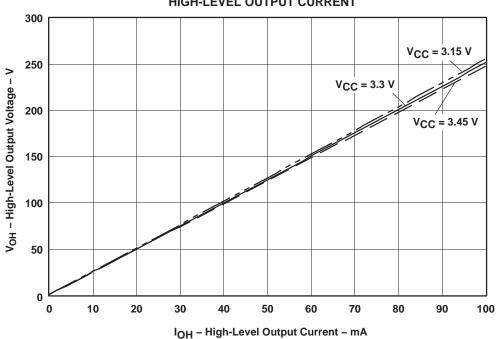


Figure 10. V_{OL} vs I_{OL}

LOW-LEVEL OUTPUT VOLTAGE

LOW-LEVEL OUTPUT CURRENT 4.0 $V_{CC} = 3.45 \text{ V}$ 3.5 $V_{CC} = 3.3 V$ VoL - Low-Level Output Voltage - V 3.0 2.5 V_{CC} = 3.15 V 2.0 1.5 1.0 0.5 0.0 0 -10 -20 -30 -40 -50 -60 -70 -80 -90 -100

Figure 11. VOH vs IOH

IOL - Low-Level Output Current - mA



VMEbus SUMMARY

In 1981, the VMEbus was introduced as a backplane bus architecture for industrial and commercial applications. The data-transfer protocols used to define the VMEbus came from the Motorola™ VERSA bus architecture, which owed its heritage to the then recently introduced Motorola 68000 microprocessor. The VMEbus, when introduced, defined two basic data-transfer operations - single-cycle transfers consisting of an address and a data transfer, and a block transfer (BLT) consisting of an address and a sequence of data transfers. These transfers were asynchronous, using a master-slave handshake. The master puts address and data on the bus and waits for an acknowledgment. The selected slave either reads or writes data to or from the bus, then provides a data-acknowledge (DTACK*) signal. The VMEbus system data throughput was 40 Mbyte/s. Previous to the VMEbus, it was not uncommon for the backplane buses to require elaborate calculations to determine loading and drive current for interface design. This approach made designs difficult and caused compatibility problems among manufacturers. To make interface design easier and to ensure compatibility, the developers of the VMEbus architecture defined specific delays based on a 21-slot terminated backplane and mandated the use of certain high-current TTL drivers, receivers, and transceivers.

In 1989, multiplexing block transfer (MBLT) effectively increased the number of bits from 32 to 64, thereby doubling the transfer rate. In 1995, the number of handshake edges was reduced from four to two in the double-edge transfer (2eVME) protocol, doubling the data rate again. In 1997, the VMEbus International Trade Association (VITA) established a task group to specify a synchronous protocol to increase data-transfer rates to 320 Mbyte/s, or more. The unreleased specification, VITA 1.5 [double-edge source synchronous transfer (2eSST)], is based on the asynchronous 2eVME protocol. It does not wait for acknowledgement of the data by the receiver and requires incident-wave switching. Sustained data rates of 1 Gbyte/s, more than ten times faster than traditional VME64 backplanes, are possible by taking advantage of 2eSST and the 21-slot VME320 star-configuration backplane. The VME320 backplane approximates a lumped load, allowing substantially higher-frequency operation over the VME64x distributed-load backplane. Traditional VME64 backplanes with no changes theoretically can sustain 320 Mbyte/s.

From BLT to 2eSST - A Look at the Evolution of VMEbus Protocols by John Rynearson, Technical Director, VITA, provides additional information on VMEbus and can be obtained at www.vita.com.

maximum data transfer rates

DATE	T000100V	22222	DATA BITS	DATA TRANSFERS	PER SYSTEM	FREQUENCY (MHz)		
DATE	TOPOLOGY	PROTOCOL	PER CYCLE	PER CLOCK CYCLE	(Mbyte/s)	BACKPLANE	CLOCK	
1981	VMEbus IEEE-1014	BLT	32	1	40	10	10	
1989	VME64	MBLT	64	1	80	10	10	
1995	VME64x	2eVME	64	2	160	10	20	
1997	VME64x	2eSST	64	2-No Ack	160–320	10–20	20–40	
1999	VME320	2eSST	64	2-No Ack	320–1000	20–62.5	40–125	

applicability

Target applications for VME backplanes include industrial controls, telecommunications, simulation, high-energy physics, office automation, and instrumentation systems.





.com 24-May-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74VMEH22501ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74VMEH22501ADGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74VMEH22501ADGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74VMEH22501ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74VMEH22501ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74VMEH22501AGQLR	NRND	BGA MI CROSTA R JUNI OR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74VMEH22501AZQLR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao =	Dimension	designed	to	accommodate	the	component	width.	
Bo =	Dímension	designed	to	accommodate	the	component	length.	
Ko =	Dímension	designed	to	accommodate	the	component	thickness.	
W = Overall width of the carrier tape.								
P =	P = Pitch between successive cavity centers.							



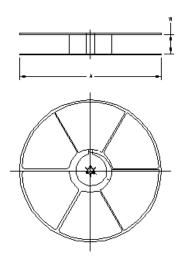
TAPE AND REEL INFORMATION



PACKAGE MATERIALS INFORMATION

19-May-2007

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74VMEH22501ADGGR	DGG	48	MLA	330	24	8.6	15.8	1.8	12	24	Q1
SN74VMEH22501ADGVR	DGV	48	MLA	330	24	6.8	10.1	1.6	12	24	Q1
SN74VMEH22501AGQLR	GQL	56	HIJ	330	16	4.8	7.3	1.45	8	16	Q1
SN74VMEH22501AZQLR	ZQL	56	HIJ	330	16	4.8	7.3	1.45	8	16	Q1



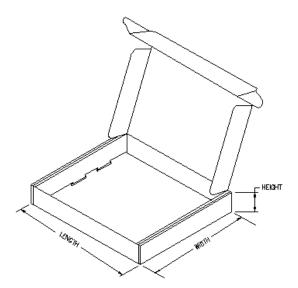
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74VMEH22501ADGGR	DGG	48	MLA	333.2	333.2	31.75
SN74VMEH22501ADGVR	DGV	48	MLA	333.2	333.2	31.75
SN74VMEH22501AGQLR	GQL	56	HIJ	346.0	346.0	33.0
SN74VMEH22501AZQLR	ZQL	56	HIJ	346.0	346.0	33.0





19-May-2007



ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

	Applications	
amplifier.ti.com	Audio	www.ti.com/audio
dataconverter.ti.com	Automotive	www.ti.com/automotive
dsp.ti.com	Broadband	www.ti.com/broadband
interface.ti.com	Digital Control	www.ti.com/digitalcontrol
logic.ti.com	Military	www.ti.com/military
power.ti.com	Optical Networking	www.ti.com/opticalnetwork
microcontroller.ti.com	Security	www.ti.com/security
www.ti-rfid.com	Telephony	www.ti.com/telephony
www.ti.com/lpw	Video & Imaging	www.ti.com/video
	Wireless	www.ti.com/wireless
	dataconverter.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com www.ti-rfid.com	amplifier.ti.com dataconverter.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com www.ti-rfid.com www.ti-com/lpw Audio Automotive Broadband Digital Control Military Optical Networking Security Telephony Video & Imaging

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2007, Texas Instruments Incorporated