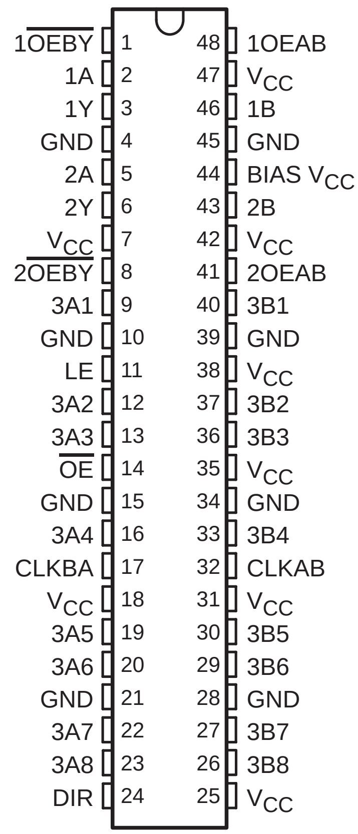
- **Member of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference (EMI)**
- **Compliant With VME64, 2eVME, and 2eSST Protocols**
- **Bus Transceiver Split LVTTL Port Provides Feedback Path for Control and Diagnostics Monitoring**
- **I/O Interfaces Are 5-V Tolerant**
- **B-Port Outputs (−48 mA/64 mA)**
- **Y and A-Port Outputs (−12 mA/12 mA)**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on 3A-Port Data Inputs**
- **26-Ω Equivalent Series Resistor on 3A Ports and Y Outputs**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − DGG	Tape and reel	SN74VMEH22501ADGGR	VMEH22501A
	TVSOP − DGV	Tape and reel	SN74VMEH22501ADGVR	VK501A
	VFBGA − GQL	Tape and reel	SN74VMEH22501AGQLR	VK501A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

The SN74VMEH22501A 8-bit universal bus transceiver has two integral 1-bit three-wire bus transceivers and is designed for 3.3-V V_{CC} operation with 5-V tolerant inputs. The UBT™ transceiver allows transparent, latched, and flip-flop modes of data transfer, and the separate LVTTL input and outputs on the bus transceivers provide a feedback path for control and diagnostics monitoring. This device provides a high-speed interface between cards operating at LVTTL logic levels and VME64, VME64x, or VME320† backplane topologies.

The SN74VMEH22501A is pin-for-pin capatible to the VMEH22501, but operates at a wider operating temperature (−40°C to 85°C) range.

High-speed backplane operation is a direct result of the improved OEC™ circuitry and high drive that has been designed and tested into the VME64x backplane model. The B-port I/Os are optimized for driving large capacitive loads and include pseudo-ETL input thresholds (1/2 V_{CC} ±50 mV) for increased noise immunity. These specifications support the 2eVME protocols in VME64x (ANSI/VITA 1.1) and 2eSST protocols in VITA 1.5. With proper design of a 21-slot VME system, a designer can achieve 320-Mbyte transfer rates on linear backplanes and, possibly, 1-Gbyte transfer rates on the VME320 backplane.

All inputs and outputs are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.

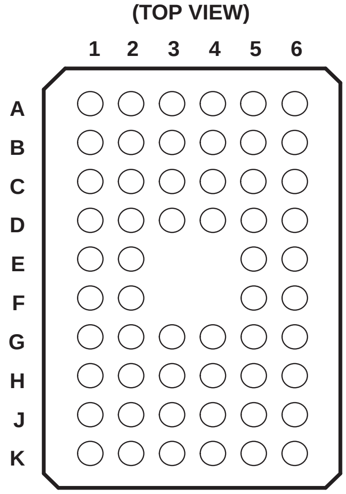
Active bus-hold circuitry holds unused or undriven 3A-port inputs at a valid logic state. Bus-hold circuitry is not provided on 1A or 2A inputs, any B-port input, or any control input. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry prevents damaging current to backflow through the device when it is powered off/on. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, output-enable ($\overline{\text{OE}}$ and $\overline{\text{OEBY}}$) inputs should be tied to V_{CC} through a pullup resistor and output-enable (OEAB) inputs should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the drive capability of the device connected to this input.

† VME320 is a patented backplane construction by Arizona Digital, Inc.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1$\overline{\text{OEBY}}$	NC	NC	NC	NC	1OEAB
B	1Y	1A	GND	GND	V_{CC}	1B
C	2Y	2A	V_{CC}	V_{CC}	BIAS V_{CC}	2B
D	3A1	2$\overline{\text{OEBY}}$	GND	GND	2OEAB	3B1
E	3A2	LE			V_{CC}	3B2
F	3A3	$\overline{\text{OE}}$			V_{CC}	3B3
G	3A4	CLKBA	GND	GND	CLKAB	3B4
H	3A5	3A6	V_{CC}	V_{CC}	3B6	3B5
J	3A7	3A8	GND	GND	3B8	3B7
K	DIR	NC	NC	NC	NC	V_{CC}

NC − No internal connection

functional description

The SN74VMEH22501A is a high-drive (–48/64 mA), 8-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or flip-flop modes. Data transmission is true logic. The device is uniquely partitioned as 8-bit UBT transceivers with two integrated 1-bit three-wire bus transceivers.

functional description for two 1-bit bus transceivers

The OEAB inputs control the activity of the 1B or 2B port. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are disabled.

Separate 1A and 2A inputs and 1Y and 2Y outputs provide a feedback path for control and diagnostics monitoring. The $\overline{\text{OEBY}}$ inputs control the 1Y or 2Y outputs. When $\overline{\text{OEBY}}$ is low, the Y outputs are active. When $\overline{\text{OEBY}}$ is high, the Y outputs are disabled.

The $\overline{\text{OEBY}}$ and OEAB inputs can be tied together to form a simple direction control where an input high yields A data to B bus and an input low yields B data to Y bus.

1-BIT BUS TRANSCEIVER FUNCTION TABLE

INPUTS		OUTPUT	MODE
OEAB	$\overline{\text{OEBY}}$		
L	H	Z	Isolation
H	H	A data to B bus	True driver
L	L	B data to Y bus	
H	L	A data to B bus, B data to Y bus	True driver with feedback path

functional description for 8-bit UBT transceiver

The 3A and 3B data flow in each direction is controlled by the $\overline{OE}$ and direction-control (DIR) inputs. When $\overline{OE}$ is low, all 3A- or 3B-port outputs are active. When $\overline{OE}$ is high, all 3A- or 3B-port outputs are in the high-impedance state.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	DIR	
H	X	Z
L	H	3A data to 3B bus
L	L	3B data to 3A bus

The UBT transceiver functions are controlled by latch-enable (LE) and clock (CLKAB and CLKBA) inputs. For 3A-to-3B data flow, the UBT operates in the transparent mode when LE is high. When LE is low, the 3A data is latched if CLKAB is held at a high or low logic level. If LE is low, the 3A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB.

The UBT transceiver data flow for 3B to 3A is similar to that of 3A to 3B, but uses CLKBA.

UBT TRANSCEIVER FUNCTION TABLE†

INPUTS				OUTPUT 3B	MODE
$\overline{OE}$	LE	CLKAB	3A		
H	X	X	X	Z	Isolation
L	L	H	X	B_0‡	Latched storage of 3A data
L	L	L	X	B_0§	
L	H	X	L	L	True transparent
L	H	X	H	H	
L	L	↑	L	L	Clocked storage of 3A data
L	L	↑	H	H	

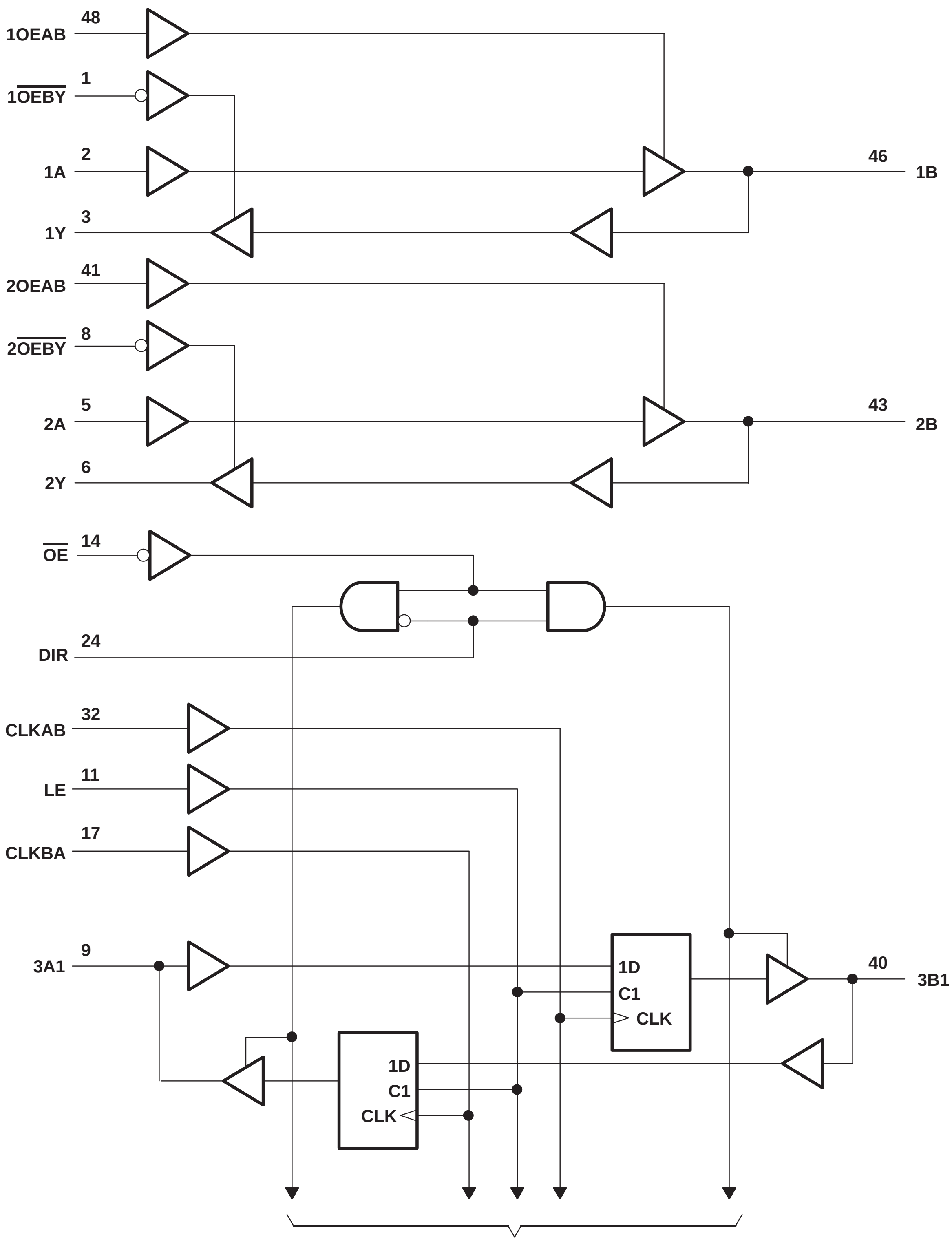
† 3A-to-3B data flow is shown; 3B-to-3A data flow is similar, but uses CLKBA.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LE went low
§ Output level before the indicated steady-state input conditions were established

The UBT transceiver can replace any of the functions shown in Table 1.

Table 1. SN74VMEH22501A UBT Transceiver Replacement Functions

FUNCTION	8 BIT
Transceiver	’245, ’623, ’645
Buffer/driver	’241, ’244, ’541
Latched transceiver	’543
Latch	’373, ’573
Registered transceiver	’646, ’652
Flip-flop	’374, ’574
SN74VMEH22501A UBT transceiver replaces all above functions	

logic diagram (positive logic)



To Seven Other Channels

Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC} . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance
or power-off state, V_O (see Note 1) . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or low state, V_O
(see Note 1): 3A port or Y output . . . . −0.5 V to V_{CC} + 0.5 V
B port . . . . −0.5 V to 4.6 V
Output current in the low state, I_O: 3A port or Y output . . . . 50 mA
B port . . . . 100 mA
Output current in the high state, I_O: 3A port or Y output . . . . −50 mA
B port . . . . −100 mA
Input clamp current, I_{IK} (V_I < 0) . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}): B port . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 70°C/W
DGV package . . . . 58°C/W
GQL package . . . . 42°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 3 and 4)

			MIN	TYP	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_I	Input voltage	Control inputs or A port		V_{CC}	5.5	V
		B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	Control inputs or A port	2			V
		B port	0.5 V_{CC} + 50 mV			
V_{IL}	Low-level input voltage	Control inputs or A port			0.8	V
		B port			0.5 V_{CC} − 50 mV	
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	3A port and Y output			−12	mA
		B port			−48	
I_{OL}	Low-level output current	3A port and Y output			12	mA
		B port			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		−40		85	°C

NOTES: 3. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

electrical characteristics over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = −18 mA			−1.2	V
V_{OH}	3A port, any B ports, and Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = −100 μA	V_{CC}−0.2			V
	3A port and Y outputs	V_{CC} = 3.15 V	I_{OH} = −6 mA	2.4			
			I_{OH} = −12 mA	2			
	Any B port	V_{CC} = 3.15 V	I_{OH} = −24 mA	2.4			
			I_{OH} = −48 mA	2			
V_{OL}	3A port, any B ports, and Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 μA			0.2	V
	3A port and Y outputs	V_{CC} = 3.15 V	I_{OL} = 6 mA			0.55	
			I_{OL} = 12 mA			0.8	
	Any B port	V_{CC} = 3.15 V	I_{OL} = 24 mA			0.4	
			I_{OL} = 48 mA			0.55	
			I_{OL} = 64 mA			0.6	
I_I	Control inputs, 1A and 2A	V_{CC} = 3.45 V,	$V_I = V_{CC}$ or GND			±1	μA
		V_{CC} = 0 or 3.45 V,	V_I = 5.5 V			5	
I_{OZH}‡	3A port, any B port, and Y outputs	V_{CC} = 3.45 V,	$V_O = V_{CC}$ or 5.5 V			5	μA
I_{OZL}‡	3A port and Y outputs	V_{CC} = 3.45 V,	V_O = GND			−5	μA
	Any B port					−20	
I_{off}		V_{CC} = 0, BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			±10	μA
I_{BHL}§	3A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			μA
I_{BHH}¶	3A port	V_{CC} = 3.15 V,	V_I = 2 V	−75			μA
I_{BHLO}#	3A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			μA
I_{BHHO}‖	3A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	−500			μA
$I_{OZ(PU/PD)}$☆		$V_{CC} \leq$ 1.3 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±10	μA

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND, then raising it to V_{IL} max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC}, then lowering it to V_{IH} min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ High-impedance state during power up or power down

electrical characteristics over recommended operating free-air temperature range for A and B ports (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{CC}		V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			30	mA
			Outputs low			30	
			Outputs disabled			30	
I_{CCD}		V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND, One data input switching at one-half clock frequency, 50% duty cycle	Outputs enabled		76		µA/ clock MHz/ input
			Outputs disabled		19		
ΔI_{CC}□		V_{CC} = 3.15 V to 3.45 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				750	µA
C_i	1A and 2A inputs	V_I = 3.15 V or 0			2.8		pF
	Control inputs				2.6		
C_o	1Y or 2Y outputs	V_O = 3.15 V or 0			5.6		pF
C_{io}	3A port	V_{CC} = 3.3 V,	V_O = 3.3 V or 0		7.9		pF
	Any B port				11	12.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
□ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

live-insertion specifications over recommended operating free-air temperature range for B port

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V,	BIAS V_{CC} = 3.15 V to 3.45 V,	$I_{O(DC)}$ = 0			5	mA
	V_{CC} = 3.15 V to 3.45 V‡,	BIAS V_{CC} = 3.15 V to 3.45 V,	$I_{O(DC)}$ = 0			10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V		1.3	1.5	1.7	V
I_O	V_{CC} = 0	V_O = 0,	BIAS V_{CC} = 3.15 V	−20		−100	µA
		V_O = 3 V,	BIAS V_{CC} = 3.15 V	20		100	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ V_{CC} − 0.5 V < BIAS V_{CC}

timing requirements over recommended operating conditions for UBT transceiver (unless otherwise noted) (see Figures 1 and 2)

				MIN	MAX	UNIT
f_{clock}	Clock frequency				120	MHz
t_w	Pulse duration	LE high		2.5		ns
		CLK high or low		3		
t_{su}	Setup time	3A before CLK↑	Data high	2.1		ns
			Data low	2.2		
		3A before LE↓	CLK high	2		
			CLK low	2		
		3B before CLK↑	Data high	2.5		
			Data low	2.7		
		3B before LE↓	CLK high	2		
			CLK low	2		
t_h	Hold time	3A after CLK↑	Data high	0		ns
			Data low	0		
		3A after LE↓	CLK high	1		
			CLK low	1		
		3B after CLK↑	Data high	0		
			Data low	0		
		3B after LE↓	CLK high	1		
			CLK low	1		

switching characteristics over recommended operating conditions for bus transceiver function (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	4.8		8.9	ns
t_{PHL}			4.5		7.8	
t_{PLH}	1A or 2A	1Y or 2Y	6.2		14.5	ns
t_{PHL}			6.1		13	
t_{PZH}	OEAB	1B or 2B	3.9		8.1	ns
t_{PZL}			3.7		7.4	
t_{PHZ}	OEAB	1B or 2B	3.3		9.7	ns
t_{PLZ}			1.8		4.8	
t_r	Transition time, B port (10%−90%)			4.3		ns
t_f	Transition time, B port (90%−10%)			4.3		ns
t_{PLH}	1B of 2B	1Y or 2Y	1.6		5.6	ns
t_{PHL}			1.6		5.6	
t_{PZH}	$\overline{OEBY}$	1Y or 2Y	1.2		5.6	ns
t_{PZL}			1.8		4.9	
t_{PHZ}	$\overline{OEBY}$	1Y or 2Y	0.9		5.4	ns
t_{PLZ}			1.4		4.5	

switching characteristics over recommended operating conditions for UBT transceiver (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}			120			MHz
t_{PLH}	3A	3B	5.1		9.3	ns
t_{PHL}			4.7		8.3	
t_{PLH}	LE	3B	5.5		10.6	ns
t_{PHL}			4.9		8.7	
t_{PLH}	CLKAB	3B	5.8		10.1	ns
t_{PHL}			4.2		8.4	
t_{PZH}	$\overline{OE}$	3B	4.2		9.3	ns
t_{PZL}			3.2		8.5	
t_{PHZ}	$\overline{OE}$	3B	4.2		9.3	ns
t_{PLZ}			2.4		5.7	
t_r	Transition time, B port (10%−90%)			4.3		ns
t_f	Transition time, B port (90%−10%)			4.3		ns
t_{PLH}	3B	3A	1.5		5.9	ns
t_{PHL}			1.7		5.9	
t_{PLH}	LE	3A	1.7		5.9	ns
t_{PHL}			1.7		5.9	
t_{PLH}	CLKBA	3A	1.1		5.5	ns
t_{PHL}			1.4		5.5	
t_{PZH}	$\overline{OE}$	3A	1.5		6.2	ns
t_{PZL}			2.1		5.5	
t_{PHZ}	$\overline{OE}$	3A	0.8		6.2	ns
t_{PLZ}			2.3		5.6	

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B		0.8	ns
$t_{sk(HL)}$				0.7	
$t_{sk(LH)}$	1B or 2B	1Y or 2Y		0.7	ns
$t_{sk(HL)}$				0.7	
$t_{sk(t)}$†	1A or 2A	1B or 2B		3.9	ns
	1B or 2B	1Y or 2Y		1.5	
$t_{sk(pp)}$	1A or 2A	1B or 2B		3.6	ns
	1B or 2B	1Y or 2Y		1.4	

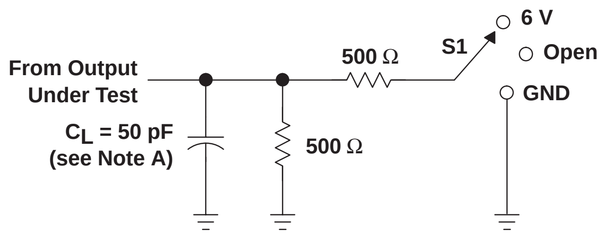
† $t_{sk(t)}$ − Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{sk(LH)}$	3A	3B		1.4	ns
$t_{sk(HL)}$				1.1	
$t_{sk(LH)}$	CLKAB	3B		0.8	ns
$t_{sk(HL)}$				0.8	
$t_{sk(LH)}$	3B	3A		0.7	ns
$t_{sk(HL)}$				0.6	
$t_{sk(LH)}$	CLKBA	3A		0.7	ns
$t_{sk(HL)}$				0.6	
$t_{sk(t)}$ †	3A	3B		3.9	ns
	CLKAB	3B		3.9	
	3B	3A		1.6	
	CLKBA	3A		1.2	
$t_{sk(pp)}$	3A	3B		3.6	ns
	CLKAB	3B		3.5	
	3B	3A		1.3	
	CLKBA	3A		1.2	

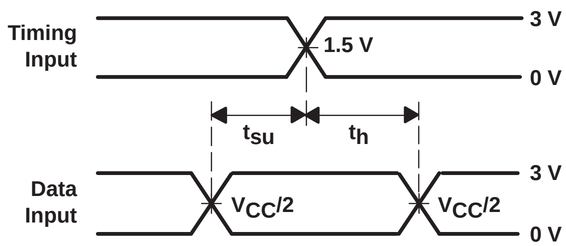
† $t_{sk(t)}$ − Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

PARAMETER MEASUREMENT INFORMATION
A PORT

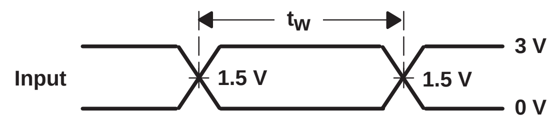


LOAD CIRCUIT

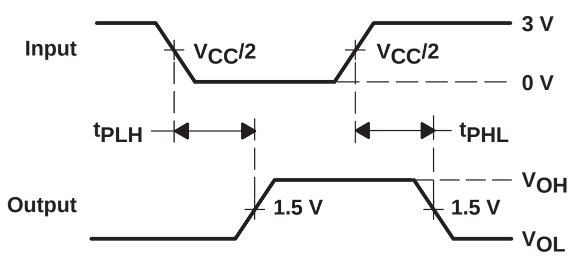
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
B-to-A Skew	Open



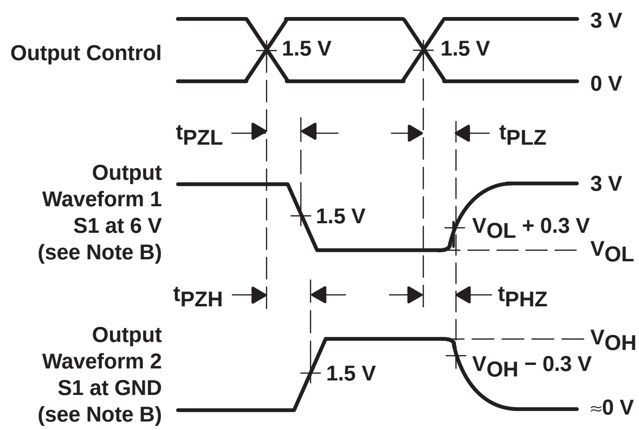
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

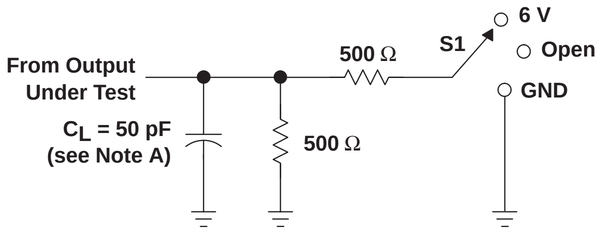


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.

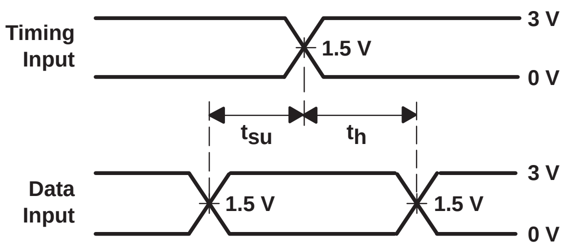
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
B PORT

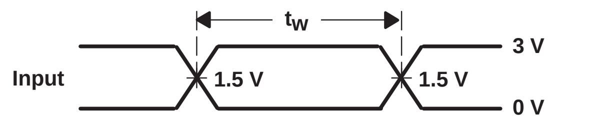


LOAD CIRCUIT

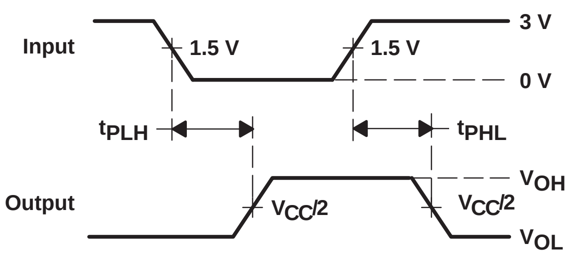
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
A-to-B Skew	Open



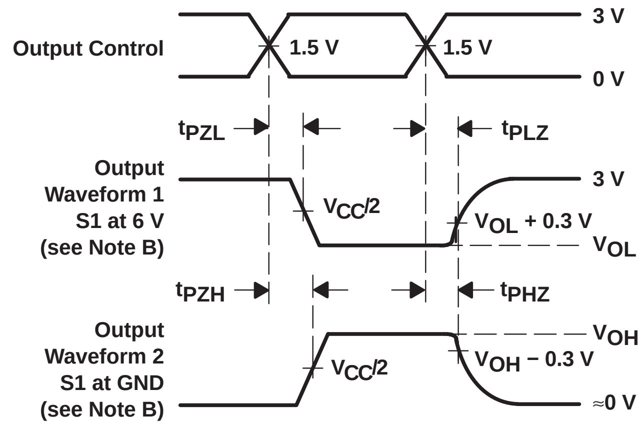
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



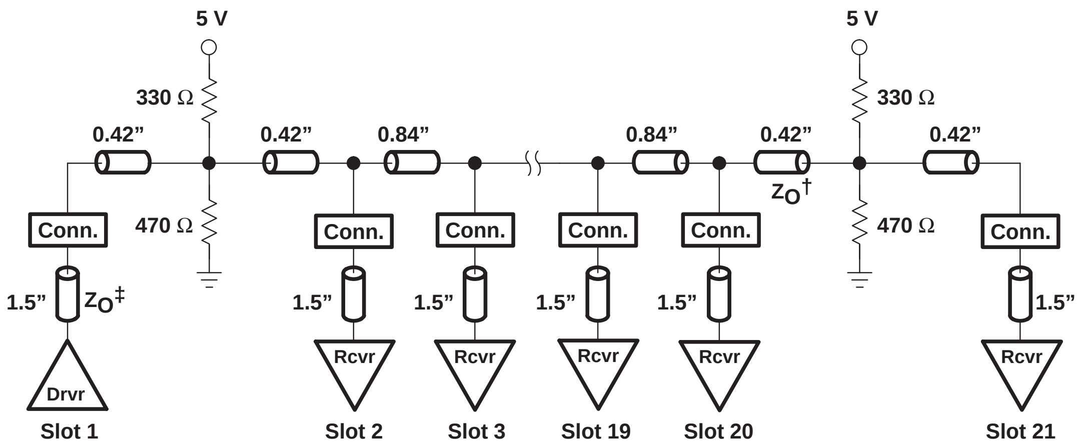
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics tables show the switching characteristics of the device into the lumped load shown in the parameter measurement information (PMI) (see Figures 1 and 2). All logic devices currently are tested into this type of load. However, the designer’s backplane application probably is a distributed load. For this reason, this device has been designed for optimum performance in the VME64x backplane as shown in Figure 3.



† Unloaded backplane trace natural impedence (Z_O) is 45 Ω. 45 Ω to 60 Ω is allowed, with 50 Ω being ideal.
‡ Card stub natural impedence (Z_O) is 60 Ω.

Figure 3. VME64x Backplane

The following switching characteristics tables derived from TI-SPICE models show the switching characteristics of the device into the backplane under full and minimum loading conditions, to help the designer better understand the performance of the VME device in this typical backplane. See www.ti.com/sc/etl for more information.

driver in slot 11, with receiver cards in all other slots (full load)

switching characteristics over recommended operating conditions for bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	5.9		8.5	ns
t_{PHL}			5.5		8.7	
t_r¶	Transition time, B port (10%−90%)		9	8.6	11.4	ns
t_f¶	Transition time, B port (90%−10%)		8.9	9	10.8	ns

§ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
¶ All t_r and t_f times are taken at the first receiver.

driver in slot 11, with receiver cards in all other slots (full load) (continued)

switching characteristics over recommended operating conditions for UBT (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	3A	3B	6.2		8.9	ns
t_{PHL}			5.6		9	
t_{PLH}	LE	3B	6.1		9.1	ns
t_{PHL}			5.6		9	
t_{PLH}	CLKAB	3B	6.2		9.1	ns
t_{PHL}			5.7		9	
t_r‡	Transition time, B port (10%−90%)		9	8.6	11.4	ns
t_f‡	Transition time, B port (90%−10%)		8.9	9	10.8	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
‡ All t_r and t_f times are taken at the first receiver.

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B			2.5	ns
$t_{sk(HL)}$					3	
$t_{sk(t)}$§	1A or 2A	1B or 2B			1	ns
$t_{sk(pp)}$	1A or 2A	1B or 2B		0.5	3.4	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
§ $t_{sk(t)}$ − Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	3A	3B			2.4	ns
$t_{sk(HL)}$					3.4	
$t_{sk(LH)}$	CLKAB	3B			2.7	ns
$t_{sk(HL)}$					3.4	
$t_{sk(t)}$§	3A	3B			1	ns
	CLKAB	3B			1	
$t_{sk(pp)}$	3A	3B		0.5	3.4	ns
	CLKAB	3B		0.6	3.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
§ $t_{sk(t)}$ − Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

driver in slot 1, with one receiver in slot 21 (minimum load)

switching characteristics over recommended operating conditions for bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	5.5		7.4	ns
t_{PHL}			5.3		7.4	
t_r‡	Transition time, B port (10%−90%)		3.9	3.4	4.4	ns
t_f‡	Transition time, B port (90%−10%)		3.7	3.4	4.8	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
‡ All t_r and t_f times are taken at the first receiver.

switching characteristics over recommended operating conditions for UBT (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	3A	3B	5.8		7.9	ns
t_{PHL}			5.5		7.7	
t_{PLH}	LE	3B	5.9		8	ns
t_{PHL}			5.5		7.8	
t_{PLH}	CLKAB	3B	5.9		8.1	ns
t_{PHL}			5.5		7.7	
t_r‡	Transition time, B port (10%−90%)		3.9	3.4	4.4	ns
t_f‡	Transition time, B port (90%−10%)		3.7	3.4	4.8	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
‡ All t_r and t_f times are taken at the first receiver.

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B			1.7	ns
$t_{sk(HL)}$					2.1	
$t_{sk(t)}$§	1A or 2A	1B or 2B			1	ns
$t_{sk(pp)}$	1A or 2A	1B or 2B		0.2	2.1	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
§ $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

driver in slot 1, with one receiver in slot 21 (minimum load) (continued)

skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	3A	3B			2	ns
$t_{sk(HL)}$					2.3	
$t_{sk(LH)}$	CLKAB	3B			2.1	ns
$t_{sk(HL)}$					2.4	
$t_{sk(t)}$‡	3A	3B			1	ns
	CLKAB	3B			1	
$t_{sk(pp)}$	3A	3B		0.2	2.5	ns
	CLKAB	3B		0.2	2.9	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
‡ $t_{sk(t)}$ − Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

By simulating the performance of the device using the VME64x backplane (see Figure 3), the maximum peak current in or out of the B-port output, as the devices switch from one logic state to another, was found to be equivalent to driving the lumped load shown in Figure 4.

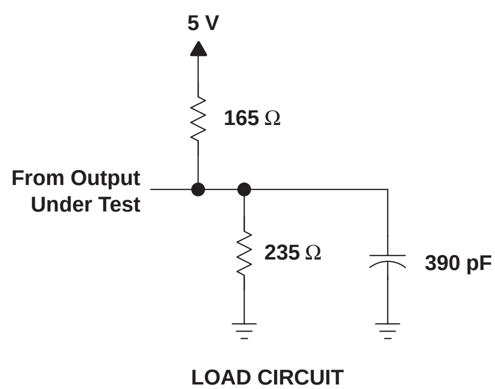


Figure 4. Equivalent AC Peak Output-Current Lumped Load

driver in slot 1, with one receiver in slot 21 (minimum load) (continued)

In general, the rise- and fall-time distribution is shown in Figure 5. Since VME devices were designed for use into distributed loads like the VME64x backplane (B/P), there are significant differences between low-to-high (LH) and high-to-low (HL) values in the lumped load shown in the PMI (see Figures 1 and 2).

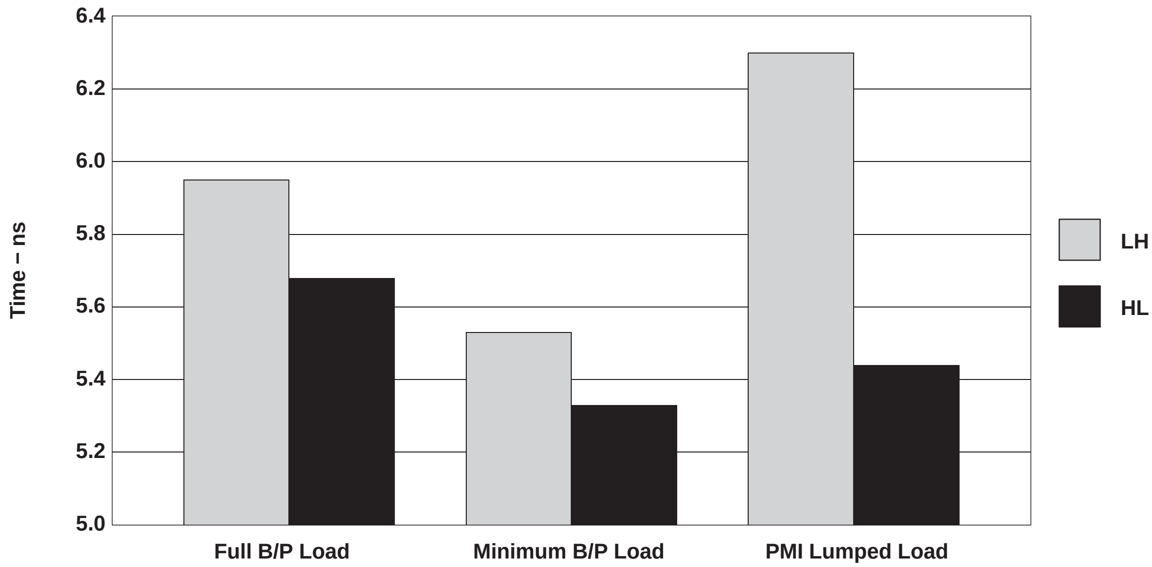


Figure 5

Characterization-laboratory data in Figures 6 and 7 show the absolute ac peak output current, with different supply voltages, as the devices change output logic state. A typical nominal process is shown to demonstrate the devices' peak ac output drive capability.

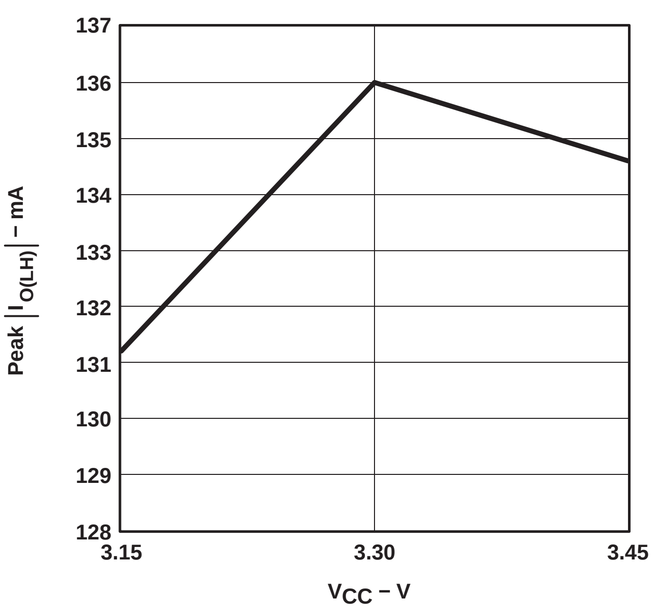


Figure 6

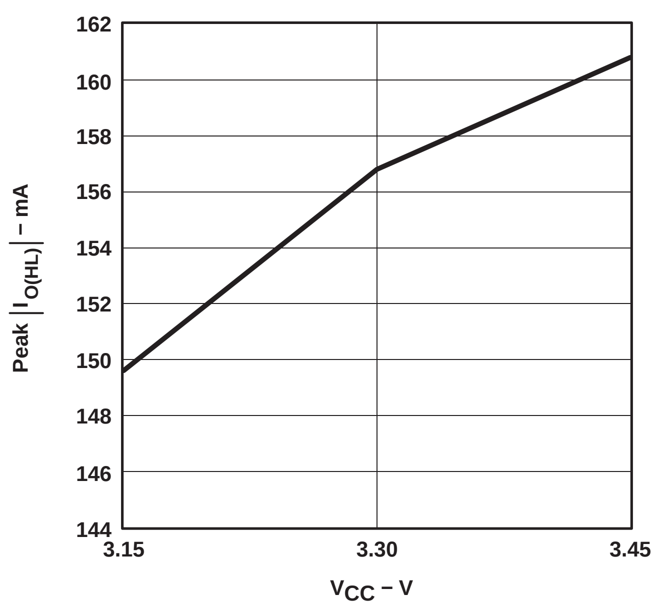


Figure 7

TYPICAL CHARACTERISTICS

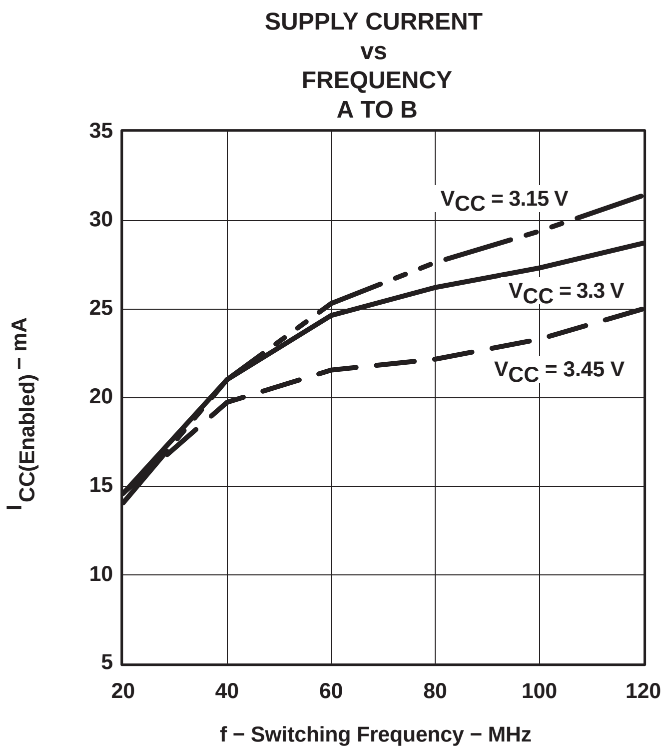


Figure 8

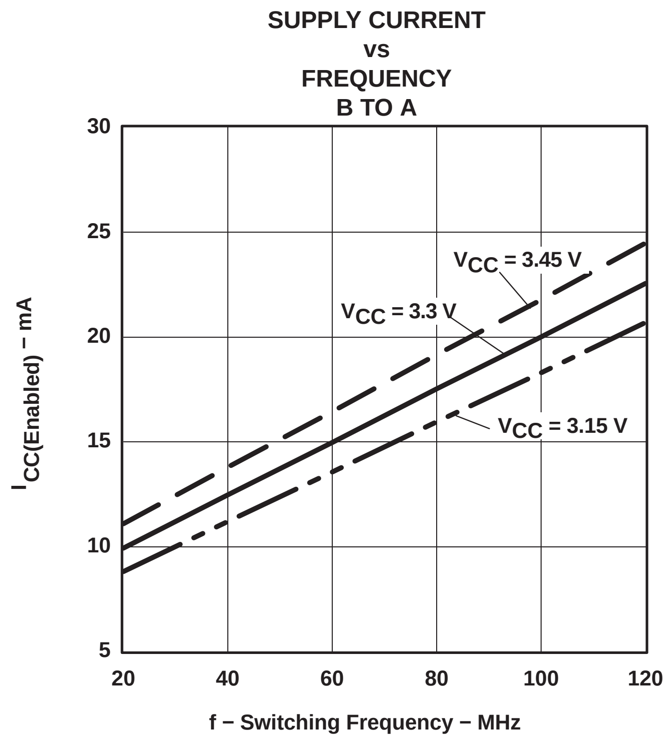


Figure 9

TYPICAL CHARACTERISTICS

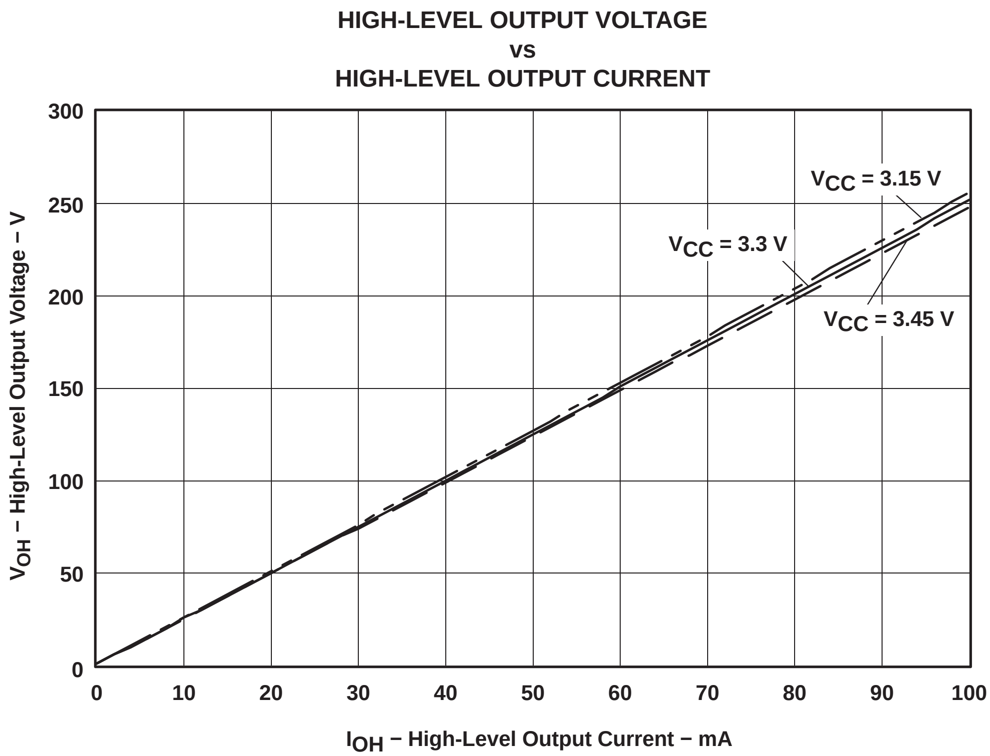


Figure 10. V_{OL} vs I_{OL}

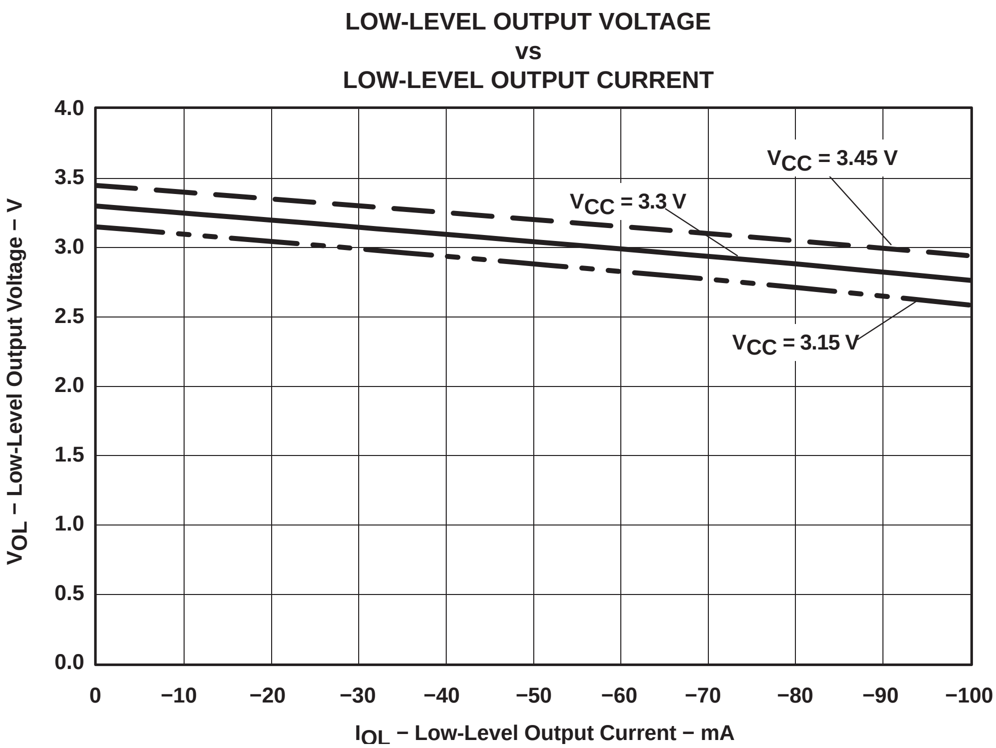


Figure 11. V_{OH} vs I_{OH}

VMEbus SUMMARY

In 1981, the VMEbus was introduced as a backplane bus architecture for industrial and commercial applications. The data-transfer protocols used to define the VMEbus came from the Motorola™ VERSA bus architecture, which owed its heritage to the then recently introduced Motorola 68000 microprocessor. The VMEbus, when introduced, defined two basic data-transfer operations – single-cycle transfers consisting of an address and a data transfer, and a block transfer (BLT) consisting of an address and a sequence of data transfers. These transfers were asynchronous, using a master-slave handshake. The master puts address and data on the bus and waits for an acknowledgment. The selected slave either reads or writes data to or from the bus, then provides a data-acknowledge (DTACK*) signal. The VMEbus system data throughput was 40 Mbyte/s. Previous to the VMEbus, it was not uncommon for the backplane buses to require elaborate calculations to determine loading and drive current for interface design. This approach made designs difficult and caused compatibility problems among manufacturers. To make interface design easier and to ensure compatibility, the developers of the VMEbus architecture defined specific delays based on a 21-slot terminated backplane and mandated the use of certain high-current TTL drivers, receivers, and transceivers.

In 1989, multiplexing block transfer (MBLT) effectively increased the number of bits from 32 to 64, thereby doubling the transfer rate. In 1995, the number of handshake edges was reduced from four to two in the double-edge transfer (2eVME) protocol, doubling the data rate again. In 1997, the VMEbus International Trade Association (VITA) established a task group to specify a synchronous protocol to increase data-transfer rates to 320 Mbyte/s, or more. The unreleased specification, VITA 1.5 [double-edge source synchronous transfer (2eSST)], is based on the asynchronous 2eVME protocol. It does not wait for acknowledgement of the data by the receiver and requires incident-wave switching. Sustained data rates of 1 Gbyte/s, more than ten times faster than traditional VME64 backplanes, are possible by taking advantage of 2eSST and the 21-slot VME320 star-configuration backplane. The VME320 backplane approximates a lumped load, allowing substantially higher-frequency operation over the VME64x distributed-load backplane. Traditional VME64 backplanes with no changes theoretically can sustain 320 Mbyte/s.

From BLT to 2eSST − A Look at the Evolution of VMEbus Protocols by John Rynearson, Technical Director, VITA, provides additional information on VMEbus and can be obtained at www.vita.com.

maximum data transfer rates

DATE	TOPOLOGY	PROTOCOL	DATA BITS PER CYCLE	DATA TRANSFERS PER CLOCK CYCLE	PER SYSTEM (Mbyte/s)	FREQUENCY (MHz)	
						BACKPLANE	CLOCK
1981	VMEbus IEEE-1014	BLT	32	1	40	10	10
1989	VME64	MBLT	64	1	80	10	10
1995	VME64x	2eVME	64	2	160	10	20
1997	VME64x	2eSST	64	2-No Ack	160−320	10−20	20−40
1999	VME320	2eSST	64	2-No Ack	320−1000	20−62.5	40−125

applicability

Target applications for VME backplanes include industrial controls, telecommunications, simulation, high-energy physics, office automation, and instrumentation systems.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74VMEH22501ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74VMEH22501ADGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74VMEH22501ADGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74VMEH22501ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74VMEH22501ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74VMEH22501AGQLR	NRND	BGA MI CROSTA R JUNI OR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74VMEH22501AZQLR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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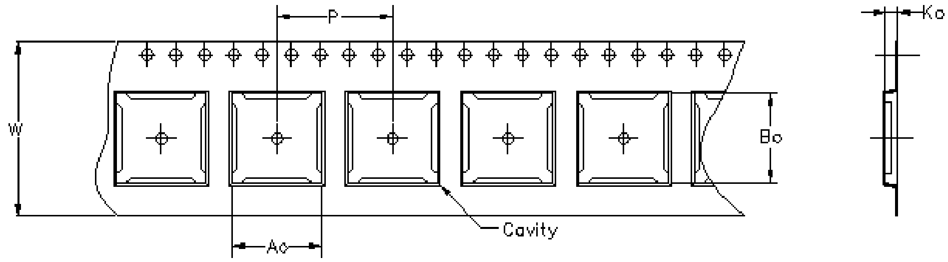
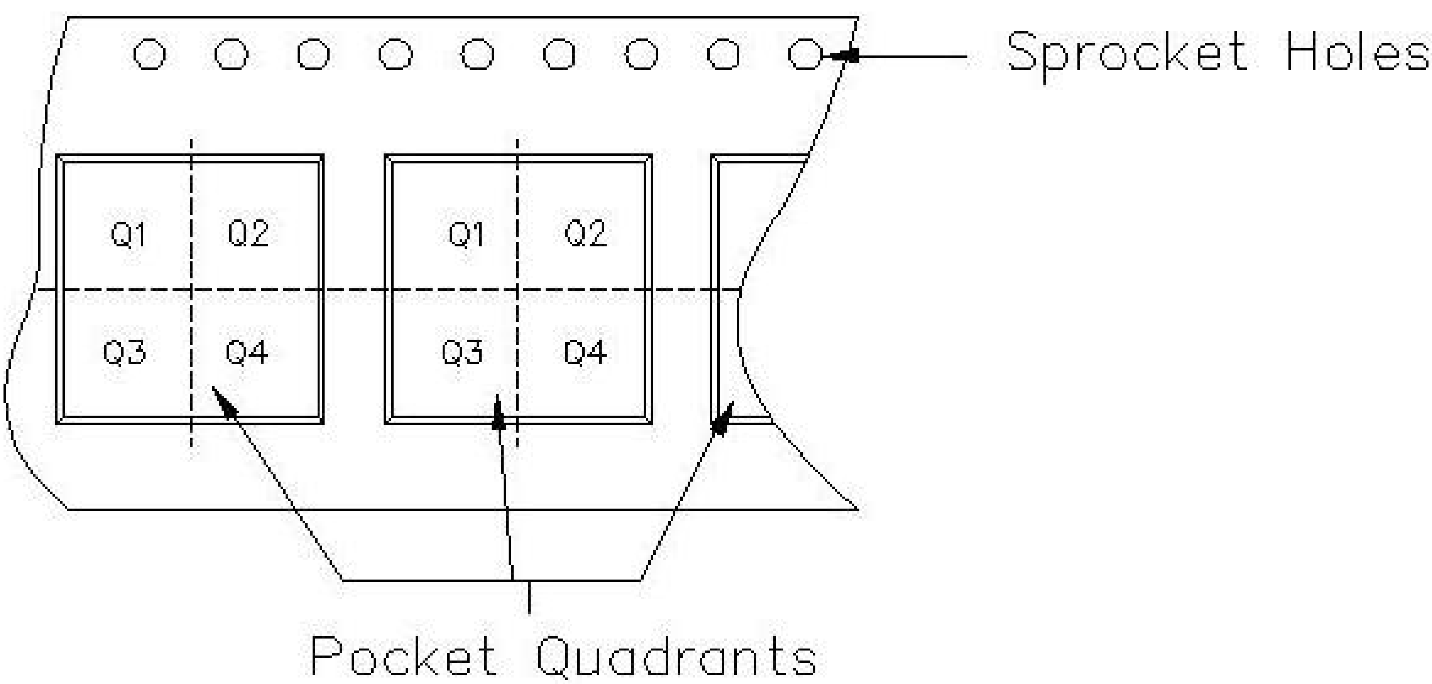


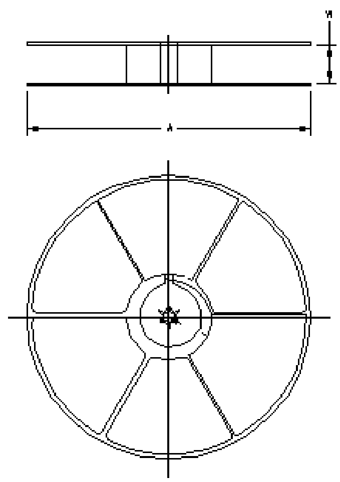
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao =	Dimension designed to accommodate the component width.
Bo =	Dimension designed to accommodate the component length.
Ko =	Dimension designed to accommodate the component thickness.
W =	Overall width of the carrier tape.
P =	Pitch between successive cavity centers.



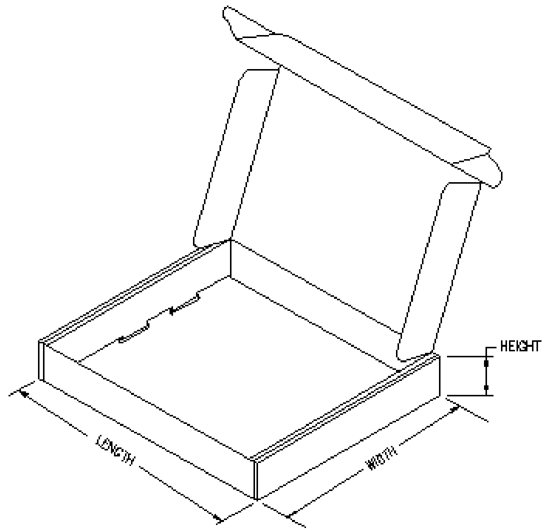
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74VMEH22501ADGGR	DGG	48	MLA	330	24	8.6	15.8	1.8	12	24	Q1
SN74VMEH22501ADGVR	DGV	48	MLA	330	24	6.8	10.1	1.6	12	24	Q1
SN74VMEH22501AGQLR	GQL	56	HIJ	330	16	4.8	7.3	1.45	8	16	Q1
SN74VMEH22501AZQLR	ZQL	56	HIJ	330	16	4.8	7.3	1.45	8	16	Q1

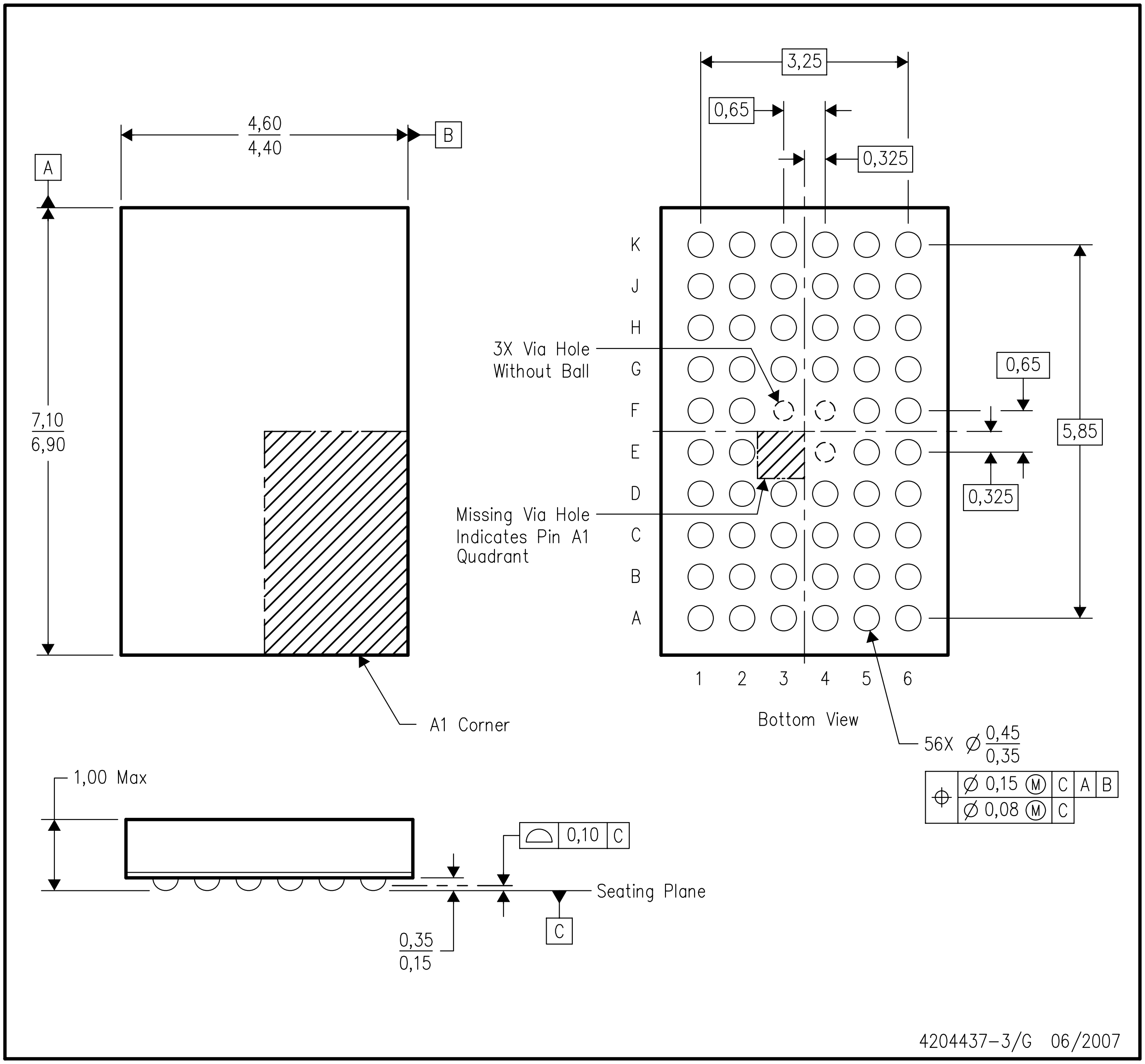


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74VMEH22501ADGGR	DGG	48	MLA	333.2	333.2	31.75
SN74VMEH22501ADGVR	DGV	48	MLA	333.2	333.2	31.75
SN74VMEH22501AGQLR	GQL	56	HIJ	346.0	346.0	33.0
SN74VMEH22501AZQLR	ZQL	56	HIJ	346.0	346.0	33.0


HEIGHT
LENGTH
WIDTH

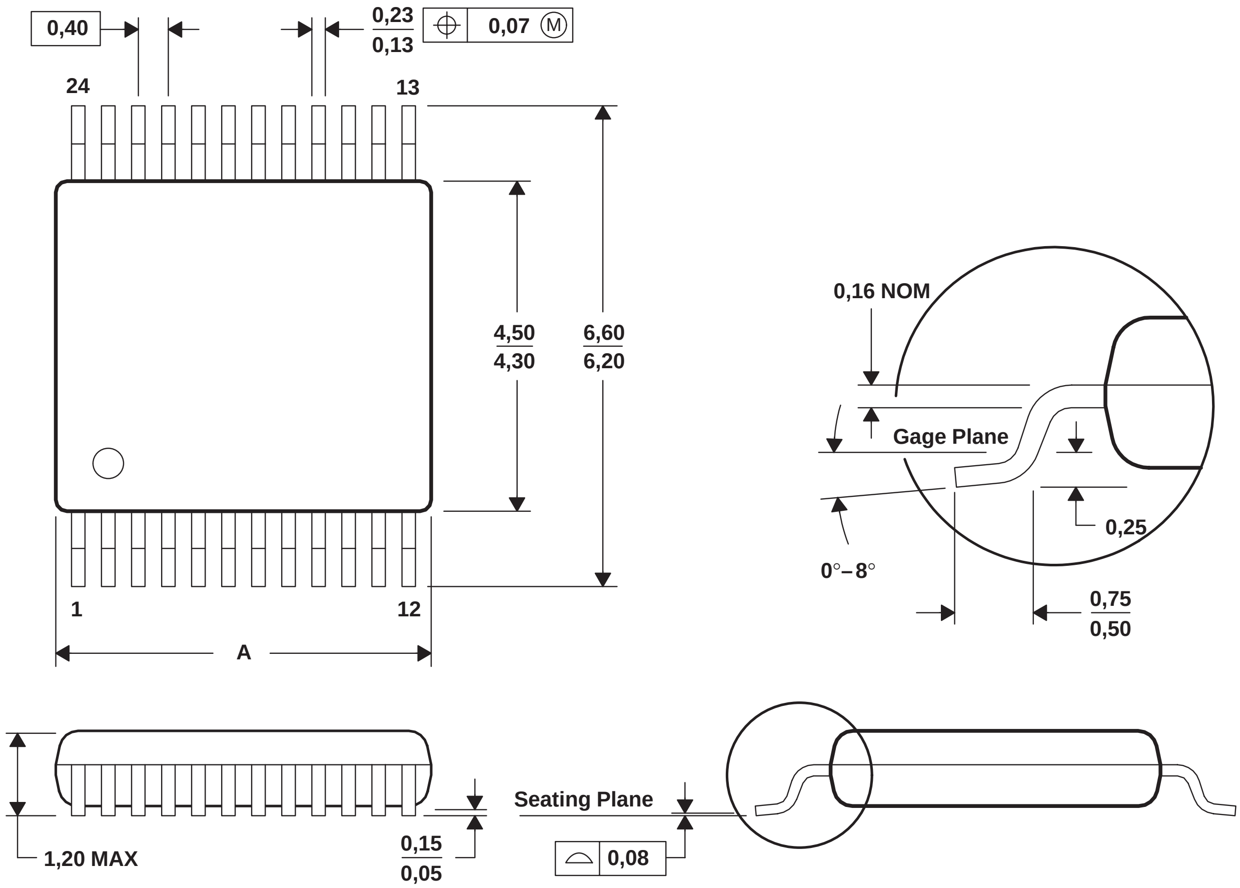
ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO–285 variation BA–2.
- D. This package is lead–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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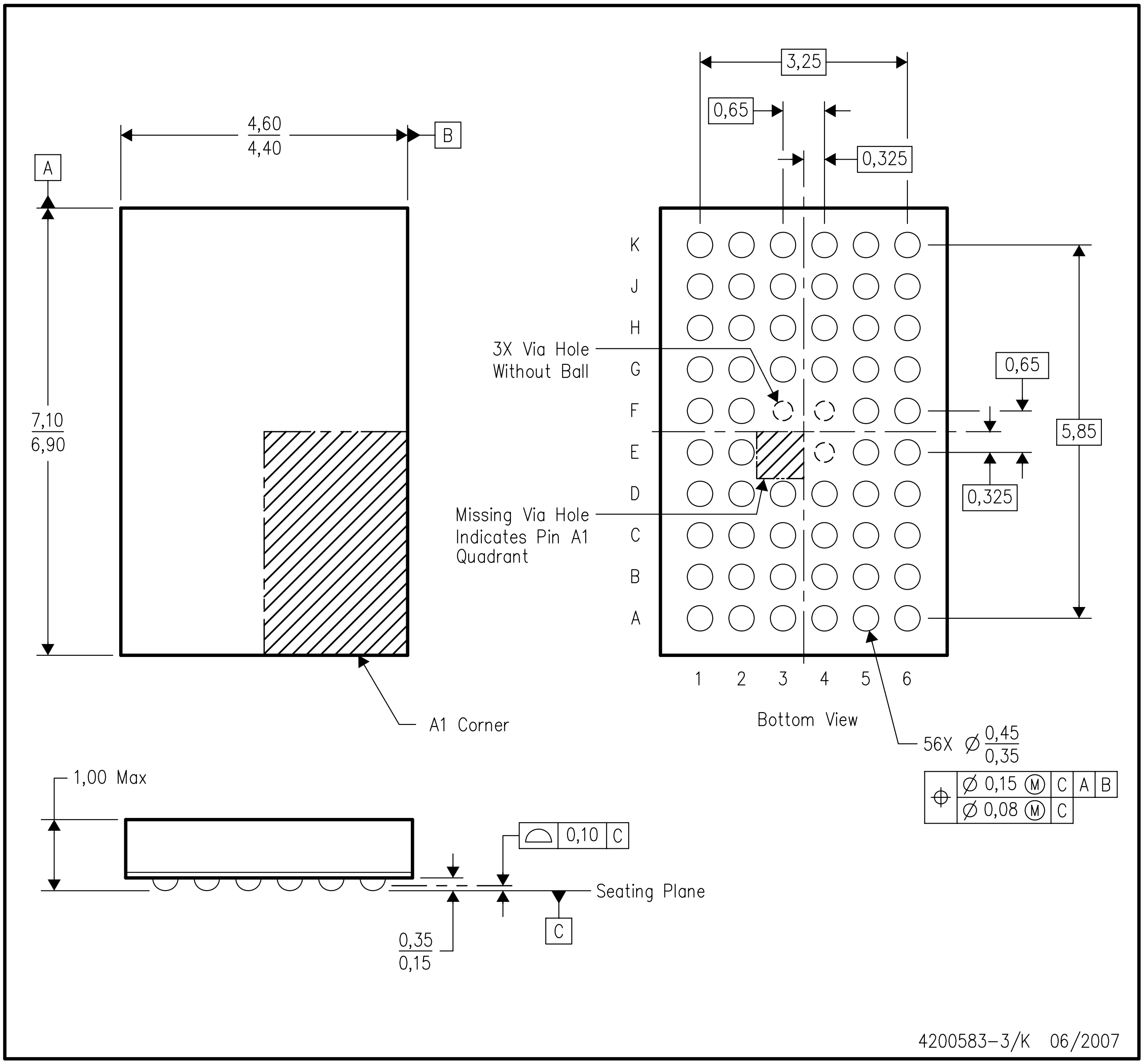
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

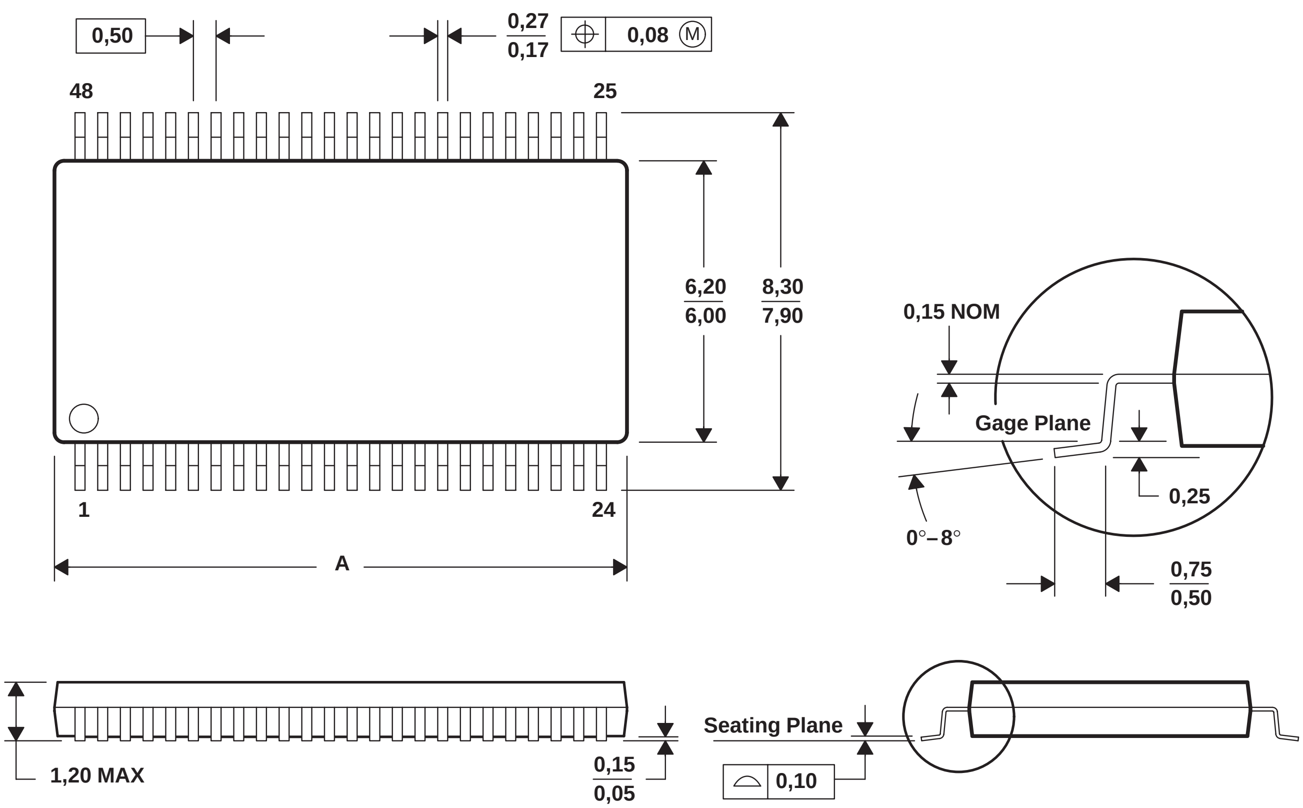
GQL (R-PBGA-N56) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-285 variation BA-2.
D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153