SNx4LV374A Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Maximum t_{pd} of 9.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Programmable Logic Controller (PLC)
- DCS and PAC: Analog Input Module
- Trains, Trams, and Subway Carriages
- AC Inverter Drives
- Printers

3 Description

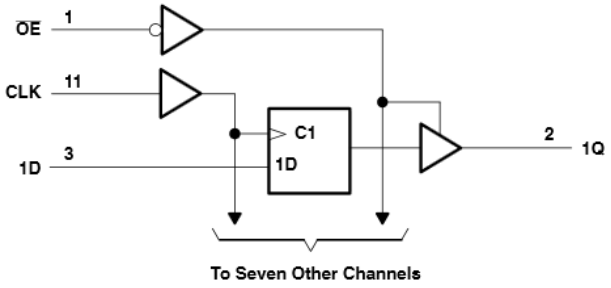
The SNx4LV374A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV374A	SSOP (20)	7.20 mm × 5.30 mm
	SOIC (20)	12.80 mm × 7.50 mm
	SOP (20)	12.60 mm × 5.30 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



Pin numbers shown are for the DB, DW, FK, J, NS, PW, RGY, and W packages.

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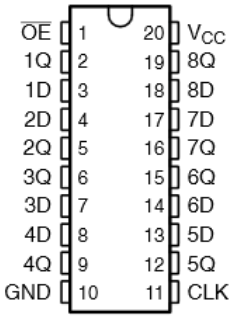
4 Revision History

Changes from Revision H (April 2005) to Revision I **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DB, DW, NS, or PW Package
20 PIN SSOP, SOIC, SOP, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Enable pin
2	1Q	O	Output 1
3	1D	I	Input 1
4	2D	I	Input 2
5	2Q	O	Output 2
6	3Q	O	Output 3
7	3D	I	Input 3
8	4D	I	Input 4
9	4Q	O	Output 4
10	GND	–	Ground pin
11	CLK	I	Clock pin
12	5Q	O	Output 5
13	5D	I	Input 5
14	6D	I	Input 6
15	6Q	O	Output 6
16	7Q	O	Output 7
17	7D	I	Input 7
18	8D	I	Input 8
19	8Q	O	Output 8
20	VCC	–	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	−0.5	7	V
V_I	Input voltage(2)	−0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state (2)	−0.5	7	V
V_O	Output voltage(2)(3)	−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current, (V_I < 0)		–20	mA
I_{OK}	Output clamp current, (V_O < 0)		–50	mA
I_O	Continuous output current, (V_O = 0 to V_{CC})		±35	mA
	Continuous current through V_{CC} or GND		±70	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			SN54LV374A (2)		SN74LV374A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.77		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.3		V_{CC} × 0.3		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.3		V_{CC} × 0.3		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.3		V_{CC} × 0.3		
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−8		−8	
		V_{CC} = 4.5 V to 5.5 V		−16		−16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) PRODUCT PREVIEW

6.4 Thermal Information

THERMAL METRIC (1)		SN74LV374A				UNIT
		DB (SSOP)	DW (SOIC)	NS (SOP)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.5	79.2	76.7	102.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	43.7	43.2	36.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	47	44.2	53.6	
ψ_{JT}	Junction-to-top characterization parameter	18.5	18.6	16.8	2.4	
ψ_{JB}	Junction-to-board characterization parameter	49.3	46.5	43.8	52.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV384A(1)			SN74LV374A –40°C to 85°C			SN74LV374A –40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V_{CC}−0.1			V
	I_{OH} = −2 mA	2.3 V	2			2			2			
	I_{OH} = –8 mA	3 V	2.48			2.48			2.48			
	I_{OH} = −16 mA	4.5 V	3.8			3.8			3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4			0.4	
	I_{OL} = 8 mA	3 V			0.44			0.44			0.44	
	I_{OL} = 16 mA	4.5 V			0.55			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1			±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±5			±5			±5	µA
I_{CC}	V_I = V_{CC} or GND , I_O = 0	5.5 V			20			20			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.9			2.9			2.9		pF

(1) PRODUCT PREVIEW

6.6 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV374A		SN74LV374A –40°C to 85°C		SN74LV374A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	60(1)	105(1)		50(1)		50		50		MHz
			C_L = 50 pF	50	85		40		40		40		
t_{pd}	CLK	Q	C_L = 15 pF		9.7(1)	16.3(1)	1(1)	19(1)	1	19	1	20.5	ns
t_{en}	$\overline{OE}$	Q			8.9(1)	15.9(1)	1(1)	19(1)	1	19	1	20.5	
t_{dis}	$\overline{OE}$	Q			6.3(1)	12.6(1)	1(1)	15(1)	1	15	1	16.5	
t_{pd}	CLK	Q	C_L = 50 pF		11.8	19.3	1	23	1	23	1	24.5	ns
t_{en}	$\overline{OE}$	Q			10.9	18.8	1	22	1	22	1	23.5	
t_{dis}	$\overline{OE}$	Q			8.2	17.3	1	19	1	19	1	20.5	
$t_{sk(o)}$						2				2			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV374A		SN74LV374A –40°C to 85°C		SN74LV374A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80(1)	150(1)		70(1)		70		70		MHz
			C_L = 50 pF	55	110		50		50		50		
t_{pd}	CLK	Q	C_L = 15 pF		6.8(1)	12.7(1)	1(1)	15(1)	1	15	1	16	ns
t_{en}	$\overline{OE}$	Q			6.3(1)	11(1)	1(1)	13(1)	1	13	1	14	
t_{dis}	$\overline{OE}$	Q			4.7(1)	10.5(1)	1(1)	12.5(1)	1	12.5	1	13.5	
t_{pd}	CLK	Q	C_L = 50 pF		8.3	16.2	1	18.5	1	18.5	1	19.5	ns
t_{en}	$\overline{OE}$	Q			7.7	14.5	1	16.5	1	16.5	1	17.5	
t_{dis}	$\overline{OE}$	Q			5.9	14	1	16	1	16	1	17	
$t_{sk(o)}$						1.5				1.5			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV374A		SN74LV374A –40°C to 85°C		SN74LV374A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	130(1)	205(1)		110(1)		110		110		MHz
			C_L = 50 pF	85	1705		75		75		75		
t_{pd}	CLK	Q	C_L = 15 pF		4.9(1)	8.1(1)	1(1)	9.5(1)	1	9.5	1	10.5	ns
t_{en}	$\overline{OE}$	Q			4.6(1)	7.6(1)	1(1)	9(1)	1	9	1	10	
t_{dis}	$\overline{OE}$	Q			3.4(1)	6.8(1)	1(1)	8(1)	1	8	1	9	
t_{pd}	CLK	Q	C_L = 50 pF		5.9	10.1	1	11.5	1	11.5	1	12.5	ns
t_{en}	$\overline{OE}$	Q			5.5	9.6	1	11	1	11	1	12	
t_{dis}	$\overline{OE}$	Q			4	8.8	1	10	1	10	1	11	
$t_{sk(o)}$						1				1			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Timing Requirements

over recommended operating free-air temperature range, (unless otherwise noted) (see Figure 3)

		T_A = 25°C		SN54LV374A (1)		SN74LV374A –40°C to 85°C		SN74LV374A –40°C to 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC} = 2.5 V ± 0.2 V										
t_w	Pulse duration, CLK high or low	6		7		7		7		ns
t_{su}	Setup time, data before CLK↑	5		5.5		5.5		6		ns
t_h	Hold time, data after CLK↑	2.5		2.5		2.5		3		ns
V_{CC} = 3.3 V ± 0.3 V										
t_w	Pulse duration, CLK high or low	5		5.5		5.5		5.5		ns
t_{su}	Setup time, data before CLK↑	4.5		45		4.5		5		ns
t_h	Hold time, data after CLK↑	2		2		2		2.5		ns
V_{CC} = 5 V ± 0.5 V										
t_w	Pulse duration, CLK high or low	5		5		5		5		ns
t_{su}	Setup time, data before CLK↑	3		3		3		3.5		ns
t_h	Hold time, data after CLK↑	2		2		2		2.5		ns

(1) PRODUCT PREVIEW

6.10 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (1)

PARAMETER		SN74LV374A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.5	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.9	2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.11 Operating Characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	21.1	pF
			5 V	22.8	

6.12 Typical Characteristics

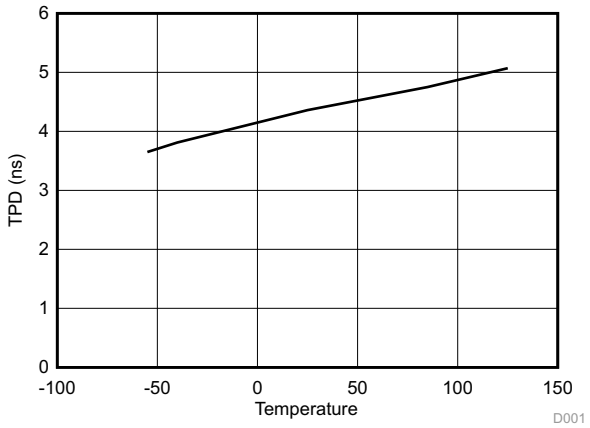


Figure 1. TPD vs. Temperature at 5 V

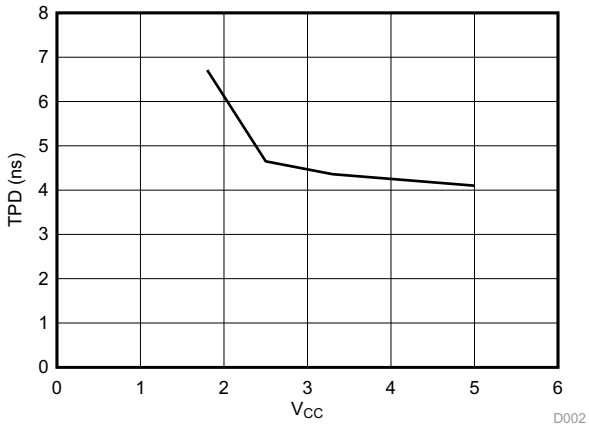
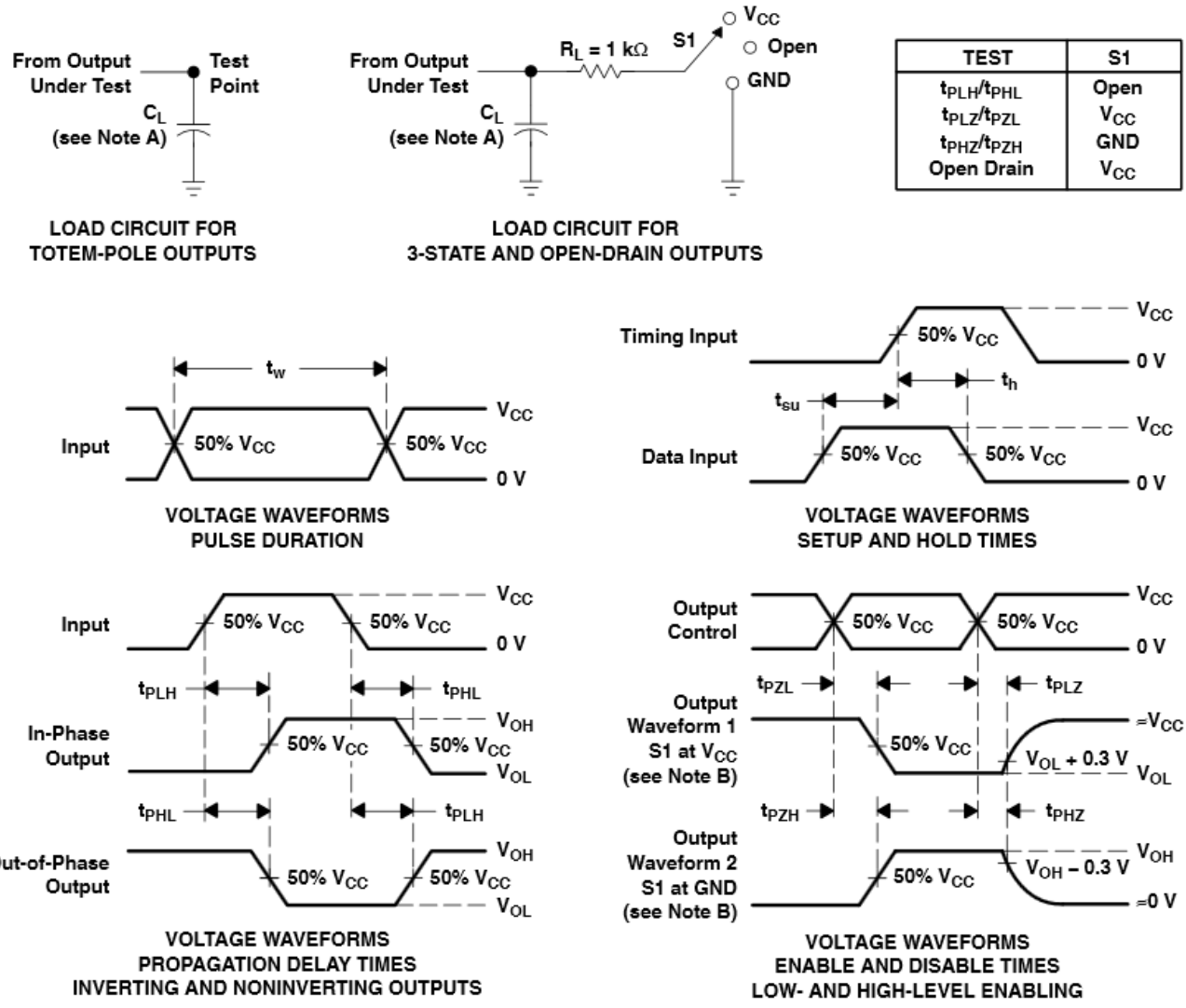


Figure 2. TPD vs. V_{CC} at 25°C

7 Parameter Measurement Information



NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4LV374A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation. These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bi-directional bus drivers, and working registers. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs. A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. These devices are fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The output of the device is unknown until the first valid rising clock edge occurs while V_{CC} is within the *Recommended Operating Conditions* range.

8.2 Functional Block Diagram

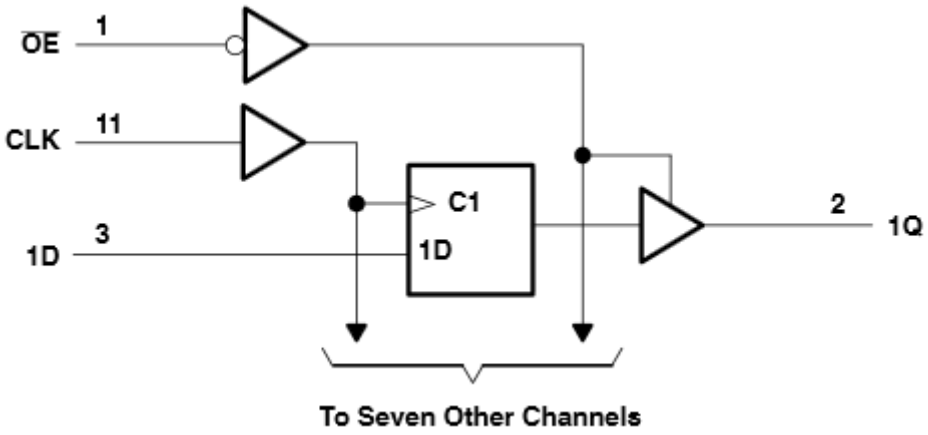


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

The device's wide operating range allows it to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

Table 1. Function Table (Each Flip-Flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV374A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V allowing down translation to the V_{CC} level.

9.2 Typical Application

Figure 5 shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

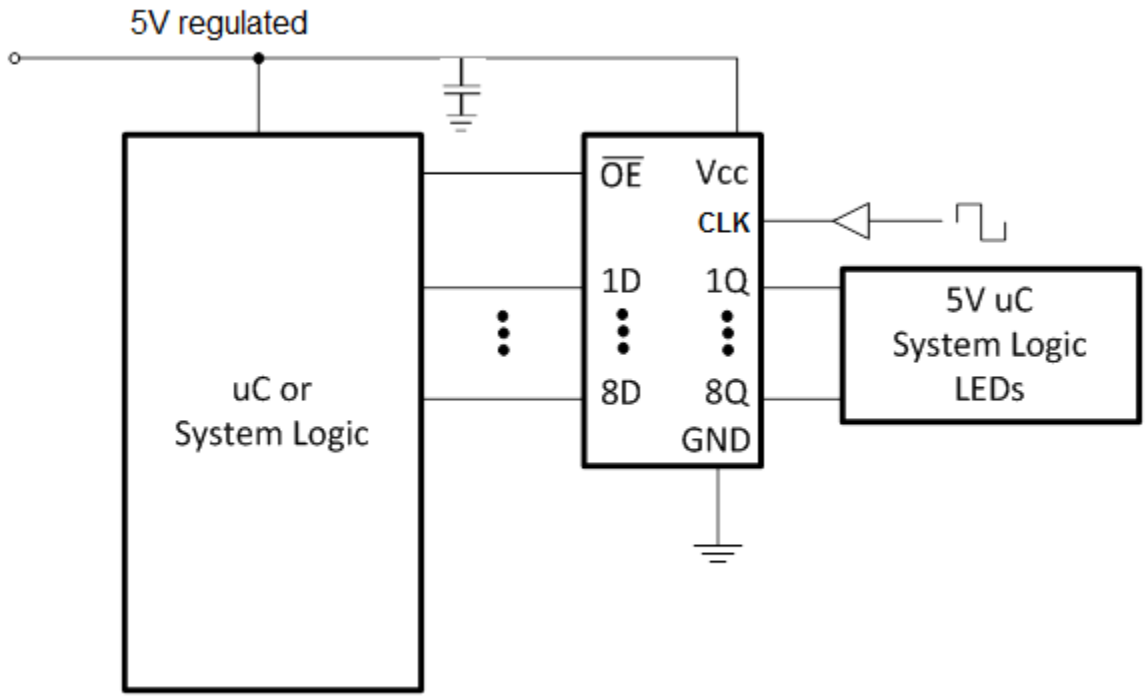


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

Typical Application (continued)

9.2.2 Detailed Design Procedure

- Recommended Input conditions:
  - Rise time and fall time specs see (Δt/ΔV) in *Recommended Operating Conditions*.
  - Specified High and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommend output conditions:
  - Load currents should not exceed 35 mA per output and 70 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

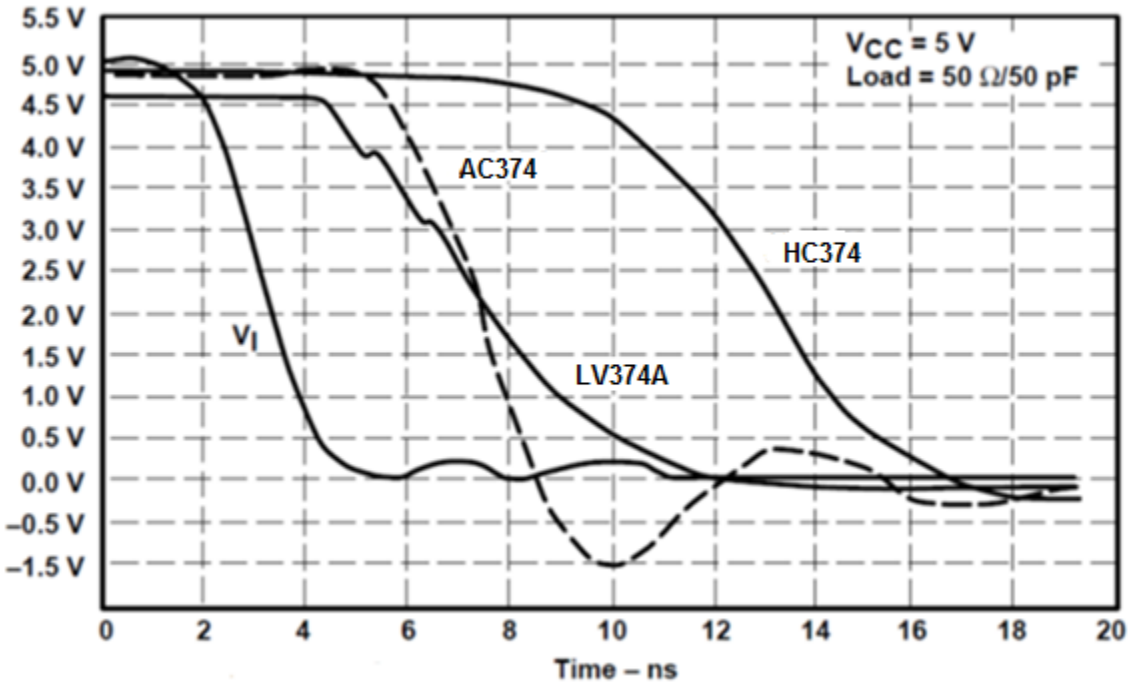


Figure 6. Switching Characteristics Comparison

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

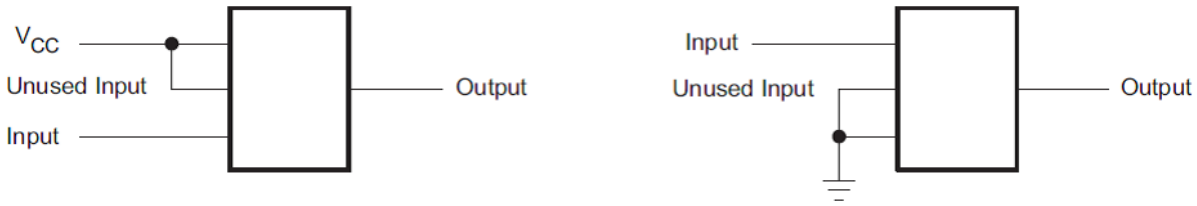


Figure 7. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV374ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A	Samples
SN74LV374ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A	Samples
SN74LV374ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A	Samples
SN74LV374ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A	Samples
SN74LV374ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV374A	Samples
SN74LV374ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV374A	Samples
SN74LV374APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A	Samples
SN74LV374APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A	Samples
SN74LV374APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LV374A :

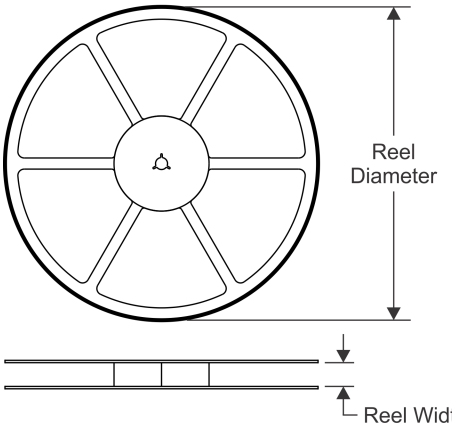
- Automotive: SN74LV374A-Q1
- Enhanced Product: SN74LV374A-EP

NOTE: Qualified Version Definitions:

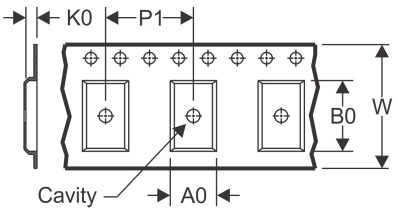
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

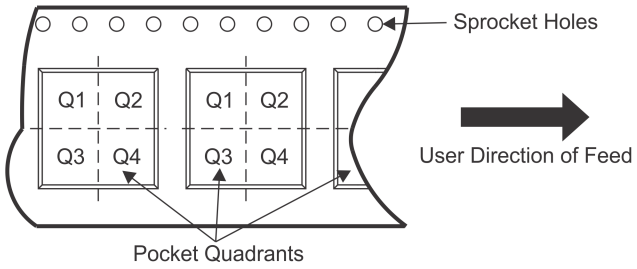


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

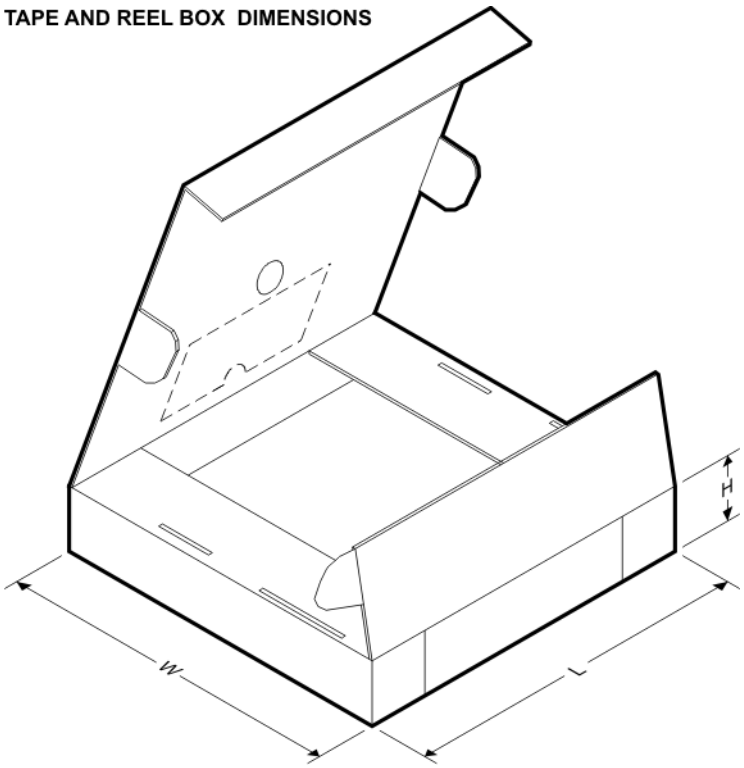
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV374ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV374ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV374ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LV374APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

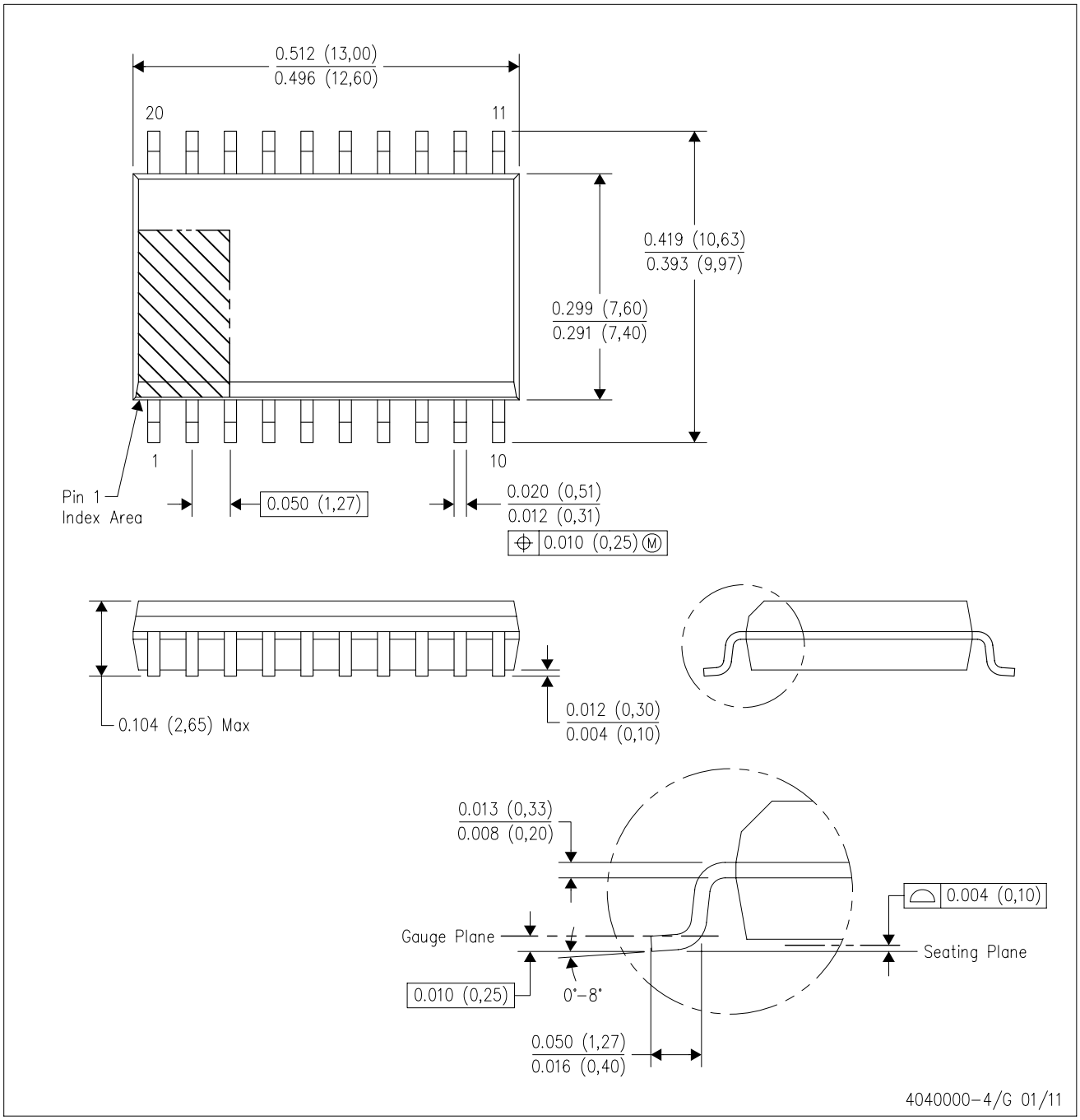
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

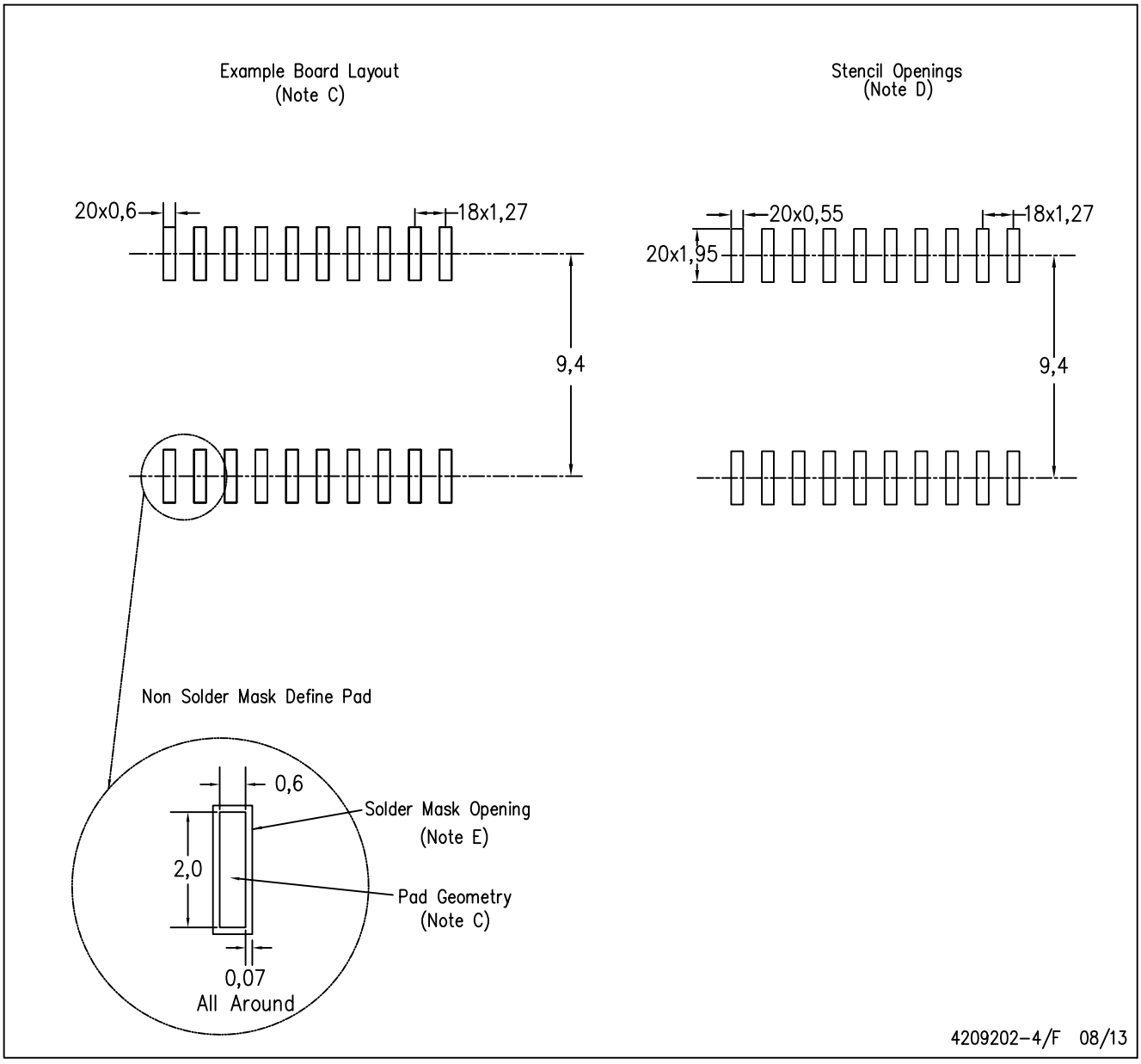
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV374ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LV374ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV374ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV374APWR	TSSOP	PW	20	2000	367.0	367.0	38.0

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



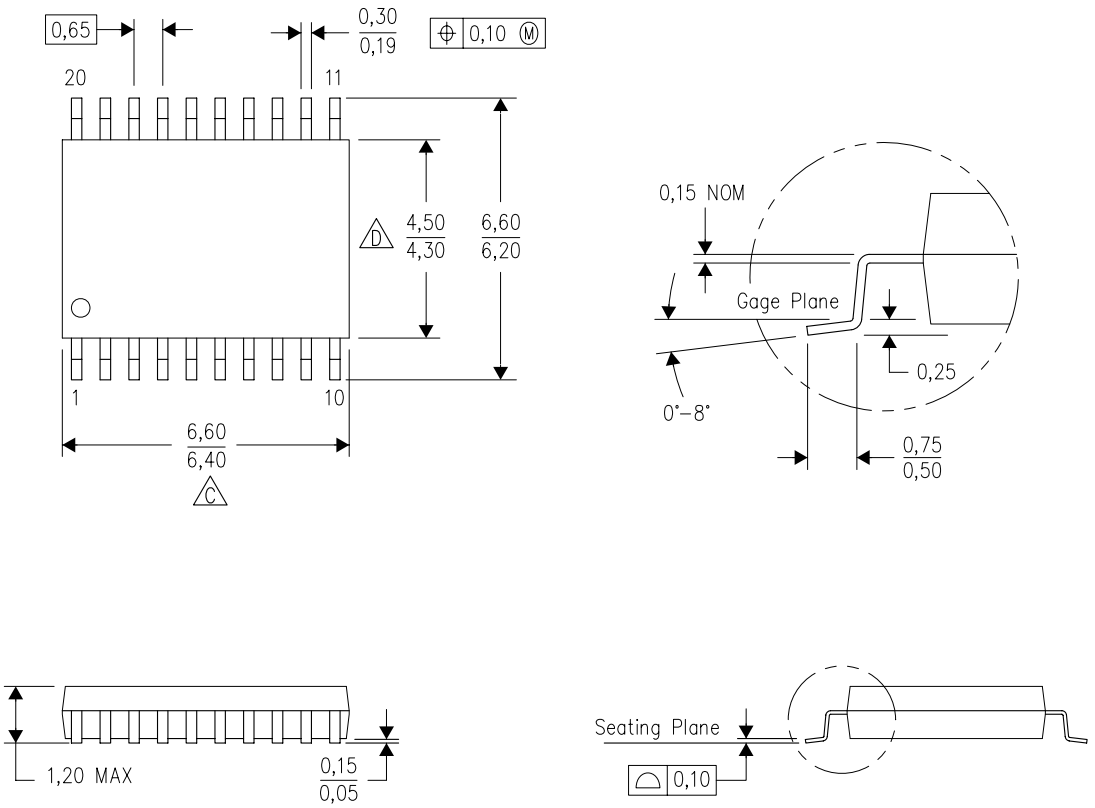
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

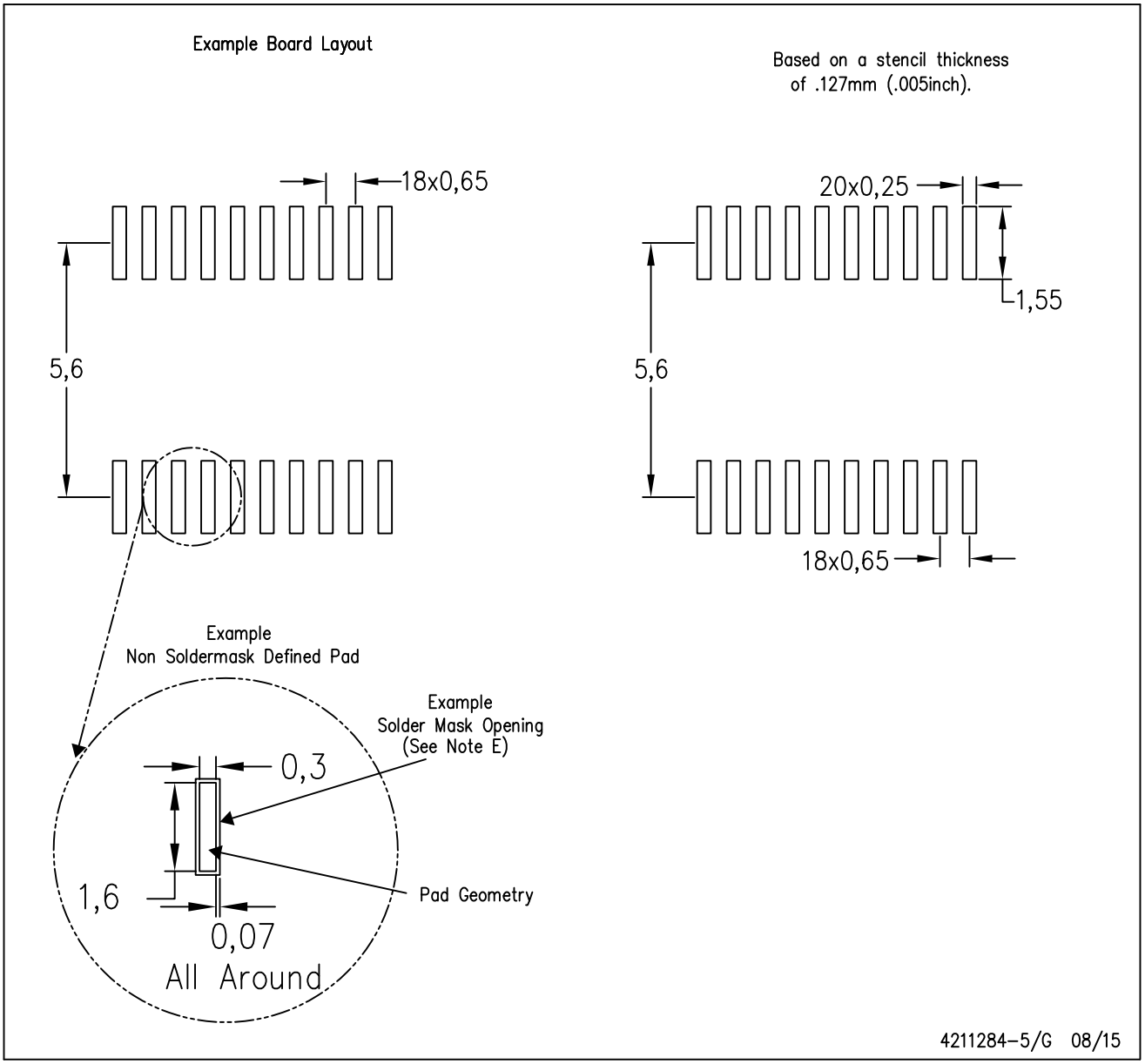
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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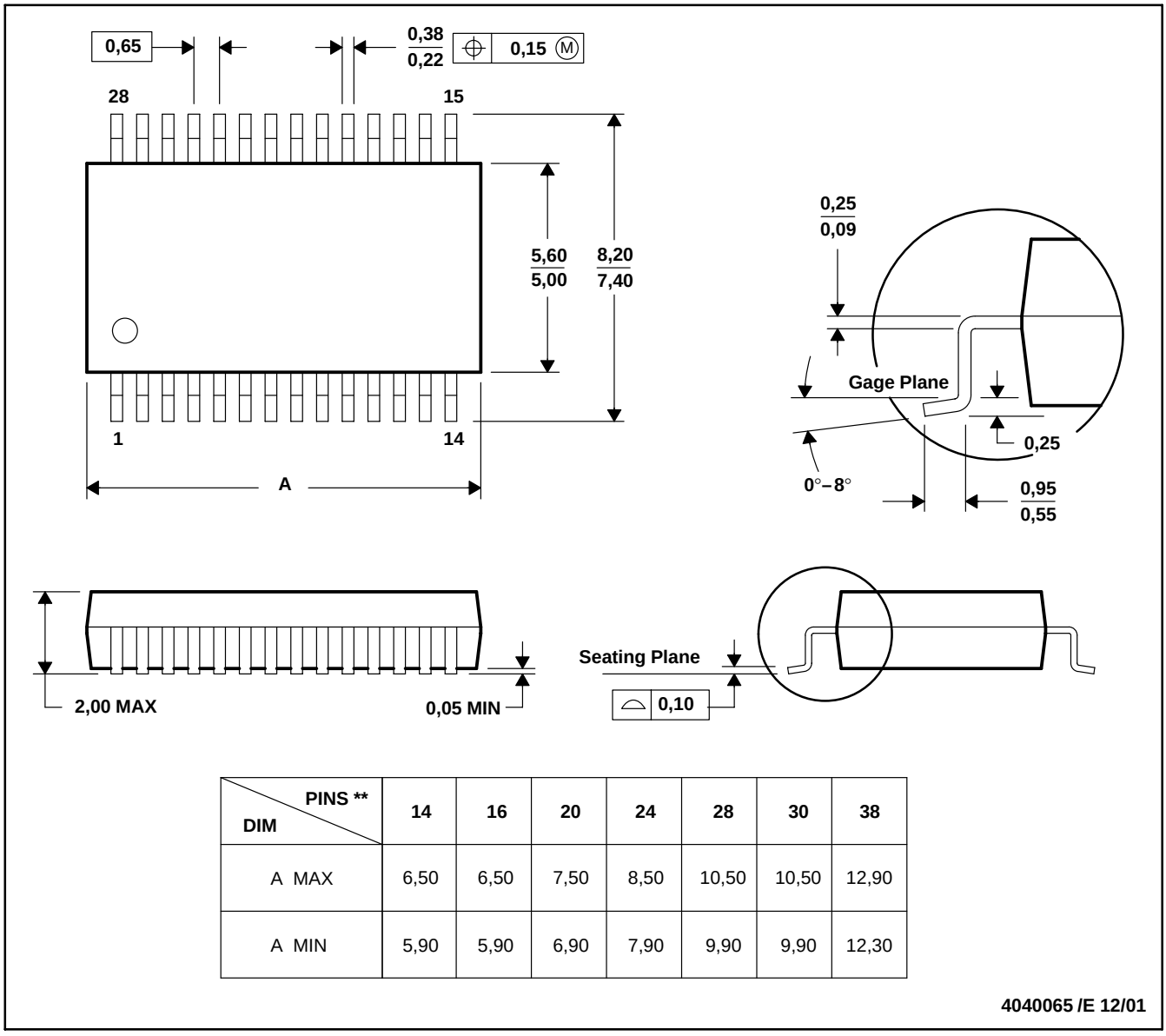
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

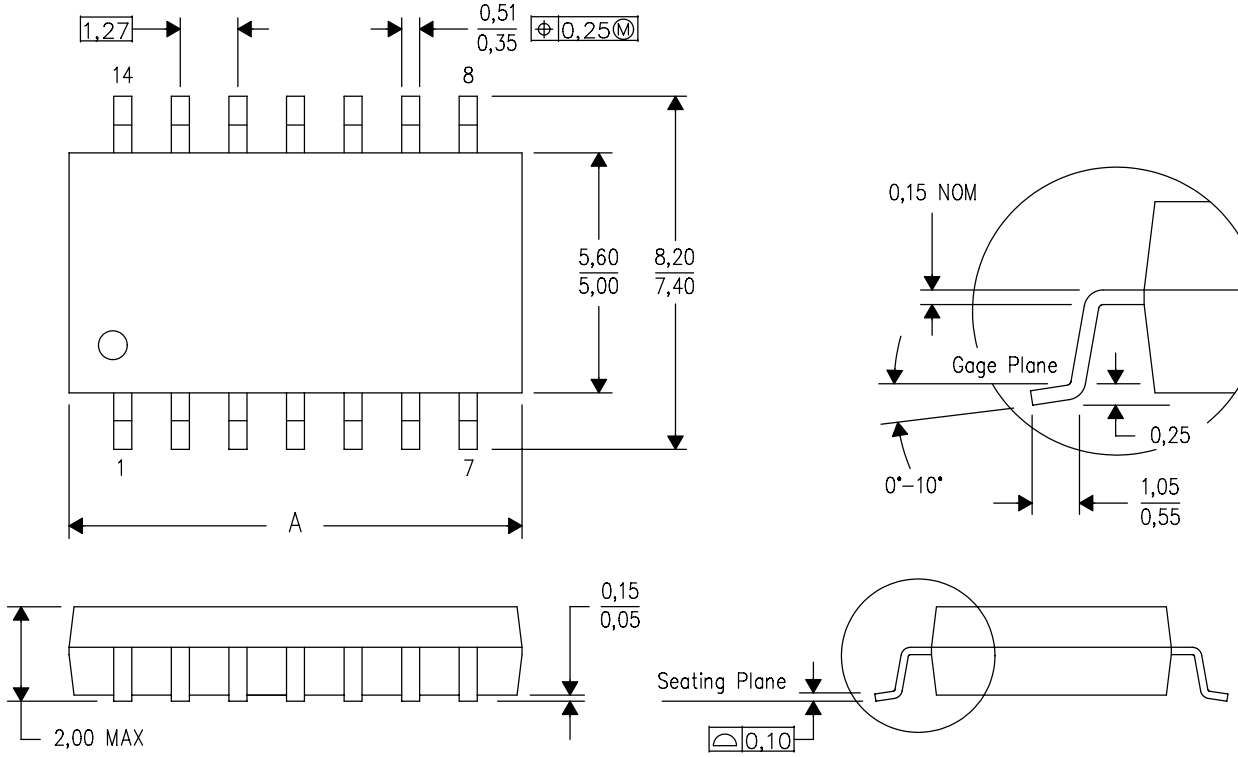
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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