

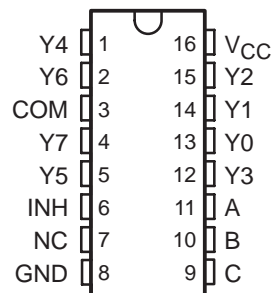
SN74HC4851

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

- Injection-Current Cross Coupling <math><1\text{mV/mA}</math> (see Figure 1)
- Low Crosstalk Between Switches
- Pin Compatible With SN74HC4051, SN74LV4051A, and CD4051B
- 2-V to 6-V V_{CC} Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

D, DGV, N, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

This eight-channel CMOS analog multiplexer/demultiplexer is pin compatible with the '4051 function and, additionally, features injection-current effect control, which has excellent value in automotive applications where voltages in excess of normal supply voltages are common.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	PDIP – N	Tube	SN74HC4851N	HC4851N
	SOIC – D	Tube	SN74HC4851D	HC4851
		Tape and reel	SN74HC4851DR	
	TSSOP – PW	Tube	SN74HC4851PW	HC4851
		Tape and reel	SN74HC4851PWR	
	TVSOP – DGV	Tape and reel	SN74HC4851DGVR	HC4851

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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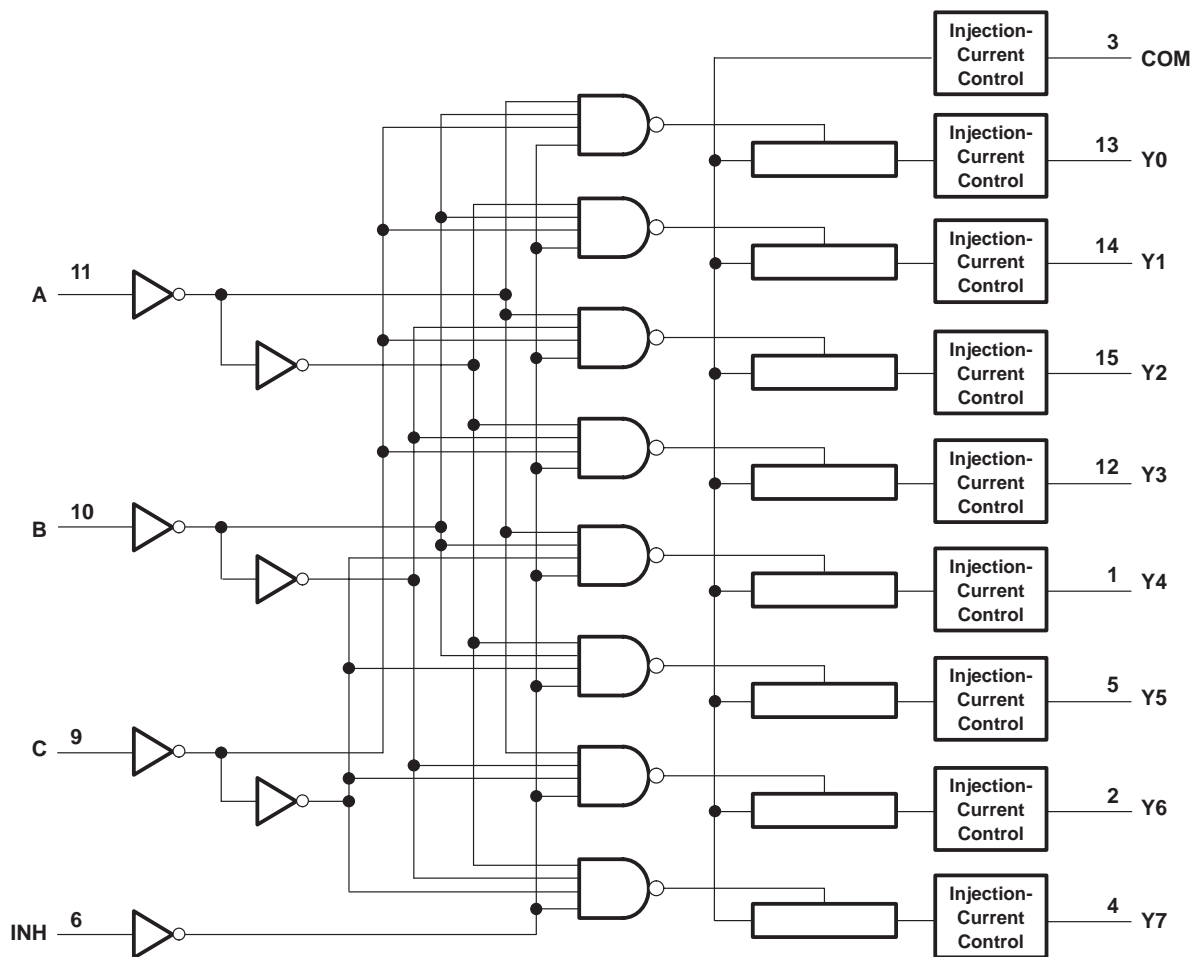
SN74HC4851
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

logic diagram (positive logic)



SN74HC4851

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)	±20 mA
Switch through current, I_T ($V_{IO} = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DGV package	120°C/W
N package	67°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	6	V
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 3.3$ V	2.3	
		$V_{CC} = 4.5$ V	3.15	
		$V_{CC} = 6$ V	4.2	
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 3.3$ V	1	
		$V_{CC} = 4.5$ V	1.35	
		$V_{CC} = 6$ V	1.8	
V_I	Control input voltage	0	V_{CC}	V
V_{IO}	Input/output voltage	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time	$V_{CC} = 2$ V	1000	ns
		$V_{CC} = 3$ V	800	
		$V_{CC} = 3.3$ V	700	
		$V_{CC} = 4.5$ V	500	
		$V_{CC} = 6$ V	400	
T_A	Operating free-air temperature	–40	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74HC4851

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r _{on}	On-state switch resistance	I _T ≤ 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL} (see Figure 5)	2. V	500	650		670	700	Ω		
			3 V	215	280		320	360			
			3.3 V	210	270		305	345			
			4.5 V	160	210		240	270			
			6 V	150	195		220	250			
Δr _{on}	Difference in on-state resistance between switches	I _T ≤ 2 mA, V _I = V _{CC} /2, V _{INH} = V _{IL}	2. V	4	10		15	20	Ω		
			3 V	2	8		12	16			
			3.3 V	2	8		12	16			
			4.5 V	2	8		12	16			
			6 V	3	9		13	18			
I _I	Control input current	V _I = V _{CC} or GND	6 V		±0.1		±0.1	±1	μA		
I _{S(off)}	Off-state switch leakage current (any one channel)	V _I = V _{CC} or GND, V _{INH} = V _{IH} (see Figure 6)	6 V		±0.1		±0.5	±1	μA		
	Off-state switch leakage current (common channel)	V _I = V _{CC} or GND, V _{INH} = V _{IH} (see Figure 7)			±0.2		±2	±4			
I _{S(on)}	On-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 8)	6 V		±0.1		±0.5	±1	μA		
I _{CC}	Supply current	V _I = V _{CC} or GND	6 V		2		20	40	μA		
C _{IC}	Control input capacitance	A, B, C, INH			3.5	10	10	10	pF		
C _{IS}	Common terminal capacitance	Switch off			22	40	40	40	pF		
C _{OS}	Switch terminal capacitance	Switch off			6.7	15	15	15	pF		

injection current coupling specifications, T_A = -40°C to 125°C

PARAMETER		V _{CC}	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{Δout}	Maximum shift of output voltage of enabled analog channel	3.3 V	R _S ≤ 3.9 kΩ	I _I ‡ ≤ 1 mA	0.05	1	mV	
		5 V			0.1	1		
		3.3 V		R _S ≤ 3.9 kΩ	I _I ‡ ≤ 10 mA	0.345		5
		5 V				0.067		5
		3.3 V	R _S ≤ 20 kΩ	I _I ‡ ≤ 1 mA	0.05	2		
		5 V			0.11	2		
		3.3 V		R _S ≤ 20 kΩ	I _I ‡ ≤ 10 mA	0.05		20
		5 V				0.024		20

† Typical values are measured at T_A = 25°C.

‡ I_I = total current injected into all disabled channels



SN74HC4851
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			UP TO 85°C		UP TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n		19.5	25		29		32	ns
t _{PLH} t _{PHL}	Propagation delay time	Channel Select		23	30		35		40	ns
t _{PZH} t _{PZL}	Enable delay time	INH			95		105		115	ns
t _{PHZ} t _{PLZ}	Disable delay time	INH			95		105		115	ns

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			UP TO 85°C		UP TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n		12	15.5		17.5		19.5	ns
t _{PLH} t _{PHL}	Propagation delay time	Channel Select		13.5	17.5		20		23	ns
t _{PZH} t _{PZL}	Enable delay time	INH			90		100		110	ns
t _{PHZ} t _{PLZ}	Disable delay time	INH			90		100		110	ns

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			UP TO 85°C		UP TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n		11	14.5		16.5		18.5	ns
t _{PLH} t _{PHL}	Propagation delay time	Channel Select		12.5	16.5		19		22	ns
t _{PZH} t _{PZL}	Enable delay time	INH			85		95		105	ns
t _{PHZ} t _{PLZ}	Disable delay time	INH			85		95		105	ns

SN74HC4851
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 4.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			UP TO 85°C		UP TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH tPHL	Propagation delay time	COM or Yn		8.6	11.5		12.5		13.5	ns
tPLH tPHL	Propagation delay time	Channel Select		10	13		15		17	ns
tPZH tPZL	Enable delay time	INH			80		90		100	ns
tPHZ tPLZ	Disable delay time	INH			80		90		100	ns

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 6\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			UP TO 85°C		UP TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH tPHL	Propagation delay time	COM or Yn		8	10		11		12	ns
tPLH tPHL	Propagation delay time	Channel Select		9.5	12.5		14.5		16.5	ns
tPZH tPZL	Enable delay time	INH			78		80		80	ns
tPHZ tPLZ	Disable delay time	INH			78		80		80	ns

operating characteristics, $T_A = 25^\circ\text{C}$ (see Figure 15)

PARAMETER		V_{CC}	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	3.3 V	No load	32	pF
		5 V		37	



SN74HC4851
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

APPLICATION INFORMATION

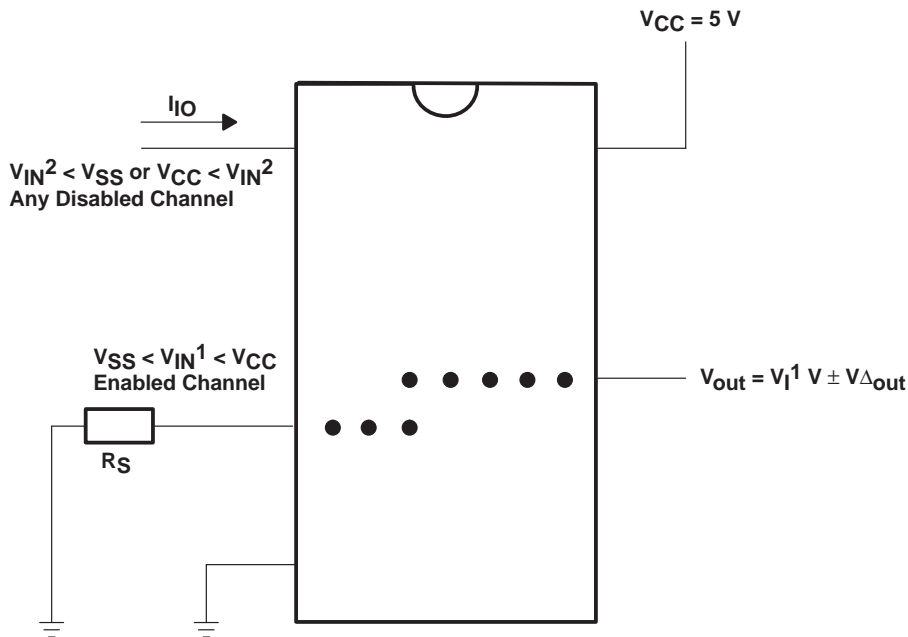


Figure 1. Injection-Current Coupling Specification

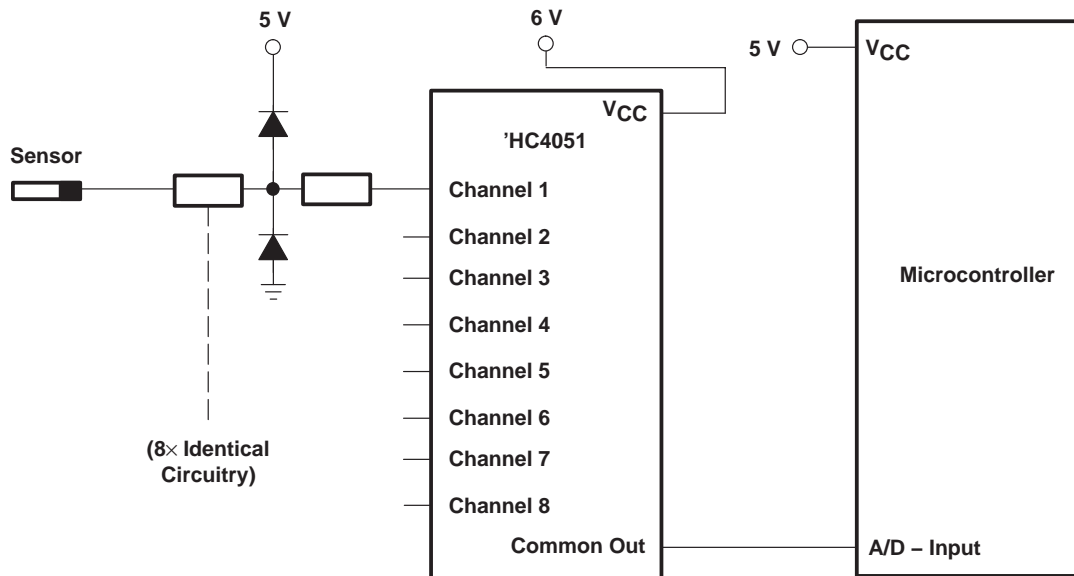


Figure 2. Alternate Solution Requires 32 Passive Components and One Extra 6-V Regulator to Suppress Injection Current Into a Standard 'HC4051 Multiplexer

SN74HC4851
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

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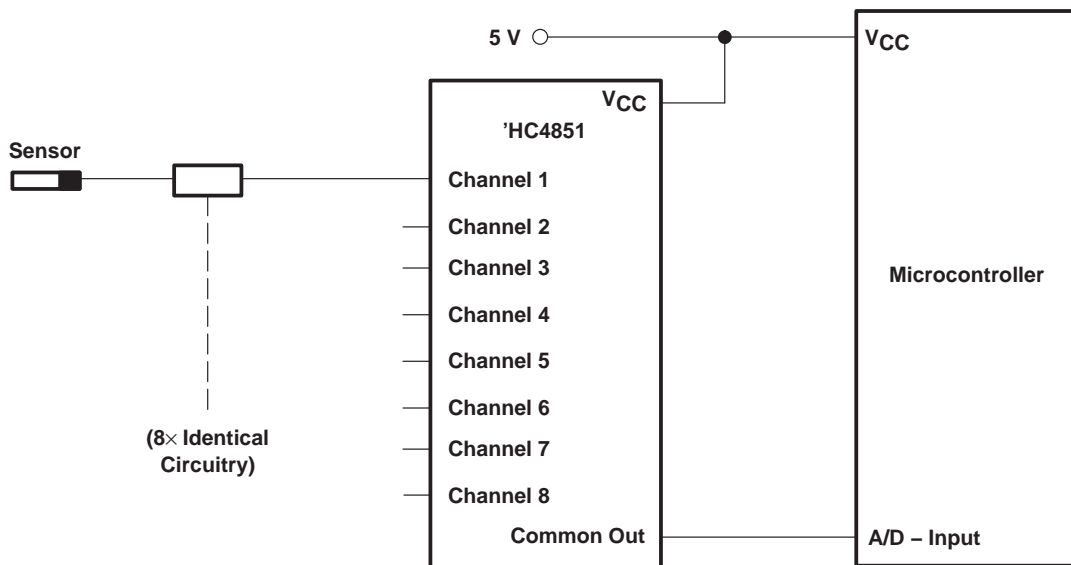


Figure 3. Solution by Applying the 'HC4851 Multiplexer

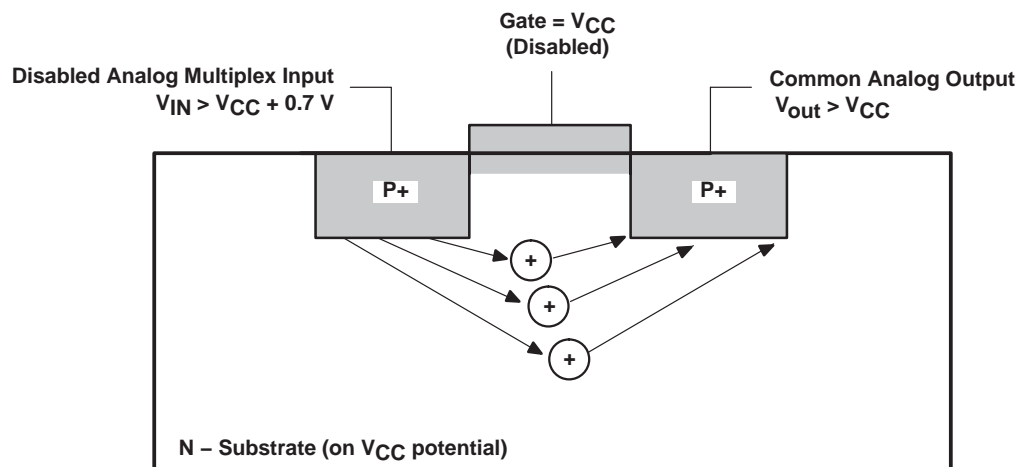


Figure 4. Diagram of Bipolar Coupling Mechanism
(Appears if V_{IN} Exceeds V_{CC}, Driving Injection Current Into the Substrate)

PARAMETER MEASUREMENT INFORMATION

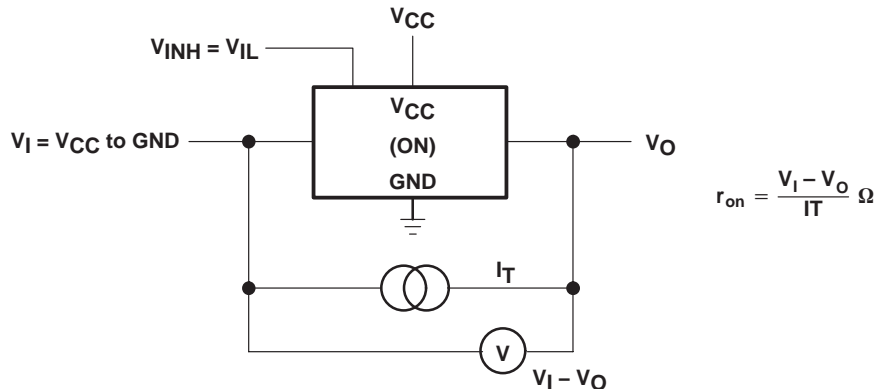


Figure 5. On-State-Resistance Test Circuit

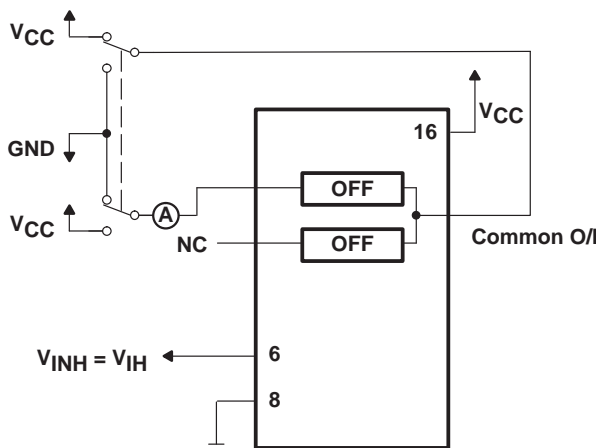


Figure 6. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup

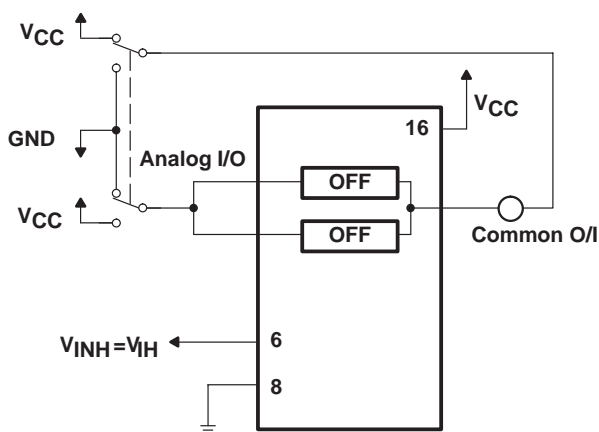


Figure 7. Maximum Off-Channel Leakage Current, Common Channel, Test Setup

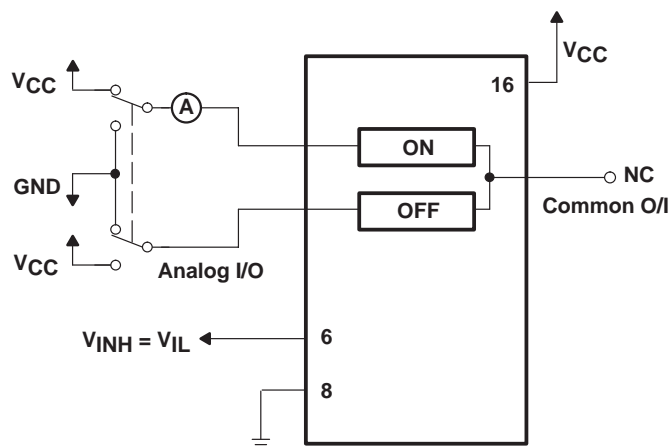


Figure 8. Maximum On-Channel Leakage Current, Channel To Channel, Test Setup

SN74HC4851
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
WITH INJECTION-CURRENT EFFECT CONTROL

SCLS542B – SEPTEMBER 2003 – REVISED JANUARY 2004

PARAMETER MEASUREMENT INFORMATION

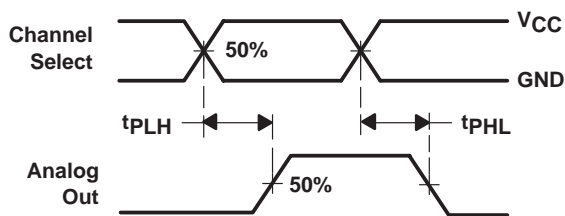


Figure 9. Propagation Delays, Channel Select to Analog Out

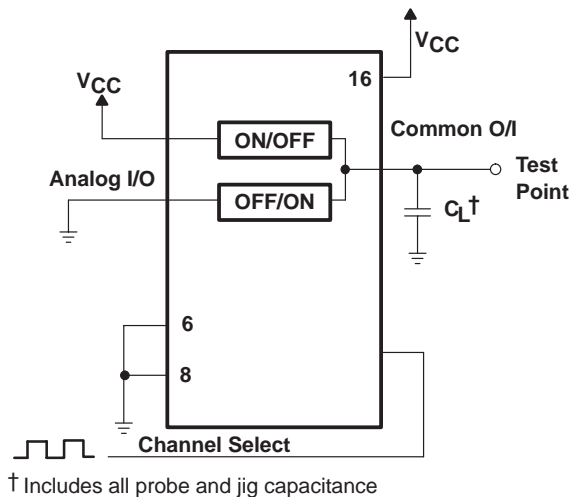


Figure 10. Propagation-Delay Test Setup, Channel Select to Analog Out

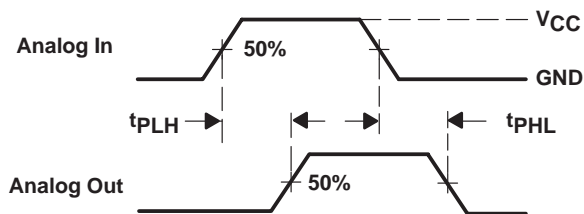


Figure 11. Propagation Delays, Analog In to Analog Out

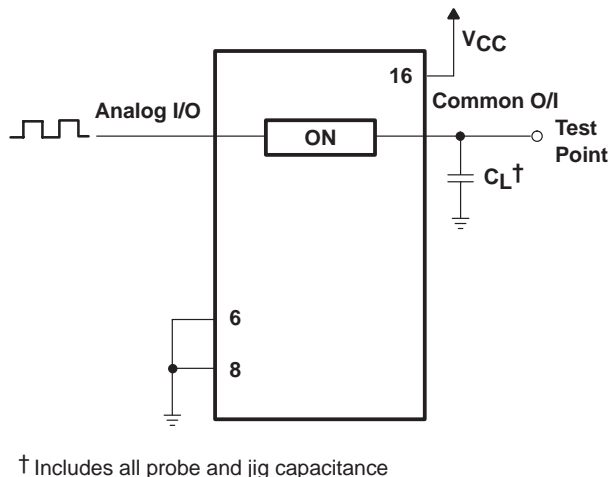


Figure 12. Propagation-Delay Test Setup, Analog In to Analog Out

PARAMETER MEASUREMENT INFORMATION

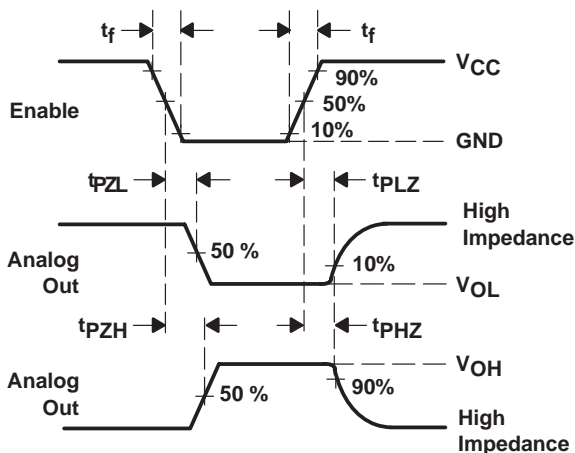


Figure 13. Propagation Delays, Enable to Analog Out

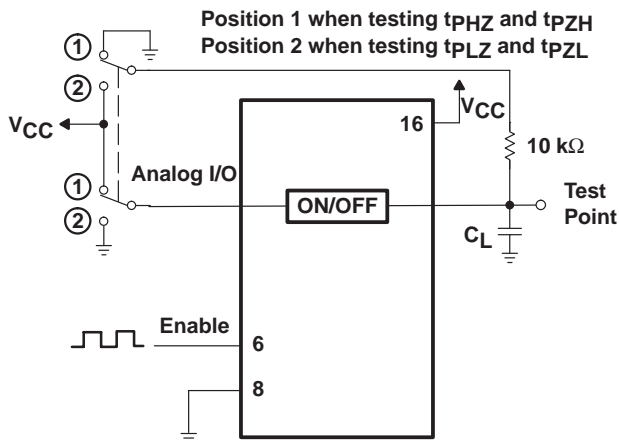


Figure 14. Propagation-Delay Test Setup, Enable to Analog Out

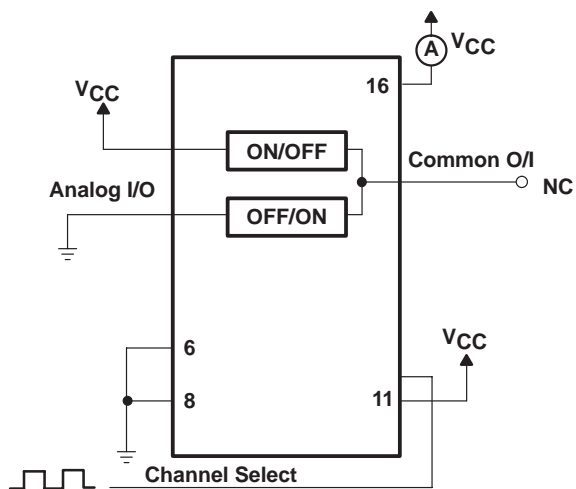


Figure 15. Power-Dissipation Capacitance Test Setup

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74HC4851D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851DGV	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC4851NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC4851PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4851PWVG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74HC4851 :

- Automotive: [SN74HC4851-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4851DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74HC4851DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4851PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

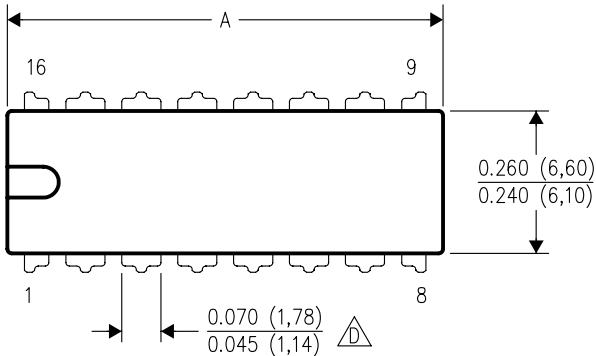

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4851DGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
SN74HC4851DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC4851PWR	TSSOP	PW	16	2000	346.0	346.0	29.0

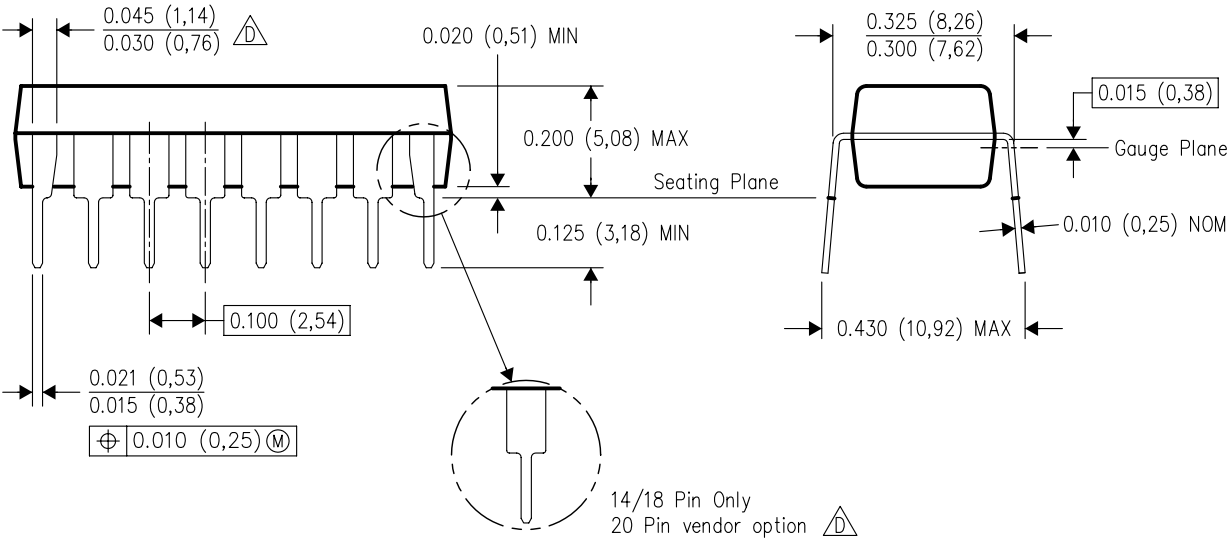
N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM	PINS **			
	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

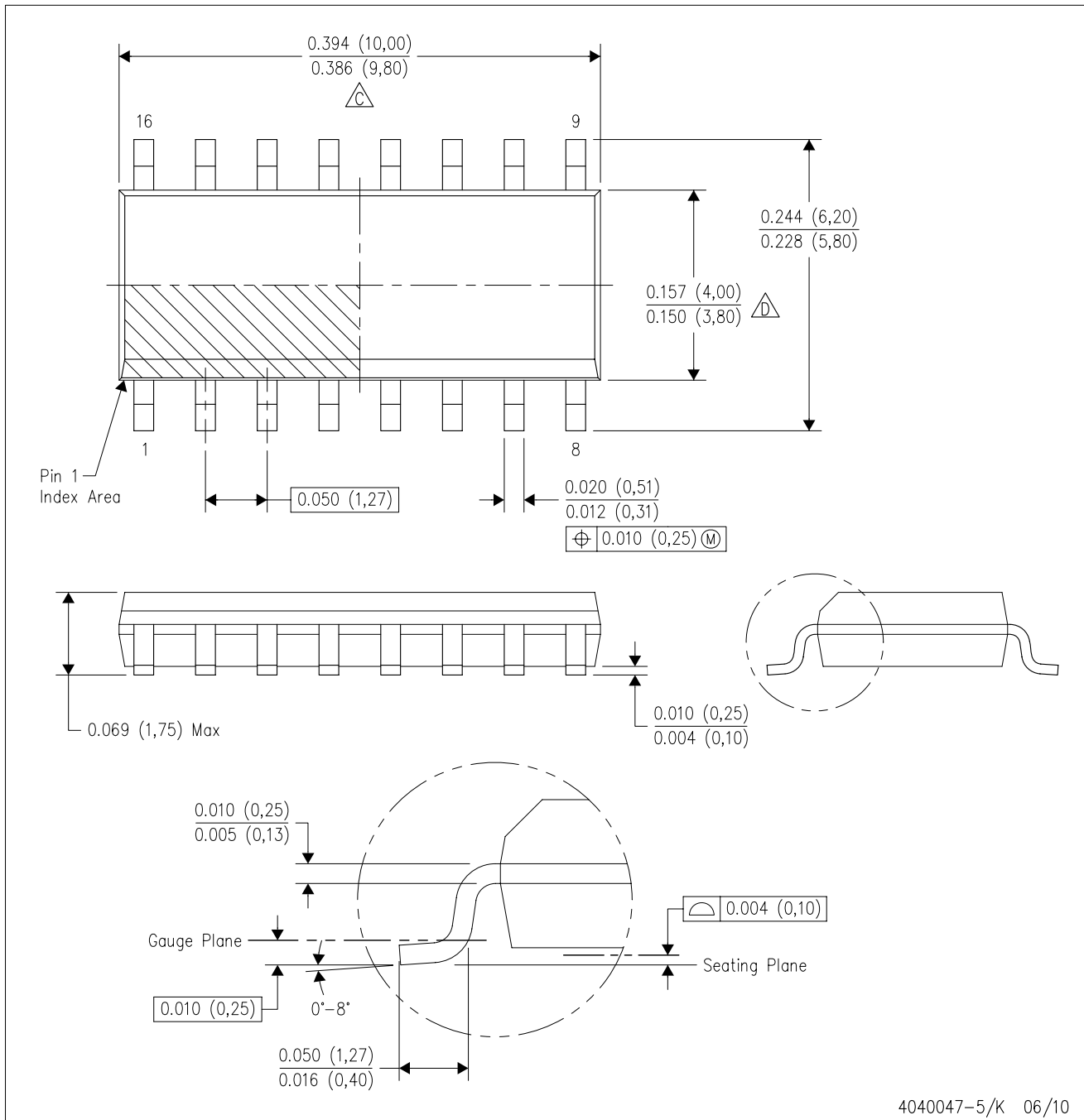
24 PINS SHOWN





- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

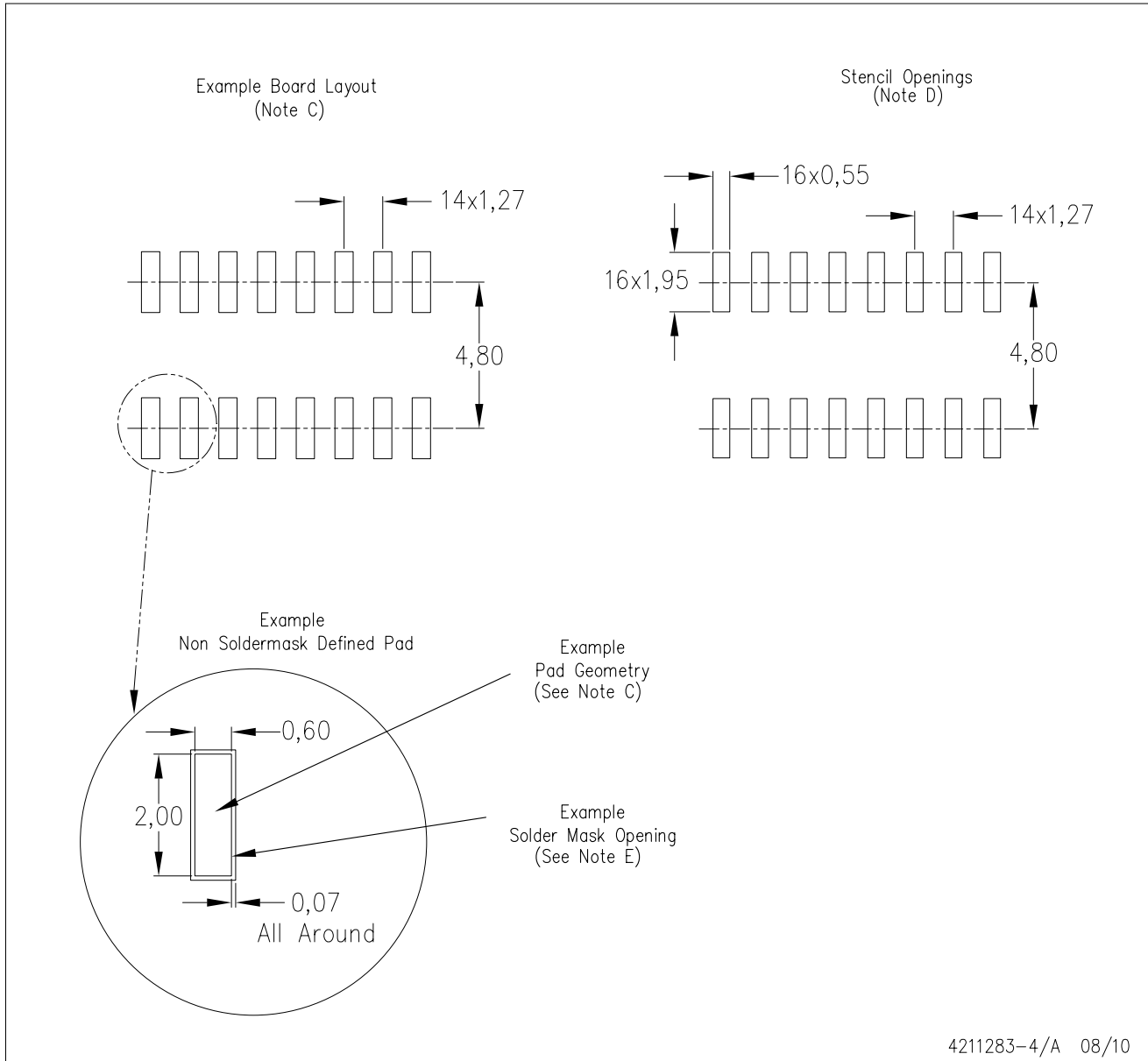


4040047-5/K 06/10

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

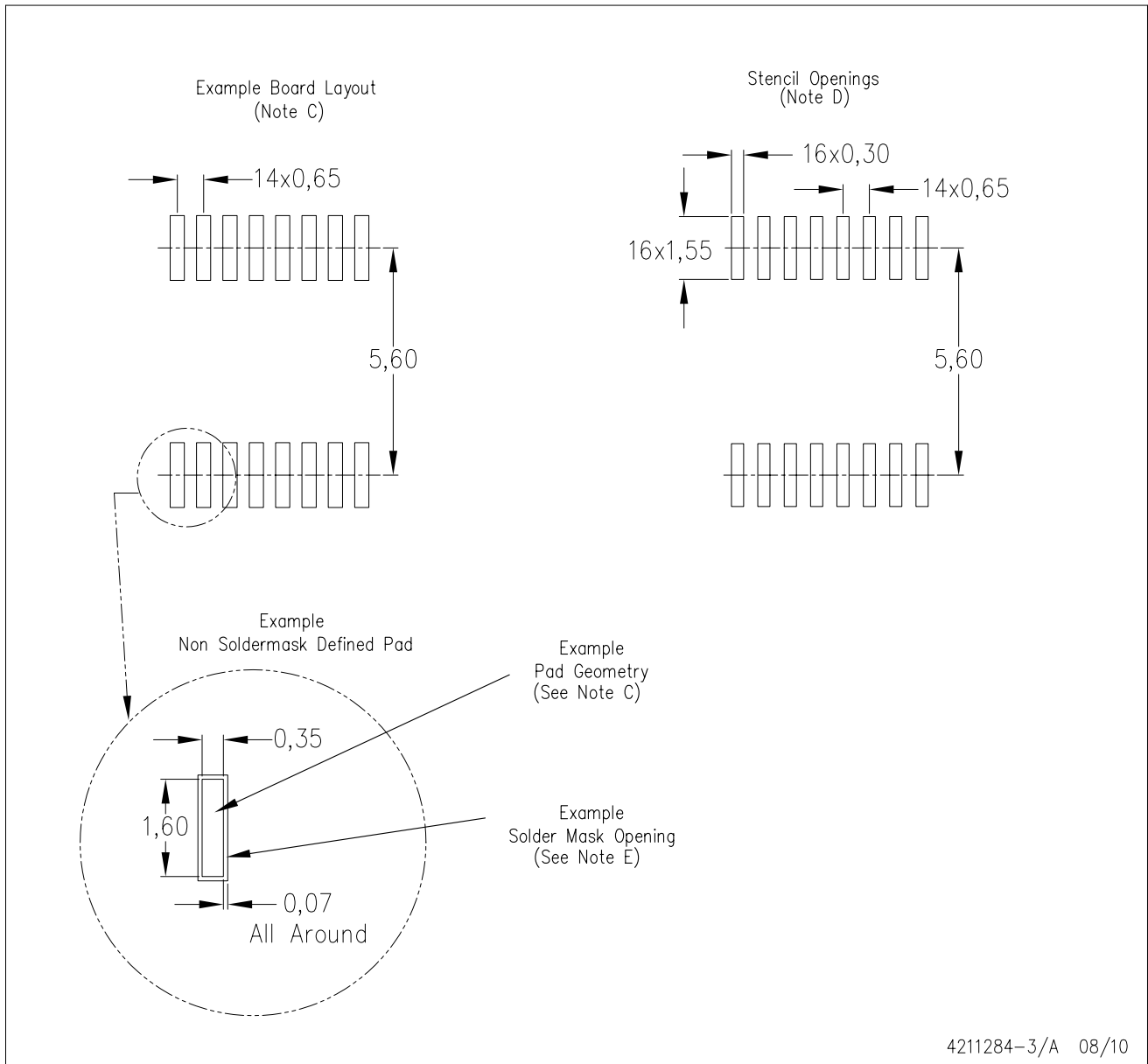


4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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