SN74AXCH4T245 Four-bit bus transceiver with configurable voltage translation, tri-state outputs, and bus-hold inputs

1 Features

- Fully configurable dual-rail design allows each port to operate with a power supply range from 0.65 V to 3.6 V
- Bus-hold on data inputs eliminates the need for external pullup or pulldown resistors
- Operating temperature from –40°C to +125°C
- Multiple direction control pins to allow simultaneous up and down translation
- Glitch-free power supply sequencing
- Up to 380 Mbps support when translating from 1.8 V to 3.3 V
- V_{CC} isolation feature
- I_{off} supports partial-power-down mode operation
- Compatible with AVC family level shifters
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 8000-V Human-body model
  - 1000-V Charged-device model

2 Applications

- Enterprise and communications
- Industrial
- Personal electronics
- Wireless infrastructure
- Building automation

3 Description

The SN74AXCH4T245 is a four-bit noninverting bus transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 0.65 V. The A port is designed to track V_{CCA}, which accepts any supply voltage from 0.65 V to 3.6 V. The B port is designed to track V_{CCB}, which accepts any supply voltage from 0.65 V to 3.6 V. The SN74AXCH4T245 device is compatible with a single-supply system.

The SN74AXCH4T245 device is designed for asynchronous communication between data buses and transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control inputs (1DIR and 2DIR). The output-enable inputs (1$\overline{OE}$ and 2$\overline{OE}$) are used to disable the outputs so the buses are effectively isolated. All control pins (xDIR and x$\overline{OE}$) are referenced to V_{CCA}.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. If a supply is present for V_{CCA} or V_{CCB}, the bus-hold circuitry always remains active on the A or B inputs respectively, independent of the state of the direction control or output enable pins.

To ensure the high-impedance state of the level shifter I/Os during power up or power down, the x$\overline{OE}$ pins should be tied to V_{CCA} through a pullup resistor.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or sourced into an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} is less than 100 mV, all I/O ports enter a high-impedance state by disabling the outputs.

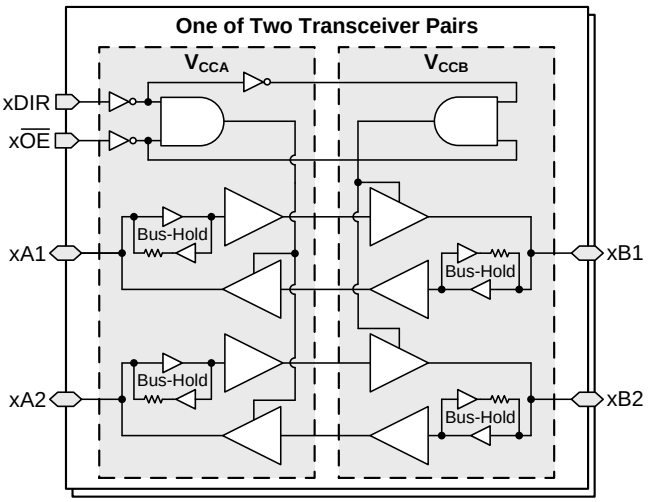
Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AXCH4T245PW	TSSOP (16)	5.00 mm x 4.40 mm
SN74AXCH4T245RSV	UQFN (16)	2.60 mm x 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



Note: Bus-hold circuits are only present for data inputs, not control inputs

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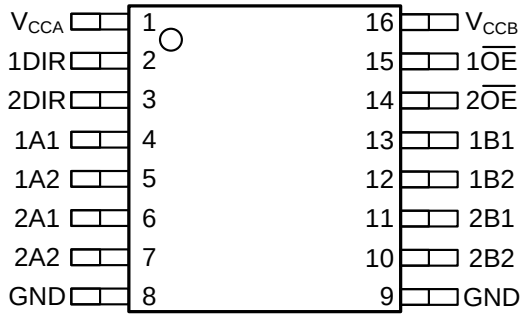
4 Revision History

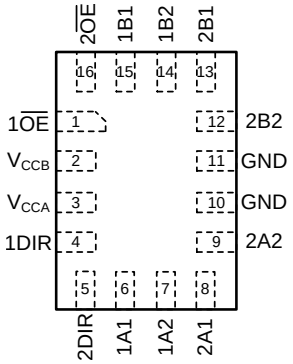
DATE	REVISION	NOTES
March 2019	*	Initial release.

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



RSV Package
16-Pin UQFN
Transparent Top View



Pin Functions

PIN	NO.		TYPE	DESCRIPTION
NAME	PW	RSV		
1A1	4	6	I/O	Input/output 1A1. Referenced to V_{CCA}.
1A2	5	7	I/O	Input/output 1A2. Referenced to V_{CCA}.
1B1	13	15	I/O	Input/output 1B1. Referenced to V_{CCB}.
1B2	12	14	I/O	Input/output 1B2. Referenced to V_{CCB}.
1DIR	2	4	I	Direction-control input for ‘1’ ports
$1\overline{OE}$	15	1	I	Tri-state output-mode enable. Pull $\overline{OE}$ high to place ‘1’ outputs in tri-state mode. Referenced to V_{CCA}.
2A1	6	8	I/O	Input/output 2A1. Referenced to V_{CCA}.
2A2	7	9	I/O	Input/output 2A2. Referenced to V_{CCA}.
2B1	11	13	I/O	Input/output 2B1. Referenced to V_{CCB}.
2B2	10	12	I/O	Input/output 2B2. Referenced to V_{CCB}.
2DIR	3	5	I	Direction-control input for ‘2’ ports
$2\overline{OE}$	14	16	I	Tri-state output-mode enable. Pull $\overline{OE}$ high to place ‘2’ outputs in tri-state mode. Referenced to V_{CCA}.
GND	8, 9	10, 11	—	Ground
V_{CCA}	1	3	—	A-port power supply voltage. 0.65 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	16	2	—	B-port power supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNITS
V_{CCA}	Supply voltage A		–0.5	4.2	V
V_{CCB}	Supply voltage B		–0.5	4.2	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V_O	Voltage applied to any output in the high or low state(2)(3)	A Port	–0.5	V_{CCA} + 0.2	V
		B Port	–0.5	V_{CCB} + 0.2	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			0.65	3.6	V
V_{CCB}	Supply voltage B			0.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} x 0.70		
			V_{CCI} = 0.76 V - 1 V	V_{CCI} x 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} x 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	V_{CCI} x 0.65		
		Control Inputs(xDIR, x$\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} x 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} x 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} x 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	V_{CCA} x 0.65		
V_{IL}	Low-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} x 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} x 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} x 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control Inputs(xDIR, x$\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} x 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} x 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} x 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
$\Delta t/\Delta v$(2)	Input transition rise and fall time				10	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AXCH4T245		UNIT
		PW (TSSOP)	RSV (UQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.9	130.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.3	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.3	57.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.1	4.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.4	55.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						-40°C to 85°C			-40°C to 125°C			
						MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = -100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = -50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = -200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = -500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_{BHL}	Bus-hold low sustaining current (Port A or Port B) (4)	V_I = 0.20 V		0.65 V	0.65 V	4			4			µA
		V_I = 0.23 V		0.76 V	0.76 V	8			7			
		V_I = 0.26 V		0.85 V	0.85 V	10			10			
		V_I = 0.39 V		1.1 V	1.1 V	20			20			
		V_I = 0.49 V		1.4 V	1.4 V	40			30			
		V_I = 0.58 V		1.65 V	1.65 V	55			45			
		V_I = 0.7 V		2.3 V	2.3 V	90			80			
		V_I = 0.8 V		3 V	3 V	145			135			
I_{BHH}	Bus-hold high sustaining current (Port A or Port B) (5)	V_I = 0.20 V		0.65 V	0.65 V	–4			–4			µA
		V_I = 0.23 V		0.76 V	0.76 V	–8			–7			
		V_I = 0.26 V		0.85 V	0.85 V	–10			–10			
		V_I = 0.39 V		1.1 V	1.1 V	–20			–20			
		V_I = 0.49 V		1.4 V	1.4 V	–40			–30			
		V_I = 0.58 V		1.65 V	1.65 V	–55			–45			
		V_I = 0.7 V		2.3 V	2.3 V	–90			–80			
		V_I = 0.8 V		3 V	3 V	–145			–135			

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All typical data is taken at 25°C.
(4) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
(5) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to VCC and then lowering it to V_{IH} min.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						-40°C to 85°C			-40°C to 125°C			
						MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	
I_{BHLO}	Bus-hold low overdrive current (Port A or Port B) (6)	V_I = 0 to V_{CC}		0.75 V	0.75 V	40			40			µA
				0.84 V	0.84 V	50			50			
				0.95 V	0.95 V	65			65			
				1.3 V	1.3 V	105			105			
				1.6 V	1.6 V	150			150			
				1.95 V	1.95 V	205			205			
				2.7 V	2.7 V	335			335			
				3.6 V	3.6 V	480			480			
I_{BHHO}	Bus-hold high overdrive current (Port A or Port B) (7)	V_I = 0 to VCC		0.75 V	0.75 V	–40			–40			µA
				0.84 V	0.84 V	–50			–50			
				0.95 V	0.95 V	–65			–65			
				1.3 V	1.3 V	–105			–105			
				1.6 V	1.6 V	–150			–150			
				1.95 V	1.95 V	–205			–205			
				2.7 V	2.7 V	–335			–335			
				3.6 V	3.6 V	–480			–480			
I_I	Input leakage current	Control inputs (xDIR, $x\overline{OE}$): $V_I = V_{CCA}$ or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	–0.5		0.5	–1		1	µA
		Data Inputs (xAx, xBx) $V_I = V_{CCI}$ or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	–4		4	–8		8	µA
I_{off}	Partial power down current	A Port: V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	–8		8	–12		12	µA
		B Port: V_I or V_O = 0 V - 3.6 V		0 V - 3.6 V	0 V	–8		8	–12		12	
I_{OZ}	Tri-state output current (8)	A or B Port $V_I = V_{CCI}$ or GND, $V_O = V_{CCO}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	–4		4	–8		8	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			13			26	µA
				0 V	3.6 V	–2			–12			
				3.6 V	0 V			8			16	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			13			26	µA
				0 V	3.6 V			8			16	
				3.6 V	0 V	–2			–12			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			20			40	µA
C_i	Control Input Capacitance	V_I = 3.3 V or GND		3.3 V	3.3 V		4.5			4.5		pF
C_{io}	Data I/O Capacitance	$\overline{OE} = V_{CCA}$, V_O = 1.65V DC +1 MHz -16 dBm sine wave		3.3 V	3.3 V		7.4			7.4		pF

(6) An external driver must source at least I_{BHLO} to switch this node from low to high.
(7) An external driver must sink at least I_{BHHO} to switch this node from high to low.
(8) For I/O ports, the parameter I_{OZ} includes the input leakage current.

6.6 Switching Characteristics, V_{CCA} = 0.7 ± 0.05 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	161	0.5	109	0.5	78	0.5	41	0.5	38	0.5	41	0.5	68	0.5	181	ns
				-40°C to 125°C	0.5	161	0.5	109	0.5	78	0.5	41	0.5	38	0.5	41	0.5	68	0.5	181	
		B	A	-40°C to 85°C	0.5	161	0.5	134	0.5	112	0.5	59	0.5	22	0.5	15	0.5	11	0.5	10	
				-40°C to 125°C	0.5	161	0.5	134	0.5	112	0.5	59	0.5	22	0.5	16	0.5	11	0.5	10	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	159	0.5	159	0.5	159	0.5	159	0.5	159	0.5	159	0.5	159	0.5	159	ns
				-40°C to 125°C	0.5	159	0.5	159	0.5	159	0.5	159	0.5	159	0.5	159	0.5	159	0.5	159	
		$\overline{OE}$	B	-40°C to 85°C	0.5	158	0.5	122	0.5	102	0.5	55	0.5	54	0.5	56	0.5	65	0.5	125	
				-40°C to 125°C	0.5	158	0.5	122	0.5	102	0.5	55	0.5	54	0.5	56	0.5	65	0.5	125	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	243	0.5	243	0.5	243	0.5	243	0.5	243	0.5	243	0.5	243	0.5	243	ns
				-40°C to 125°C	0.5	243	0.5	243	0.5	243	0.5	243	0.5	243	0.5	243	0.5	243	0.5	243	
		$\overline{OE}$	B	-40°C to 85°C	0.5	292	0.5	192	0.5	134	0.5	87	0.5	73	0.5	69	0.5	70	0.5	148	
				-40°C to 125°C	0.5	292	0.5	192	0.5	134	0.5	88	0.5	74	0.5	69	0.5	70	0.5	148	

6.7 Switching Characteristics, V_{CCA} = 0.8 ± 0.04 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	134	0.5	90	0.5	64	0.5	30	0.5	24	0.5	23	0.5	25	0.5	34	ns
				-40°C to 125°C	0.5	134	0.5	90	0.5	64	0.5	30	0.5	24	0.5	23	0.5	25	0.5	34	
		B	A	-40°C to 85°C	0.5	109	0.5	90	0.5	72	0.5	39	0.5	22	0.5	15	0.5	11	0.5	10	
				-40°C to 125°C	0.5	109	0.5	90	0.5	72	0.5	39	0.5	22	0.5	15	0.5	11	0.5	10	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	110	0.5	110	0.5	110	0.5	110	0.5	110	0.5	110	0.5	110	0.5	110	ns
				-40°C to 125°C	0.5	110	0.5	110	0.5	110	0.5	110	0.5	110	0.5	110	0.5	110	0.5	110	
		$\overline{OE}$	B	-40°C to 85°C	0.5	147	0.5	111	0.5	91	0.5	42	0.5	36	0.5	35	0.5	37	0.5	47	
				-40°C to 125°C	0.5	147	0.5	111	0.5	91	0.5	42	0.5	36	0.5	35	0.5	37	0.5	47	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	ns
				-40°C to 125°C	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	
		$\overline{OE}$	B	-40°C to 85°C	0.5	253	0.5	164	0.5	117	0.5	71	0.5	57	0.5	52	0.5	47	0.5	53	
				-40°C to 125°C	0.5	253	0.5	164	0.5	117	0.5	73	0.5	58	0.5	53	0.5	48	0.5	53	

6.8 Switching Characteristics, V_{CCA} = 0.9 ± 0.045 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	112	0.5	72	0.5	54	0.5	24	0.5	19	0.5	17	0.5	16	0.5	19	ns
				-40°C to 125°C	0.5	112	0.5	72	0.5	54	0.5	24	0.5	19	0.5	17	0.5	16	0.5	19	
		B	A	-40°C to 85°C	0.5	78	0.5	64	0.5	54	0.5	27	0.5	19	0.5	14	0.5	10	0.5	10	
				-40°C to 125°C	0.5	78	0.5	64	0.5	54	0.5	27	0.5	19	0.5	14	0.5	10	0.5	10	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	ns
				-40°C to 125°C	0.5	82	0.5	82	0.5	82	0.5	82	0.5	82	0.5	82	0.5	82	0.5	82	
		$\overline{OE}$	B	-40°C to 85°C	0.5	141	0.5	106	0.5	85	0.5	36	0.5	29	0.5	27	0.5	26	0.5	30	
				-40°C to 125°C	0.5	141	0.5	106	0.5	85	0.5	37	0.5	30	0.5	28	0.5	26	0.5	30	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	84	0.5	84	0.5	84	0.5	84	0.5	84	0.5	84	0.5	84	0.5	84	ns
				-40°C to 125°C	0.5	84	0.5	84	0.5	84	0.5	84	0.5	84	0.5	84	0.5	84	0.5	84	
		$\overline{OE}$	B	-40°C to 85°C	0.5	229	0.5	149	0.5	107	0.5	63	0.5	48	0.5	43	0.5	37	0.5	38	
				-40°C to 125°C	0.5	229	0.5	149	0.5	107	0.5	65	0.5	50	0.5	45	0.5	39	0.5	39	

6.9 Switching Characteristics, V_{CCA} = 1.2 ± 0.1 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	60	0.5	39	0.5	27	0.5	15	0.5	11	0.5	10	0.5	8	0.5	9	ns
				-40°C to 125°C	0.5	60	0.5	39	0.5	27	0.5	15	0.5	12	0.5	10	0.5	9	0.5	9	
		B	A	-40°C to 85°C	0.5	41	0.5	30	0.5	24	0.5	15	0.5	11	0.5	9	0.5	7	0.5	7	
				-40°C to 125°C	0.5	41	0.5	30	0.5	24	0.5	15	0.5	11	0.5	9	0.5	7	0.5	7	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	ns
				-40°C to 125°C	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	
		$\overline{OE}$	B	-40°C to 85°C	0.5	133	0.5	100	0.5	79	0.5	29	0.5	22	0.5	20	0.5	17	0.5	17	
				-40°C to 125°C	0.5	134	0.5	100	0.5	80	0.5	31	0.5	23	0.5	21	0.5	18	0.5	18	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	0.5	37	0.5	37	0.5	37	0.5	37	ns
				-40°C to 125°C	0.5	39	0.5	39	0.5	39	0.5	39	0.5	39	0.5	39	0.5	39	0.5	39	
		$\overline{OE}$	B	-40°C to 85°C	0.5	168	0.5	109	0.5	77	0.5	51	0.5	37	0.5	31	0.5	25	0.5	23	
				-40°C to 125°C	0.5	168	0.5	109	0.5	78	0.5	53	0.5	39	0.5	34	0.5	27	0.5	24	

6.10 Switching Characteristics, V_{CCA} = 1.5 ± 0.1 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	22	0.5	22	0.5	19	0.5	11	0.5	9	0.5	8	0.5	7	0.5	6	ns
				-40°C to 125°C	0.5	22	0.5	22	0.5	19	0.5	11	0.5	9	0.5	8	0.5	7	0.5	6	
		B	A	-40°C to 85°C	0.5	38	0.5	24	0.5	19	0.5	11	0.5	9	0.5	8	0.5	5	0.5	5	
				-40°C to 125°C	0.5	38	0.5	24	0.5	19	0.5	11	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	ns
				-40°C to 125°C	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	
		$\overline{OE}$	B	-40°C to 85°C	0.5	131	0.5	98	0.5	78	0.5	27	0.5	20	0.5	18	0.5	14	0.5	14	
				-40°C to 125°C	0.5	132	0.5	98	0.5	78	0.5	29	0.5	21	0.5	19	0.5	15	0.5	15	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	23	0.5	23	0.5	23	0.5	23	0.5	23	0.5	23	0.5	23	0.5	23	ns
				-40°C to 125°C	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	
		$\overline{OE}$	B	-40°C to 85°C	0.5	109	0.5	84	0.5	67	0.5	43	0.5	31	0.5	26	0.5	20	0.5	18	
				-40°C to 125°C	0.5	109	0.5	84	0.5	68	0.5	45	0.5	34	0.5	29	0.5	22	0.5	19	

6.11 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	15	0.5	15	0.5	14	0.5	9	0.5	8	0.5	7	0.5	6	0.5	6	ns
				-40°C to 125°C	0.5	16	0.5	15	0.5	14	0.5	9	0.5	8	0.5	7	0.5	6	0.5	6	
		B	A	-40°C to 85°C	0.5	41	0.5	23	0.5	17	0.5	10	0.5	8	0.5	7	0.5	5	0.5	4	
				-40°C to 125°C	0.5	41	0.5	23	0.5	17	0.5	10	0.5	8	0.5	7	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	ns
				-40°C to 125°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	
		$\overline{OE}$	B	-40°C to 85°C	0.5	129	0.5	98	0.5	77	0.5	27	0.5	19	0.5	17	0.5	13	0.5	13	
				-40°C to 125°C	0.5	131	0.5	98	0.5	77	0.5	28	0.5	21	0.5	18	0.5	14	0.5	14	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	ns
				-40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	
		$\overline{OE}$	B	-40°C to 85°C	0.5	102	0.5	73	0.5	60	0.5	38	0.5	28	0.5	24	0.5	19	0.5	16	
				-40°C to 125°C	0.5	102	0.5	75	0.5	62	0.5	41	0.5	31	0.5	26	0.5	20	0.5	18	

6.12 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	11	0.5	11	0.5	10	0.5	7	0.5	6	0.5	5	0.5	5	0.5	5	ns
				-40°C to 125°C	0.5	11	0.5	11	0.5	10	0.5	7	0.5	6	0.5	5	0.5	5	0.5	5	
		B	A	-40°C to 85°C	0.5	68	0.5	25	0.5	17	0.5	8	0.5	7	0.5	6	0.5	5	0.5	4	
				-40°C to 125°C	0.5	68	0.5	25	0.5	17	0.5	9	0.5	7	0.5	6	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	ns
				-40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$	B	-40°C to 85°C	0.5	128	0.5	96	0.5	76	0.5	26	0.5	18	0.5	16	0.5	12	0.5	12	
				-40°C to 125°C	0.5	129	0.5	96	0.5	77	0.5	27	0.5	20	0.5	17	0.5	13	0.5	13	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	ns
				-40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$	B	-40°C to 85°C	0.5	120	0.5	69	0.5	54	0.5	33	0.5	24	0.5	20	0.5	16	0.5	14	
				-40°C to 125°C	0.5	120	0.5	70	0.5	56	0.5	36	0.5	26	0.5	22	0.5	18	0.5	15	

6.13 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Condtions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	10	0.5	10	0.5	10	0.5	7	0.5	5	0.5	5	0.5	5	0.5	4	ns
				-40°C to 125°C	0.5	10	0.5	10	0.5	10	0.5	7	0.5	5	0.5	5	0.5	5	0.5	4	
		B	A	-40°C to 85°C	0.5	182	0.5	34	0.5	19	0.5	9	0.5	6	0.5	5	0.5	5	0.5	4	
				-40°C to 125°C	0.5	182	0.5	34	0.5	19	0.5	9	0.5	6	0.5	6	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	ns
				-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	
		$\overline{OE}$	B	-40°C to 85°C	0.5	142	0.5	96	0.5	76	0.5	26	0.5	18	0.5	16	0.5	12	0.5	11	
				-40°C to 125°C	0.5	142	0.5	97	0.5	77	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	ns
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	
		$\overline{OE}$	B	-40°C to 85°C	0.5	194	0.5	82	0.5	57	0.5	33	0.5	22	0.5	18	0.5	14	0.5	13	
				-40°C to 125°C	0.5	194	0.5	82	0.5	58	0.5	35	0.5	24	0.5	20	0.5	16	0.5	14	

6.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.2		pF
			0.8 V	0.8 V		2.3		
			0.9 V	0.9 V		2.3		
			1.2 V	1.2 V		2.3		
			1.5 V	1.5 V		2.2		
			1.8 V	1.8 V		2.2		
			2.5 V	2.5 V		2.5		
			3.3 V	3.3 V		2.6		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.5		pF
			0.8 V	0.8 V		1.7		
			0.9 V	0.9 V		1.7		
			1.2 V	1.2 V		1.7		
			1.5 V	1.5 V		1.5		
			1.8 V	1.8 V		1.5		
			2.5 V	2.5 V		1.8		
			3.3 V	3.3 V		2.1		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		12.6		pF
			0.8 V	0.8 V		12.4		
			0.9 V	0.9 V		12.4		
			1.2 V	1.2 V		12.8		
			1.5 V	1.5 V		13.3		
			1.8 V	1.8 V		14.6		
			2.5 V	2.5 V		18.0		
			3.3 V	3.3 V		21.1		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.1		pF
			0.8 V	0.8 V		1.1		
			0.9 V	0.9 V		1.0		
			1.2 V	1.2 V		1.0		
			1.5 V	1.5 V		1.0		
			1.8 V	1.8 V		0.9		
			2.5 V	2.5 V		0.9		
			3.3 V	3.3 V		0.9		

Operating Characteristics: T_A = 25°C (continued)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		12.6		pF
			0.8 V	0.8 V		12.4		
			0.9 V	0.9 V		12.4		
			1.2 V	1.2 V		12.8		
			1.5 V	1.5 V		13.3		
			1.8 V	1.8 V		14.6		
			2.5 V	2.5 V		17.8		
			3.3 V	3.3 V		21.0		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.1		pF
			0.8 V	0.8 V		1.1		
			0.9 V	0.9 V		1.0		
			1.2 V	1.2 V		1.0		
			1.5 V	1.5 V		1.0		
			1.8 V	1.8 V		0.9		
			2.5 V	2.5 V		0.9		
			3.3 V	3.3 V		0.9		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.2		pF
			0.8 V	0.8 V		2.2		
			0.9 V	0.9 V		2.2		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		2.0		
			1.8 V	1.8 V		1.9		
			2.5 V	2.5 V		2.0		
			3.3 V	3.3 V		2.6		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.6		pF
			0.8 V	0.8 V		1.5		
			0.9 V	0.9 V		1.6		
			1.2 V	1.2 V		1.4		
			1.5 V	1.5 V		1.3		
			1.8 V	1.8 V		1.2		
			2.5 V	2.5 V		1.4		
			3.3 V	3.3 V		1.9		

6.15 Typical Characteristics

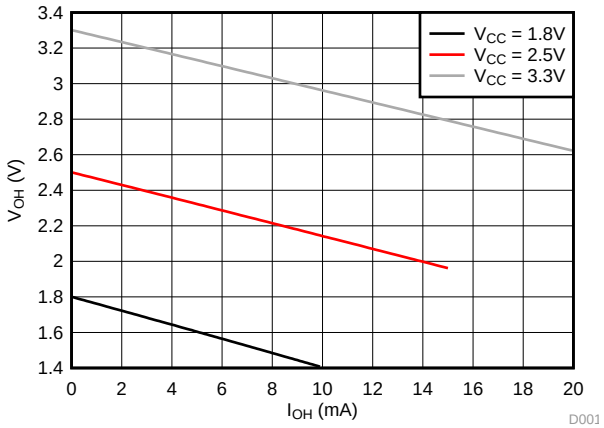


Figure 1. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

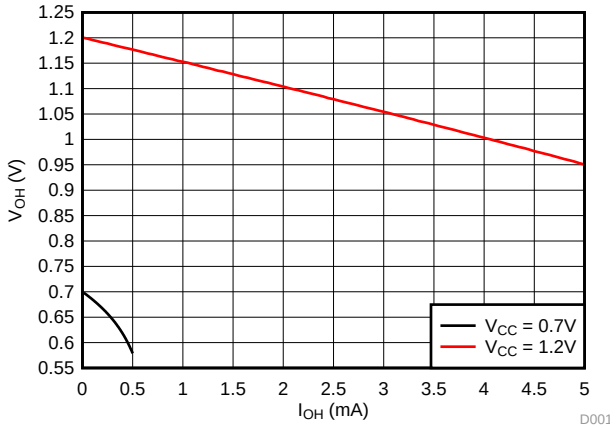


Figure 2. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

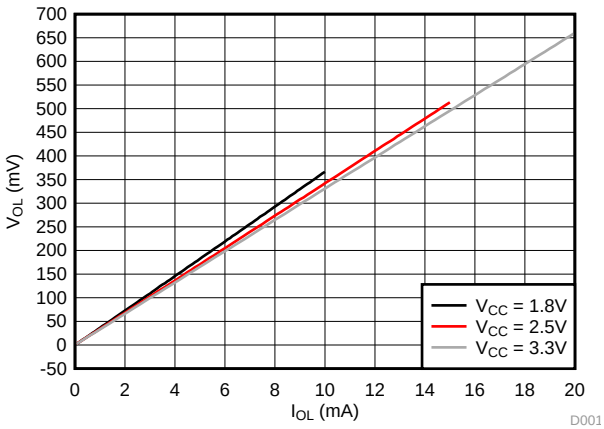


Figure 3. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

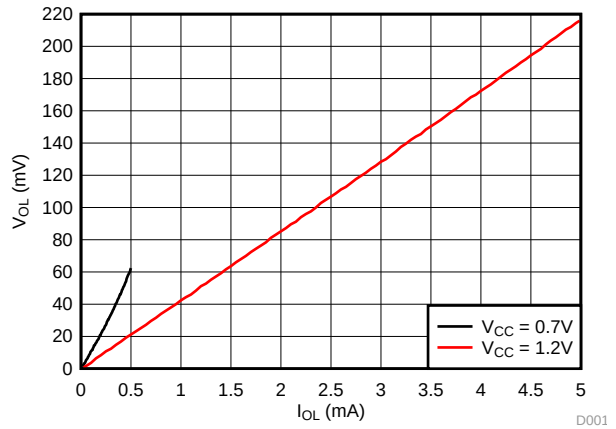


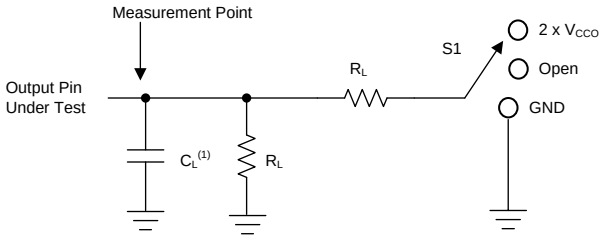
Figure 4. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

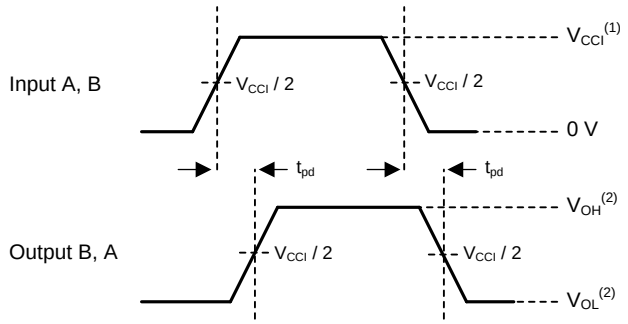


(1) C_L includes probe and jig capacitance.

Figure 5. Load Circuit

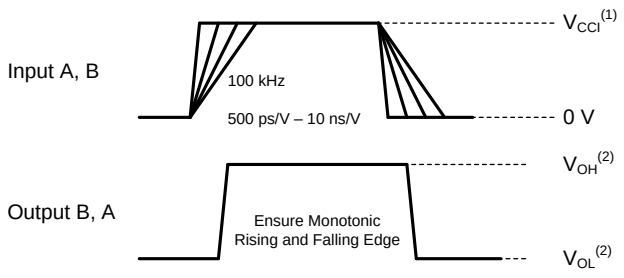
Table 1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
Δt/Δv	Input transition rise or fall rate	0.65 V – 3.6 V	1 MΩ	15 pF	Open	N/A
t_{pd}	Propagation (delay) time	1.1 V – 3.6 V	2 kΩ	15 pF	Open	N/A
		0.65 V – 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	2 × V_{CCO}	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	2 × V_{CCO}	0.1 V
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	GND	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	GND	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	GND	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	GND	0.1 V



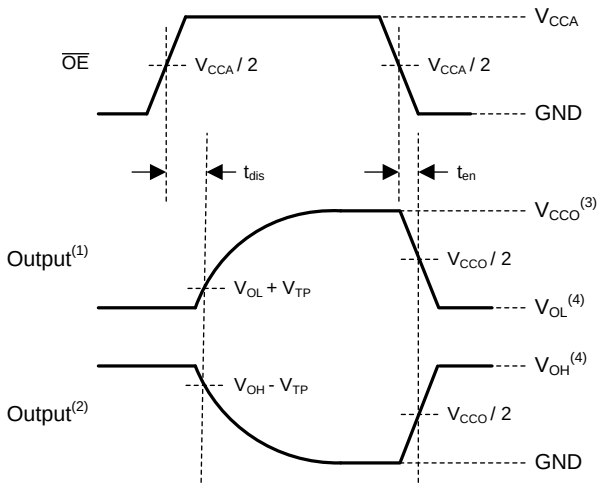
1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 7. Input Transition Rise or Fall Rate



(1) Output waveform on the condition that input is driven to a valid Logic Low.

(2) Output waveform on the condition that input is driven to a valid Logic High.

(3) V_{CCO} is the supply pin associated with the output port.

(4) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

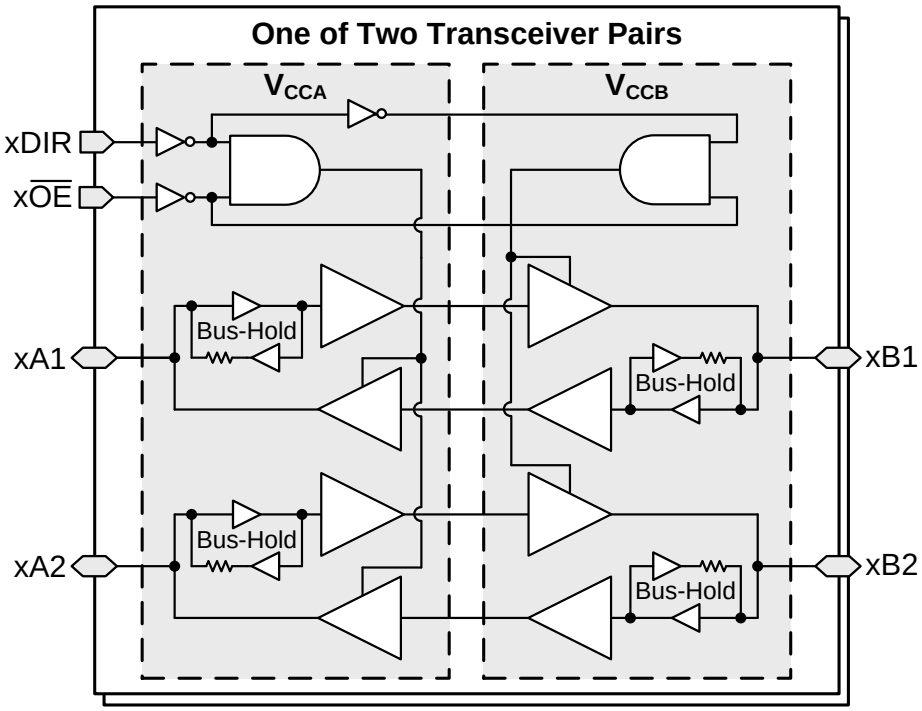
Figure 8. Enable Time and Disable Time

8 Detailed Description

8.1 Overview

The SN74AXCH4T245 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device with bus-hold inputs. xAx pins and control pins (1DIR, 2DIR, 1$\overline{OE}$, and 2$\overline{OE}$) are reference to V_{CCA} logic levels, and xBx pins are referenced to V_{CCB} logic levels. The A port is able to accept I/O voltages ranging from 0.65 V to 3.6 V, while the B port can accept I/O voltages from 0.65 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both xAx and xBx pins are in the high-impedance state. See *Device Functional Modes* for a summary of the operation of the control logic.

8.2 Functional Block Diagram



Note: Bus-hold circuits are only present for data inputs, not control inputs

8.3 Feature Description

8.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Feature Description (continued)

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.4 V_{CC} Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100mV.

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.3.6 Glitch-free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

8.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 9.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

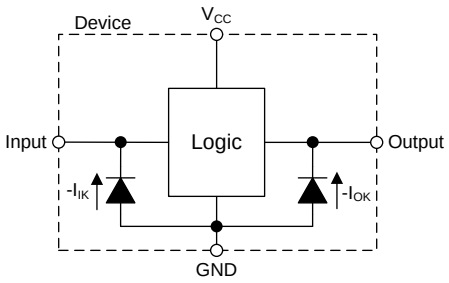


Figure 9. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.8 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V and 3.3 V).

8.3.9 Supports High-Speed Translation

The SN74AXCH4T245 device can support high data-rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

Feature Description (continued)

8.3.10 Bus-Hold Data Inputs

Each data input on this device includes a weak latch that maintains a valid logic level on the input. The state of these latches is unknown at startup and remains unknown until the input has been forced to a valid high or low state. After data has been sent through a channel, the latch then maintains the previous state on the input if the line is left floating. It is not recommended to use pull-up or pull-down resistors together with a bus-hold input, as it may cause undefined inputs to occur which leads to excessive current consumption.

Bus-hold data inputs prevent floating inputs on this device. The *Implications of Slow or Floating CMOS Inputs* application report explains the problems associated with leaving CMOS inputs floating.

These latches remain active at all times, independent of all control signals such as direction control or output enable.

The *Bus-Hold Circuit* application report has additional details regarding bus-hold inputs.

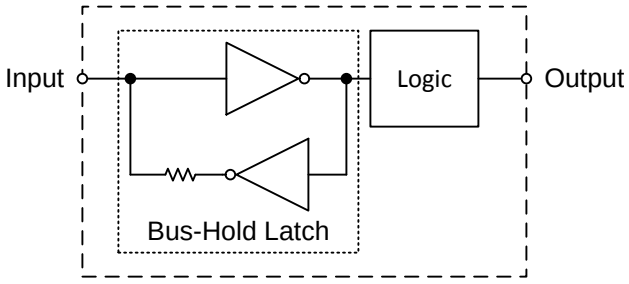


Figure 10. Simplified Schematic For Device With Bus-Hold Data Inputs

8.4 Device Functional Modes

Table 2. Function Table (Each 2-Bit Section)(1)(2)

CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Bus-hold circuits of the data I/Os are always active, independent of the state of the control inputs.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AXCH4T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AXCH4T245 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

One example application is shown in Figure 11, where the SN74AXCH4T245 device is used to translate a low voltage UART signal from an SoC to a higher voltage signal which properly drive the inputs of the bluetooth module, and vice versa.

9.2 Typical Application

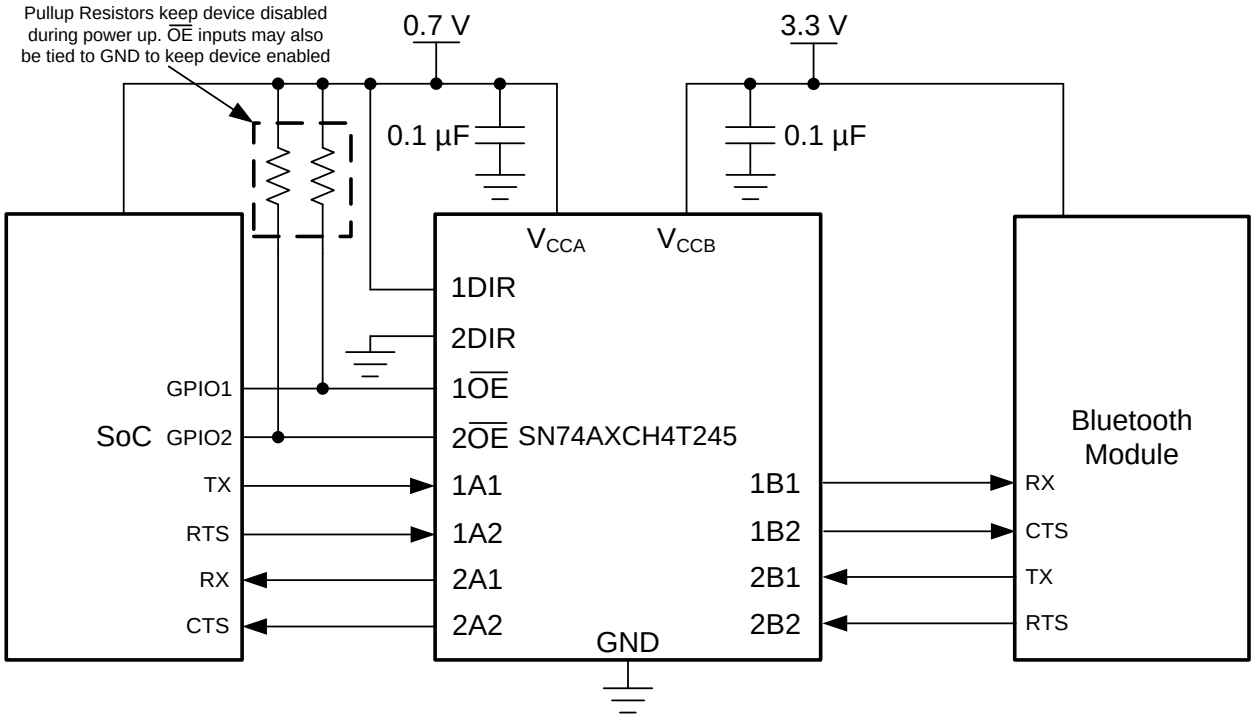


Figure 11. UART Interface Application

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 3.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXCH4T245 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXCH4T245 device is driving to determine the output voltage range.

9.2.3 Application Curve

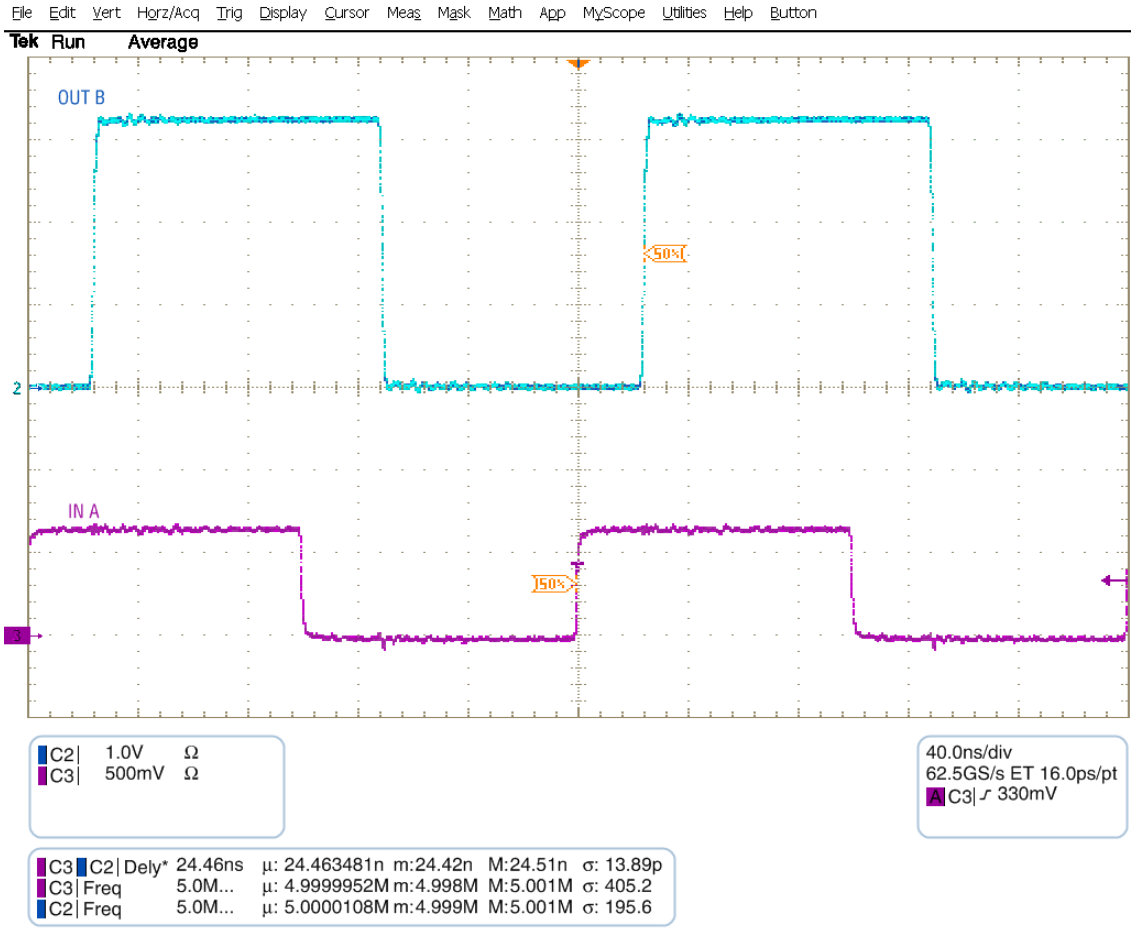


Figure 12. Up Translation at 2.5 MHz (0.7 V to 3.3 V)

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

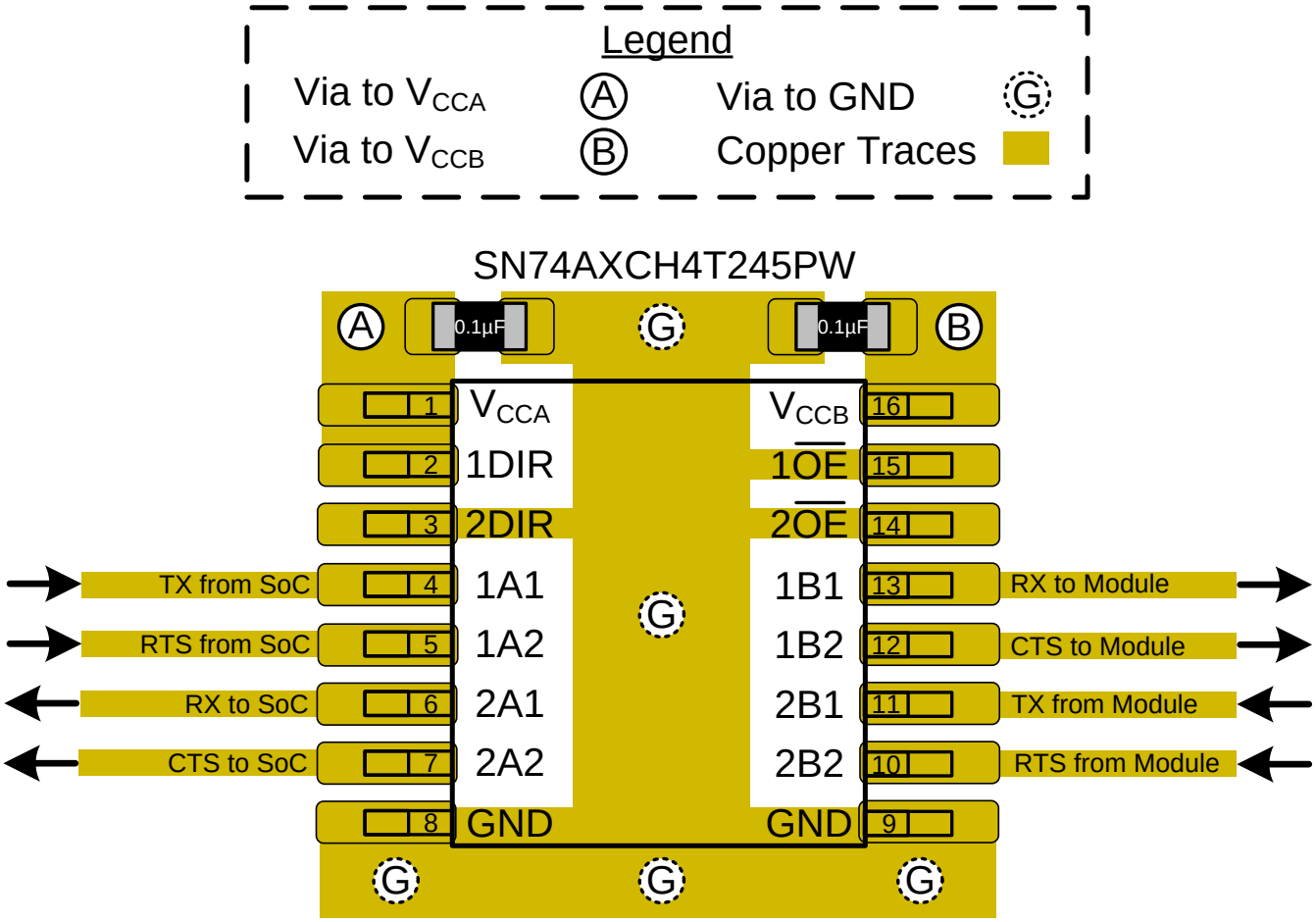
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- Use short trace lengths to avoid excessive loading.
- Do not use pullup or pulldown resistors on data inputs for devices with bus-hold circuits.

11.2 Layout Example



12 Device and Documentation Support

12.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

Texas Instruments, *Power Sequencing for AXC Family of Devices* application report

Texas Instruments, *System Considerations for Using Bus-hold Circuits to Avoid Floating Inputs* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXCH4T245PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	S4TH245	Samples
SN74AXCH4T245RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1U7R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

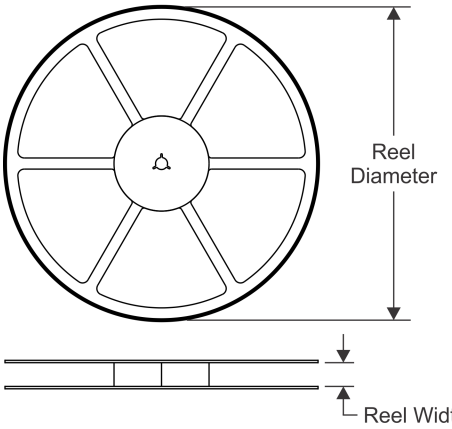
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

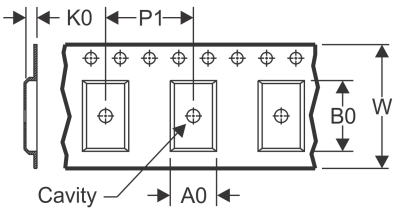
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

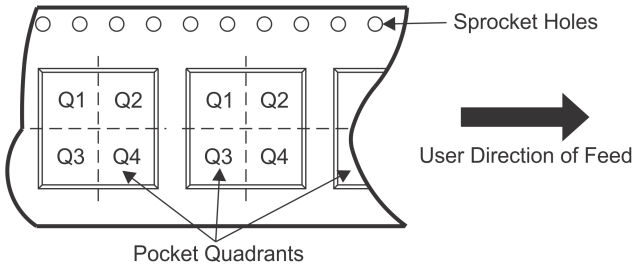


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

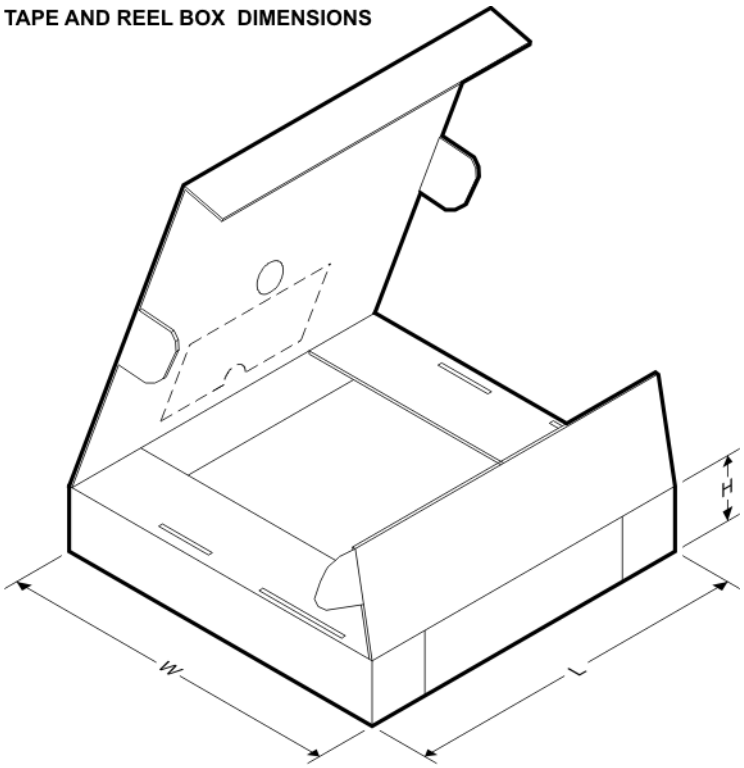
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXCH4T245PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AXCH4T245RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

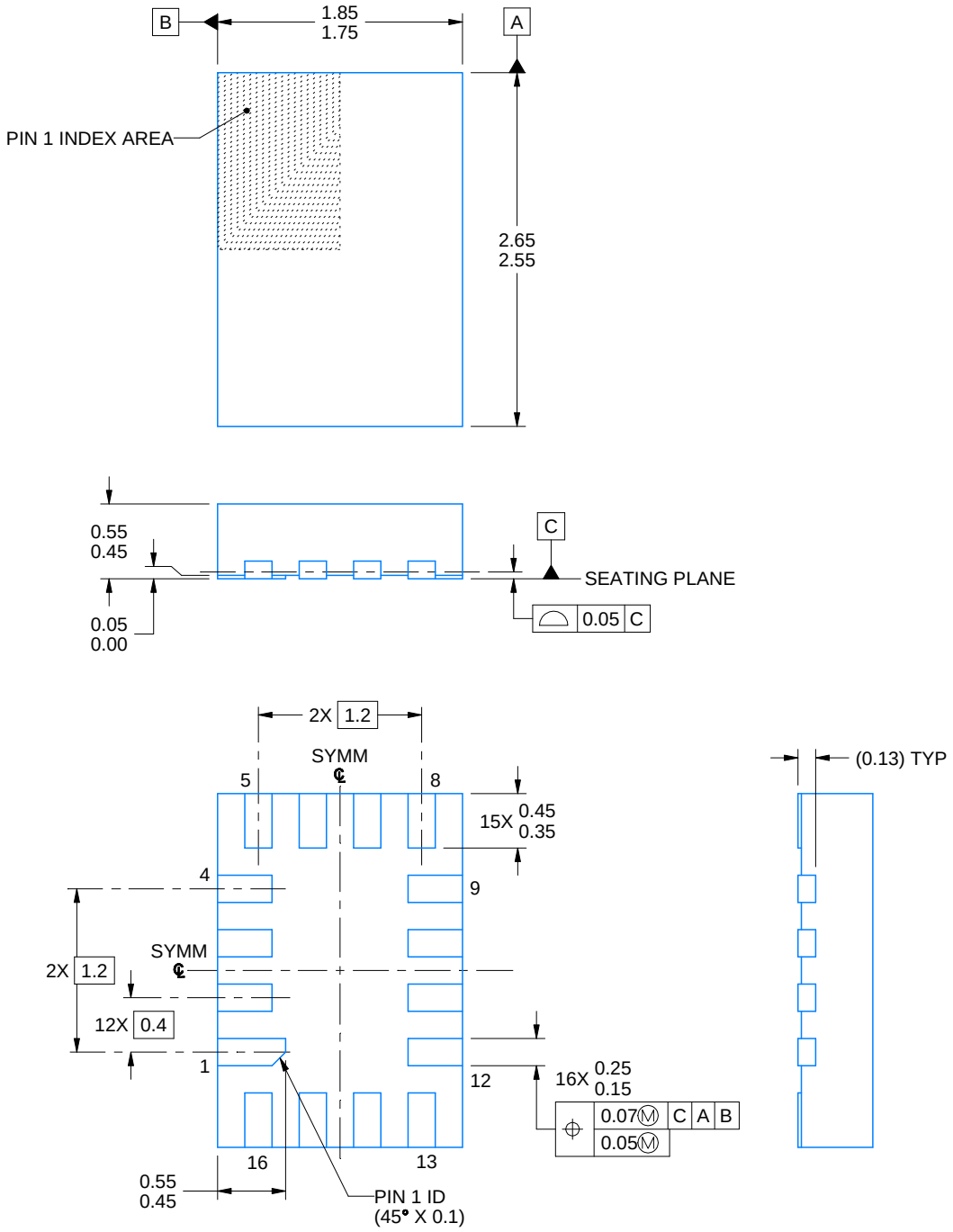
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXCH4T245PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74AXCH4T245RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

PACKAGE OUTLINE

RSV0016A

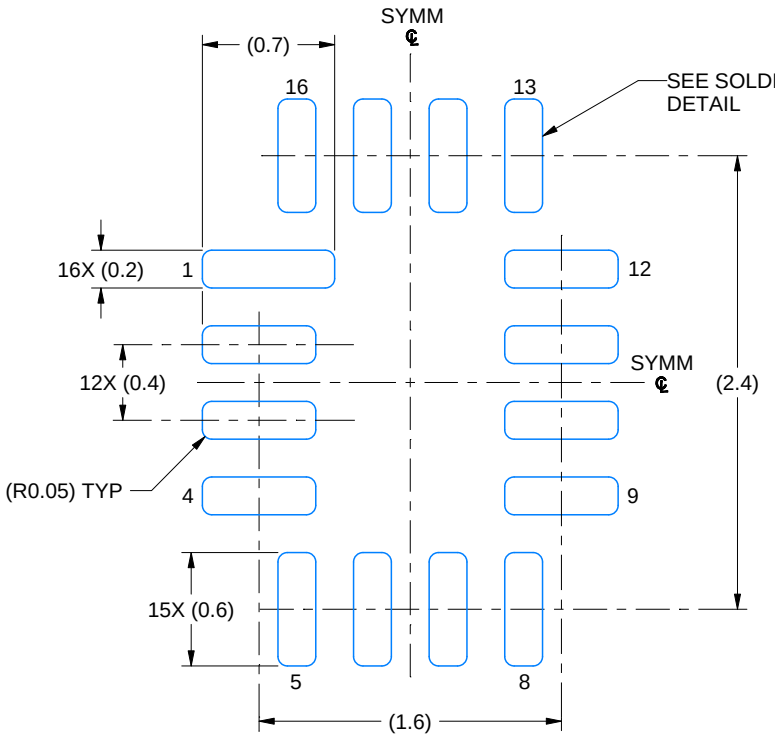
VQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

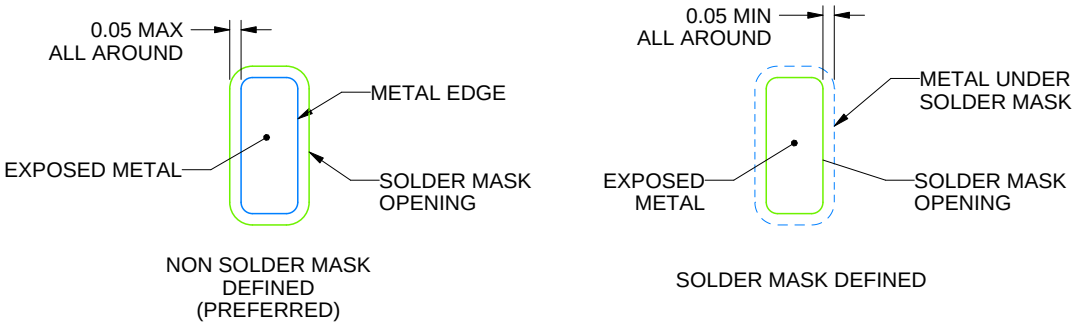


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

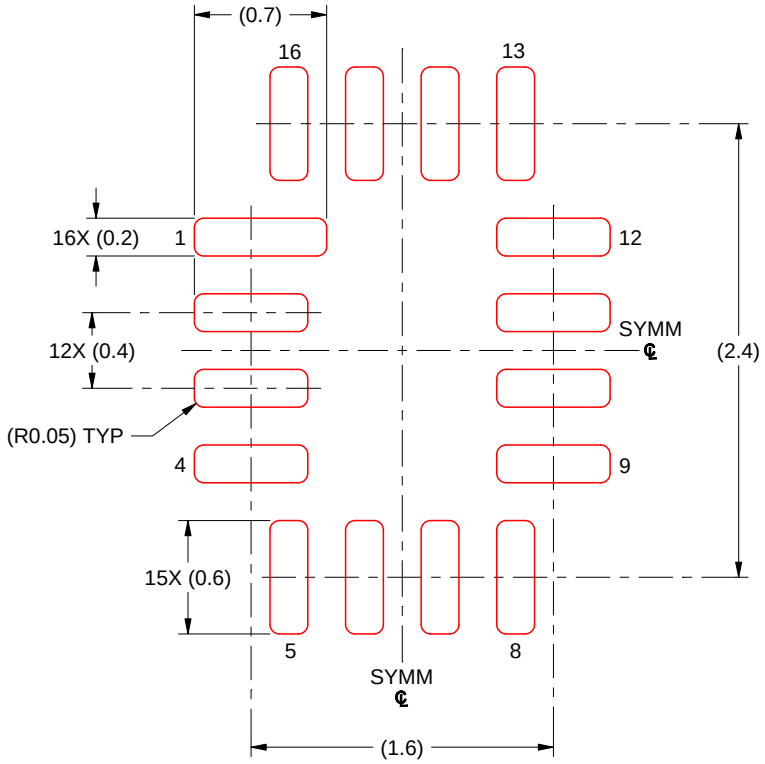


SOLDER MASK DETAILS

4220314/A 03/2019

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/A 03/2019

NOTES: (continued)

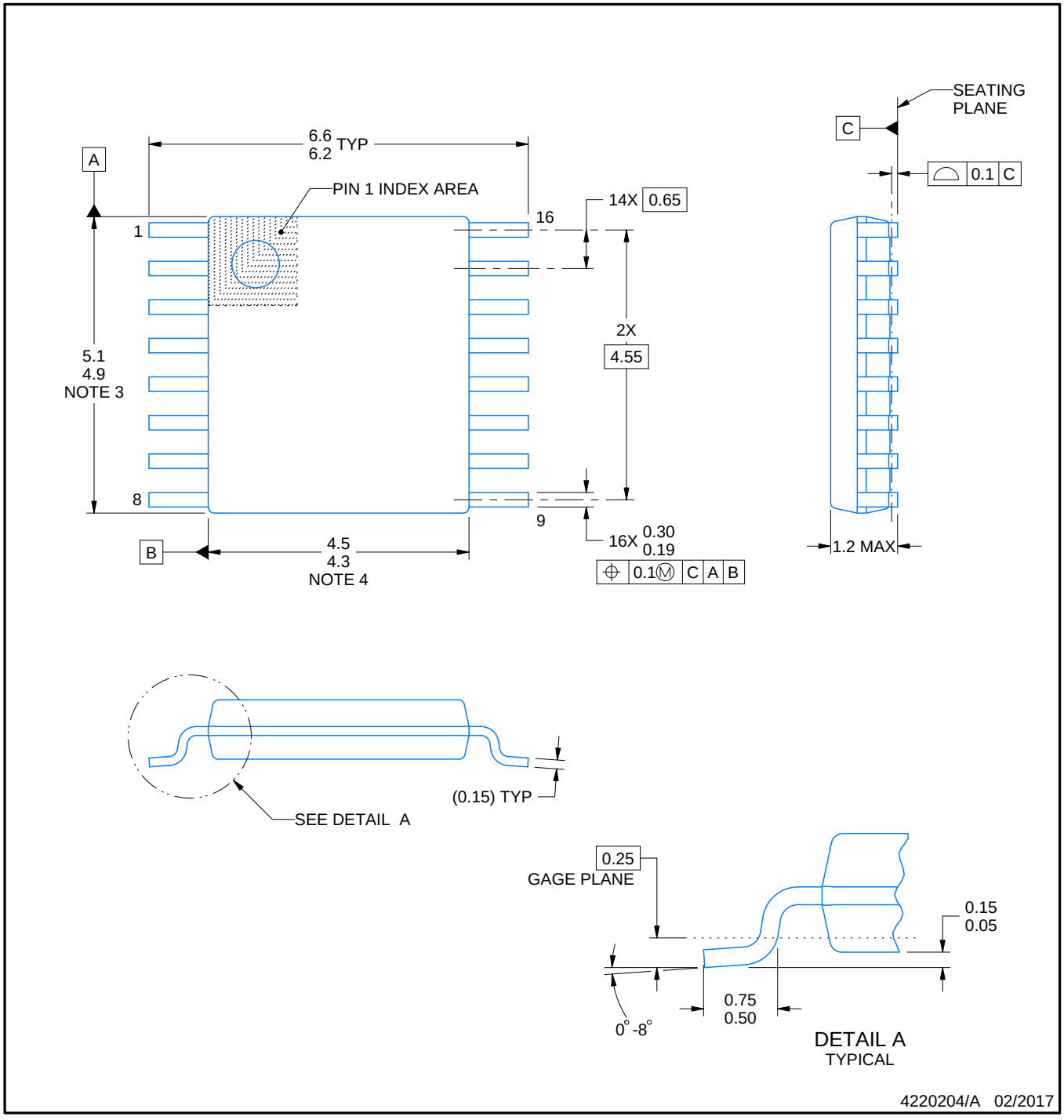
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

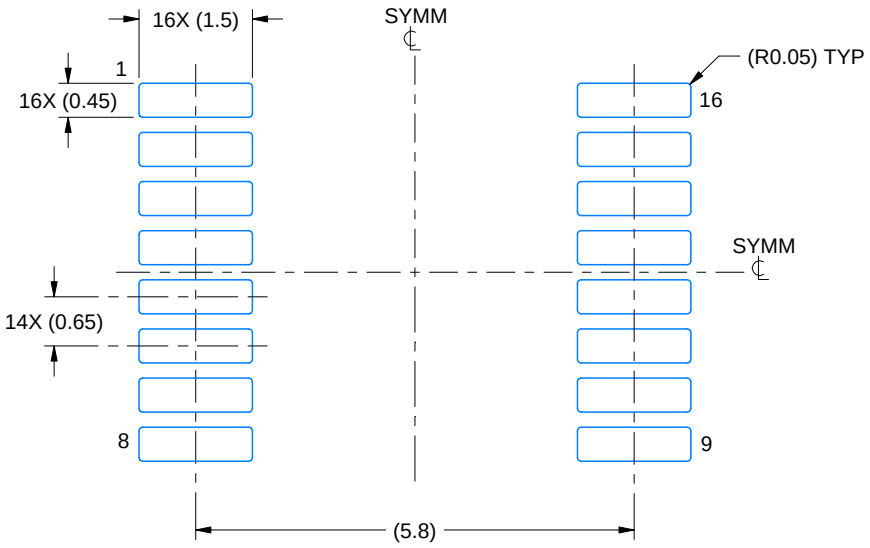
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

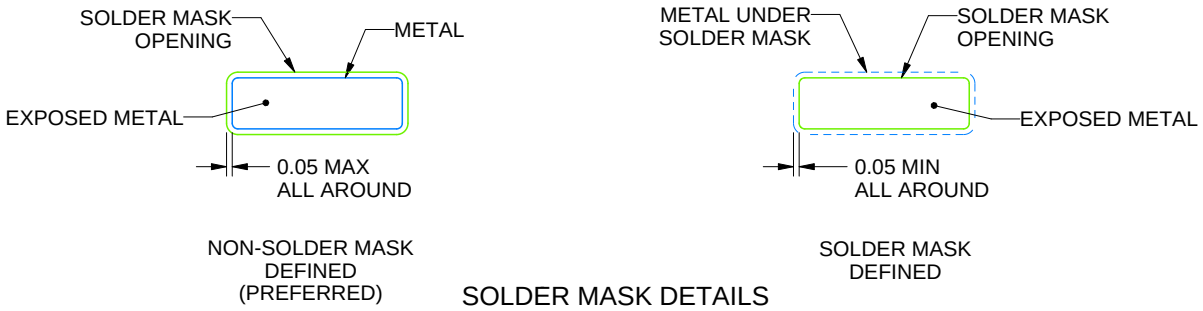


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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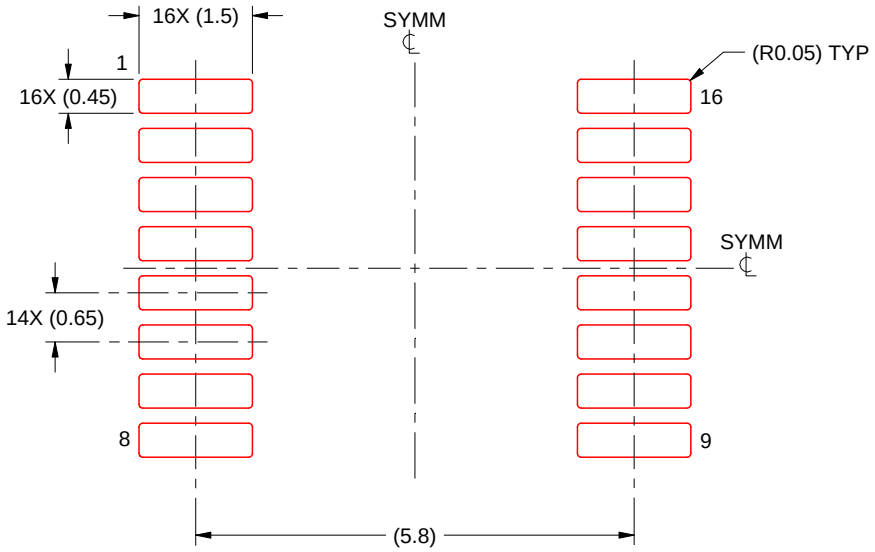
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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