SN74AXC8T245 8-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and Tri-State Outputs

1 Features

- Qualified Fully Configurable Dual-Rail Design Allows Each Port to Operate With a Power Supply Range From 0.65 V to 3.6 V
- Operating Temperature From –40°C to +125°C
- Multiple Direction Control Pins to Allow Simultaneous Up and Down Translation
- Up to 380 Mbps Support When Translating from 1.8 V to 3.3 V
- V_{CC} Isolation Feature to Effectively Isolate Both Buses in a Power-Down Scenario
- Partial Power-Down Mode to Limit Backflow Current in a Power-Down Scenario
- Compatible With SN74AVC8T245 and 74AVC8T245 Level Shifters
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model
  - 1000-V Charged-Device Model

2 Applications

- Enterprise and Communications
- Industrial
- Personal Electronics
- Wireless Infrastructure
- Building Automation
- Point of Sale

3 Description

The SN74AXC8T245 device is an 8-bit non-inverting bus transceiver that resolves voltage level mismatch between devices operating at the latest voltage nodes (0.7 V, 0.8 V, and 0.9 V) and devices operating at industry standard voltage nodes (1.8 V, 2.5 V, 3.3 V) and vice versa.

The device operates by using two independent power-supply rails (V_{CCA} and V_{CCB}) that operate as low as 0.65 V. Data pins A1 through A8 are designed to track V_{CCA}, which accepts any supply voltage from 0.65 V to 3.6 V. Data pins B1 through B8 are designed to track V_{CCB}, which accepts any supply voltage from 0.65 V to 3.6 V.

The SN74AXC8T245 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control inputs (DIR1 and DIR2). The output-enable ($\overline{OE}$) input is used to disable the outputs so the buses are effectively isolated.

The SN74AXC8T245 device is designed so the control pins (DIR and $\overline{OE}$) are referenced to V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

The V_{CC} isolation feature ensures that if either V_{CC} input supply is below 100 mV, all level shifter outputs are disabled and placed into a high-impedance state.

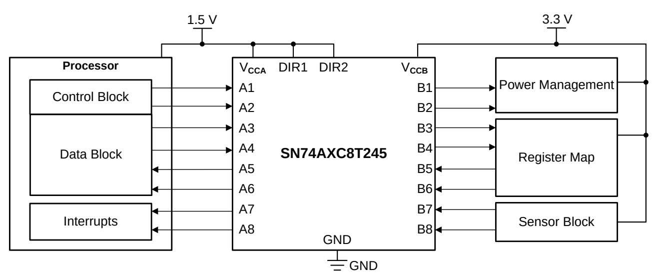
To ensure the high-impedance state of the level shifter I/Os during power up or power down, $\overline{OE}$ should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AXC8T245PW	TSSOP (24)	4.40 mm × 7.80 mm
SN74AXC8T245RHL	VQFN (24)	3.50 mm × 5.50 mm
SN74AXC8T245RJW	UQFN (24)	2.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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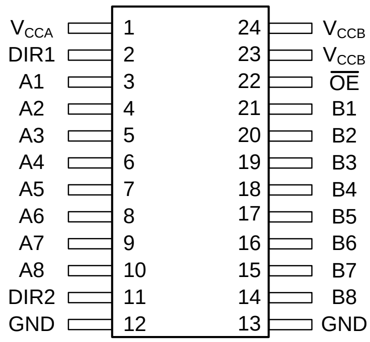
4 Revision History

Changes from Revision A (July 2018) to Revision B	**Page**
• Changed data sheet status from Mixed Production to Production Data	1
• Removed package preview note from RJW package	1

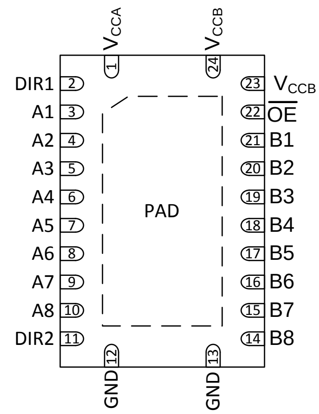
Changes from Original (March 2018) to Revision A	**Page**
• Added RJW as a new package option (preview)	1

5 Pin Configuration and Functions

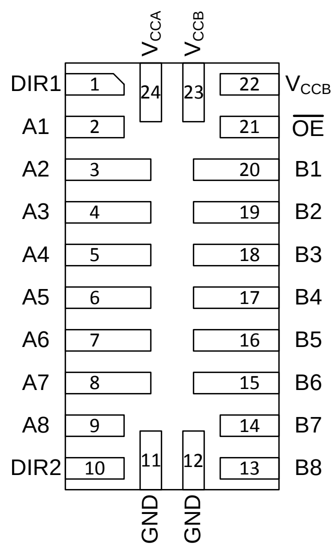
PW Package
24-Pin TSSOP
Top View



RHL Package
24-Pin VQFN
Top View



RJW Package
24-Pin UQFN
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	PW, RHL	RJW		
A1	3	2	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	3	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	4	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	5	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	6	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	7	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	8	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	9	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	20	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	19	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	18	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	17	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	16	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	15	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	14	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	13	I/O	Input/output B8. Referenced to V_{CCB}.
DIR1	2	1	I	Direction-control signal. Referenced to V_{CCA}.
DIR2	11	10	I	Direction-control signal when both V_{CCA} and V_{CCB} ≥ 1.4 V. Referenced to V_{CCA}. Tie to GND to maintain backward compatibility with SN74AVC8T245 device.
GND	12	11	—	Ground
	13	12	—	Ground
$\overline{\text{OE}}$	22	21	I	Output Enable. Pull to GND to enable all outputs. Pull to V_{CCA} to place all outputs in high-impedance mode. Referenced to V_{CCA}.
V_{CCA}	1	24	—	A-port supply voltage. 0.65 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	23	22	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V
	24	23	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_{CCA}		–0.5	4.2	V
Supply voltage, V_{CCB}		–0.5	4.2	V
Input voltage, V_I[2]	I/O ports (A port)	–0.5	4.2	V
	I/O ports (B port)	–0.5	4.2	
	Control inputs	–0.5	4.2	
Voltage applied to any output in the high-impedance or power-off state, V_O[2]	A port	–0.5	4.2	V
	B port	–0.5	4.2	
Voltage applied to any output in the high or low state, V_O[2] [3]	A port	–0.5	V_{CCA} + 0.2	V
	B port	–0.5	V_{CCB} + 0.2	
Input clamp current, I_{IK}	$V_I < 0$	–50		mA
Output clamp current, I_{OK}	$V_O < 0$	–50		mA
Continuous output current, I_O		–50	50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage			0.65	3.6	V
V_{CCB}	Supply voltage			0.65	3.6	V
V_{IH}	High-level input voltage	Data inputs	V_{CCI} = 0.65 V - 0.75 V	$V_{CCI} \times 0.70$		V
			V_{CCI} = 0.76 V - 1 V	$V_{CCI} \times 0.70$		
			V_{CCI} = 1.1 V - 1.95 V	$V_{CCI} \times 0.65$		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control inputs (DIR, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	$V_{CCA} \times 0.70$		
			V_{CCA} = 0.76 V - 1 V	$V_{CCA} \times 0.70$		
			V_{CCA} = 1.1 V - 1.95 V	$V_{CCA} \times 0.65$		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data inputs	V_{CCI} = 0.65 V - 0.75 V		$V_{CCI} \times 0.30$	V
			V_{CCI} = 0.76 V - 1 V		$V_{CCI} \times 0.30$	
			V_{CCI} = 1.1 V - 1.95 V		$V_{CCI} \times 0.35$	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control inputs (DIR, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		$V_{CCA} \times 0.30$	
			V_{CCA} = 0.76 V - 1 V		$V_{CCA} \times 0.30$	
			V_{CCA} = 1.1 V - 1.95 V		$V_{CCA} \times 0.35$	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active state		0	V_{CCO} (2)	V
		Tri-state		0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate				10	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

6.4 Thermal Information

THERMAL METRIC		SN74AXC8T245			UNIT
		PW (TSSOP)	RHL (VQFN)	RJW (UQFN)	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.0	35.0	123.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.3	39.9	65.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	13.8	55.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	0.3	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.2	13.8	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1.4	N/A	°C/W

6.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	–40°C to 85°C			–40°C to 125°C			UNIT
						MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = –100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = –50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = –200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = –500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_I	Input leakage current	Control Inputs (DIR, $\overline{OE}$): $V_I = V_{CCA}$ or GND		0.65 V - 3.6 V	0.65 V - 3.6 V	-0.5		0.5	-1		1	µA
I_{off}	Partial power down current	A Port: V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	-4		4	-8		8	µA
		B Port: V_I or V_O = 0 V - 3.6 V		0 V - 3.6 V	0 V	-4		4	-8		8	
I_{OZ}	High-impedance state output current	A Port: $V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	-4		4	-8		8	µA
		B Port: $V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	-4		4	-8		8	
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA		0.65 V - 3.6 V	0.65 V - 3.6 V			19			40	µA
				0 V	3.6 V	-2			-12			
				3.6 V	0 V			12			25	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA		0.65 V - 3.6 V	0.65 V - 3.6 V			18			38	µA
				0 V	3.6 V			12			25	
				3.6 V	0 V	-2			-12			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA		0.65 V - 3.6 V	0.65 V - 3.6 V			25			55	µA
C_i	Input capacitance	Control Inputs (DIR, $\overline{OE}$): V_I = 3.3 V or GND		3.3 V	3.3 V		4.5			4.5		pF
C_{io}	Data I/O capacitance	Ports A and B: $\overline{OE} = V_{CCA}$, V_O = 1.65V DC + 1 MHz -16 dBm sine wave		3.3 V	3.3 V		5.7			5.7		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) All typical values are for T_A = 25°C

6.6 Switching Characteristics, V_{CCA} = 0.7 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB}) 0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	172	0.5	114	0.5	82	0.5	49	ns
			–40°C to 125°C	0.5	172	0.5	114	0.5	82	0.5	49	
		From input B to output A	–40°C to 85°C	0.5	172	0.5	153	0.5	126	0.5	88	
			–40°C to 125°C	0.5	172	0.5	153	0.5	126	0.5	88	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	192	0.5	192	0.5	192	0.5	192	ns
			–40°C to 125°C	0.5	195	0.5	195	0.5	195	0.5	195	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	156	0.5	129	0.5	118	0.5	120	
			–40°C to 125°C	0.5	157	0.5	129	0.5	120	0.5	122	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	237	0.5	237	0.5	237	0.5	237	ns
			–40°C to 125°C	0.5	237	0.5	237	0.5	237	0.5	237	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	223	0.5	145	0.5	106	0.5	74	
			–40°C to 125°C	0.5	223	0.5	145	0.5	106	0.5	74	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB}) 1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	46	0.5	49	0.5	61	0.5	142	ns
			–40°C to 125°C	0.5	46	0.5	49	0.5	61	0.5	142	
		From input B to output A	–40°C to 85°C	0.5	83	0.5	82	0.5	81	0.5	81	
			–40°C to 125°C	0.5	83	0.5	82	0.5	81	0.5	81	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	192	0.5	192	0.5	192	0.5	192	ns
			–40°C to 125°C	0.5	195	0.5	195	0.5	195	0.5	195	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	69	0.5	66	0.5	67	0.5	150	
			–40°C to 125°C	0.5	70	0.5	67	0.5	67	0.5	150	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	237	0.5	237	0.5	237	0.5	237	ns
			–40°C to 125°C	0.5	237	0.5	237	0.5	237	0.5	237	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	68	0.5	69	0.5	84	0.5	552	
			–40°C to 125°C	0.5	68	0.5	69	0.5	84	0.5	552	

6.7 Switching Characteristics, V_{CCA} = 0.8 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	153	0.5	95	0.5	62	0.5	32	ns
			–40°C to 125°C	0.5	153	0.5	95	0.5	62	0.5	32	
		From input B to output A	–40°C to 85°C	0.5	114	0.5	95	0.5	78	0.5	52	
			–40°C to 125°C	0.5	114	0.5	95	0.5	78	0.5	52	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	101	0.5	101	0.5	101	0.5	101	ns
			–40°C to 125°C	0.5	103	0.5	103	0.5	103	0.5	103	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	141	0.5	114	0.5	104	0.5	106	
			–40°C to 125°C	0.5	142	0.5	115	0.5	106	0.5	109	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	102	0.5	102	0.5	102	0.5	102	ns
			–40°C to 125°C	0.5	102	0.5	102	0.5	102	0.5	102	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	202	0.5	124	0.5	86	0.5	52	
			–40°C to 125°C	0.5	202	0.5	124	0.5	86	0.5	52	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	26	0.5	25	0.5	25	0.5	35	ns
			–40°C to 125°C	0.5	26	0.5	25	0.5	25	0.5	35	
		From input B to output A	–40°C to 85°C	0.5	42	0.5	41	0.5	40	0.5	40	
			–40°C to 125°C	0.5	42	0.5	41	0.5	40	0.5	40	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	101	0.5	101	0.5	101	0.5	101	ns
			–40°C to 125°C	0.5	103	0.5	103	0.5	103	0.5	103	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	55	0.5	51	0.5	49	0.5	51	
			–40°C to 125°C	0.5	57	0.5	53	0.5	50	0.5	52	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	102	0.5	102	0.5	102	0.5	102	ns
			–40°C to 125°C	0.5	102	0.5	102	0.5	102	0.5	102	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	44	0.5	43	0.5	45	0.5	58	
			–40°C to 125°C	0.5	44	0.5	43	0.5	45	0.5	58	

6.8 Switching Characteristics, V_{CCA} = 0.9 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	127	0.5	78	0.5	52	0.5	23	ns
			–40°C to 125°C	0.5	127	0.5	78	0.5	52	0.5	23	
		From input B to output A	–40°C to 85°C	0.5	82	0.5	63	0.5	52	0.5	39	
			–40°C to 125°C	0.5	82	0.5	63	0.5	52	0.5	39	
t_{dis}	Disable time	From input$\overline{OE}$ to output A	–40°C to 85°C	0.5	125	0.5	125	0.5	125	0.5	125	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		From input$\overline{OE}$ to output B	–40°C to 85°C	0.5	131	0.5	105	0.5	96	0.5	99	
			–40°C to 125°C	0.5	133	0.5	107	0.5	98	0.5	101	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	124	0.5	124	0.5	124	0.5	124	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	191	0.5	113	0.5	75	0.5	41	
			–40°C to 125°C	0.5	191	0.5	113	0.5	75	0.5	41	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	17	0.5	15	0.5	14	0.5	17	ns
			–40°C to 125°C	0.5	17	0.5	15	0.5	14	0.5	17	
		From input B to output A	–40°C to 85°C	0.5	28	0.5	24	0.5	22	0.5	22	
			–40°C to 125°C	0.5	28	0.5	24	0.5	22	0.5	22	
t_{dis}	Disable time	From input$\overline{OE}$ to output A	–40°C to 85°C	0.5	125	0.5	125	0.5	125	0.5	125	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		From input$\overline{OE}$ to output B	–40°C to 85°C	0.5	47	0.5	44	0.5	40	0.5	73	
			–40°C to 125°C	0.5	50	0.5	46	0.5	42	0.5	73	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	124	0.5	124	0.5	124	0.5	124	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	34	0.5	32	0.5	31	0.5	35	
			–40°C to 125°C	0.5	34	0.5	32	0.5	31	0.5	35	

6.9 Switching Characteristics, V_{CCA} = 1.2 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	88	0.5	52	0.5	39	0.5	15	ns
			–40°C to 125°C	0.5	88	0.5	52	0.5	39	0.5	15	
		From input B to output A	–40°C to 85°C	0.5	49	0.5	32	0.5	23	0.5	15	
			–40°C to 125°C	0.5	49	0.5	32	0.5	23	0.5	15	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	87	0.5	87	0.5	87	0.5	87	ns
			–40°C to 125°C	0.5	91	0.5	91	0.5	91	0.5	91	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	119	0.5	94	0.5	85	0.5	89	
			–40°C to 125°C	0.5	121	0.5	96	0.5	88	0.5	93	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	ns
			–40°C to 125°C	0.5	36	0.5	36	0.5	36	0.5	36	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	168	0.5	98	0.5	61	0.5	29	
			–40°C to 125°C	0.5	168	0.5	98	0.5	61	0.5	30	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	10	0.5	9	0.5	7	0.5	7	ns
			–40°C to 125°C	0.5	10	0.5	9	0.5	7	0.5	8	
		From input B to output A	–40°C to 85°C	0.5	13	0.5	11	0.5	8	0.5	7	
			–40°C to 125°C	0.5	13	0.5	11	0.5	8	0.5	7	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	87	0.5	87	0.5	87	0.5	87	ns
			–40°C to 125°C	0.5	91	0.5	91	0.5	91	0.5	91	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	38	0.5	35	0.5	31	0.5	29	
			–40°C to 125°C	0.5	41	0.5	38	0.5	33	0.5	31	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	ns
			–40°C to 125°C	0.5	36	0.5	36	0.5	36	0.5	36	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	22	0.5	19	0.5	17	0.5	17	
			–40°C to 125°C	0.5	23	0.5	20	0.5	18	0.5	18	

6.10 Switching Characteristics, V_{CCA} = 1.5 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB}) 0.7 V ± 0.05 V MIN	0.7 V ± 0.05 V MAX	0.8 V ± 0.04 V MIN	0.8 V ± 0.04 V MAX	0.9 V ± 0.045 V MIN	0.9 V ± 0.045 V MAX	1.2 V ± 0.1 V MIN	1.2 V ± 0.1 V MAX	UNIT
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	84	0.5	42	0.5	28	0.5	13	ns
			–40°C to 125°C	0.5	84	0.5	42	0.5	28	0.5	13	
		From input B to output A	–40°C to 85°C	0.5	46	0.5	26	0.5	17	0.5	10	
			–40°C to 125°C	0.5	46	0.5	26	0.5	17	0.5	10	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	ns
			–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	115	0.5	89	0.5	80	0.5	85	
			–40°C to 125°C	0.5	117	0.5	91	0.5	83	0.5	89	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	21	0.5	21	0.5	21	0.5	21	ns
			–40°C to 125°C	0.5	23	0.5	23	0.5	23	0.5	23	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	159	0.5	90	0.5	55	0.5	24	
			–40°C to 125°C	0.5	159	0.5	90	0.5	55	0.5	25	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB}) 1.5 V ± 0.1 V MIN	1.5 V ± 0.1 V MAX	1.8 V ± 0.15 V MIN	1.8 V ± 0.15 V MAX	2.5 V ± 0.2 V MIN	2.5 V ± 0.2 V MAX	3.3 V ± 0.3 V MIN	3.3 V ± 0.3 V MAX	UNIT
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	9	0.5	7	0.5	6	0.5	5	ns
			–40°C to 125°C	0.5	9	0.5	7	0.5	6	0.5	6	
		From input B to output A	–40°C to 85°C	0.5	9	0.5	7	0.5	6	0.5	5	
			–40°C to 125°C	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	ns
			–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	35	0.5	31	0.5	28	0.5	25	
			–40°C to 125°C	0.5	38	0.5	34	0.5	31	0.5	27	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	21	0.5	21	0.5	21	0.5	21	ns
			–40°C to 125°C	0.5	23	0.5	23	0.5	23	0.5	23	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	17	0.5	15	0.5	12	0.5	11	
			–40°C to 125°C	0.5	18	0.5	15	0.5	13	0.5	12	

6.11 Switching Characteristics, V_{CCA} = 1.8 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	82	0.5	41	0.5	24	0.5	11	ns
			–40°C to 125°C	0.5	82	0.5	41	0.5	24	0.5	11	
		From input B to output A	–40°C to 85°C	0.5	49	0.5	25	0.5	15	0.5	9	
			–40°C to 125°C	0.5	49	0.5	25	0.5	15	0.5	9	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	113	0.5	87	0.5	78	0.5	83	
			–40°C to 125°C	0.5	115	0.5	89	0.5	81	0.5	87	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	ns
			–40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	157	0.5	88	0.5	54	0.5	23	
			–40°C to 125°C	0.5	157	0.5	88	0.5	54	0.5	23	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	8	0.5	6	0.5	5	0.5	5	ns
			–40°C to 125°C	0.5	8	0.5	7	0.5	6	0.5	5	
		From input B to output A	–40°C to 85°C	0.5	7	0.5	6	0.5	5	0.5	4	
			–40°C to 125°C	0.5	7	0.5	7	0.5	5	0.5	4	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	33	0.5	30	0.5	27	0.5	57	
			–40°C to 125°C	0.5	36	0.5	33	0.5	29	0.5	60	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	ns
			–40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	15	0.5	13	0.5	10	0.5	9	
			–40°C to 125°C	0.5	16	0.5	14	0.5	11	0.5	10	

6.12 Switching Characteristics, V_{CCA} = 2.5 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB}) 0.7 V ± 0.05 V MIN	0.7 V ± 0.05 V MAX	0.8 V ± 0.04 V MIN	0.8 V ± 0.04 V MAX	0.9 V ± 0.045 V MIN	0.9 V ± 0.045 V MAX	1.2 V ± 0.1 V MIN	1.2 V ± 0.1 V MAX	UNIT
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	81	0.5	40	0.5	22	0.5	8	ns
			–40°C to 125°C	0.5	81	0.5	40	0.5	22	0.5	8	
		From input B to output A	–40°C to 85°C	0.5	61	0.5	25	0.5	14	0.5	7	
			–40°C to 125°C	0.5	61	0.5	25	0.5	14	0.5	7	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	111	0.5	85	0.5	76	0.5	81	
			–40°C to 125°C	0.5	113	0.5	87	0.5	78	0.5	84	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	155	0.5	86	0.5	52	0.5	21	
			–40°C to 125°C	0.5	155	0.5	86	0.5	52	0.5	21	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB}) 1.5 V ± 0.1 V MIN	1.5 V ± 0.1 V MAX	1.8 V ± 0.15 V MIN	1.8 V ± 0.15 V MAX	2.5 V ± 0.2 V MIN	2.5 V ± 0.2 V MAX	3.3 V ± 0.3 V MIN	3.3 V ± 0.3 V MAX	UNIT
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	6	0.5	5	0.5	4	0.5	4	ns
			–40°C to 125°C	0.5	6	0.5	5	0.5	5	0.5	4	
		From input B to output A	–40°C to 85°C	0.5	6	0.5	5	0.5	4	0.5	4	
			–40°C to 125°C	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	31	0.5	28	0.5	25	0.5	23	
			–40°C to 125°C	0.5	34	0.5	31	0.5	28	0.5	25	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	14	0.5	11	0.5	9	0.5	7	
			–40°C to 125°C	0.5	14	0.5	12	0.5	9	0.5	8	

6.13 Switching Characteristics, V_{CCA} = 3.3 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	81	0.5	40	0.5	22	0.5	7	ns
			–40°C to 125°C	0.5	81	0.5	40	0.5	22	0.5	7	
		From input B to output A	–40°C to 85°C	0.5	142	0.5	35	0.5	17	0.5	7	
			–40°C to 125°C	0.5	142	0.5	35	0.5	17	0.5	8	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	22	0.5	22	0.5	22	0.5	22	ns
			–40°C to 125°C	0.5	24	0.5	24	0.5	24	0.5	24	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	111	0.5	84	0.5	75	0.5	80	
			–40°C to 125°C	0.5	113	0.5	86	0.5	78	0.5	83	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	9	0.5	9	0.5	9	0.5	9	ns
			–40°C to 125°C	0.5	10	0.5	10	0.5	10	0.5	10	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	154	0.5	86	0.5	51	0.5	20	
			–40°C to 125°C	0.5	154	0.5	86	0.5	51	0.5	20	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	5	0.5	4	0.5	4	0.5	4	ns
			–40°C to 125°C	0.5	5	0.5	4	0.5	4	0.5	4	
		From input B to output A	–40°C to 85°C	0.5	5	0.5	5	0.5	4	0.5	4	
			–40°C to 125°C	0.5	6	0.5	5	0.5	4	0.5	4	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	22	0.5	22	0.5	22	0.5	22	ns
			–40°C to 125°C	0.5	24	0.5	24	0.5	24	0.5	24	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	30	0.5	27	0.5	25	0.5	23	
			–40°C to 125°C	0.5	33	0.5	30	0.5	27	0.5	25	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	9	0.5	9	0.5	9	0.5	9	ns
			–40°C to 125°C	0.5	10	0.5	10	0.5	10	0.5	10	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	13	0.5	10	0.5	8	0.5	7	
			–40°C to 125°C	0.5	14	0.5	11	0.5	8	0.5	7	

6.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdA}	Power dissipation capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open, f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.2		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.8		
			V_{CCA} = V_{CCB} = 0.9 V		1.8		
			V_{CCA} = V_{CCB} = 1.2 V		1.7		
			V_{CCA} = V_{CCB} = 1.5 V		1.7		
			V_{CCA} = V_{CCB} = 1.8 V		1.7		
			V_{CCA} = V_{CCB} = 2.5 V		2		
			V_{CCA} = V_{CCB} = 3.3 V		2.5		
C_{pdA}	Power dissipation capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open, f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.1		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.8		
			V_{CCA} = V_{CCB} = 0.9 V		1.8		
			V_{CCA} = V_{CCB} = 1.2 V		1.7		
			V_{CCA} = V_{CCB} = 1.5 V		1.7		
			V_{CCA} = V_{CCB} = 1.8 V		1.7		
			V_{CCA} = V_{CCB} = 2.5 V		2		
			V_{CCA} = V_{CCB} = 3.3 V		2.1		
C_{pdA}	Power dissipation capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open, f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		9.3		pF
			V_{CCA} = V_{CCB} = 0.8 V		11.8		
			V_{CCA} = V_{CCB} = 0.9 V		11.8		
			V_{CCA} = V_{CCB} = 1.2 V		12		
			V_{CCA} = V_{CCB} = 1.5 V		12.2		
			V_{CCA} = V_{CCB} = 1.8 V		13		
			V_{CCA} = V_{CCB} = 2.5 V		16.4		
			V_{CCA} = V_{CCB} = 3.3 V		18.1		
C_{pdA}	Power dissipation capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open, f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		2.6		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.2		
			V_{CCA} = V_{CCB} = 0.9 V		1.1		
			V_{CCA} = V_{CCB} = 1.2 V		1.2		
			V_{CCA} = V_{CCB} = 1.5 V		1.2		
			V_{CCA} = V_{CCB} = 1.8 V		1.3		
			V_{CCA} = V_{CCB} = 2.5 V		1.6		
			V_{CCA} = V_{CCB} = 3.3 V		3.9		

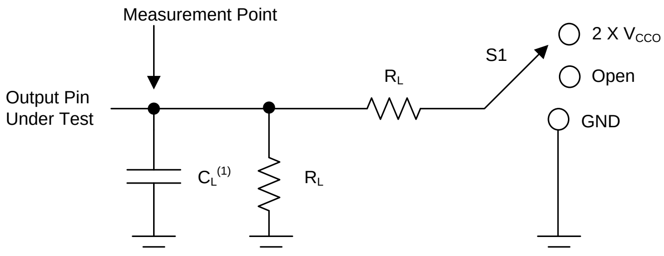
Operating Characteristics: T_A = 25°C (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdB}	Power dissipation capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		9.3		pF
			V_{CCA} = V_{CCB} = 0.8 V		11.7		
			V_{CCA} = V_{CCB} = 0.9 V		11.8		
			V_{CCA} = V_{CCB} = 1.2 V		11.9		
			V_{CCA} = V_{CCB} = 1.5 V		12.2		
			V_{CCA} = V_{CCB} = 1.8 V		12.9		
			V_{CCA} = V_{CCB} = 2.5 V		16.3		
			V_{CCA} = V_{CCB} = 3.3 V		18		
C_{pdB}	Power dissipation capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		2.6		
			V_{CCA} = V_{CCB} = 0.8 V		11.7		pF
			V_{CCA} = V_{CCB} = 0.9 V		11.8		
			V_{CCA} = V_{CCB} = 1.2 V		11.9		
			V_{CCA} = V_{CCB} = 1.5 V		12.2		
			V_{CCA} = V_{CCB} = 1.8 V		12.9		
			V_{CCA} = V_{CCB} = 2.5 V		16.3		
			V_{CCA} = V_{CCB} = 3.3 V		3.9		
C_{pdB}	Power dissipation capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.2		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.8		
			V_{CCA} = V_{CCB} = 0.9 V		1.8		
			V_{CCA} = V_{CCB} = 1.2 V		1.7		
			V_{CCA} = V_{CCB} = 1.5 V		1.7		
			V_{CCA} = V_{CCB} = 1.8 V		1.7		
			V_{CCA} = V_{CCB} = 2.5 V		2		
			V_{CCA} = V_{CCB} = 3.3 V		2.5		
C_{pdB}	Power dissipation capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.1		
			V_{CCA} = V_{CCB} = 0.8 V		1.8		pF
			V_{CCA} = V_{CCB} = 0.9 V		1.8		
			V_{CCA} = V_{CCB} = 1.2 V		1.7		
			V_{CCA} = V_{CCB} = 1.5 V		1.7		
			V_{CCA} = V_{CCB} = 1.8 V		1.7		
			V_{CCA} = V_{CCB} = 2.5 V		2		
			V_{CCA} = V_{CCB} = 3.3 V		2.1		

7 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f =1 MHz
- Z_0 = 50 Ω
- dv / dt ≤ 1 ns/V



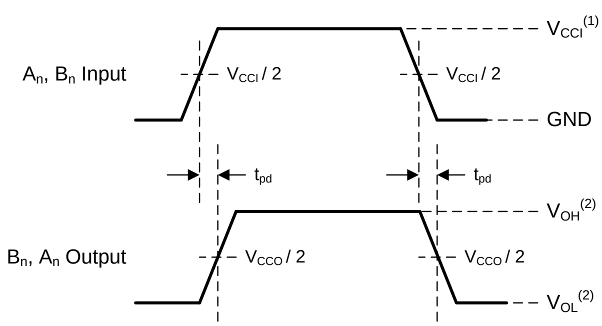
(1) C_L includes probe and jig capacitance.

Figure 1. Load Circuit

Parameter	V_{CCO}	R_L	C_L	S1	V_{TP}
t_{pd}	1.1 V - 3.6 V	2 kΩ	15 pF	Open	N/A
	0.65 V - 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}(1), t_{dis}(1)	3 V - 3.6 V	2 kΩ	15 pF	2 X V_{CCO}	0.3 V
	1.65 V - 2.7 V	2 kΩ	15 pF	2 X V_{CCO}	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	2 X V_{CCO}	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	2 X V_{CCO}	0.1 V
t_{en}(2), t_{dis}(2)	3 V - 3.6 V	2 kΩ	15 pF	GND	0.3 V
	1.65V - 2.7 V	2 kΩ	15 pF	GND	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	GND	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	GND	0.1 V

(1) Output waveform on the conditions that input is driven to a valid Logic Low.
(2) Output waveform on the condition that input is driven to a valid Logic High.

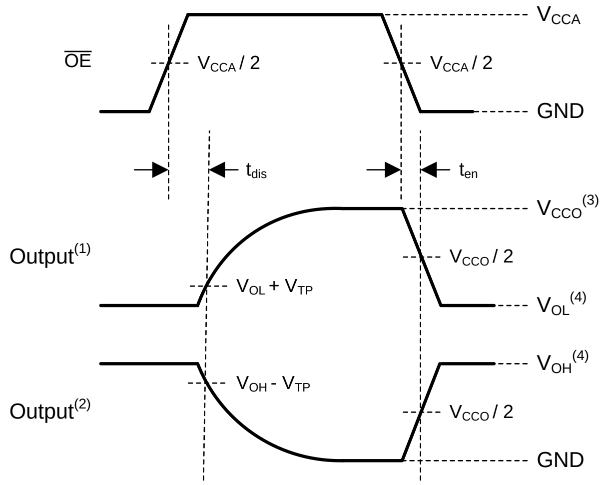
Figure 2. Load Circuit Conditions



(1) V_{CCI} is the supply pin associated with the input port.
(2) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

Figure 3. Propagation Delay

Parameter Measurement Information (continued)



(1) Output waveform on the condition that input is driven to a valid Logic Low.
(2) Output waveform on the condition that input is driven to a valid Logic High.
(3) V_{CCO} is the supply pin associated with the output port.
(4) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

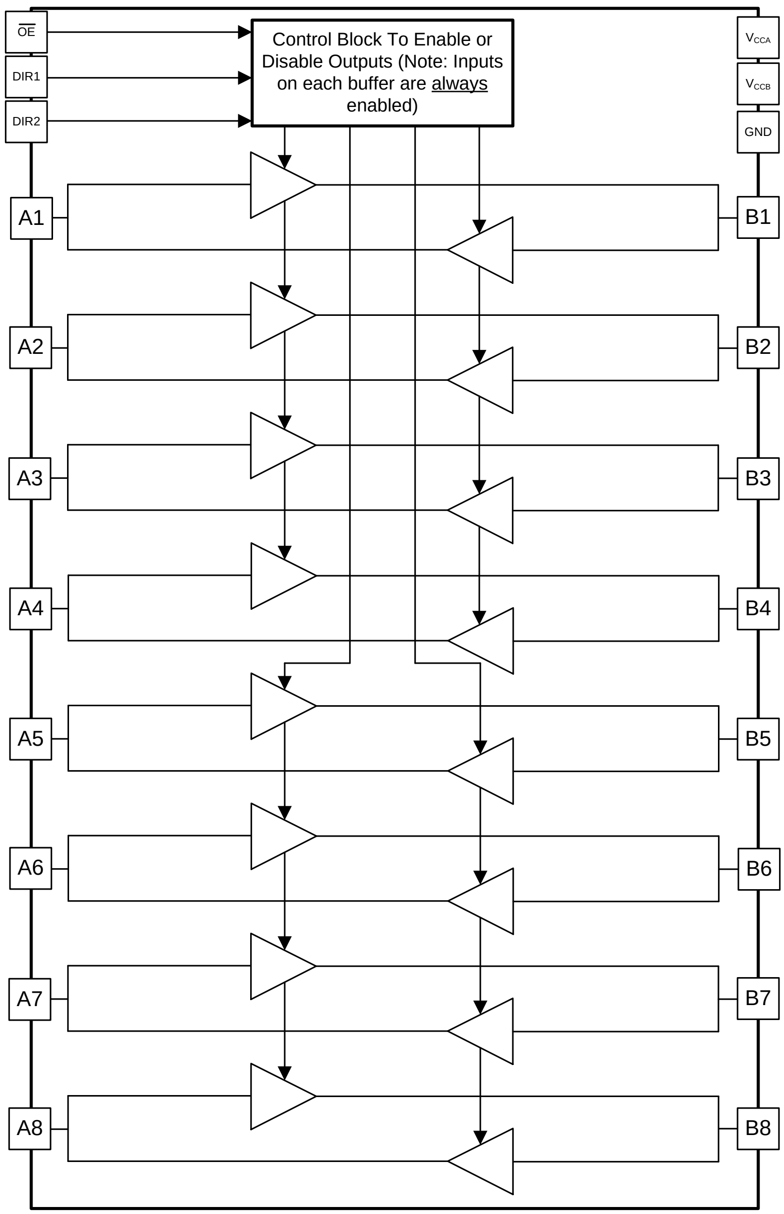
Figure 4. Enable Time And Disable Time

8 Detailed Description

8.1 Overview

The SN74AXC8T245 device is an 8-bit, dual-supply non-inverting transceiver with bidirectional voltage level translation. The I/O pins labeled with A and the control pins (DIR1, DIR2, and $\overline{OE}$) are supported by V_{CCA}, and the I/O pins labeled with B are supported by V_{CCB}. Both the A port and the B port are able to accept I/O voltages ranging from 0.65 V to 3.6 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Up-Translation and Down-Translation From 0.65 V to 3.6 V

Both supply pins are configured from 0.65 V to 3.6 V, which makes the device suitable for translating between any of the low voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Multiple Direction Control Pins

Two control pins are used to configure the 8 data I/Os. I/O channels 1 through 4 are grouped together and I/O channels 5 through 8 are banked together. The benefit of this is to permit simultaneous up-translation and down-translation within one device. This eliminates the need for multiple devices, where each device can only provide up-translation or down-translation sequentially. Simultaneous up and down translation is supported when both V_{CCA} and V_{CCB} are at least 1.40 V.

8.3.3 I_{off} Supports Partial-Power-Down Mode Operation

This feature is to limit the leakage current of an I/O pin being driven to a voltage as large as 3.6 V while having its corresponding power supply rail powered down. This is represented by the I_{off} parameter in the *Electrical Characteristics* table.

8.4 Device Functional Modes

All control inputs are referenced to V_{CCA} and must be driven to a valid Logic High or Logic Low (that is, not floating) to assure proper device operation and to prevent excessive power consumption. Table 1 summarizes the possible modes of device operation based on the configuration of the control inputs.

Table 1. Function Table(1)

CONTROL INPUTS			Signal Direction	
$\overline{OE}$	DIR1	DIR2	Bits 1:4	Bits 5:8
H	X	X	Disabled (Hi-Z)	
L	L	L	B to A	
L	L	H	B to A	A to B
L	H	L	A to B	
L	H	H	A to B	B to A

(1) Input circuits of the data I/Os are always active and must be driven to a valid logic level.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AXC8T245 device can be used in level-translation applications for interfacing devices or systems operating at different voltage nodes. Figure 5 depicts an application in which the SN74AXC8T245 device is up-translating a 0.7 V input to a 3.3 V output to interface between a system controller and a peripheral device.

9.2 Typical Application

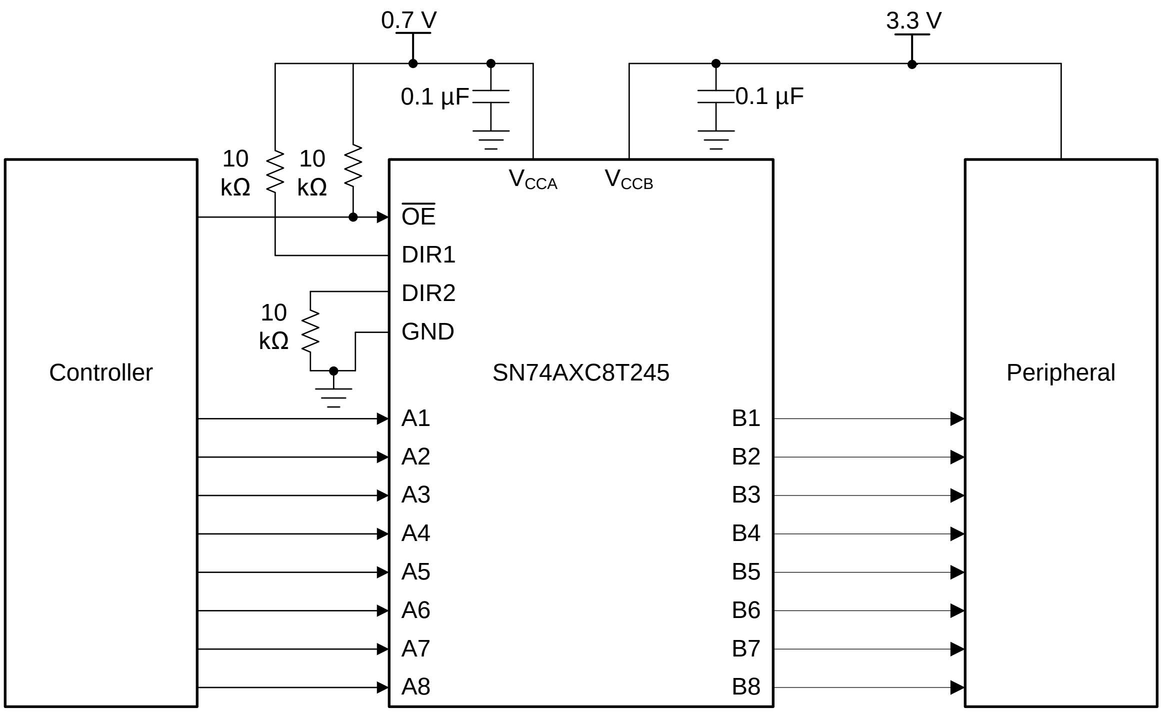


Figure 5. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC8T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC8T245 device is driving to determine the output voltage range.

9.2.3 Application Curve

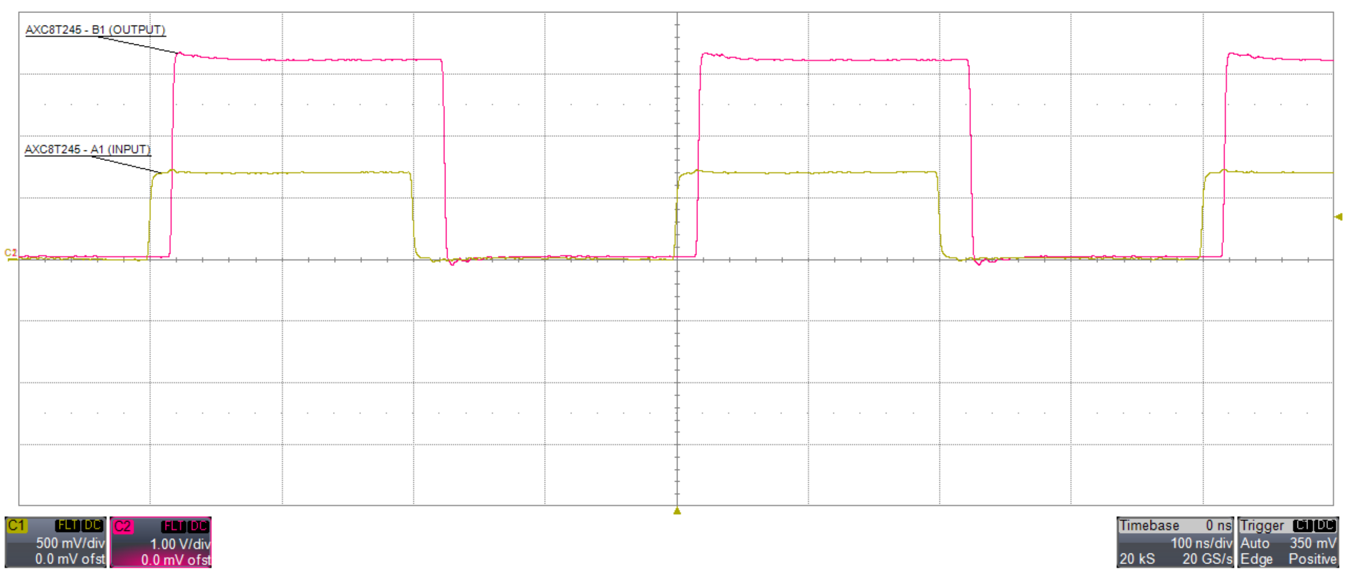


Figure 6. Translation Up (0.7 V to 3.3 V) at 2.5 MHz

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. However, there are no additional requirements for power supply sequencing.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Power Sequencing for AXC Family of Devices* application report.

11 Layout

11.1 Layout Guidelines

To assure reliability of the device, follow common printed-circuit board layout guidelines.

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

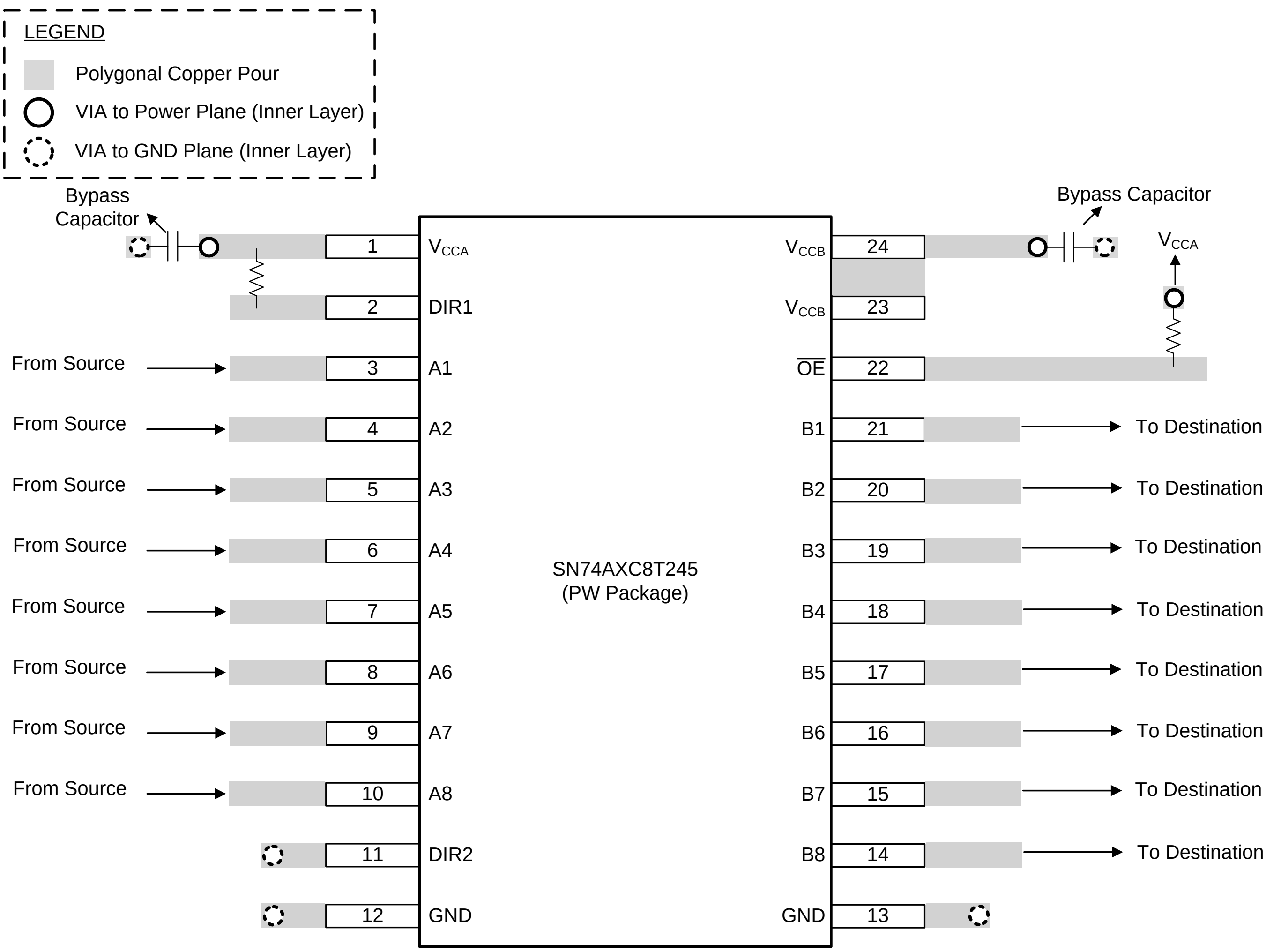


Figure 7. SN74AXC8T245 Device Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

Texas Instruments, *Power Sequencing for AXC Family of Devices* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXC8T245PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AX8T245	Samples
SN74AXC8T245RHLR	ACTIVE	VQFN	RHL	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AX8T245	Samples
SN74AXC8T245RJWR	ACTIVE	UQFN	RJW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AX8T245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

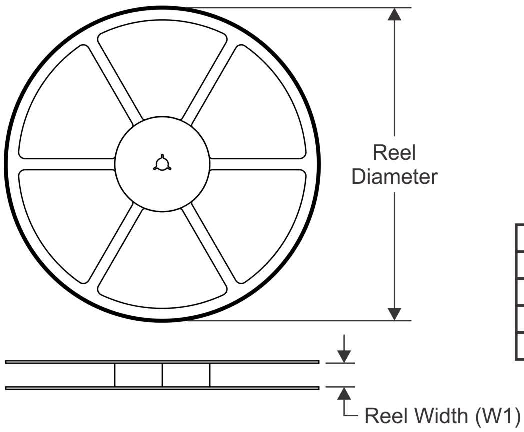
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

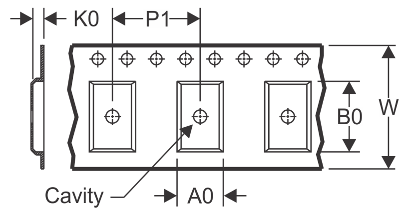
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

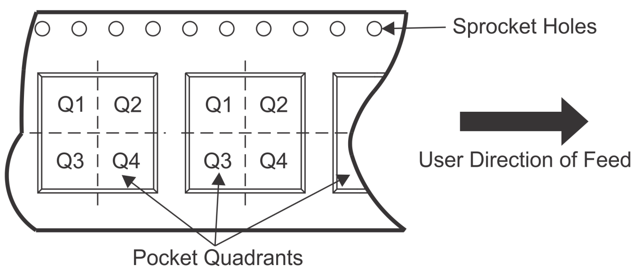


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

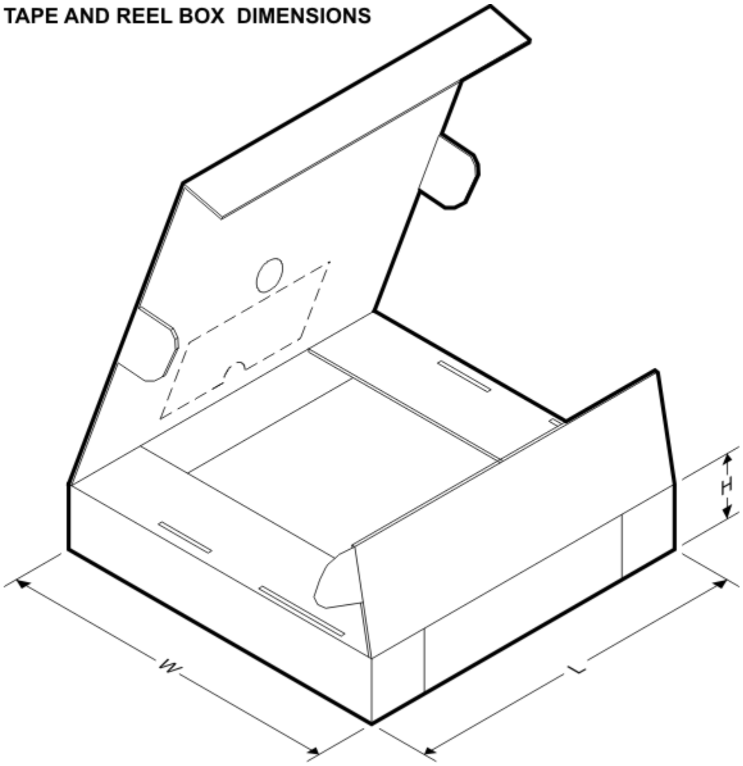
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXC8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74AXC8T245RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74AXC8T245RJWR	UQFN	RJW	24	3000	177.8	12.4	2.21	4.22	0.81	4.0	12.0	Q1

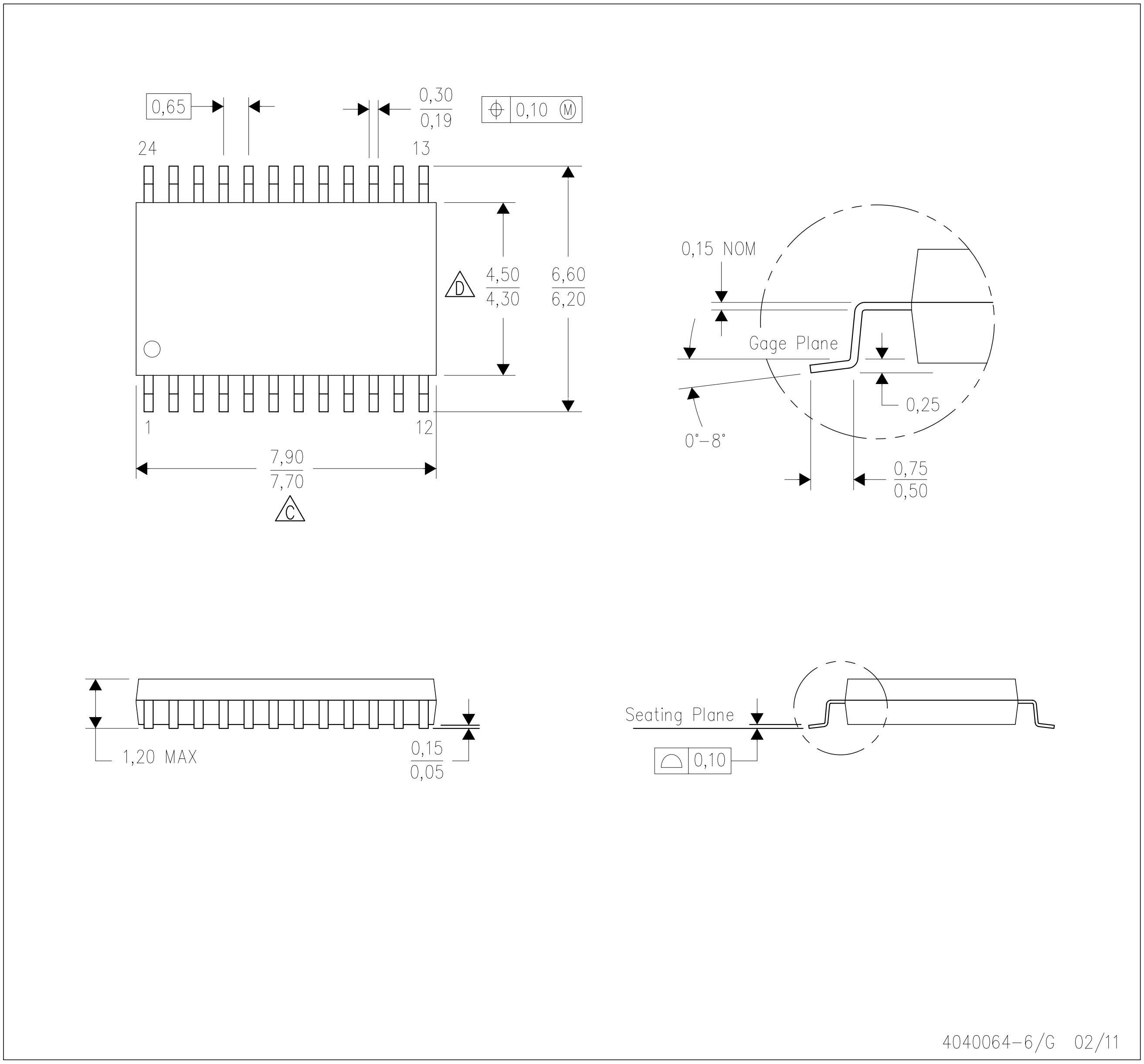
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

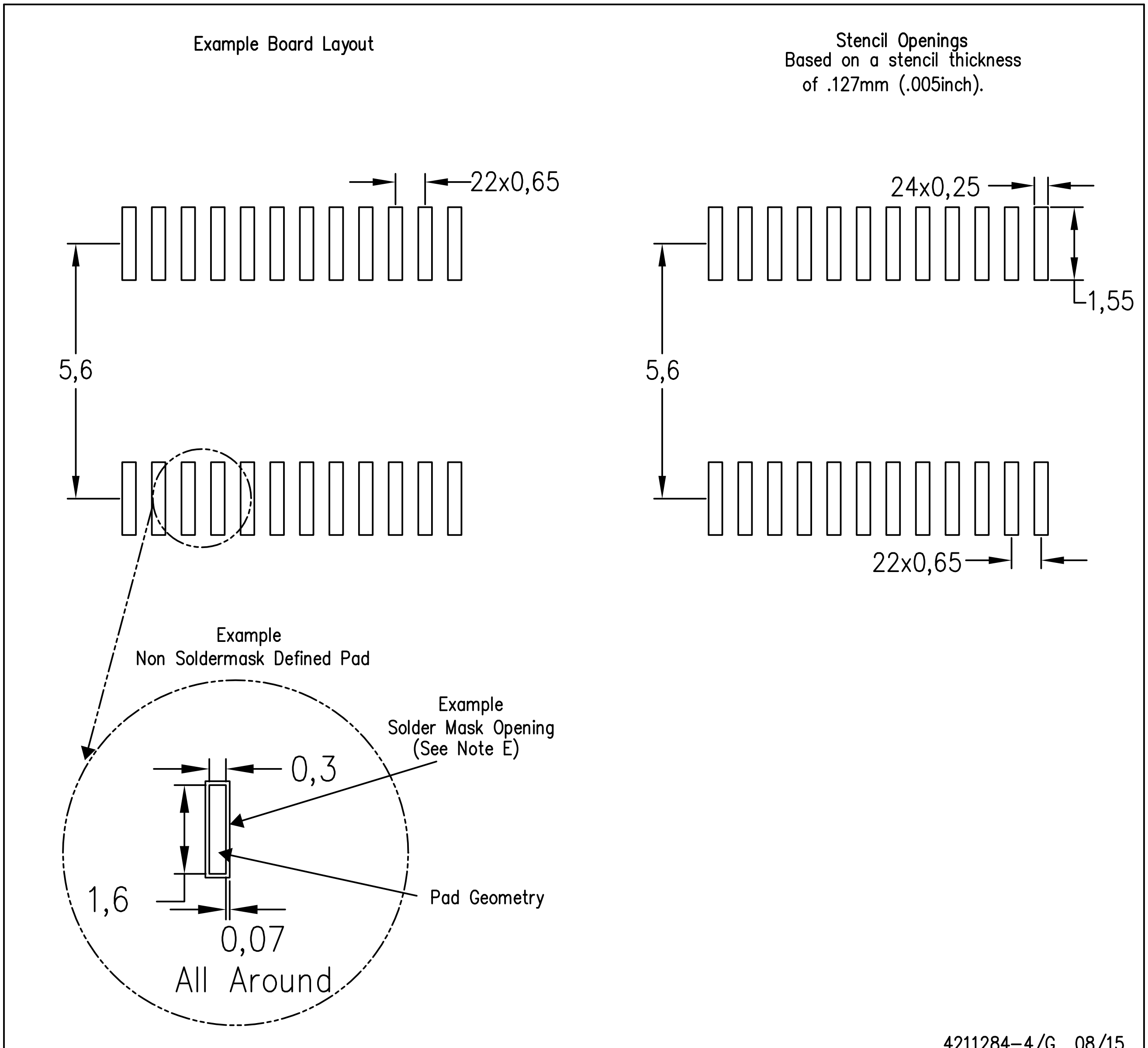
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXC8T245PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74AXC8T245RHLR	VQFN	RHL	24	3000	367.0	367.0	35.0
SN74AXC8T245RJWR	UQFN	RJW	24	3000	183.0	183.0	20.0

PW (R-PDSO-G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



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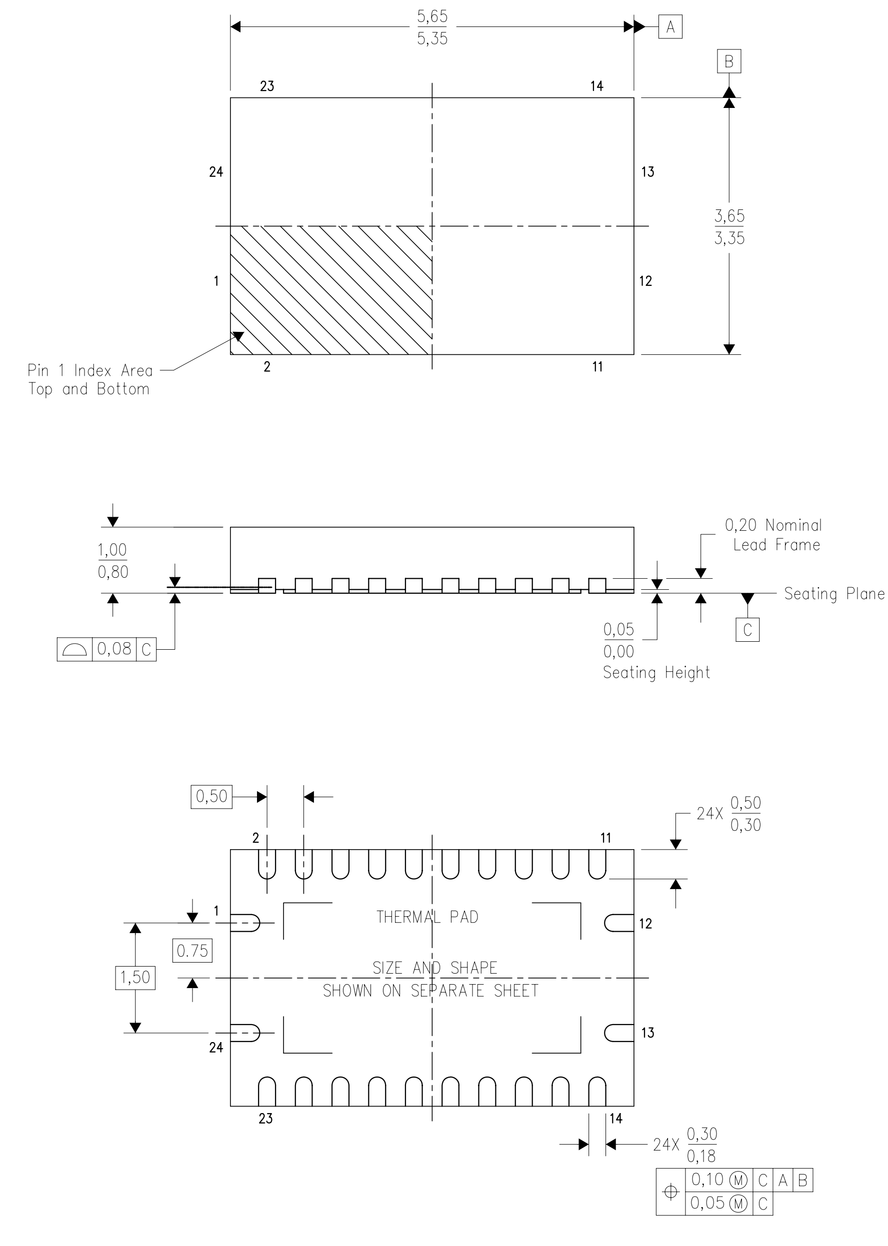
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHL (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. JEDEC MO-241 package registration pending.

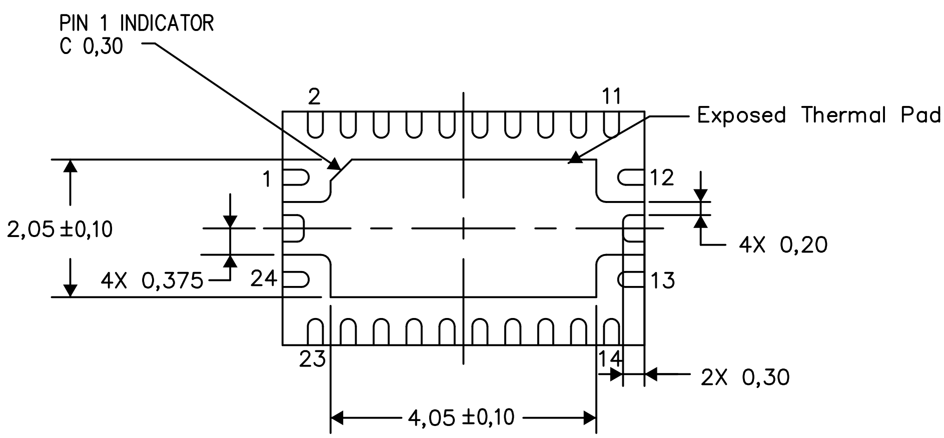
RHL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



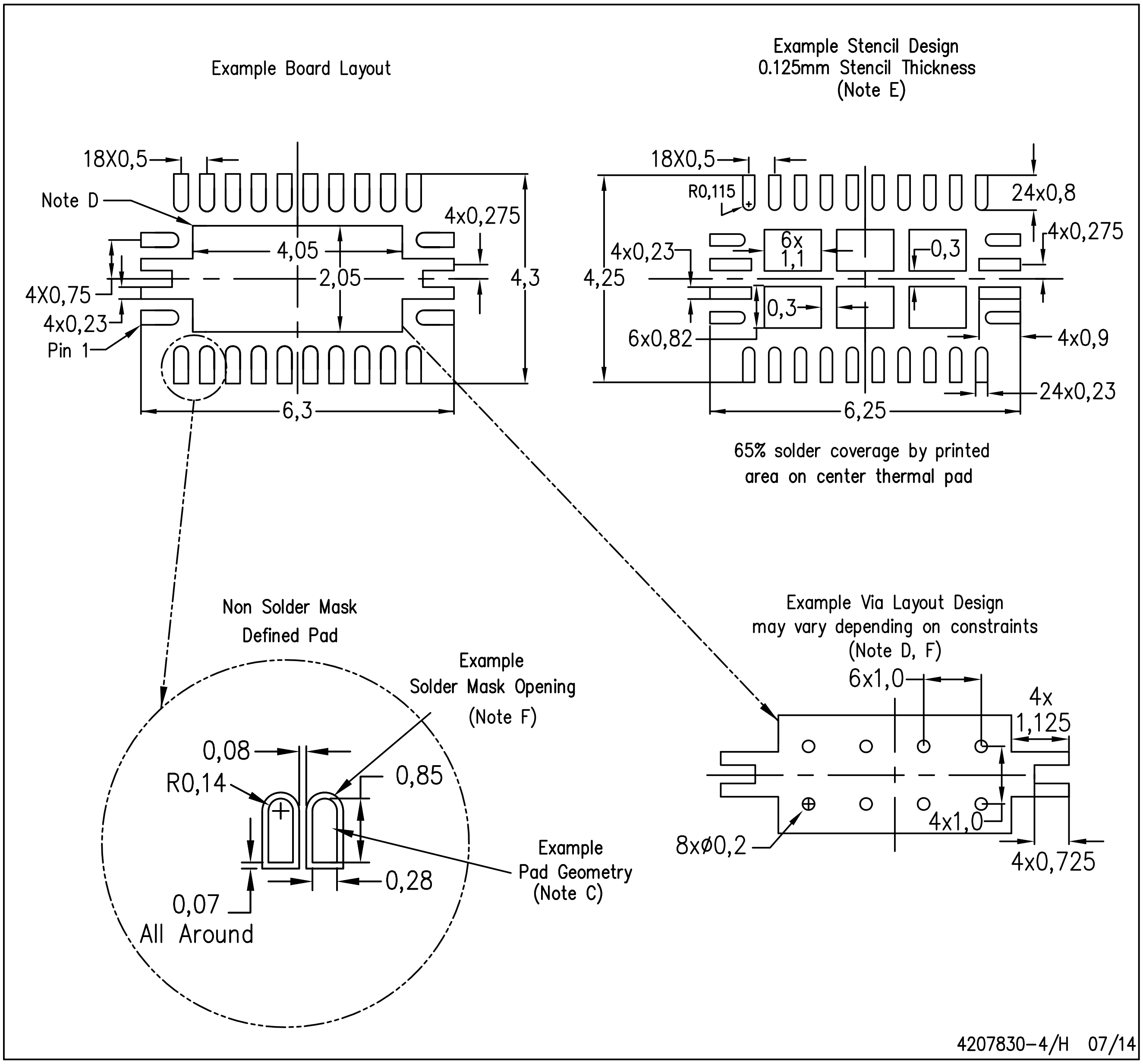
Bottom View

Exposed Thermal Pad Dimensions

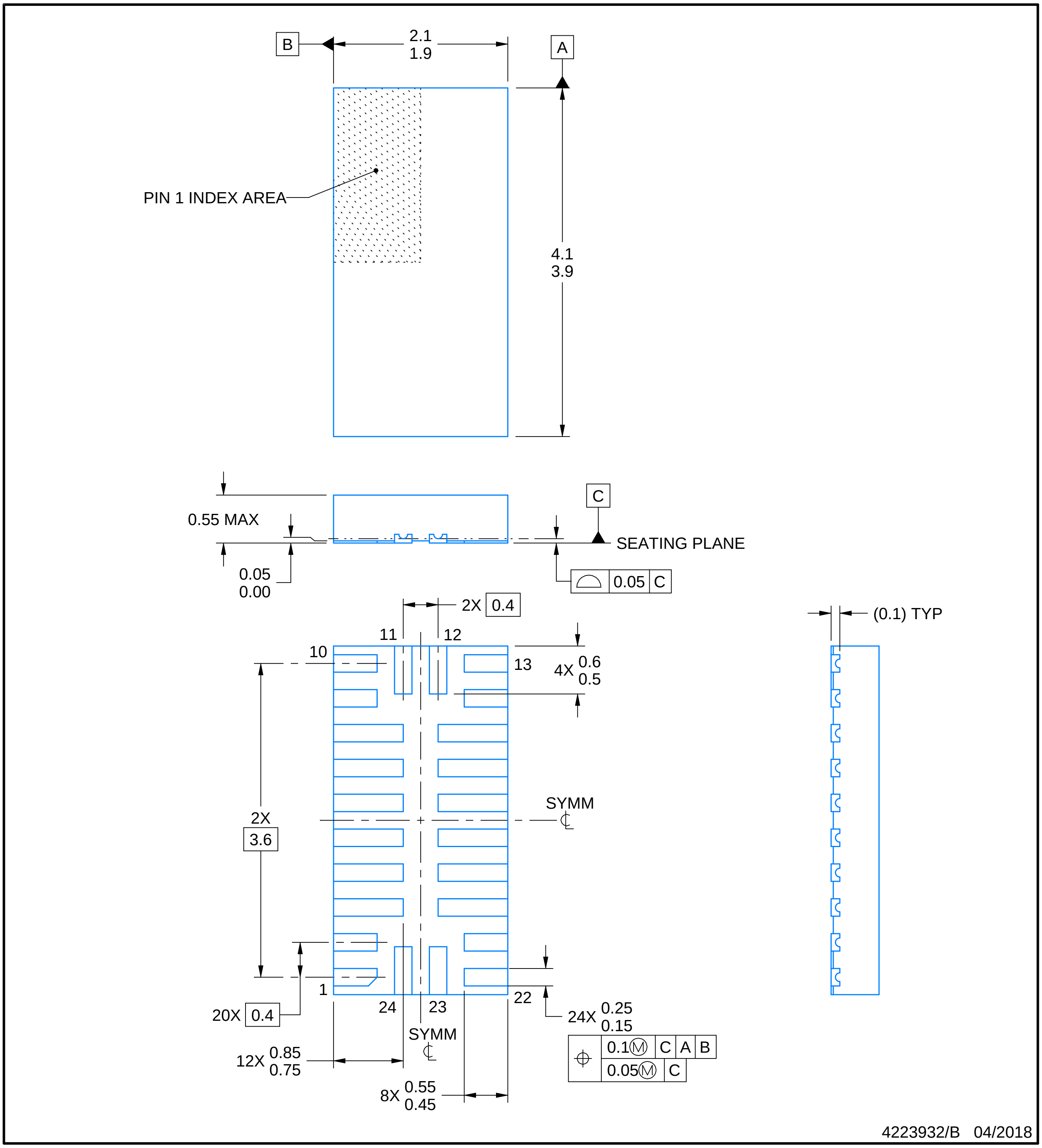
4206363-4/N 07/14

NOTE: All linear dimensions are in millimeters

RHL (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

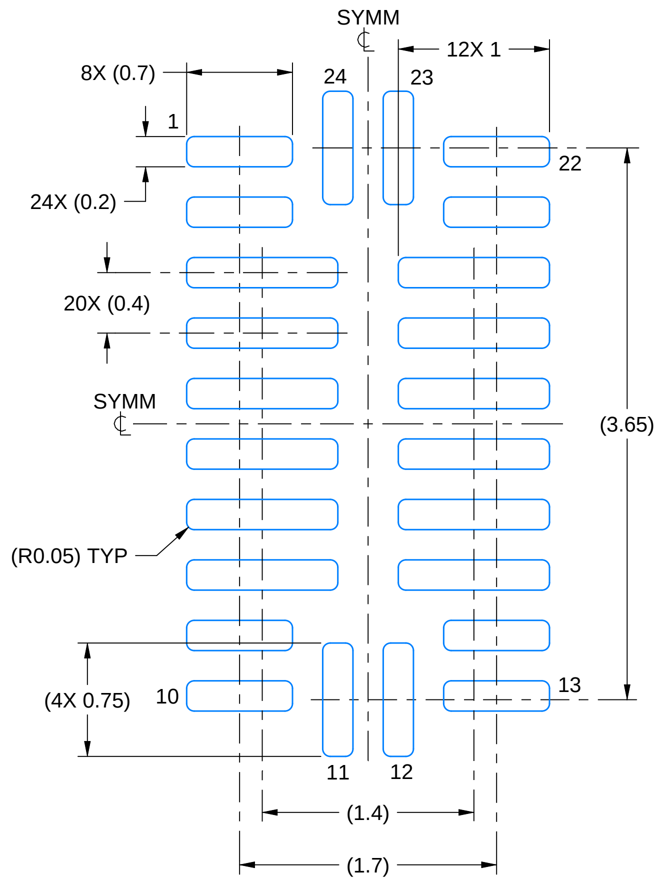


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

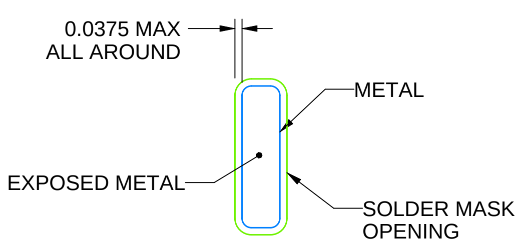


NOTES:

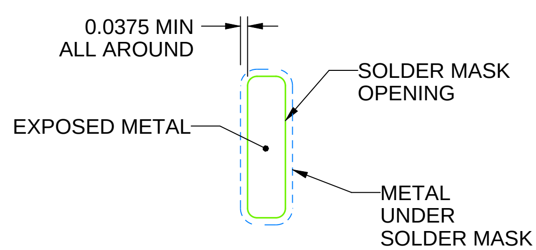
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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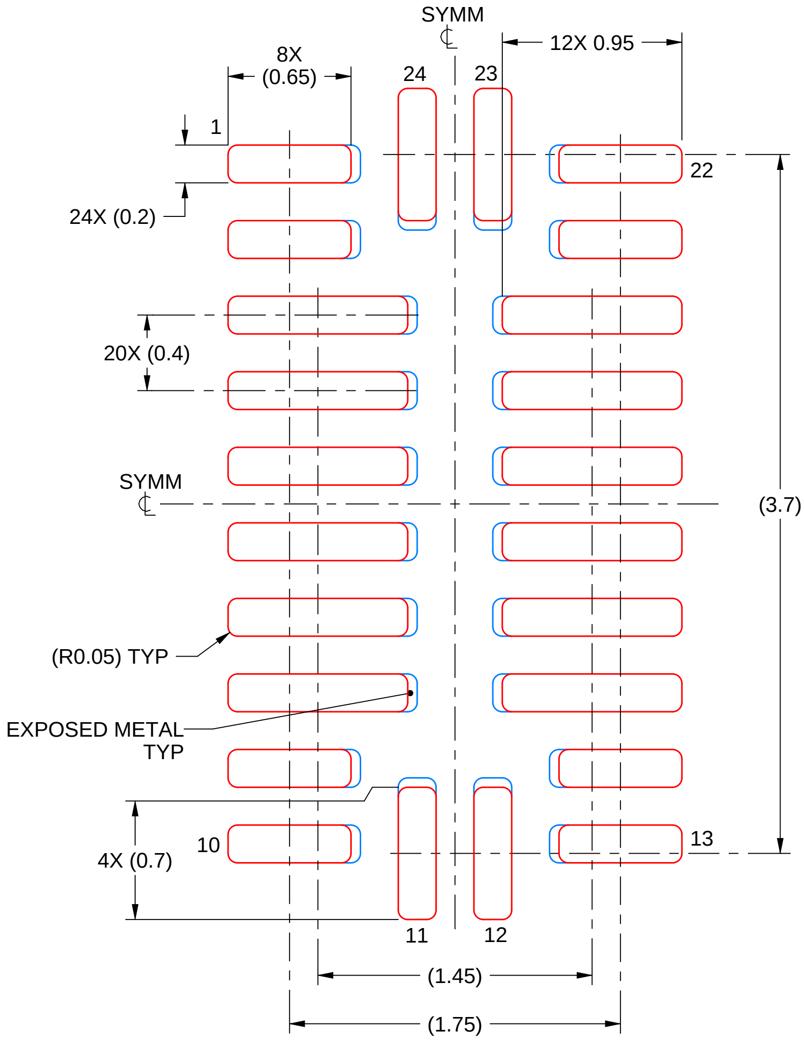
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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