MEMORY STICK™ INTERCONNECT EXTENDER CHIPSET WITH LVDS SN65LVDT14—ONE DRIVER PLUS FOUR RECEIVERS SN65LVDT41—FOUR DRIVERS PLUS ONE RECEIVER

FEATURES

- Integrated 110-Ω Nominal Receiver Line Termination Resistor
- Operates From a Single 3.3-V Supply
- Greater Than 125 Mbps Data Rate
- Flow-Through Pin-Out
- LVTTL Compatible Logic I/Os
- ESD Protection On Bus Pins Exceeds 16 kV
- Meets or Exceeds the Requirements of ANSI/TIA/EIA-644A Standard for LVDS
- 20-Pin PW Thin Shrink Small-Outline Package With 26-Mil Terminal Pitch

APPLICATIONS

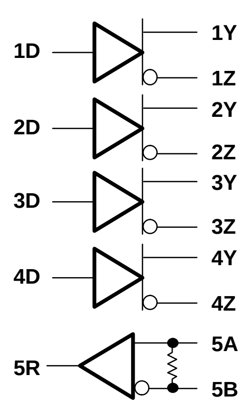
- Memory Stick Interface Extensions With Long Interconnects Between Host and Memory Stick™
- Serial Peripheral Interface™ (SPI) Interface Extension to Allow Long Interconnects Between Master and Slave
- MultiMediaCard™ Interface in SPI Mode
- General-Purpose Asymmetric Bidirectional Communication

DESCRIPTION

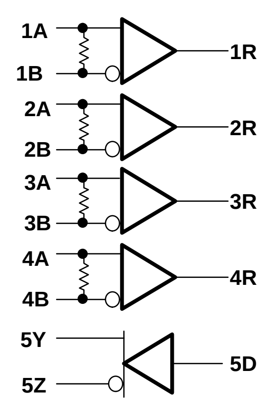
The SN65LVDT14 combines one LVDS line driver with four terminated LVDS line receivers in one package. It is designed to be used at the Memory Stick end of an LVDS based Memory Stick interface extension.

The SN65LVDT41 combines four LVDS line drivers with a single terminated LVDS line receiver in one package. It is designed to be used at the host end of an LVDS based Memory Stick interface extension.

SN65LVDT41 LOGIC DIAGRAM (POSITIVE LOGIC)

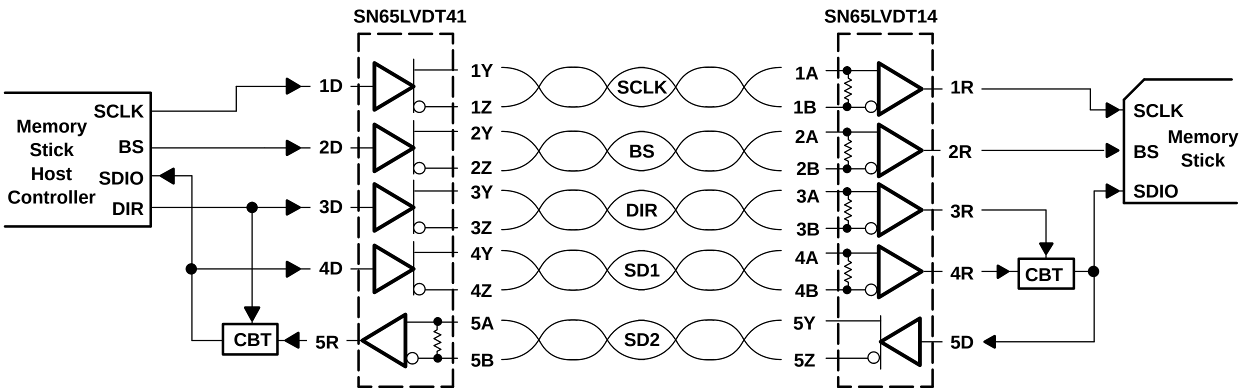


SN65LVDT14 LOGIC DIAGRAM (POSITIVE LOGIC)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL MEMORY STICK INTERFACE EXTENSION



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		SN65LVDT14, SN65LVDT41	UNIT
Supply voltage range(2)	V_{CC}	-0.5 to 4	V
Input voltage range	D or R	-0.5 to 6	V
	A, B, Y, or Z	-0.5 to 4	V
Electrostatic discharge	Human body model(3), A, B, Y, Z, and GND	±16	KV
	Human body model(3), all pins	±8	KV
	Charged device model(4), all pins	±500	V
Continuous total power dissipation		See Dissipation Rating Table	
Storage temperature range		-65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

PACKAGE DISSIPATION RATINGS

PACKAGE	T_A <25°C POWER RATING	OPERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
PW	774 mW	6.2 mW/°C	402 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage, See Figure 1	$\frac{\|V_{ID}\|}{2}$		$2.4 - \frac{\|V_{ID}\|}{2}$	V
				V_{CC} - 0.8	V
T_A	Operating free-air temperature	-40		85	°C

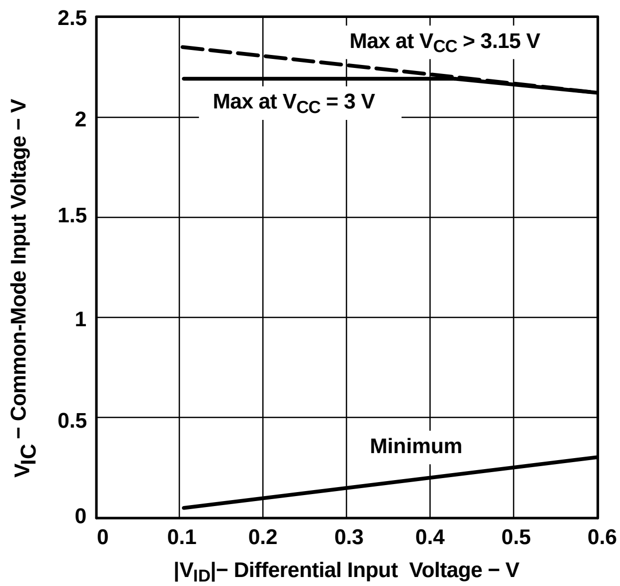


Figure 1. V_{IC} vs V_{ID} and V_{CC}

RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 2 and Table 1			100	mV
V_{ITH-}	Negative-going differential input voltage threshold		-100			
V_{OH}	High-level output voltage	I_{OH} = -8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (A or B inputs)	V_I = 0 V and V_I = 2.4 V, other input open			±40	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0 V, V_I = 2.4 V			±40	µA
C_i	Input capacitance, A or B input to GND	V_I = A sin 2πft + CV		5		pF
Z_t	Termination impedance	V_{ID} = 0.4 sin2.5E09 t V	88		132	Ω

(1) All typical values are at 25°C and with a 3.3-V supply.

DRIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 3 and Figure 5	247	340	454	mV
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage magnitude between logic states		-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 6	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{IH}	High-level input current	V_{IH} = 2 V			20	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			10	μA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±24	mA
		V_{OD} = 0 V			±12	
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V			±1	μA

(1) All typical values are at 25°C and with a 3.3-V supply.

DEVICE ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	SN65LVDT14	Driver R_L = 100 Ω, Driver V_I = 0.8 V or 2 V, Receiver V_I = ±0.4 V			25	mA
		SN65LVDT41				35	

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 4	1	2.6	3.8	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	2.6	3.8	ns
t_r	Output signal rise time		0.15		1.2	ns
t_f	Output signal fall time		0.15		1.2	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL}$ - $t_{PLH}\rvert$)			150	600	ps
$t_{sk(o)}$	Output skew(1)			100	400	ps
$t_{sk(pp)}$	Part-to-part skew(2)				1	ns

(1) $t_{sk(o)}$ is the magnitude of the time difference between the t_{pLH} or t_{pHL} of all the receivers of a single device with all of their inputs connected together.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

DRIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 7	0.9	1.7	2.9	ns
t_{PHL}	Propagation delay time, high-to-low-level output		0.9	1.6	2.9	
t_r	Differential output signal rise time		0.26		1	
t_f	Differential output signal fall time		0.26		1	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL}$ - $t_{PLH}\|$)	R_L = 100 Ω, C_L = 10 pF, See Figure 7		150	500	ps
$t_{sk(o)}$	Output skew(1)			80	150	ps
$t_{sk(pp)}$	Part-to-part skew(2)				1.5	ns

(1) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

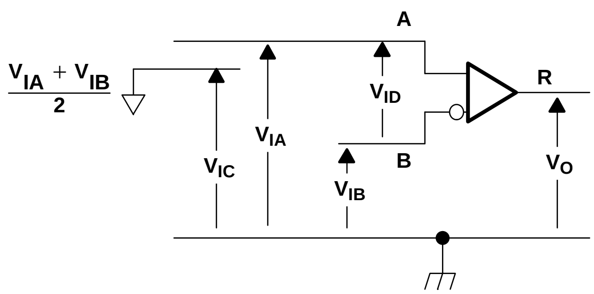


Figure 2. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0.0 V	100 mV	0.05 V
0.0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0.0 V	600 mV	0.3 V
0.0 V	0.6 V	-600 mV	0.3 V

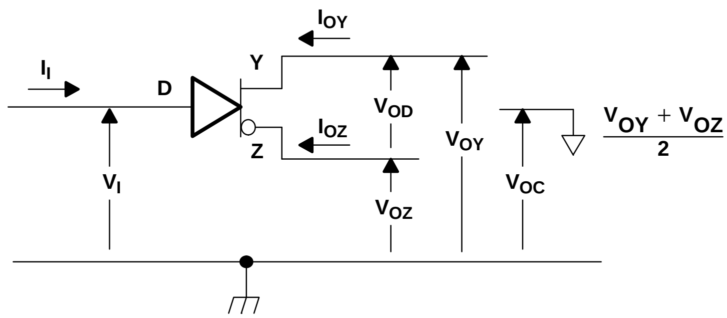
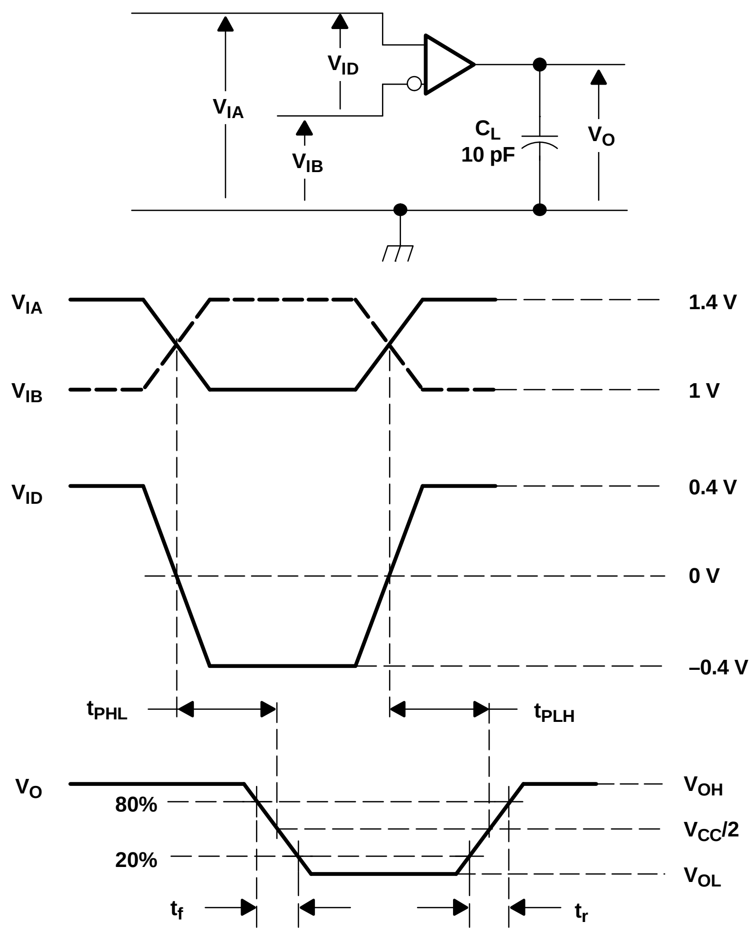


Figure 3. Driver Voltage and Current Definitions



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ± 0.05 µs. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 4. Receiver Timing Test Circuit and Waveforms

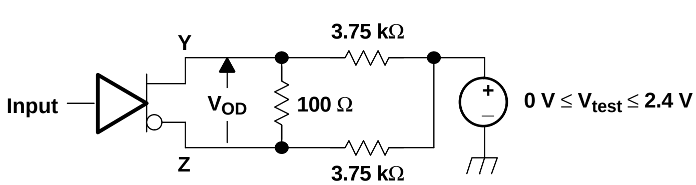
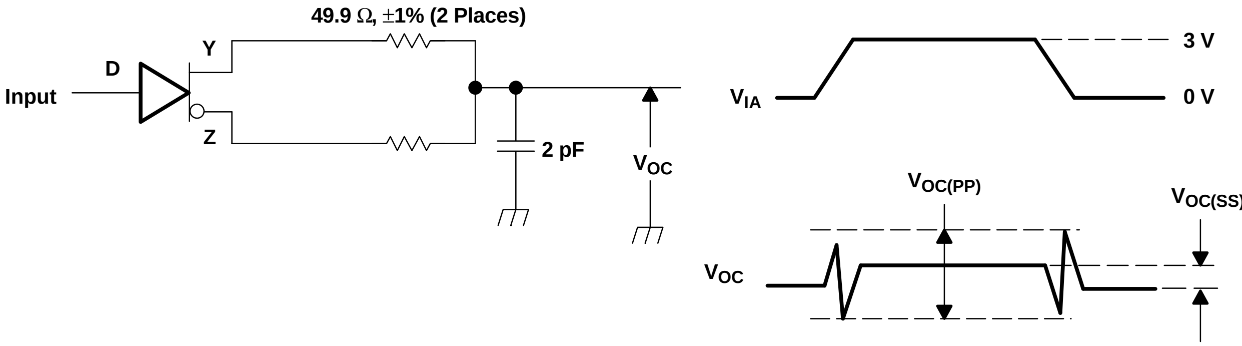
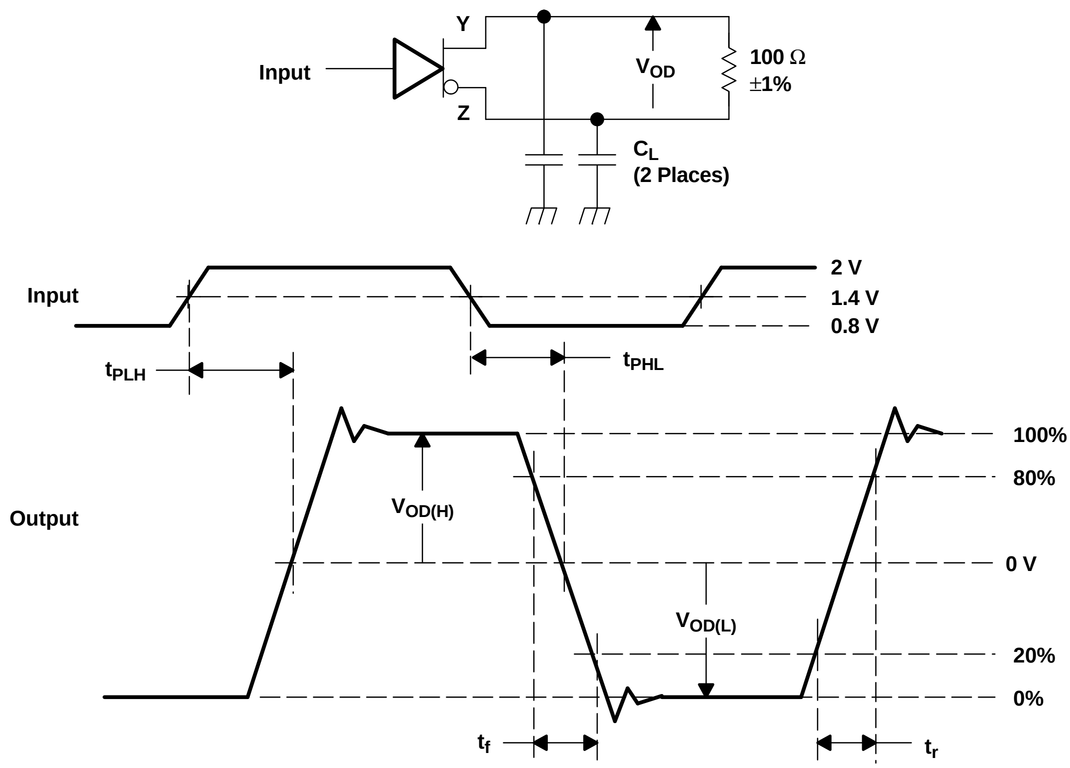


Figure 5. Driver VDO Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

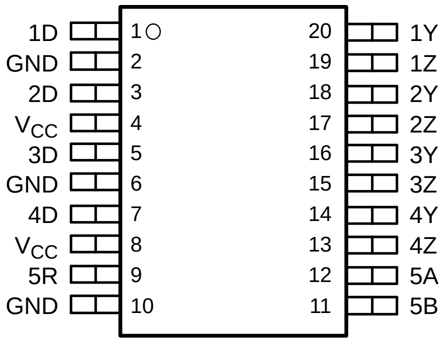
Figure 6. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



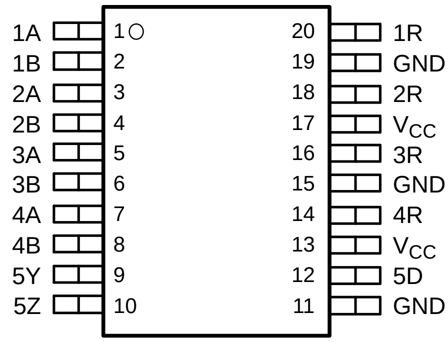
A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ± 0.05 µs. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 7. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

SN65LVDT41 (Marked as LVDT41)



SN65LVDT14 (Marked as LVDT14)



Function Tables

RECEIVER

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

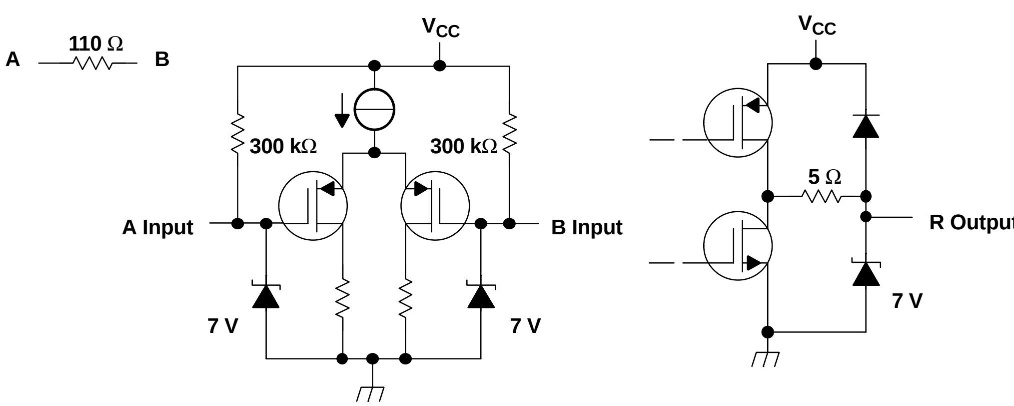
H = high level, L = low level , ? = indeterminate

DRIVER

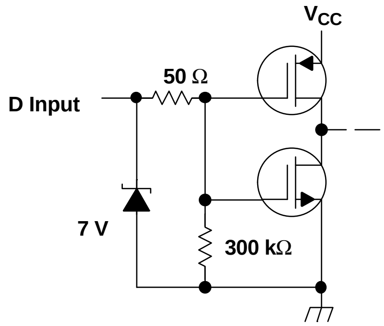
INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

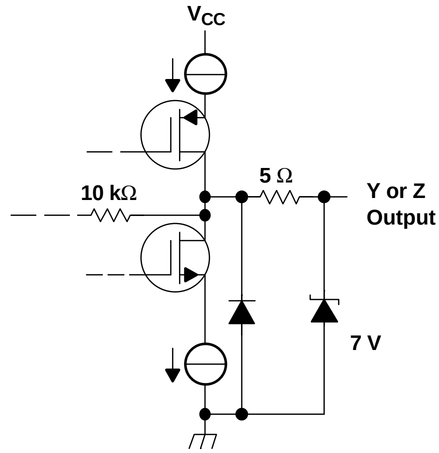
H = high level, L = low level

RECEIVER EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



DRIVER EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS





TYPICAL CHARACTERISTICS

RECEIVER

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

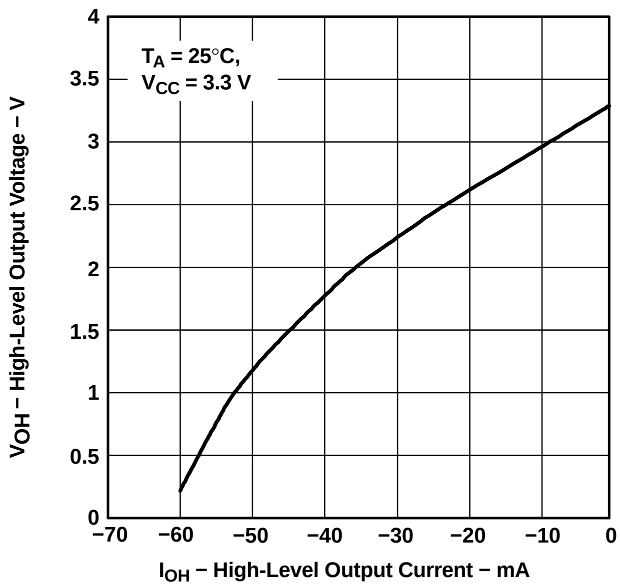


Figure 8.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

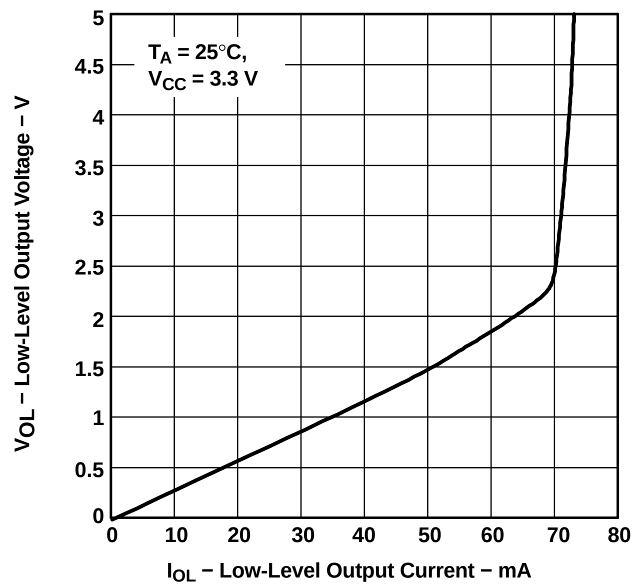


Figure 9.

RECEIVER (continued)

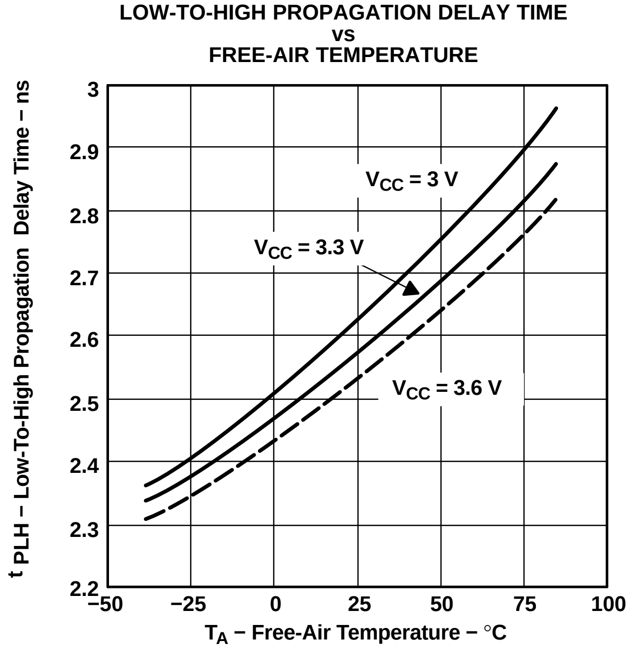


Figure 10.

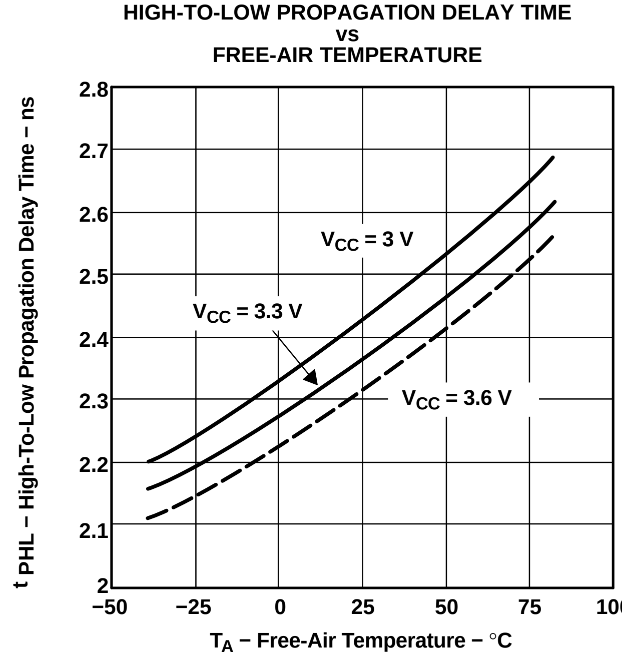


Figure 11.

DRIVER

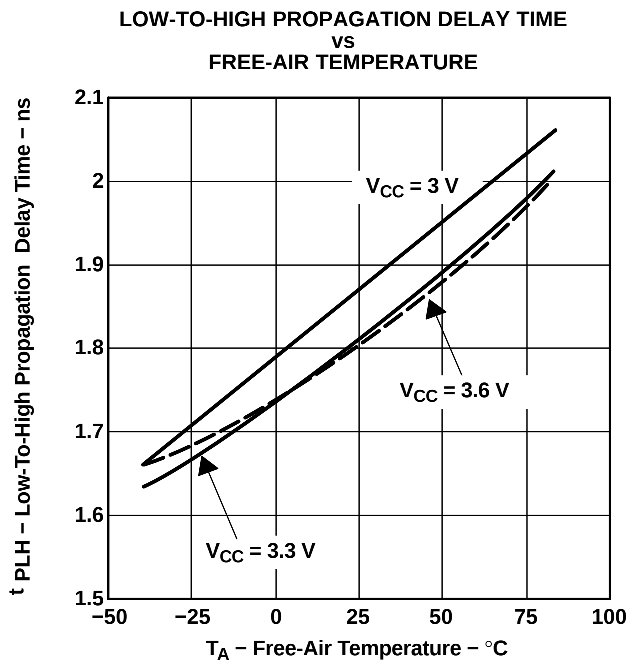


Figure 12.

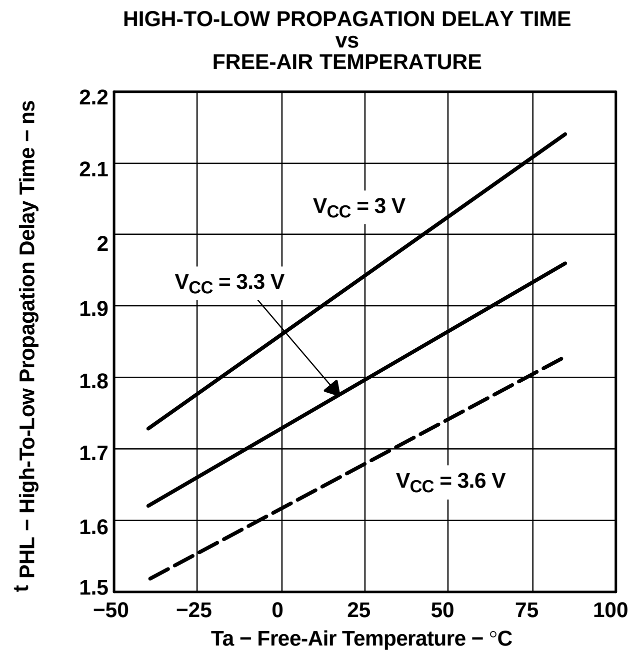


Figure 13.

APPLICATION INFORMATION

EXTENDING THE MEMORY STICK INTERFACE USING LVDS SIGNALING OVER DIFFERENTIAL TRANSMISSION CABLES

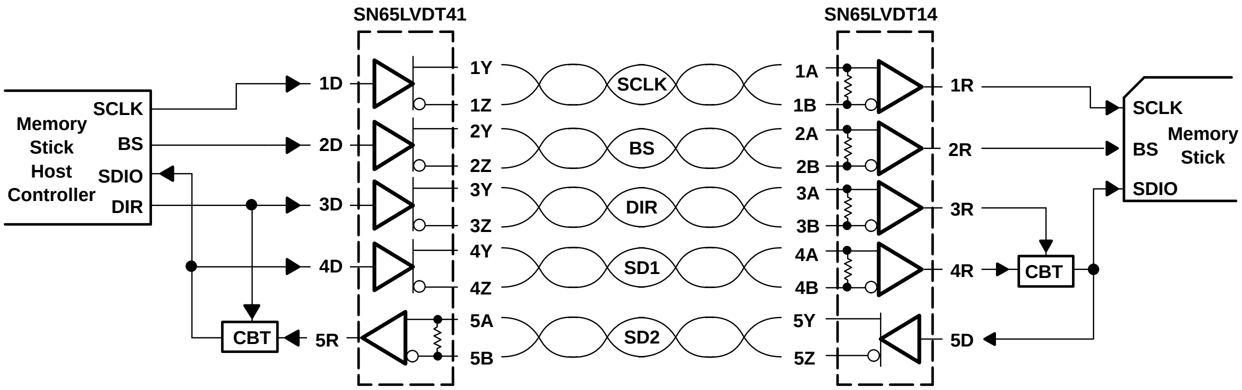


Figure 14. System Level Block Diagram

The Memory Stick signaling interface operates in a master-slave architecture, with three active signal lines. The host (master) supplies a clock (SCLK) and bus-state (BS) signal to control the operation of the system. The SCLK and BS signals are unidirectional (simplex) from the host to the Memory Stick. The serial data input-output (SDIO) signal is a bidirectional (half-duplex) signal used to communicate both control and data information between the host and the Memory Stick. The direction of data control is managed by the host through a combination of BS line states and control information delivered to the Memory Stick.

The basic Memory Stick interface is capable of operating only over short distances due to the single-ended nature of the digital I/O signals. Such a configuration is entirely suitable for compact and portable devices where there is little if any separation between the host and the Memory Stick. In applications where a greater distance is needed between the host controller and the Memory Stick, it is necessary to utilize a different signaling method such as low voltage differential signaling, or LVDS.

LVDS, as specified by the TIA/EIA-644-A standard, provides several benefits when compared to alternative long-distance signaling technologies: low radiated emissions, high noise immunity, low power consumption, inexpensive interconnect cables.

This device pair provides the necessary LVDS drivers and receivers specifically targeted at implementing a Memory Stick interconnect extension. It utilizes simplex links for the SCLK and BS signals, and two simplex links for the SDIO data. The half-duplex SDIO data is split into two simplex streams under control of the host processor by means of the direction (DIR) signal. The DIR signal is also carried from the host to the Memory Stick on a simplex LVDS link.

The switching of the SDIO signal flow direction in the single-ended interfaces is managed by electronic switch devices, identified by the CBT symbol in Figure 14. A suggested CBT device for this application is the SN74CBTLV1G125 from Texas Instruments Incorporated. These devices are available in space saving SOT-23 or SC-70 packages.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDT14PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT14PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT14PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT14PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT41PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT41PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT41PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDT41PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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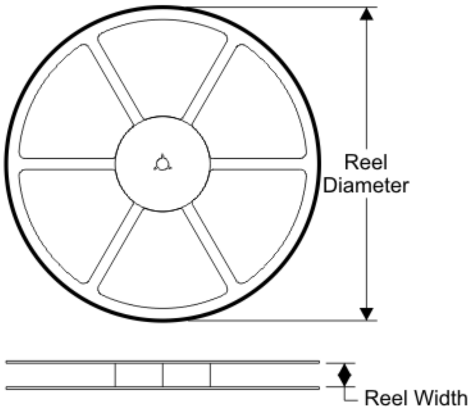
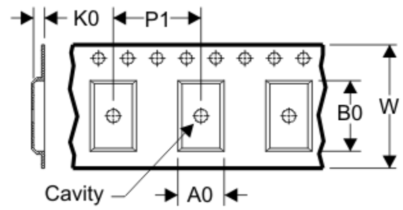
TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

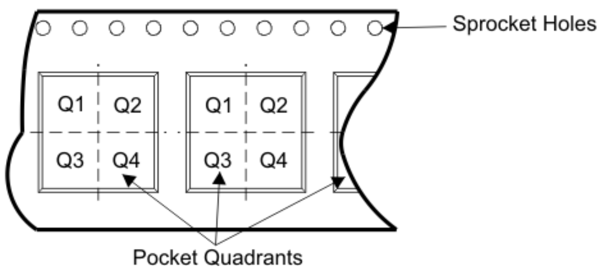


TAPE DIMENSIONS



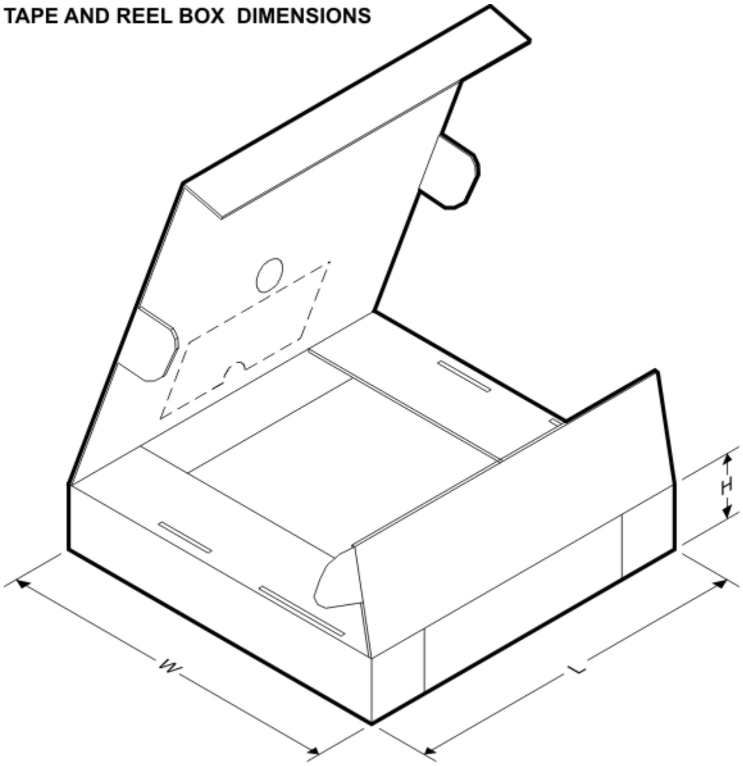
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDT14PWR	PW	20	SITE 41	330	16	6.95	7.1	1.6	8	16	Q1
SN65LVDT14PWR	PW	20	SITE 60	330	16	6.95	7.1	1.6	8	16	Q1
SN65LVDT41PWR	PW	20	SITE 41	330	16	6.95	7.1	1.6	8	16	Q1
SN65LVDT41PWR	PW	20	SITE 60	330	16	6.95	7.1	1.6	8	16	Q1

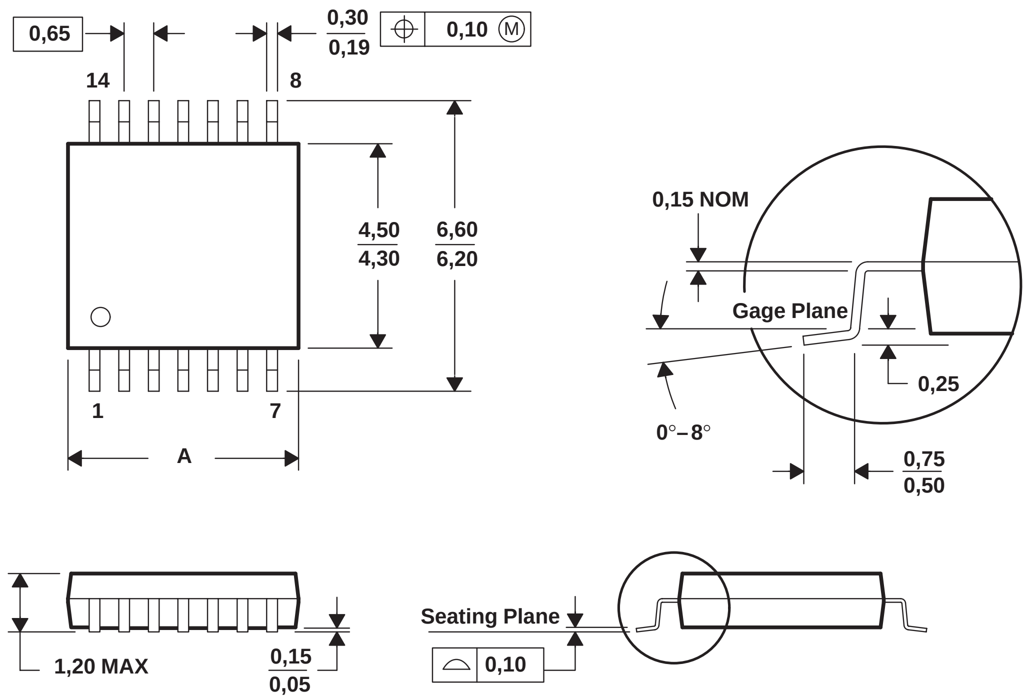
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65LVDT14PWR	PW	20	SITE 41	346.0	346.0	33.0
SN65LVDT14PWR	PW	20	SITE 60	346.0	346.0	33.0
SN65LVDT41PWR	PW	20	SITE 41	346.0	346.0	33.0
SN65LVDT41PWR	PW	20	SITE 60	346.0	346.0	33.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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