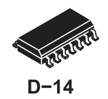
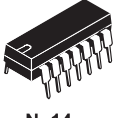
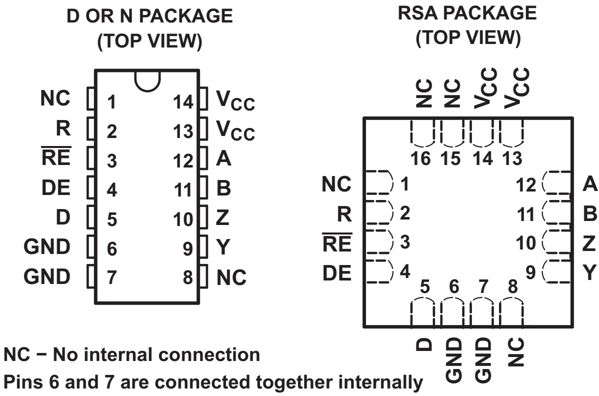




LOW-POWER RS-485 LINE DRIVER AND RECEIVER PAIRS

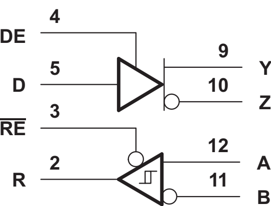
FEATURES

- **Designed for High-Speed Multipoint Data Transmission Over Long Cables**
- **Operate With Pulse Durations as Low as 30 ns**
- **Low Supply Current . . . 5 mA Max**
- **Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **3-State Outputs for Party-Line Buses**
- **Common-Mode Voltage Range of –7 V to 12 V**
- **Thermal Shutdown Protection Prevents Driver Damage From Bus Contention**
- **Positive and Negative Output Current Limiting**
- **Pin Compatible With the SN75ALS180**



NC − No internal connection
Pins 6 and 7 are connected together internally
Pins 13 and 14 are connected together internally

logic diagram (positive logic)



DESCRIPTION

The SN55LBC180, SN65LBC180 and SN75LBC180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that meet or exceed the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). These devices are designed using TI's proprietary LinBiCMOS™ with the low-power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER	PART MARKING
0°C to 70°C	PDIP	SN75LBC180N	SN75LBC180N
	SOIC	SN75LBC180D	7LB180
	QFN	SN75LBC180RSA	LB180
–40°C to 85°C	PDIP	SN65LBC180N	65LBC180N
	SOIC	SN65LBC180D	6LB180
	QFN	SN65LBC180RSA	BL180
–55°C to 125°C	QFN	SN55LBC180RSA	SN55LBC180

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
LinBiCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1994–2009, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The SN55LBC180, SN65LBC180 and SN75LBC180 combine a differential line driver and receiver with 3-state outputs and operate from a single 5-V supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus whether disabled or powered off (V_{CC} = 0). These parts feature a wide common-mode voltage range making them suitable for point-to-point or multipoint data-bus applications.

The devices also provide positive and negative output-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

The SN75LBC180 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC180 is characterized over the industrial temperature range of –40°C to 85°C.

The SN55LBC180 is characterized for operation over the military temperature range of –55°C to 125°C.

FUNCTION TABLES(1)

DRIVER			
INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER		
DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
V_{ID} ≥ 0.2 V	L	H
–0.2 V < V_{ID} < 0.2 V	L	?
V_{ID} ≤ –0.2 V	L	L
X	H	Z
Open circuit	L	H

(1) H = high level, L = low level, ? = Indeterminate, X = irrelevant, Z = high impedance (off)

Copyright © 1994–2009, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS[1]

				UNIT
V_{CC}	Supply voltage range [2]		–0.3 to 7	V
V_{BUS}	Bus voltage range (A, B, Y, Z)[2]		–10 to 15	V
	Voltage range at D, R, DE, $\overline{RE}$[2]		–0.3 to V_{CC} + 0.5	V
	Continuous total power dissipation[3]		Internally limited	
	Total power dissipation		See Dissipation Rating Table	
T_{stg}	Storage temperature range		–65 to 150	°C
I_O	Receiver output current range		–50 to 50	mA
ESD	Electrostatic discharge	HBM (Human Body Model) EIA/JESD22-A114	±4	kV
		MM (Machine Model) EIA/JESD22-A115	400	V
		CDM (Charge Device Model) EIA/JESD22-C101	1.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE[1]	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—
RSA	3333 mW	26.67 mW/°C	2133 mW	1733 mW	400 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage		–6[1]		6	V
V_O, V_I, or V_{IC}	Voltage at any bus terminal (separately or common mode)	A, B, Y, or Z	–7[1]		12	V
I_{OH}	High-level output current	Y or Z			–60	mA
		R			–8	
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_A	Operating free-air temperature	SN55LBC180	–55		125	°C
		SN65LBC180	–40		85	
		SN75LBC180	0		70	

(1) The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.

Copyright © 1994–2009, Texas Instruments Incorporated

DRIVER SECTION

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

<table>
<tr><th colspan="2">PARAMETER</th><th colspan="2">TEST CONDITIONS</th><th>MIN</th><th>TYP(1)</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>V_{IK}</td><td>Input clamp voltage</td><td colspan="2">I_I = -18 mA</td><td></td><td></td><td>–1.5</td><td>V</td></tr>
<tr><td rowspan="6">| V_{OD} |</td><td rowspan="6">Differential output voltage magnitude(2)</td><td rowspan="3">R_L = 54 Ω, See Figure 1</td><td>SN55LBC180</td><td>1</td><td>2.5</td><td>5</td><td rowspan="6">V</td></tr>
<tr><td>SN65LBC180</td><td>1.1</td><td>2.5</td><td>5</td></tr>
<tr><td>SN75LBC180</td><td>1.5</td><td>2.5</td><td>5</td></tr>
<tr><td rowspan="3">R_L = 60 Ω, See Figure 2</td><td>SN55LBC180</td><td>1</td><td>2.5</td><td>5</td></tr>
<tr><td>SN65LBC180</td><td>1.1</td><td>2</td><td>5</td></tr>
<tr><td>SN75LBC180</td><td>1.5</td><td>2</td><td>5</td></tr>
<tr><td>Δ| V_{OD} |</td><td>Change in magnitude of differential output voltage(3)</td><td colspan="2">See Figure 1 and Figure 2</td><td></td><td></td><td>±0.2</td><td>V</td></tr>
<tr><td>V_{OC}</td><td>Common-mode output voltage</td><td rowspan="2">R_L = 54 Ω,</td><td rowspan="2">See Figure 1</td><td>1</td><td>2.5</td><td>3</td><td>V</td></tr>
<tr><td>Δ| V_{OC} |</td><td>Change in magnitude of common-mode output voltage(3)</td><td></td><td></td><td>±0.2</td><td>V</td></tr>
<tr><td>I_O</td><td>Output current with power off</td><td>V_{CC} = 0,</td><td>V_O = –7 V to 12 V</td><td></td><td></td><td>±100</td><td>μA</td></tr>
<tr><td>I_{OZ}</td><td>High-impedance-state output current</td><td colspan="2">V_O = –7 V to 12 V</td><td></td><td></td><td>±100</td><td>μA</td></tr>
<tr><td>I_{IH}</td><td>High-level input current</td><td colspan="2">V_I = 2.4 V</td><td></td><td></td><td>100</td><td>μA</td></tr>
<tr><td>I_{IL}</td><td>Low-level input current</td><td colspan="2">V_I = 0.4 V</td><td></td><td></td><td>100</td><td>μA</td></tr>
<tr><td>I_{OS}</td><td>Short-circuit output current</td><td colspan="2">–7 V ≤ V_O ≤ 12 V</td><td></td><td></td><td>±250</td><td>mA</td></tr>
<tr><td rowspan="2">I_{CC}</td><td rowspan="2">Supply current</td><td rowspan="2">Receiver disabled</td><td>Outputs enabled</td><td></td><td></td><td>5</td><td rowspan="2">mA</td></tr>
<tr><td>Outputs disabled</td><td></td><td></td><td>3</td></tr>
</table>

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The minimum V_{OD} specification may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.
(3) Δ|V_{OD}| and Δ|V_{OC}| are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C

<table>
<tr><th colspan="2">PARAMETER</th><th colspan="2">TEST CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>$t_{d(OD)}$</td><td>Differential output delay time</td><td rowspan="2">R_L = 54 Ω,</td><td rowspan="2">See Figure 3</td><td>7</td><td>12</td><td>18</td><td>ns</td></tr>
<tr><td>$t_{t(OD)}$</td><td>Differential output transition time</td><td>5</td><td>10</td><td>20</td><td>ns</td></tr>
<tr><td>t_{PZH}</td><td>Output enable time to high level</td><td>R_L = 110 Ω,</td><td>See Figure 4</td><td></td><td></td><td>35</td><td>ns</td></tr>
<tr><td>t_{PZL}</td><td>Output enable time to low level</td><td>R_L = 110 Ω,</td><td>See Figure 5</td><td></td><td></td><td>35</td><td>ns</td></tr>
<tr><td>t_{PHZ}</td><td>Output disable time from high level</td><td>R_L = 110 Ω,</td><td>See Figure 4</td><td></td><td></td><td>50</td><td>ns</td></tr>
<tr><td>t_{PLZ}</td><td>Output disable time from low level</td><td>R_L = 110 Ω,</td><td>See Figure 5</td><td></td><td></td><td>35</td><td>ns</td></tr>
</table>

SWITCHING CHARACTERISTICS (SN55LBC180)

V_{CC} = 5 V, T_A = 25°C

<table>
<tr><th colspan="2">PARAMETER</th><th colspan="2">TEST CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNIT</th></tr>
<tr><td>$t_{d(OD)}$</td><td>Differential output delay time</td><td rowspan="2">R_L = 54 Ω,</td><td rowspan="2">See Figure 3</td><td></td><td>15</td><td></td><td>ns</td></tr>
<tr><td>$t_{t(OD)}$</td><td>Differential output transition time</td><td></td><td>21</td><td></td><td>ns</td></tr>
<tr><td>t_{PZH}</td><td>Output enable time to high level</td><td rowspan="2">R_L = 110 Ω,</td><td rowspan="2">See Figure 4</td><td></td><td>32</td><td></td><td rowspan="2">ns</td></tr>
<tr><td>t_{PHZ}</td><td>Output disable time from high level</td><td></td><td>55</td><td></td></tr>
<tr><td>t_{PZL}</td><td>Output enable time to low level</td><td rowspan="2">R_L = 110 Ω,</td><td rowspan="2">See Figure 5</td><td></td><td>32</td><td></td><td rowspan="2">ns</td></tr>
<tr><td>t_{PLZ}</td><td>Output disable time from low level</td><td></td><td>20</td><td></td></tr>
</table>

Copyright © 1994–2009, Texas Instruments Incorporated

RECEIVER SECTION

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		–0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})				45		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA		-1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA		0.3	0.5	V
I_{OZ}	High-impedance-state output current	V_O = 0 V to V_{CC}				±20	µA
I_{IH}	High-level enable-input current	V_{IH} = 2.4 V		–50			A
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V		–100			µA
I_I	Bus input current	V_I = 12 V, V_{CC} = 5 V,	Other input at 0 V		0.7	1	mA
		V_I = 12 V, V_{CC} = 0 V,	Other input at 0 V		0.8	1	
		V_I = -7 V, V_{CC} = 5 V,	Other input at 0 V	–0.8	-0.5		
		V_I = -7 V, V_{CC} = 0 V,	Other input at 0 V	–0.8	–0.5		
I_{CC}	Supply current	Driver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 6	11	22	33	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	33	ns
$t_{sk(p)}$	Pulse skew (| t_{PHL} – t_{PLH}|)			3	6	ns
t_t	Transition time			5	8	ns
t_{PZH}	Output enable time to high level	See Figure 7			35	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level				35	ns
t_{PLZ}	Output disable time from low level				30	ns

SWITCHING CHARACTERISTICS (SN55LBC180)

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 6		26		ns
t_{PLH}	Propagation delay time, low- to high-level output			23		ns
$t_{sk(p)}$	Pulse skew (| t_{PHL} – t_{PLH}|)			3		ns
$t_{sk(p)t}$	Transition time			4		ns
t_{PZH}	Output enable time to high level	See Figure 4		30		ns
t_{PHZ}	Output disable time from high level			26		ns
t_{PZL}	Output enable time to low level			30		ns
t_{PLZ}	Output disable time from low level			30		ns

Copyright © 1994–2009, Texas Instruments Incorporated

PARAMETER MEASUREMENT INFORMATION

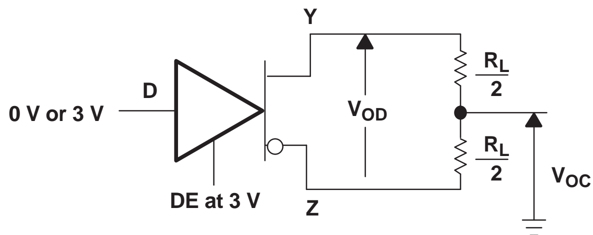


Figure 1. Differential and Common-Mode Output Voltages

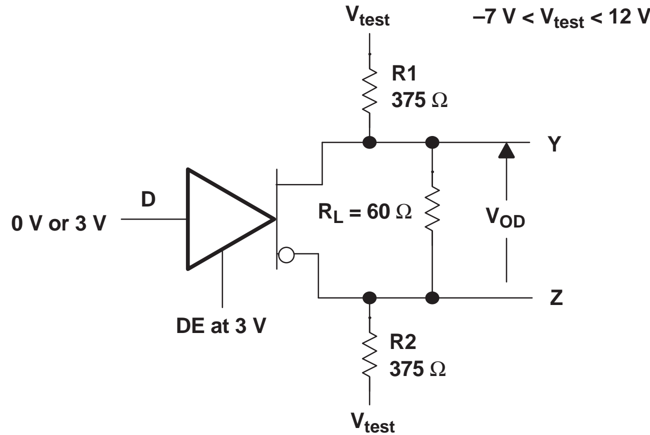
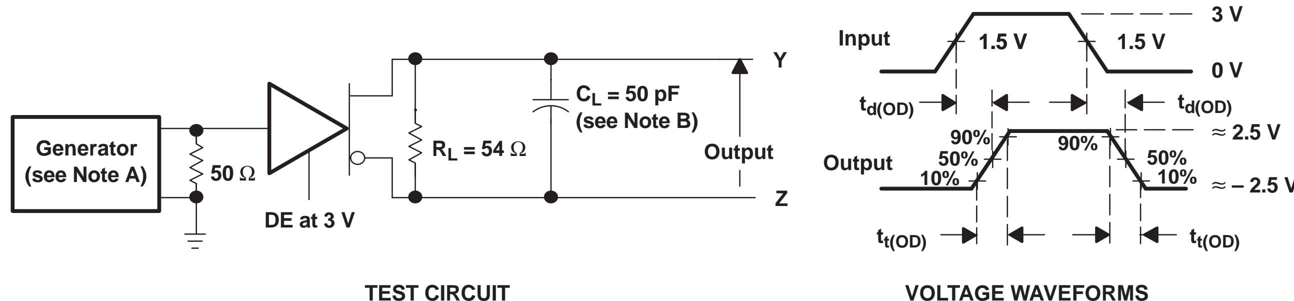


Figure 2. Driver V_{OD} Test Circuit



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms

Copyright © 1994–2009, Texas Instruments Incorporated

PARAMETER MEASUREMENT INFORMATION (continued)

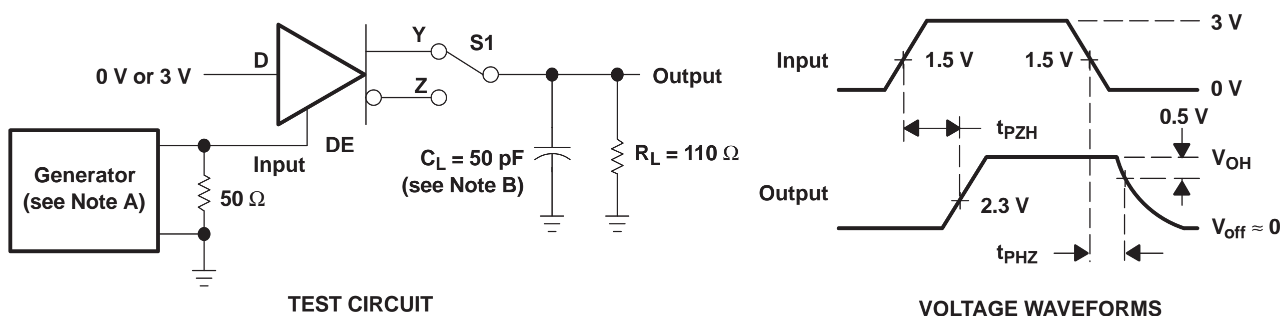


Figure 4. Driver Test Circuit and Enable and Disable Time Waveforms

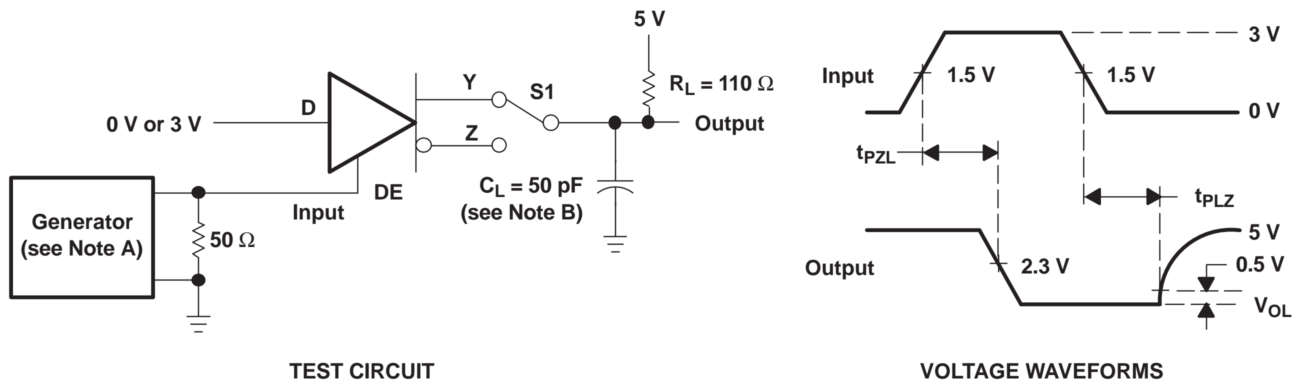
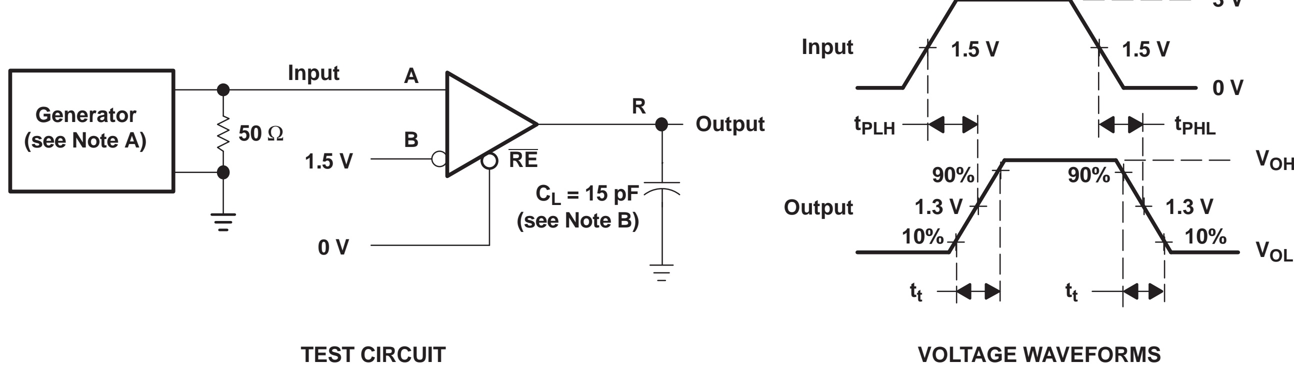


Figure 5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

1.5 V
– 1.5 V
S1
A
B
RE
R
Output
2 kΩ
S2
5 V
C_L = 15 pF
(see Note B)
5 kΩ
IN916 or Equivalent
(4 places)
Generator
(see Note A)
Input
50 Ω
S3

TEST CIRCUIT

Input
3 V
1.5 V
0 V
S1 to 1.5 V
S2 Open
S3 Closed
t_{PZH}
Output
V_{OH}
1.5 V
0 V

Input
3 V
1.5 V
0 V
S1 to – 1.5 V
S2 Closed
S3 Open
t_{PZL}
Output
≈ 4.5 V
1.5 V
V_{OL}

Input
3 V
1.5 V
0 V
S1 to 1.5 V
S2 Closed
S3 Closed
t_{PHZ}
Output
V_{OH}
≈ 1.3 V
0.5 V

Input
3 V
1.5 V
0 V
S1 to – 1.5 V
S2 Closed
S3 Closed
t_{PLZ}
Output
≈ 1.3 V
0.5 V
V_{OL}

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Output Enable and Disable Times

Copyright © 1994–2009, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS

SCHEMATICS OF INPUTS AND OUTPUTS

EQUIVALENT OF D, DE, AND $\overline{RE}$ INPUTS

V_{CC}
22 kΩ
Input

RECEIVER A INPUT

V_{CC}
100 kΩ NOM
3 kΩ NOM
18 kΩ NOM
Input
12 kΩ
1.1 kΩ NOM

RECEIVER B INPUT

V_{CC}
3 kΩ NOM
18 kΩ NOM
Input
100 kΩ NOM
12 kΩ
1.1 kΩ NOM

DRIVER OUTPUT

V_{CC}
Output

TYPICAL OF RECEIVER OUTPUT

V_{CC}
R Output

Copyright © 1994–2009, Texas Instruments Incorporated

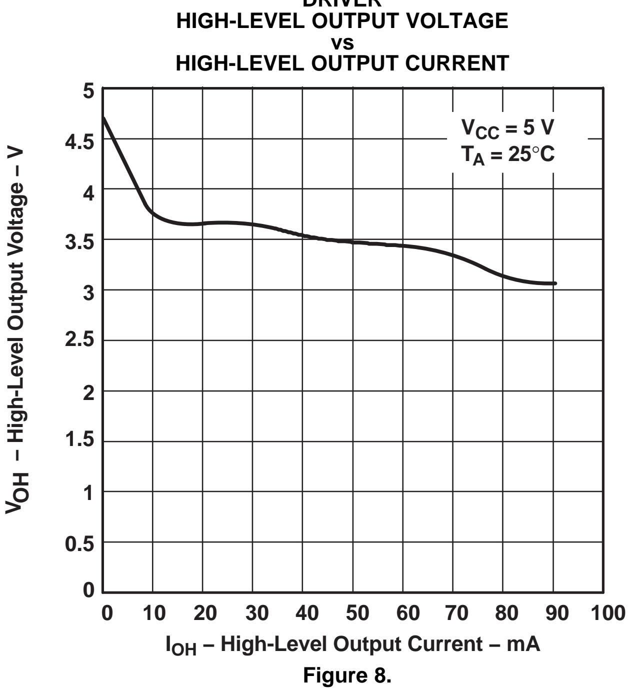


Figure 8.

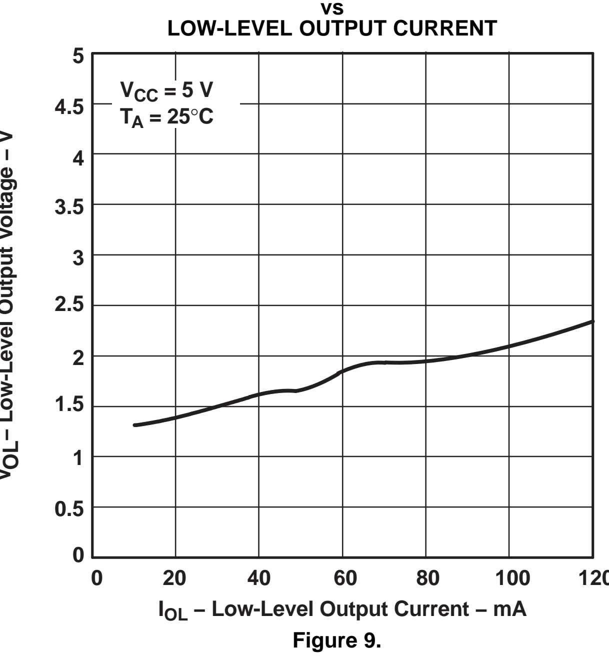


Figure 9.

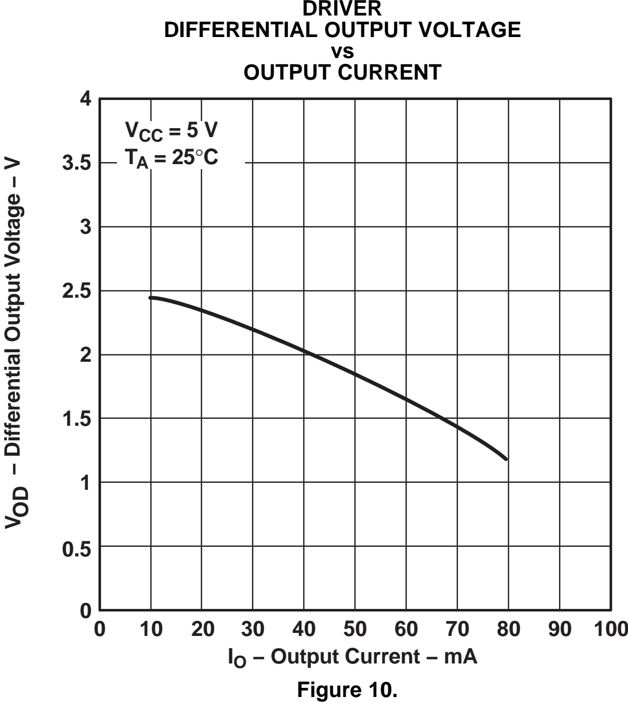


Figure 10.

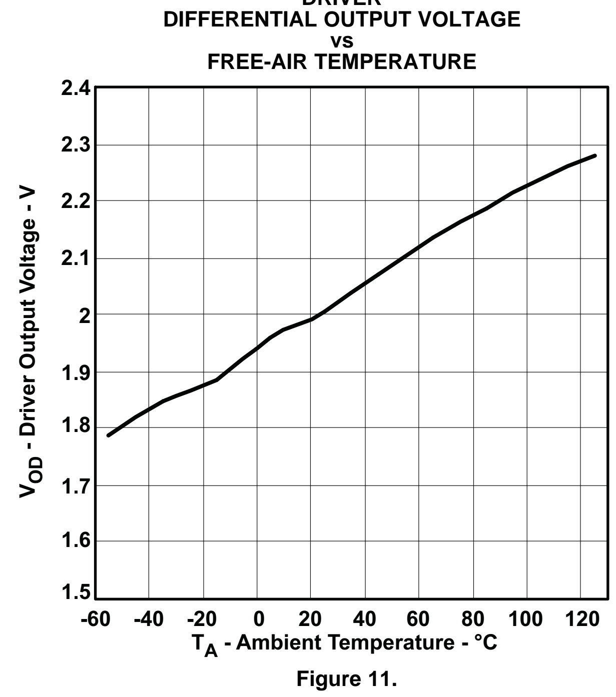


Figure 11.

Copyright © 1994–2009, Texas Instruments Incorporated

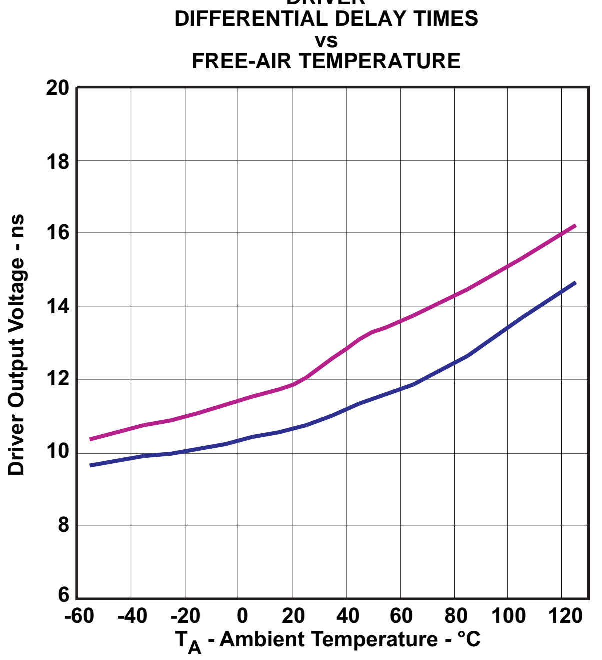


Figure 12.

DRIVER
OUTPUT CURRENT
vs
SUPPLY VOLTAGE

R_L = 54 Ω

I_{OL}

I_{OH}

I_O – Output Current – mA

V_{CC} – Supply Voltage – V

Figure 13.

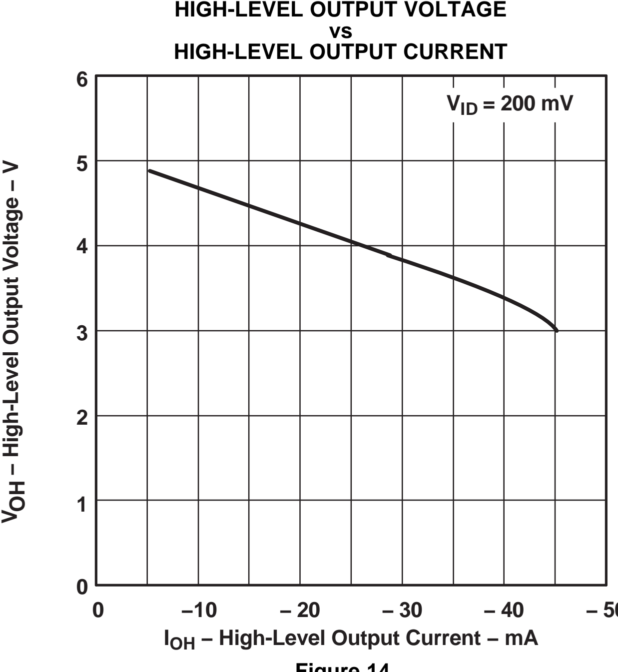


Figure 14.

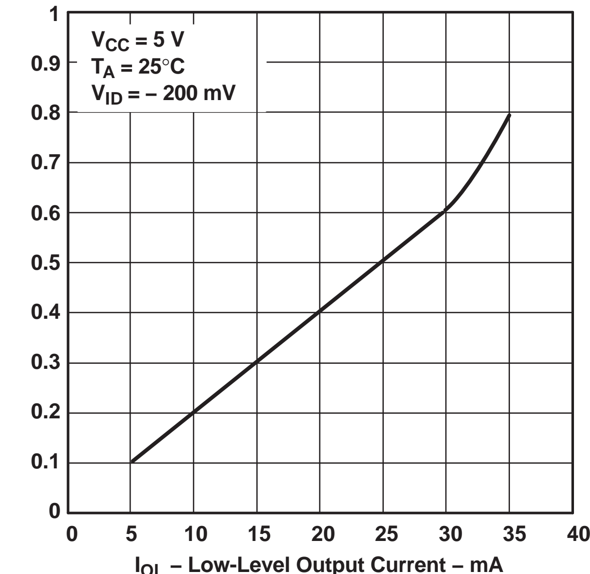


Figure 15.

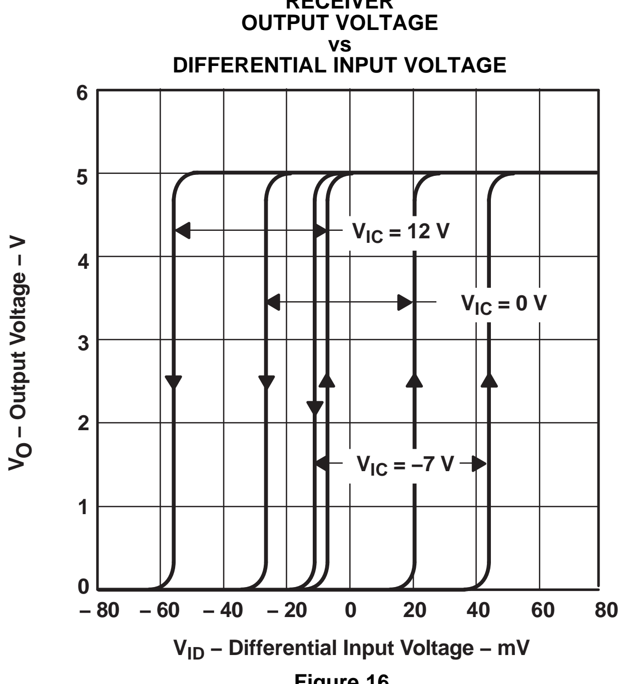


Figure 16.

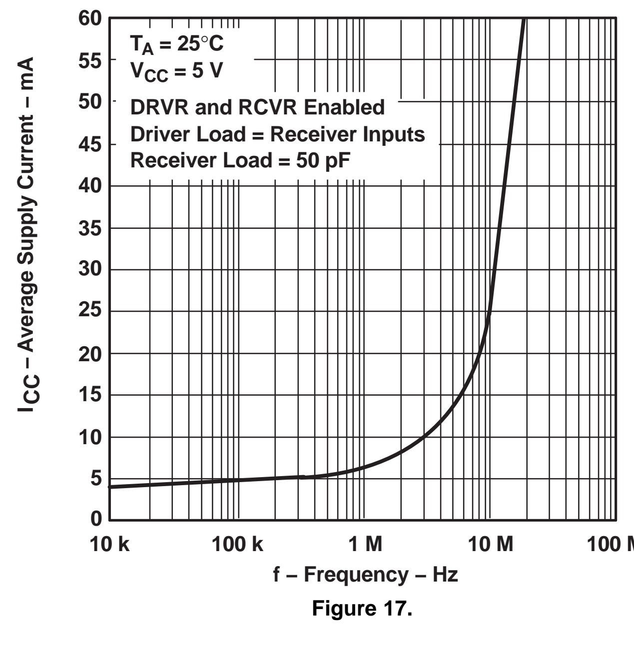


Figure 17.

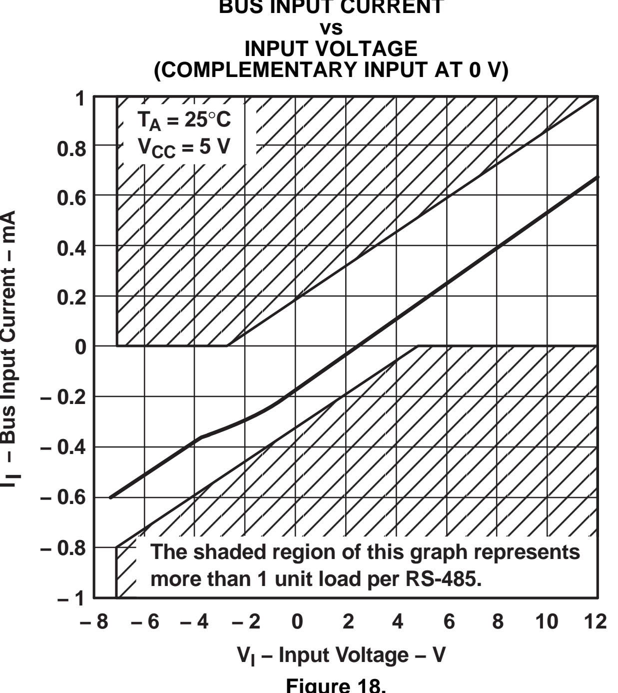


Figure 18.

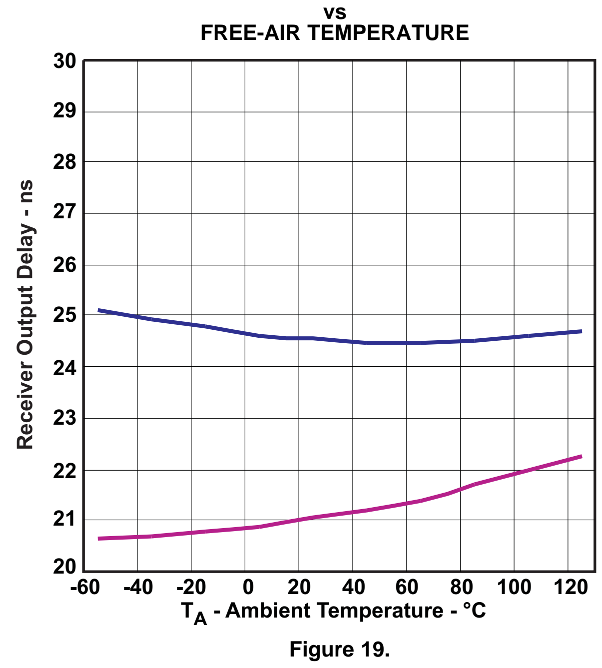


Figure 19.

Copyright © 1994–2009, Texas Instruments Incorporated

APPLICATION INFORMATION

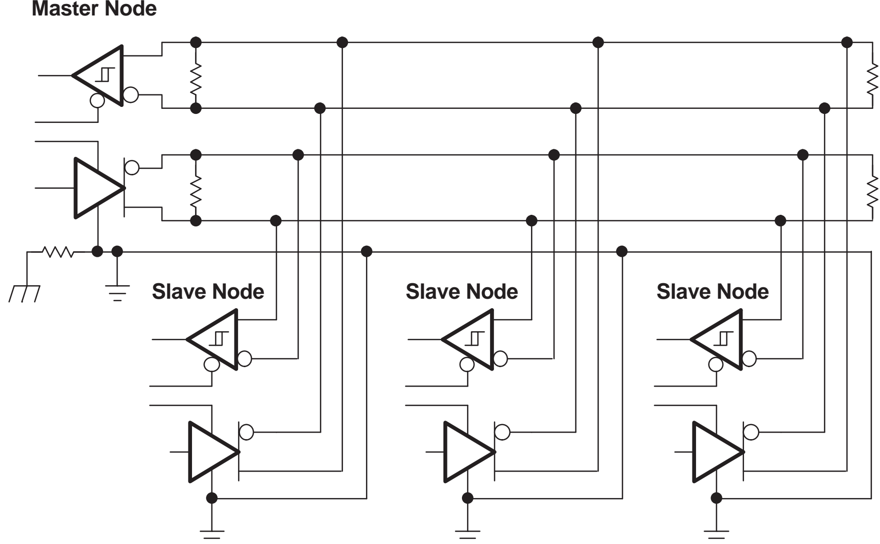


Figure 20. Full Duplex Application Circuit

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN55LBC180RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN55LBC180RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LBC180D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC180DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC180DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC180DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC180N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC180NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC180RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LBC180RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LBC180RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LBC180RSATG4	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC180D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC180NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC180RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC180RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC180RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC180RSATG4	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55LBC180, SN65LBC180, SN75LBC180 :

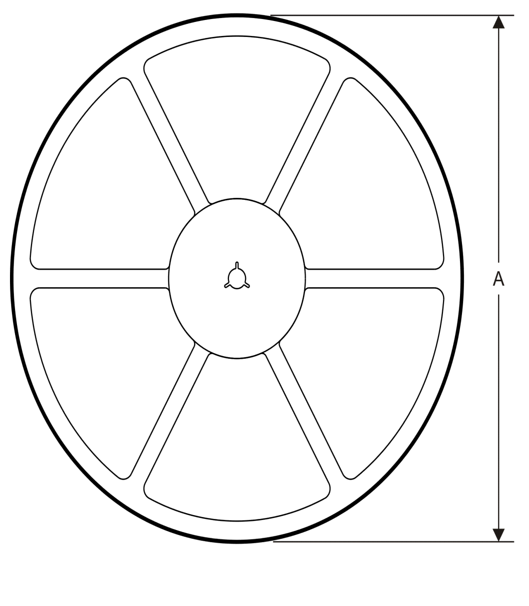
- Automotive: SN65LBC180-Q1

NOTE: Qualified Version Definitions:

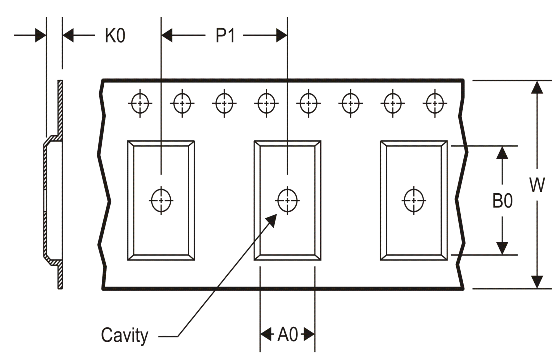
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



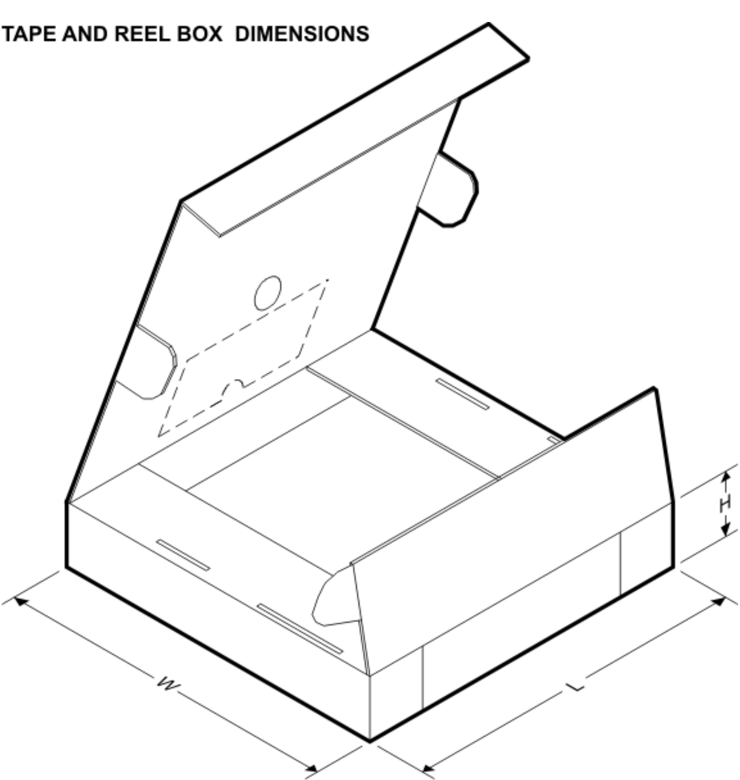
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55LBC180RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN55LBC180RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LBC180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65LBC180RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LBC180RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LBC180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75LBC180RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LBC180RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55LBC180RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
SN55LBC180RSAT	QFN	RSA	16	250	210.0	185.0	35.0
SN65LBC180DR	SOIC	D	14	2500	333.2	345.9	28.6
SN65LBC180RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
SN65LBC180RSAT	QFN	RSA	16	250	210.0	185.0	35.0
SN75LBC180DR	SOIC	D	14	2500	333.2	345.9	28.6
SN75LBC180RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
SN75LBC180RSAT	QFN	RSA	16	250	210.0	185.0	35.0

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55) C

14 8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) D

1 7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⌖ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040047-5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x1,27

5,40

Stencil Openings
(Note D)

14x0,55

12x1,27

14x1,50

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283–3/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

4,10
3,90
A
B
4,10
3,90
PIN 1 INDEX AREA
TOP AND BOTTOM

1,00
0,80
0,20 REF.
SEATING PLANE
C
0,08
0,05
0,00

16X 0,50
0,30
0,65
1
4
16
5
THERMAL PAD
SIZE AND SHAPE
SHOWN ON SEPARATE SHEET
13
8
12
9
16X 0,38
0,23

⌖	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		

4205141/D 06/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

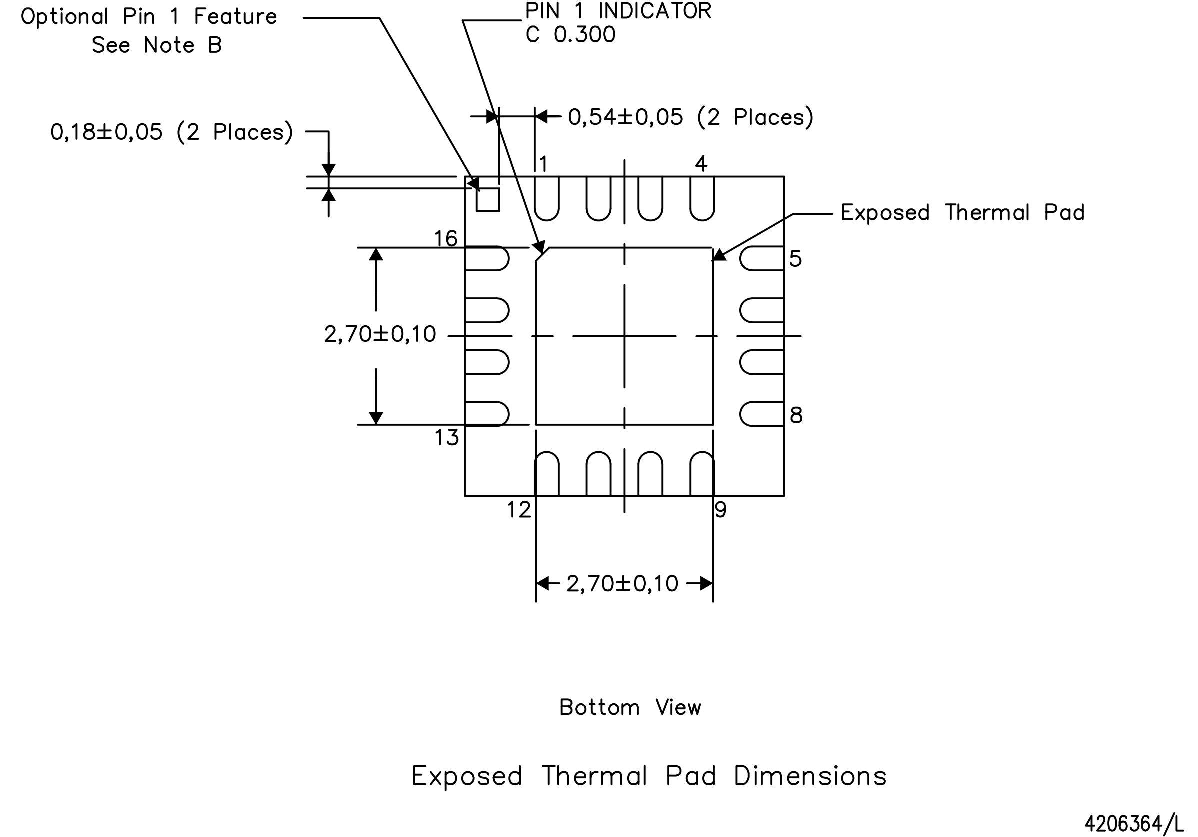
RSA (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206364/L 08/12

NOTES:

A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices
In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RSA (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

Pin 1 0,5x0,5mm
Route Keep
Out Area

0,4
12x0,65
Note D
0,4
3,1
4,8
3,1
4,8

Non Solder Mask Defined Pad

Example
Solder Mask Opening
(Note F)

R0,175
0,85
0,07
all around
0,35

Pad Geometry
(Note C)

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

16x0,3
12x0,65
16x0,8
R0,15
0,3
12x0,65
4x1,1
0,3
4x1,1
3,15
4,75
3,15
4,75

66% Printed Solder Coverage

Center Pad Layout
(Note D)

9xØ0,3
6x1,0
6x1,0
2,7
2,7

4207807/E 06/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2012, Texas Instruments Incorporated