MIPI® DSI BRIDGE TO FLATLINK™ LVDS
Single Channel DSI to Dual-Link LVDS Bridge

Check for Samples: SN65DSI84

FEATURES

- **Implements MIPI® D-PHY Version 1.00.00 Physical Layer Front-End and Display Serial Interface (DSI) Version 1.02.00**
- **Single Channel DSI Receiver Configurable for One, Two, Three, or Four D-PHY Data Lanes Per Channel Operating up to 1 Gbps Per Lane**
- **Supports 18 bpp and 24 bpp DSI Video Packets with RGB666 and RGB888 Formats**
- **Suitable for 60 fps WUXGA 1920 x 1200 Resolution at 18 bpp and 24 bpp Color, 60 fps 1366 x 768 at 18 bpp and 24 bpp**
- **FlatLink™ Output Configurable for Single-Link or Dual-Link LVDS**
- **Supports Single Channel DSI to Dual-Link LVDS Operating Mode**
- **LVDS Output Clock Range of 25 MHz to 154 MHz in Dual-Link or Single-Link Modes**
- **LVDS Pixel Clock May be Sourced from Free-Running Continuous D-PHY Clock or External Reference Clock (REFCLK)**
- **1.8 V Main V_{CC} Power Supply**
- **Low Power Features Include SHUTDOWN Mode, Reduced LVDS Output Voltage Swing, Common Mode, and MIPI® Ultra-Low Power State (ULPS) Support**
- **LVDS Channel SWAP, LVDS PIN Order Reverse Feature for Ease of PCB Routing**
- **ESD Rating ±2 kV (HBM)**
- **Packaged in 64-pin 5x5mm PBGA (ZQE)**
- **Temperature Range: -40°C to 85°C**

APPLICATIONS

- **Tablet PC, Notebook PC, Netbooks**
- **Mobile Internet Devices**

PRODUCT PREVIEW

DESCRIPTION

The SN65DSI84 DSI to FlatLink™ bridge features a single-channel MIPI® D-PHY receiver front-end configuration with 4 lanes per channel operating at 1 Gbps per lane; a maximum input bandwidth of 4 Gbps. The bridge decodes MIPI® DSI 18bpp RGB666 and 24 bpp RGB888 packets and converts the formatted video data stream to a FlatLink™ compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Dual-Link LVDS, Single-Link LVDS interface with four data lanes per link.

The SN65DSI84 is well suited for WUXGA 1920 x 1200 at 60 frames per second, with up to 24 bits-per-pixel. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces.

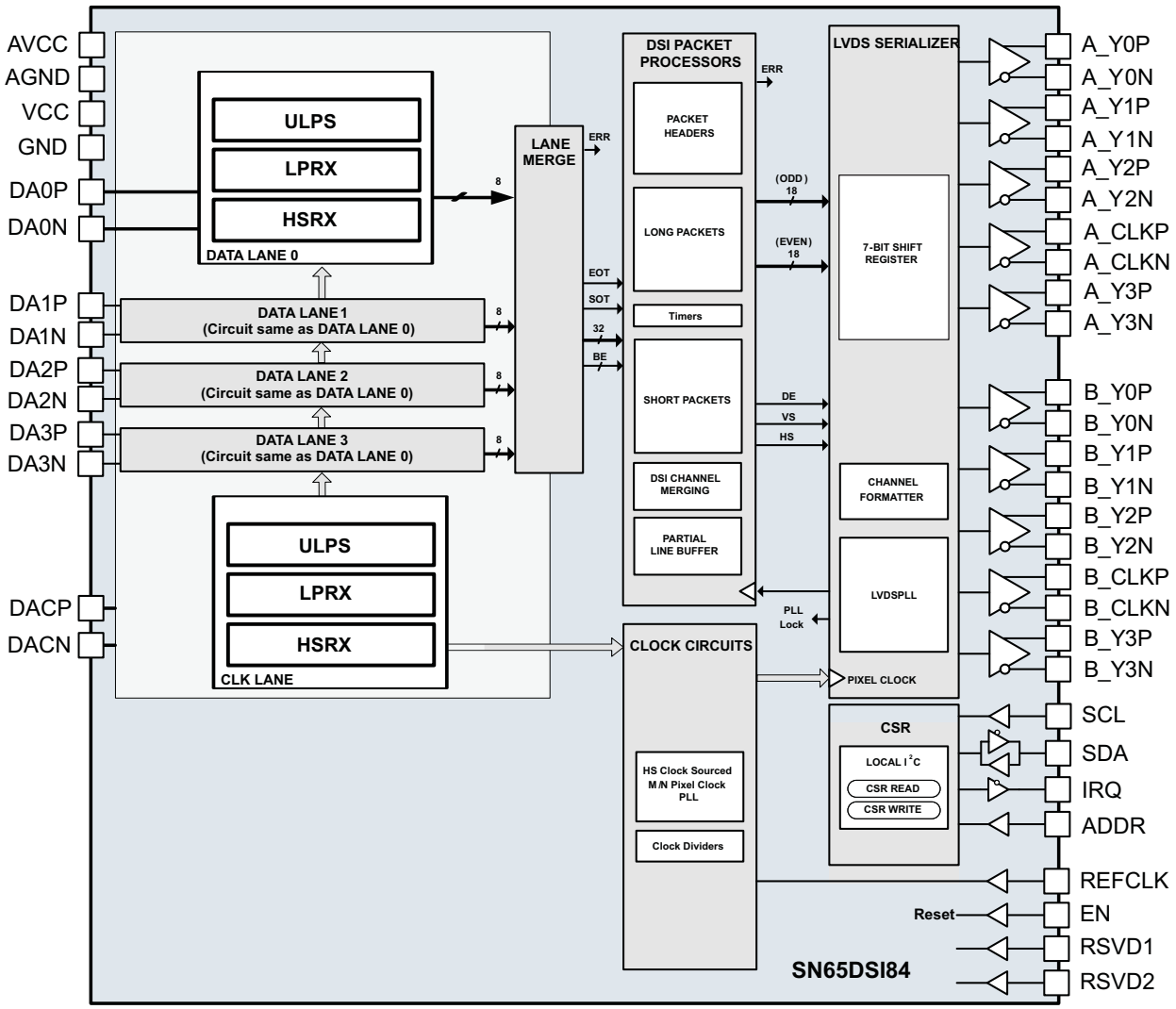
Designed with industry compliant interface technology, the SN65DSI84 is compatible with a wide range of micro-processors, and is designed with a range of power management features including low-swing LVDS outputs, and the MIPI® defined ultra-low power state (ULPS) support.

The SN65DSI84 is implemented in a small outline 5x5mm PBGA at 0.5 mm pitch package, and operates across a temperature range from -40ºC to 85ºC.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

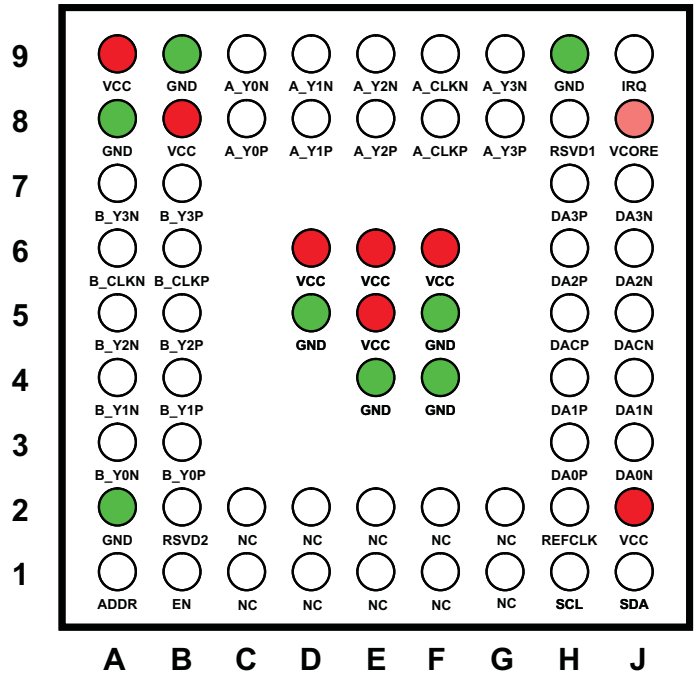
DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



PRODUCT PREVIEW

ZQE PACKAGE
(TOP VIEW)



To minimize the power supply noise floor, provide good decoupling near the SN65DSI84 power pins. The use of four ceramic capacitors (2x 0.1 µF and 2x 0.01 µF) provides good performance. At the least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65DSI84. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSI84 on the bottom of the PCB is often a good choice.

PIN FUNCTIONS

PIN			DESCRIPTION
SIGNAL	PIN	I/O	
DA0P, DA0N	H3, J3	LVDS Input (HS) CMOS Input (LS) (Failsafe)	MIPI® D-PHY Channel A Data Lane 0; data rate up to 1 Gbps.
DA1P, DA1N	H4, J4		MIPI® D-PHY Channel A Data Lane 1; data rate up to 1 Gbps.
DA2P, DA2N	H6, J6		MIPI® D-PHY Channel A Data Lane 2; data rate up to 1 Gbps.
DA3P, DA3N	H7, J7		MIPI® D-PHY Channel A Data Lane 3; data rate up to 1 Gbps.
DACP, DACN	H5, J5		MIPI® D-PHY Channel A Clock Lane; operates up to 500 MHz.
NC	C2, C1, D2, D1, F2, F1, G2, G1, E2, E1	No connects.	These pins should not be connected to any signal, power or ground.

PRODUCT PREVIEW

PIN FUNCTIONS (continued)

PIN			DESCRIPTION
SIGNAL	PIN	I/O	
A_Y0P, A_Y0N	C8, C9	LVDS Output	FlatLink™ Channel A LVDS Data Output 0.
A_Y1P, A_Y1N	D8, D9		FlatLink™ Channel A LVDS Data Output 1.
A_Y2P, A_Y2N	E8, E9		FlatLink™ Channel A LVDS Data Output 2.
A_Y3P, A_Y3N	G8, G9		FlatLink™ Channel A LVDS Data Output 3. A_Y3P and A_Y3N shall be left NC for 18 bpp panels.
A_CLKP, A_CLKN	F8, F9		FlatLink™ Channel A LVDS Clock
B_Y0P, B_Y0N	B3, A3		FlatLink™ Channel B LVDS Data Output 0.
B_Y1P, B_Y1N	B4, A4		FlatLink™ Channel B LVDS Data Output 1.
B_Y2P, B_Y2N	B5, A5		FlatLink™ Channel B LVDS Data Output 2.
B_Y3P, B_Y3N	B7, A7		FlatLink™ Channel B LVDS Data Output 3. B_Y3P and B_Y3N shall be left NC for 18 bpp panels.
B_CLKP, B_CLKN	B6, A6		FlatLink™ Channel B LVDS Clock.
RSVD1	H8	CMOS Input/Output with pulldown	Reserved. This pin should be left unconnected for normal operation.
RSVD2	B2	CMOS Input with pulldown	Reserved. This pin should be left unconnected for normal operation.
ADDR	A1	CMOS Input/Output	Local I^2C Interface Target Address Select. See Table 3. In normal operation this pin is an input. When the ADDR pin is programmed high, it should be tied to the same 1.8 V power rails where the SN65DSI84 VCC 1.8 V power rail is connected.
EN	B1	CMOS Input with pullup (Failsafe)	Chip Enable and Reset. Device is reset (shutdown) when EN is low.
REFCLK	H2	CMOS Input (Failsafe)	Optional External Reference Clock for LVDS Pixel Clock. If an External Reference Clock is not used, this pin should be pulled to GND with an external resistor. The source of the reference clock should be placed as close as possible with a series resistor near the source to reduce EMI.
SCL	H1		Local I^2C Interface Clock.
SDA	J1	Open Drain Input/Output (Failsafe)	Local I^2C Interface Bi-directional Data Signal.
IRQ	J9	CMOS Output	Interrupt Signal.
GND	A2, A8, B9, D5, E4, F4, F5, H9	Power Supply	Reference Ground.
VCC	A9, B8, D6, E5, E6, F6, J2		1.8 V Power Supply.
VCORE	J8		1.1 V Output from Voltage Regulator. This pin must have a 1 µF external capacitor to GND.

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE / SHIPPING
SN65DSI84ZQER	DSI84	64-Ball PBGA, Reel

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage Range	V_{CC}	-0.3	2.175	V
Input Voltage Range	CMOS Input Terminals	-0.5	2.175	V
	DSI Input Terminals (DA x P/N, DB x P/N)	-0.4	1.4	V
Storage Temperature	T_S	-65	105	°C
Electrostatic discharge	Human Body Model (2)		±2	kV
	Charged-device model (3)		±500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(3) Tested in accordance with JEDEC Standard 22, Test Method C101-A

THERMAL INFORMATION

THERMAL METRIC(1)		SN65DSI84 ZQE 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	72.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	35.7	
θ_{JB}	Junction-to-board thermal resistance	35.2	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	36.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	VCC Power supply	1.65	1.8	1.95	V
V_{PSN}	Supply noise on any V_{CC} pin	$f_{(noise)}$ > 1MHz		0.05	V
T_A	Operating free-air temperature	-40		85	°C
T_{CASE}	Case temperature			92.2	
V_{DSI_PIN}	DSI input pin voltage range	-50		1350	mV
$f_{(I2C)}$	Local I^2C input frequency			400	kHz
f_{HS_CLK}	DSI HS clock input frequency	40		500	MHz
t_{setup}	DSI HS data to clock setup time	0.15			UI (1)
t_{hold}	DSI HS data to clock hold time; see Figure 1	0.15			
Z_L	LVDS output differential impedance	90		132	Ω

(1) The unit interval (UI) is one half of the period of the HS clock; at 500 MHz the minimum setup and hold time is 150 ps

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IL}	Low-level control signal input voltage				0.3 x VCC	V
V_{IH}	High-level control signal input voltage		0.7 x VCC			
V_{OH}	High-level output voltage	I_{OH} = –4 mA	1.25			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	
I_{LKG}	Input failsafe leakage current	V_{CC} = 0; $V_{CC(PIN)}$ = 1.8 V			±30	µA
I_{IH}	High level input current	Any input terminal			±30	
I_{IL}	Low level input current					
I_{OZ}	High-impedance output current	Any output terminal			±10	
I_{OS}	Short-circuit output current	Any output driving GND short			±20	mA
I_{CC}	Device active current	see (2)		106	150	mA
I_{ULPS}	Device standby current	All data and clock lanes are in ultra-low power state (ULPS)		7.7	10	
I_{RST}	Shutdown current	EN = 0		0.04	0.06	
R_{EN}	EN control input resistor			200		kΩ
MIPI DSI INTERFACE						
V_{IH-LP}	LP receiver input high threshold	see Figure 2	880			mV
V_{IL-LP}	LP receiver input low threshold				550	
$\|V_{ID}\|$	HS differential input voltage		70		270	
$\|V_{IDT}\|$	HS differential input voltage threshold				50	
$V_{IL-ULPS}$	LP receiver input low threshold; ultra-low power state (ULPS)				300	
V_{CM-HS}	HS common mode voltage; steady-state		70		330	
ΔV_{CM-HS}	HS common mode peak-to-peak variation including symbol delta and interference				100	
V_{IH-HS}	HS single-ended input high voltage	see Figure 2			460	
V_{IL-HS}	HS single-ended input low voltage		-40			
$V_{TERM-EN}$	HS termination enable; single-ended input voltage (both Dp AND Dn apply to enable)	Termination is switched simultaneous for Dn and Dp			450	
$R_{DIFF-HS}$	HS mode differential input impedance		80		125	Ω

(1) All typical values are at V_{CC} = 1.8V and T_A = 25°C

(2) SN65DSI84: SINGLE Channel DSI to DUAL Channel LVDS, 1440 x 900
- (a) number of LVDS lanes = 2 x (3 data lanes + 1 CLK lane)
- (b) number of DSI lanes = 2 data lanes + 1 CLK lane
- (c) LVDS CLK OUT = 53.25 M
- (d) DSI CLK = 500 M
- (e) RGB888, LVDS18bpp

Maximum values are at V_{CC} = 1.95 V and T_A = 85°C

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
FLATLINK LVDS OUTPUT						
$\|V_{OD}\|$	Steady-state differential output voltage for A_Y x P/N and B_Y x P/N	CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00; 100Ω near end termination	180	245	313	mV
		CSR 0x19.3:2=01 and/or CSR 0x19.1:0=01; 100Ω near end termination	215	293	372	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10; 100Ω near end termination	250	341	430	
		CSR 0x19.3:2=11 and/or CSR 0x19.1:0=11; 100Ω near end termination	290	389	488	
		CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00; 200Ω near end termination	150	204	261	
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01; 200Ω near end termination	200	271	346	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10; 200Ω near end termination	250	337	428	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11; 200Ω near end termination	300	402	511	
	Steady-state differential output voltage for A_CLKP/N and B_CLKP/N	CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 100Ω near end termination	140	191	244	mV
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 100Ω near end termination	168	229	290	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 100Ω near end termination	195	266	335	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 100Ω near end termination	226	303	381	
		CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 200Ω near end termination	117	159	204	
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 200Ω near end termination	156	211	270	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 200Ω near end termination	195	263	334	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 200Ω near end termination	234	314	399	
$\Delta\|V_{OD}\|$	Change in steady-state differential output voltage between opposite binary states	RL = 100Ω			35	mV
$V_{OC(SS)}$	Steady state common-mode output voltage(3)	CSR 0x19.6 = 1 and CSR 0x1B.6 = 1; and, or CSR 0x19.4 = 1 and CSR 0x1B.4 = 1; see Figure 3	0.8	0.9	1	V
		CSR 0x19.6 = 0 and, or CSR 0x19.4 = 0; see Figure 3	1.15	1.25	1.35	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	see Figure 3			35	mV
R_{LVDS_DIS}	Pull-down resistance for disabled LVDS outputs			1		kΩ

(3) Tested at V_{CC} = 1.8V , T_A = -40°C for MIN, T_A = 25°C for TYP, T_A = 85°C for MAX.

PRODUCT PREVIEW

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DSI						
t_{GS}	DSI LP glitch suppression pulse width				300	ps
LVDS						
t_c	Output clock period		6.49		40	ns
t_w	High-level output clock (CLK) pulse duration			4/7 tc		ns
t_0	Delay time, CLK↑ to 1st serial bit position	t_c = 6.49ns; Input clock jitter < 25ps (REFCLK)	-0.15		0.15	ns
t_1	Delay time, CLK↑ to 2nd serial bit position		1/7 t_c – 0.15		1/7 t_c + 0.15	ns
t_2	Delay time, CLK↑ to 3rd serial bit position		2/7 t_c – 0.15		2/7 t_c + 0.15	ns
t_3	Delay time, CLK↑ to 4th serial bit position		3/7 t_c – 0.15		3/7 t_c + 0.15	ns
t_4	Delay time, CLK↑ to 5th serial bit position		4/7 t_c – 0.15		4/7 t_c + 0.15	ns
t_5	Delay time, CLK↑ to 6th serial bit position		5/7 t_c – 0.15		5/7 t_c + 0.15	ns
t_6	Delay time, CLK↑ to 7th serial bit position		6/7 t_c – 0.15		6/7 t_c + 0.15	ns
t_r	Differential output rise-time	See Figure 4	180		500	ps
t_f	Differential output fall-time					
EN, ULPS, RESET						
t_{en}	Enable time from EN or ULPS	$t_{c(o)}$ = 12.9 ns			1	ms
t_{dis}	Disable time to standby; see Figure 5				0.1	
t_{reset}	Reset time		10			ms
R_{EFCLK}						
F_{REFCLK}	REFCLK Freqeuncy. Supported frequencies: 25 MHz-154 MHz		25		154	MHz
t_r, t_f	REFCLK rise and fall time		100ps		1ns	s
t_{pj}	REFCLK Peak-to-Peak Phase Jitter				50	ps
Duty	REFCLK Duty Cycle		40%	50%	60%	
REFCLK or DSI CLK (DACP/N, DBCP/N)						
SSC_CLKIN	SSC enabled Input CLK center spread depth (2)		0.5%	1%	2%	
	Modulation Frequency Range		30		60	KHz

(1) All typical values are at V_{CC} = 1.8 V and T_A = 25°C

(2) For EMI reduction purpose, SN65DSI84 supports the center spreading of the LVDS CLK output through the REFCLK or DSI CLK input. The center spread CLK input to the REFCLK or DSI CLK is passed through to the LVDS CLK output A_CLKP/N and/or B_CLKP/N.

PRODUCT PREVIEW

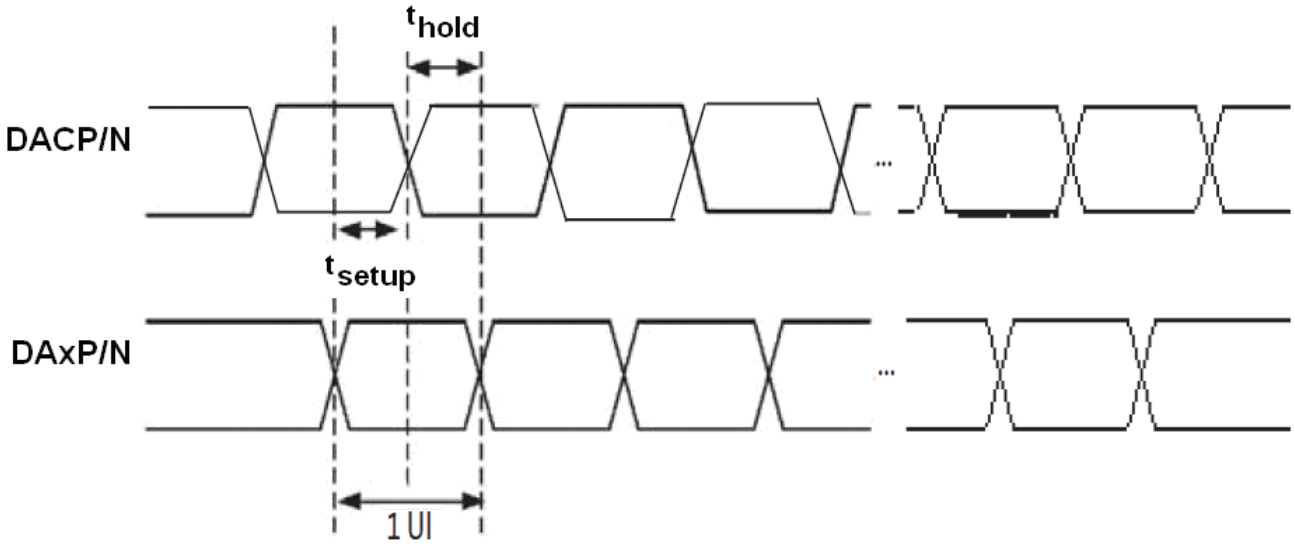


Figure 1. DSI HS Mode Receiver Timing Definitions

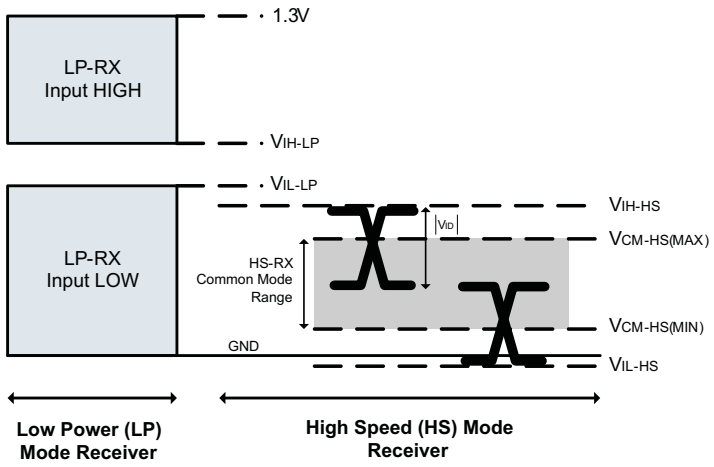


Figure 2. DSI Receiver Voltage Definitions

PRODUCT PREVIEW

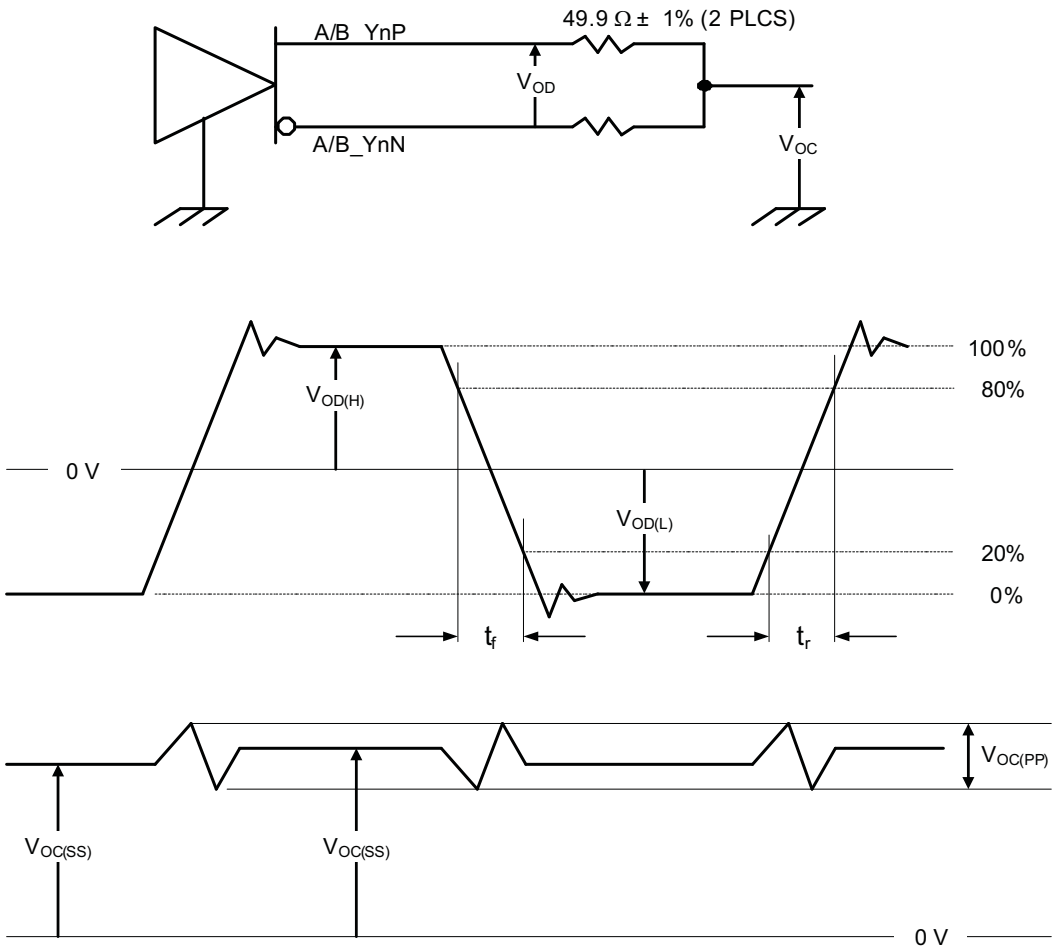


Figure 3. Test Load and Voltage Definitions for FlatLink™ Outputs

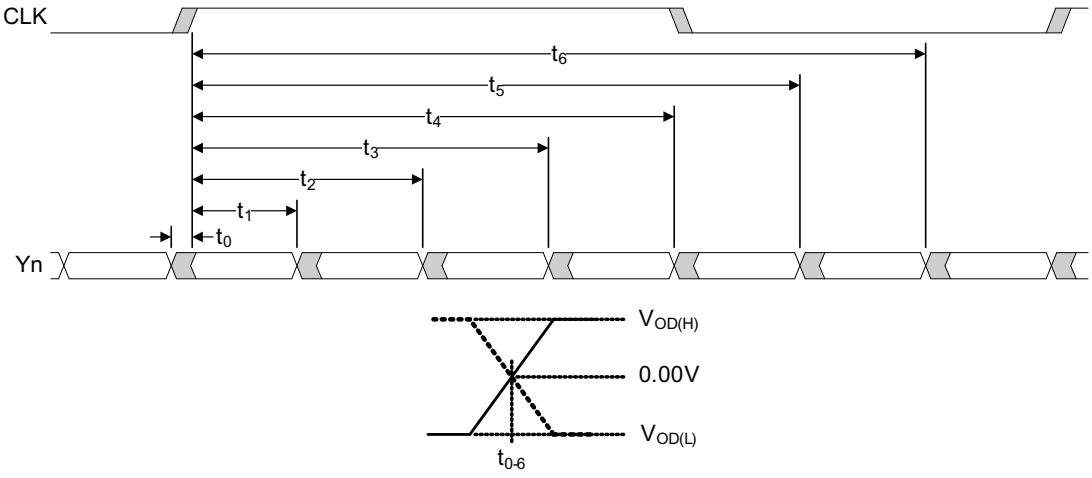
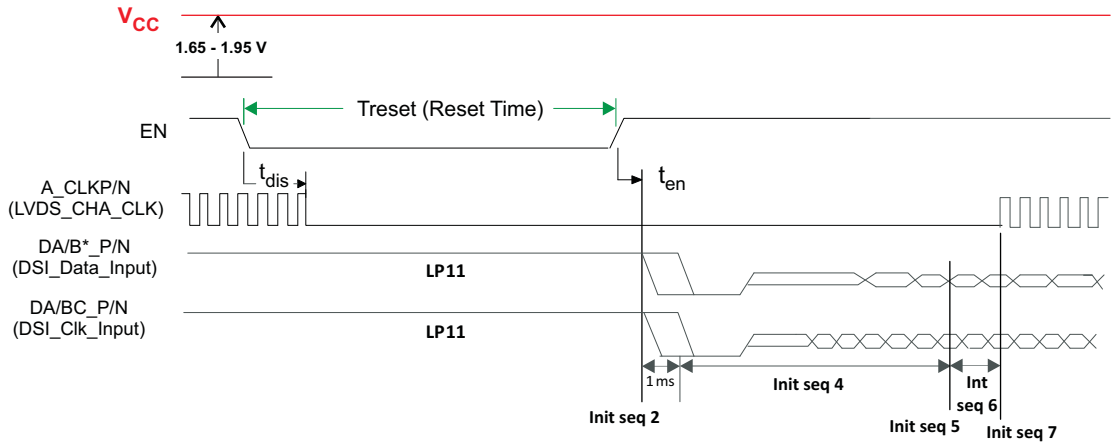


Figure 4. SN65DSI84 FlatLink™ Timing Definitions

PRODUCT PREVIEW

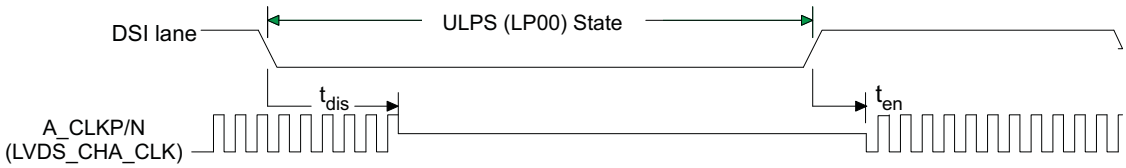


(1) The Initialization sequence can be found at Recommended Initialization Sequence section of this document. The "Init seq*" corresponds to the sequence number in the Recommended Initialization Sequence section.

(2) A_CLKP/N(LVDS_CHA_CLK) becomes active along with CHA LVDS data lanes0-2 after PLL lock event occurs and CLK source(REF_CLK or DSI HS CLK) is active(Init seq7). Other LVDS CLK/data lanes stay low until they are configured to be enabled in corresponding CSRs

(3) The LP11 to HS transition to the data lanes and the CLK lane MUST be done per the timing requirements specified in the MIPI® D-PHY Specification.

Figure 5. Shutdown and RESET Timing Definition While V_{CC} is High



(1) See the ULPS section of the data sheet for the ULPS entry and exit sequence.

(2) ULPS entry and exit protocol and timing requirements must be met per MIPI® DPHY specification.

Figure 6. ULPS Timing Definition

PRODUCT PREVIEW

DEVICE INFORMATION

Reset Implementation

When EN is de-asserted (low), the SN65DSI84 is in SHUTDOWN or RESET state. In this state, CMOS inputs are ignored, the MIPI® D-PHY inputs are disabled and outputs are high impedance. It is critical to transition the EN input from a low to a high level after the V_{CC} supply has reached the minimum operating voltage as shown in Figure 7. This is achieved by a control signal to the EN input, or by an external capacitor connected between EN and GND.

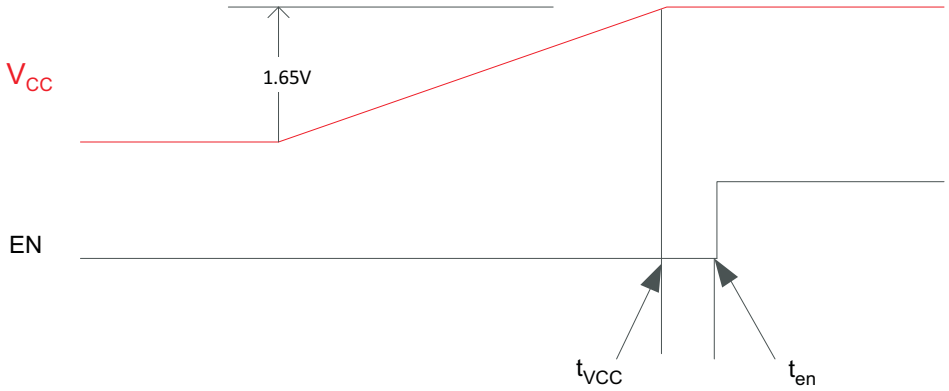


Figure 7. Cold Start V_{CC} Ramp up to EN

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{CC} supply, where a slower ramp-up results in a larger value external capacitor. See the latest reference schematic for the SN65DSI84 device and, or consider approximately 200 nF capacitor as a reasonable first estimate for the size of the external capacitor.

Both EN implementations are shown in Figure 8 and Figure 9.

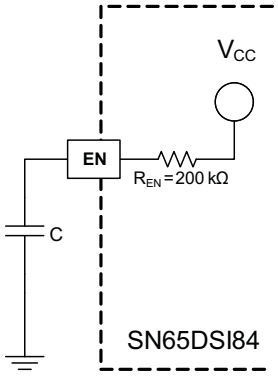


Figure 8. External Capacitor Controlled EN

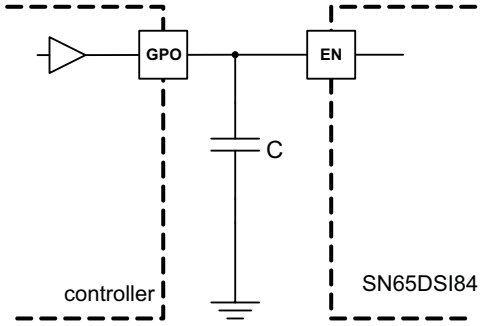


Figure 9. EN Input from Active Controller

When the SN65DSI84 is reset while V_{CC} is high, the EN pin must be held low for at least 10 ms before being asserted high as shown in Figure 5 to be sure that the device is properly reset. The DSI lanes including the CLK lanes MUST be driven to LP11 while the device is in reset until the EN pin is asserted high per the timing shown in Figure 5.

PRODUCT PREVIEW

Recommended Initialization Sequence

It is recommended to use the following initialization sequence for the SN65DSI84.

Also see to Figure 7.

Initialization Sequence Number	Initialization Sequence Description
Init seq1	After power is applied and stable, all DSI Input lanes including DSI CLK(DA x P/N, DB x P/N) MUST be driven to LP11 state.
Init seq2	Assert the EN pin
Init seq3	Wait for 1ms for the internal voltage regulator to stabilize
Init seq4	Initialize all CSR registers to their appropriate values based on the implementation (The SN65DSI84 is not functional until the CSR registers are initialized)
Init seq5	Start the DSI video stream
Init seq6	Set the PLL_EN bit(CSR 0x0D.0)
Init seq7	Wait for the PLL_LOCK bit to be set(CSR 0x0A.7)
Init seq8	Set the SOFT_RESET bit (CSR 0x09.0)

Clock Configurations and Multipliers

The FlatLink™ LVDS clock may be derived from the DSI channel A clock, or from an external reference clock source. When the MIPI® D-PHY channel A HS clock is used as the LVDS clock source, the D-PHY clock lane must operate in HS free-running (continuous) mode; this feature eliminates the need for an external reference clock reducing system costs

The reference clock source is selected by HS_CLK_SRC (CSR 0x0A.0) programmed through the local I^2C interface. If an external reference clock is selected, it is multiplied by the factor in REFCLK_MULTIPLIER (CSR 0x0B.1:0) to generate the FlatLink™ LVDS output clock. When an external reference clock is selected, it must be between 25 MHz and 154 MHz. If the DSI channel A clock is selected, it is divided by the factor in DSI_CLK_DIVIDER (CSR 0x0B.7:3) to generate the FlatLink™ LVDS output clock. Additionally, LVDS_CLK_RANGE (CSR 0x0A.3:1) and CH_DSI_CLK_RANGE(CSR 0x12) must be set to the frequency range of the FlatLink™ LVDS output clock for and DSI Channel A input clock respectively the internal PLL to operate correctly. After these settings are programmed, PLL_EN (CSR 0x0D.0) must be set to enable the internal PLL.

Operating Modes

The SN65DSI84 can be configured for several different operating modes via LVDS_LINK_CFG (CSR 0x18.4), LEFT_RIGHT_PIXELS (CSR 0x10.7), and DSI_CHANNEL_MODE (CSR 0x10.6:5). These modes are summarized in Table 1. In each of the modes, video data can be 18 bpp or 24 bpp.

Table 1. SN65DSI84 Operating Modes

MODE	CSR 0x18.4	DESCRIPTION
	LVDS_LINK_CFG	
Single DSI Input to Single-Link LVDS	1	Single DSI Input on Channel A to Single-Link LVDS output on Channel A.
Single DSI Input to Dual-Link LVDS	0	Single DSI Input on Channel A to Dual-Link LVDS output with Odd pixels on Channel A and Even pixels on Channel B.

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LVDS Output Formats

The SN65DSI84 processes DSI packets and produces video data driven to the FlatLink™ LVDS interface in an industry standard format. Single-Link LVDS and Dual-Link LVDS are supported by the SN65DSI84; when the FlatLink™ output is implemented in a Dual-Link configuration, channel A carries the odd pixel data, and channel B carries the even pixel data. During conditions such as the default condition, and some video synchronization periods, where no video stream data is passing from the DSI input to the LVDS output, the SN65DSI84 transmits zero value pixel data on the LVDS outputs while maintaining transmission of the vertical sync and horizontal sync status.

Figure 10 illustrates a Single-Link LVDS 18bpp application.

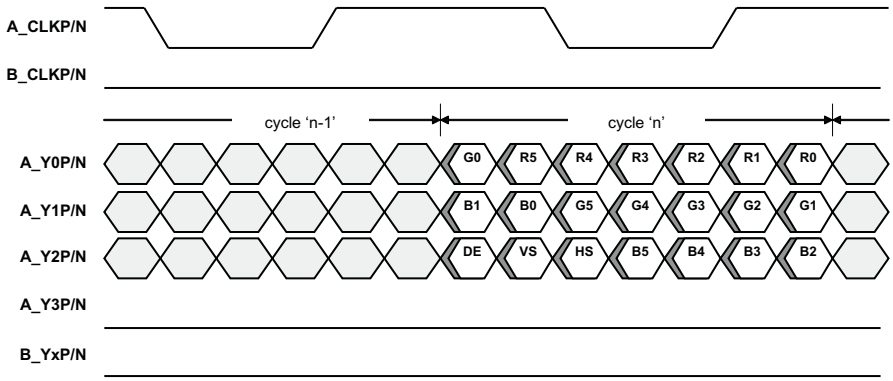
Figure 11 illustrates a Dual-Link 24 bpp application using Format 2, controlled by CHA_24BPP_FORMAT1 (CSR 0x18.1) and CHB_24BPP_FORMAT1 (CSR 0x18.0). In data Format 2, the two MSB per color are transferred on the Y3P/N LVDS lane.

Figure 12 illustrates a 24 bpp Single-Link application using Format 1. In data Format 1, the two LSB per color are transferred on the Y3P/N LVDS lane.

Figure 13 illustrates a Single-Link LVDS application where 24 bpp data is received from DSI and converted to 18 bpp data for transmission to an 18 bpp panel. This application is configured by setting CHA_24BPP_FORMAT1 (CSR 0x18.1) to '1' and CHA_24BPP_MODE (CSR 0x18.3) to '0'. In this configuration, the SN65DSI84 will not transmit the 2 LSB per color since the Y3P/N LVDS lane is disabled.

NOTE

Note: Figure 10, Figure 11, Figure 12, and Figure 13 only illustrate a few example applications for the SN65DSI84. Other applications are also supported.



DE = Data Enable; Channel B Clock, Channel B Data, and A_Y3P/N are Output Low

Figure 10. FlatLink™ Output Data; Single-Link 18 bpp

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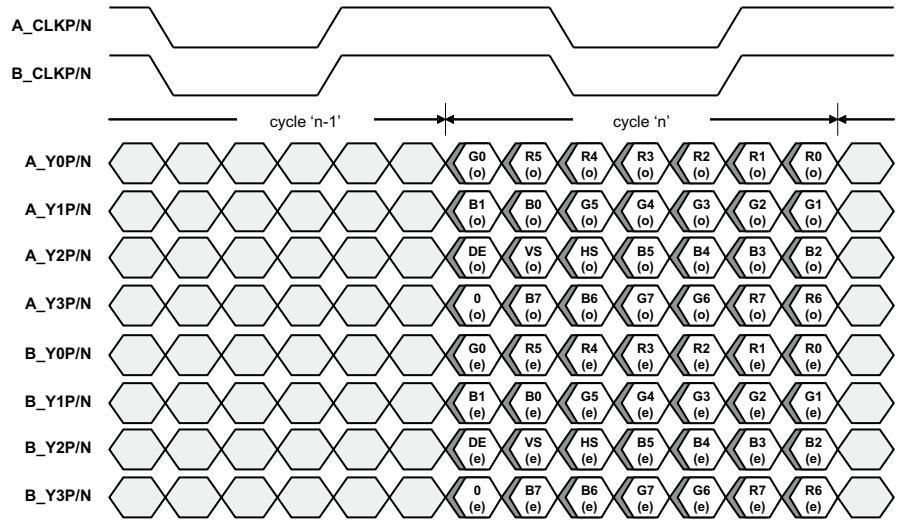
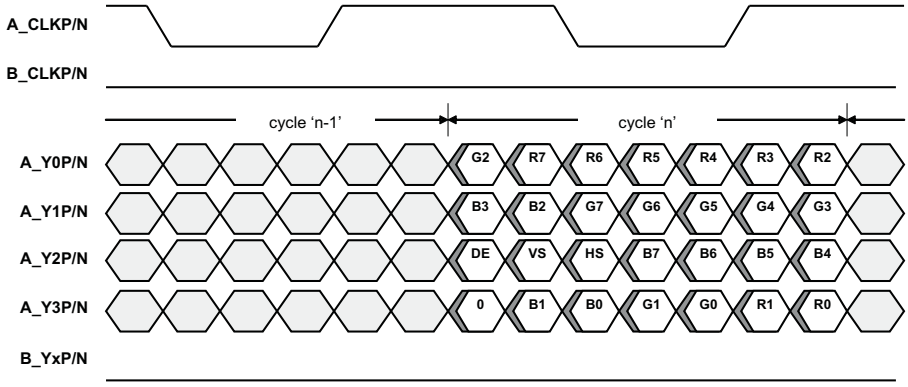


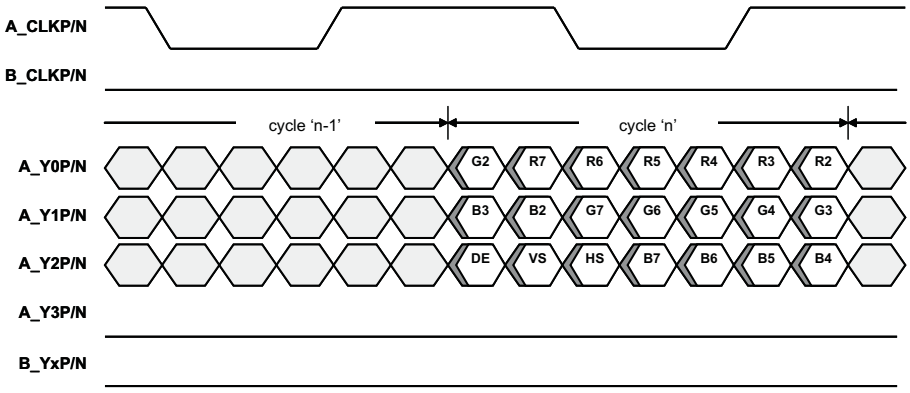
DE = Data Enable; (o) = Odd Pixels; (e) = Even Pixels

Figure 11. FlatLink™ Output Data (Format 2); Dual-Link 24 bpp



DE = Data Enable; Channel B Clock and Data are Output Low

Figure 12. FlatLink™ Output Data (Format 1); Single-Link 24 bpp



DE = Data Enable; Channel B Clock, Channel B Data, and A_Y3P/N a re Output Low; Channel B Clock, Channel B Data, and A_Y3P/N are Output Low

Figure 13. FlatLink™ Output Data (Format 1); 24 bpp to Single-Link 18 bpp Conversion

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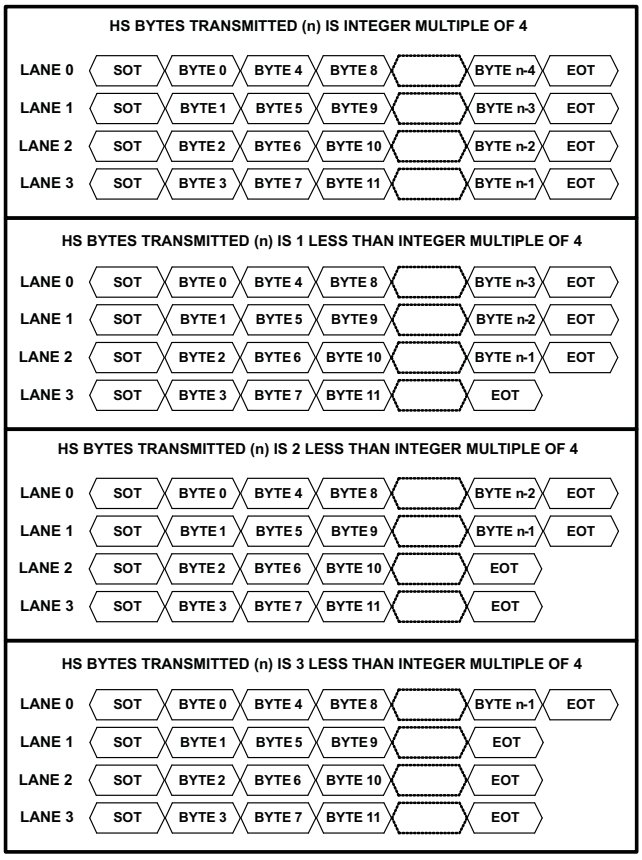
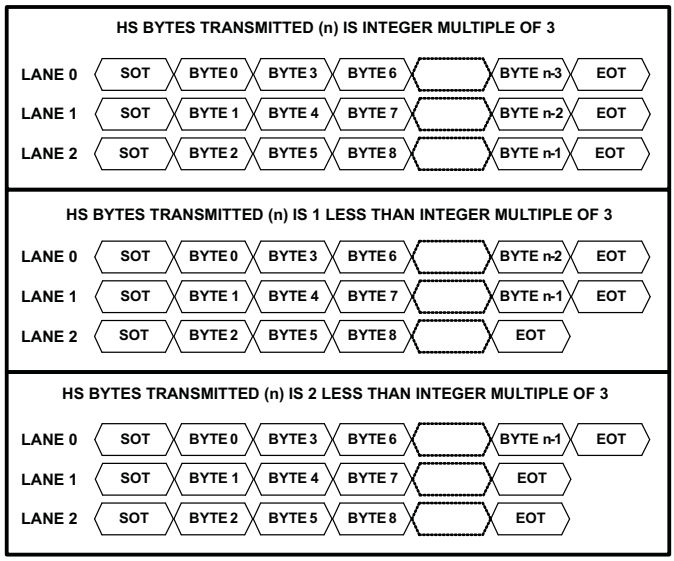
DSI Lane Merging

The SN65DSI84 supports four DSI data lanes per input channel, and may be configured to support one, two, or three DSI data lanes per channel. Unused DSI input pins on the SN65DSI84 should be left unconnected or driven to LP11 state. The bytes received from the data lanes are merged in HS mode to form packets that carry the video stream. DSI data lanes are bit and byte aligned.

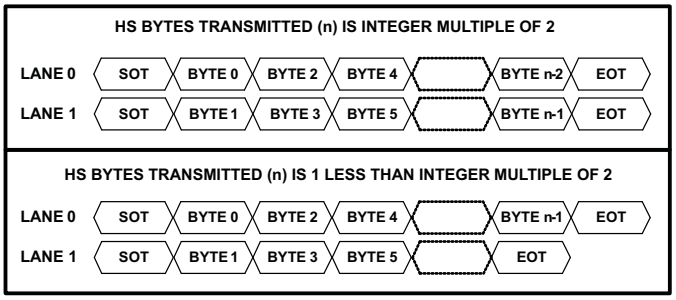
Figure 14 illustrates the lane merging function for each channel; 4-Lane, 3-Lane, and 2-Lane modes are illustrated



4 DSI Data Lane Configuration (default)



3 DSI Data Lane Configuration



2 DSI Data Lane Configuration

Figure 14. SN65DSI84 DSI Lane Merging Illustration

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DSI Pixel Stream Packets

The SN65DSI84 processes 18bpp (RGB666) and 24 bpp (RGB888) DSI packets on each channel as shown in Figure 15, Figure 16, andFigure 17.

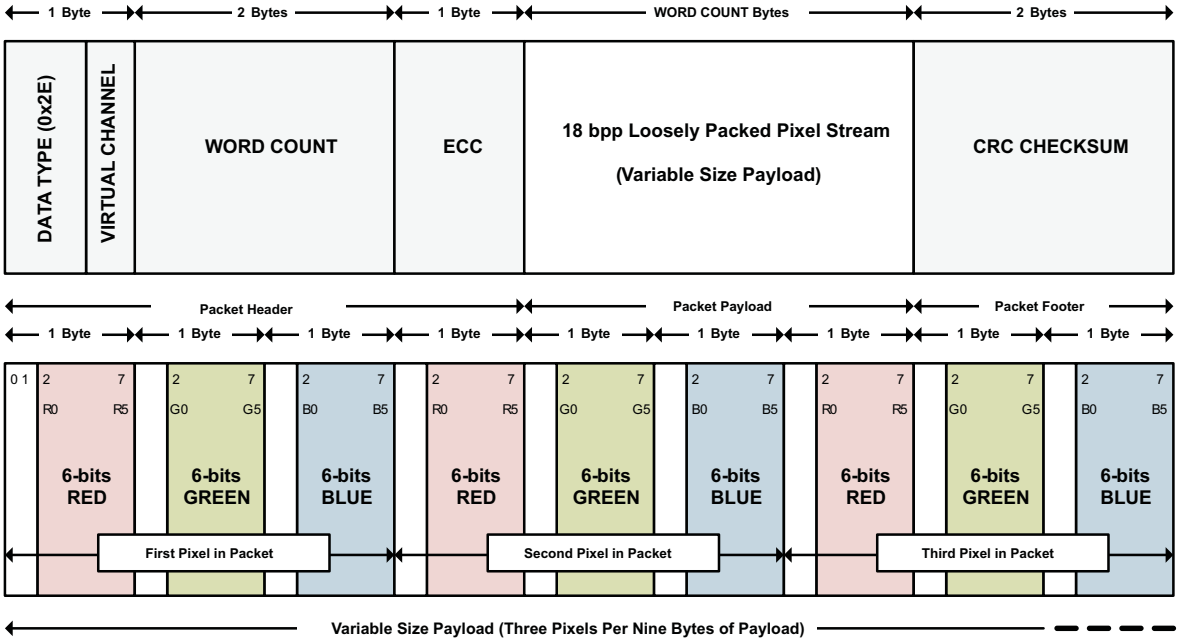

Figure 15. 18 bpp (Loosely Packed) DSI Packet Structure

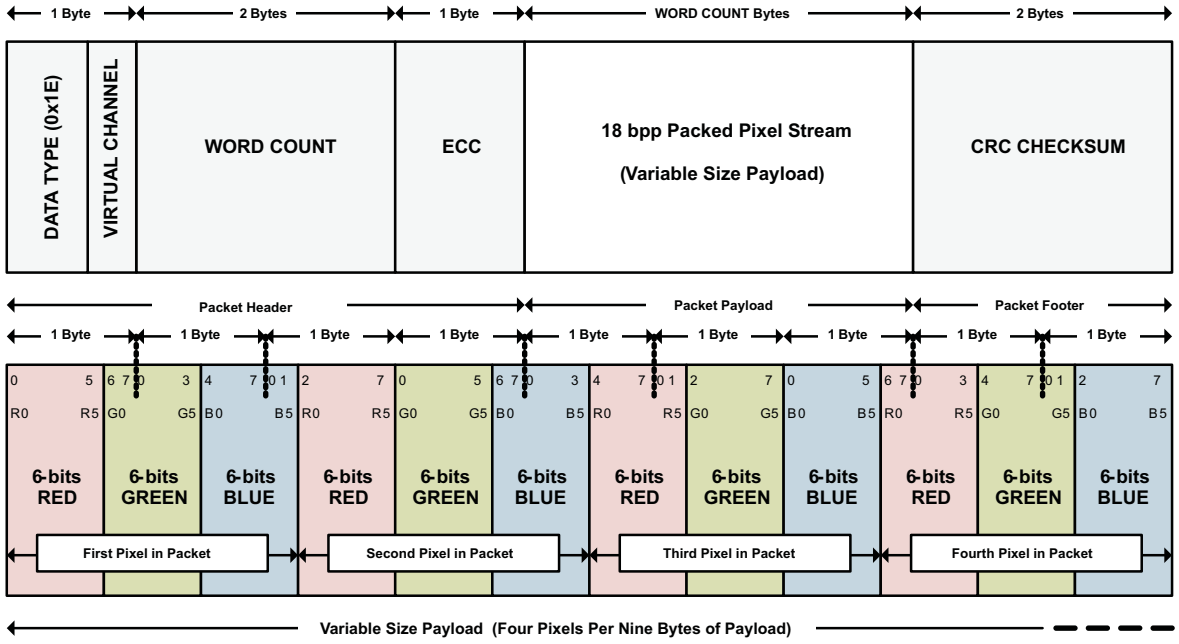

Figure 16. 18 bpp (Tightly Packed) DSI Packet Structure

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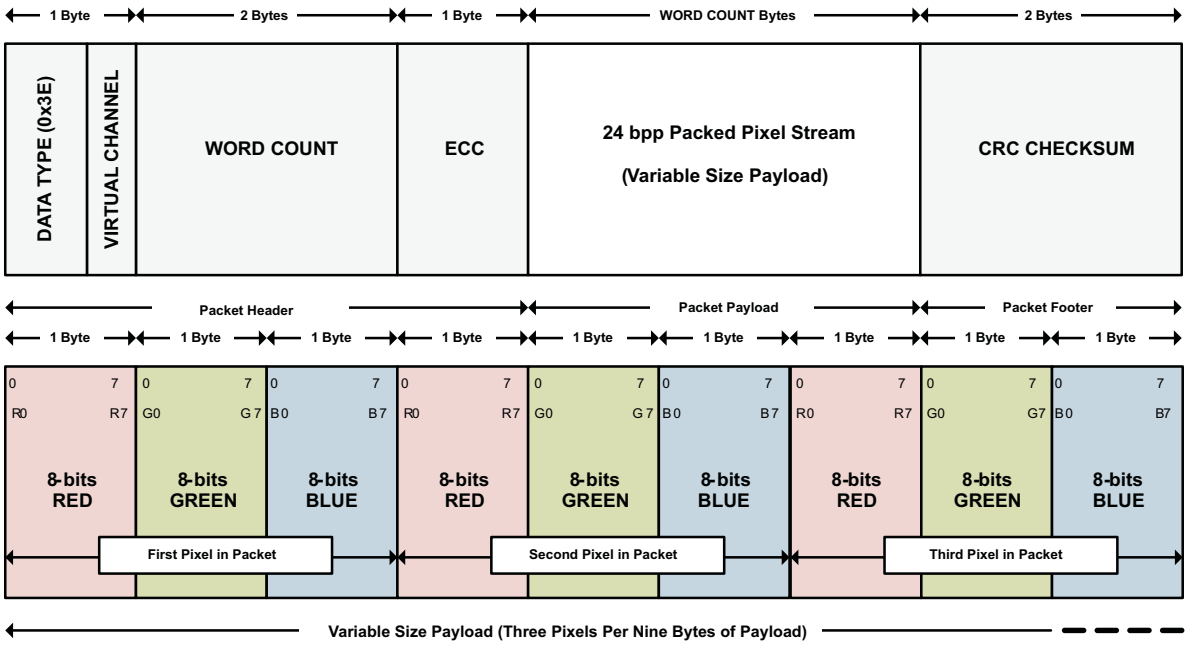

Figure 17. 24 bpp DSI Packet Structure

DSI Video Transmission Specifications

The SN65DSI84 supports burst video mode and non-burst video mode with sync events or with sync pulses packet transmission as described in the DSI specification. The burst mode supports time-compressed pixel stream packets that leave added time per scan line for power savings LP mode. The SN65DSI84 requires a transition to LP mode once per frame to enable PHY synchronization with the DSI host processor; however, for a robust and low-power implementation, the transition to LP mode is recommended on every video line.

Figure 18 illustrates the DSI video transmission applied to SN65DSI84 applications. In all applications, the LVDS output rate must be less than or equal to the DSI input rate. The first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance since this has a direct impact on the visual performance of the display panel; that is, these packets generate the HS and VS (horizontal and vertical sync) signals on the LVDS interface after the delay programmed into CHA_SYNC_DELAY_LOW/HIGH (CSR 0x28.7:0 and 0x29.3:0).

As required in the DSI specification, the SN65DSI84 requires that pixel stream packets contain an integer number of pixels (i.e. end on a pixel boundary); it is recommended to transmit an entire scan line on one pixel stream packet. When a scan line is broken in to multiple packets, inter-packet latency shall be considered such that the video pipeline (ie. pixel queue or partial line buffer) does not run empty (i.e. under-run); during scan line processing, if the pixel queue runs empty, the SN65DSI84 transmits zero data (18'b0 or 24'b0) on the LVDS interface.

NOTE

When the HS clock is used as a source for the LVDS pixel clock, the LP mode transitions apply only to the data lanes, and the DSI clock lane remains in the HS mode during the entire video transmission.

NOTE

The DSI84 does not support the DSI Virtual Channel capability or reverse direction (peripheral to processor) transmissions.

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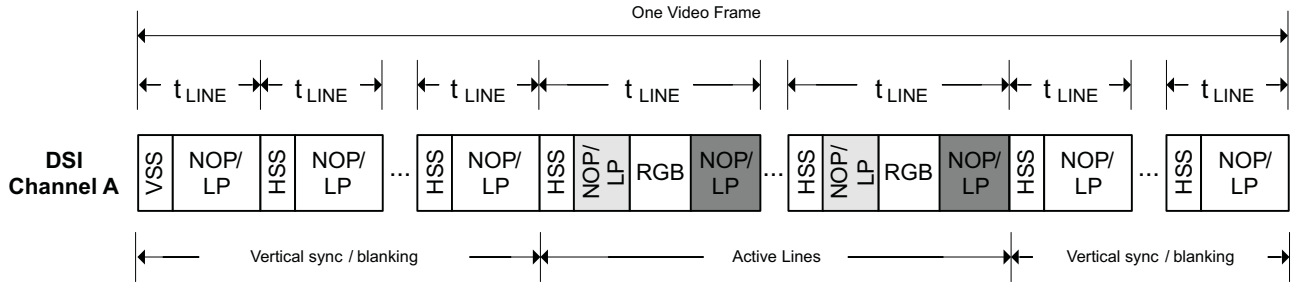
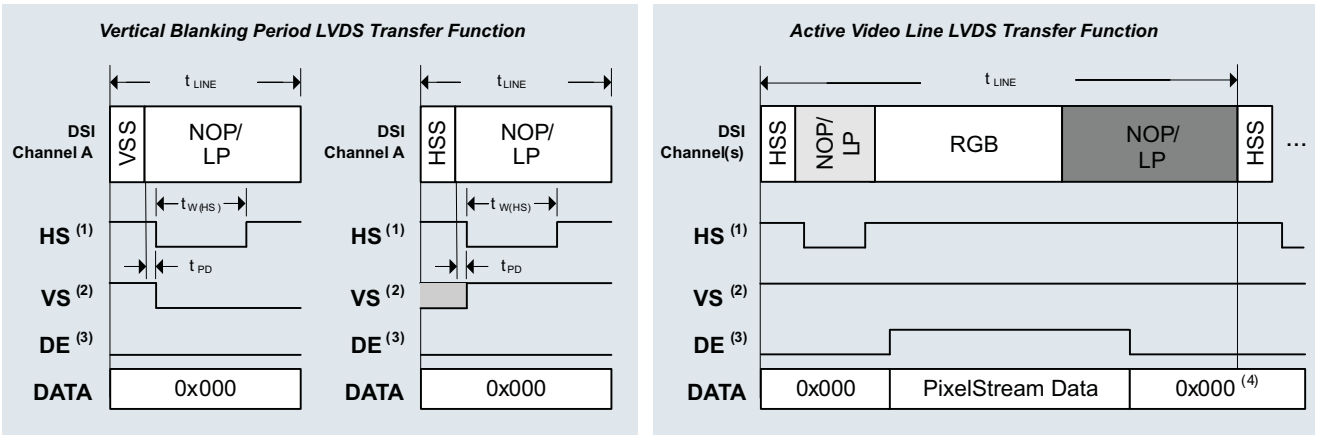


* VSS and HSS packets are required for DSI Channel B, although LVDS video sync signals are derived from DSI Channel A VSS and HSS packets



(1) The assertion of HS is delayed (t_{PD}) by a programmable number of pixel clocks from the last bit of VSS/HSS packet received on DSI. The HS pulse width ($t_{W(HS)}$) is also programmable. The illustration shows HS active low.

(2) VS is signaled for a programmable number of lines (t_{LINE}) and is asserted when HS is asserted for the first line of the frame . VS is de -asserted when HS is asserted after the number of lines programmed has been reached. The illustration shows VS active low

(3) DE is asserted when active pixel data is transmitted on LVDS , and polarity is set independent to HS/VS. The illustration shows DE active high

(4) After the last pixel in an active line is output to LVDS, the LVDS data is output zero

LEGEND

VSS	**DSI Sync Event Packet: V Sync Start**
HSS	**DSI Sync Event Packet: H Sync Start**
RGB	**A sequence of DSI Pixel Stream Packets and Null Packets**
NOP/LP	**DSI Null Packet , Blanking Packet , or a transition to LP Mode**

Figure 18. DSI Channel Transmission and Transfer Function

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ULPS

The SN65DSI84 supports the MIPI® defined ultra-low power state (ULPS). While the device is in the ULPS, the CSR registers are accessible via I2C interface. ULPS sequence should be issued to all active DSI CLK and/or DSI data lanes of the enabled DSI Channels for the SN65DSI84 enter the ULPS. The Following sequence should be followed to enter and exit the ULPS.

1. Host issues a ULPS entry sequence to all DSI CLK and data lanes enabled.
2. When host is ready to exit the ULPS mode, host issues a ULPS exit sequence to all DSI CLK and data lanes that need to be active in normal operation.
3. Wait for the PLL_LOCK bit (CSR 0x0A.7) to be set.
4. Set the SOFT_RESET bit (CSR 0x09.0).
5. Device resumes normal operation.(i.e video streaming resumes on the panel).

LVDS Pattern Generation

The SN65DSI84 supports a pattern generation feature on LVDS Channels. This feature can be used to test the LVDS output path and LVDS panels in a system platform. The pattern generation feature can be enabled by setting the CHA_TEST_PATTERN bit at address 0x3C. No DSI data is received while the pattern generation feature is enabled.

There are three modes available for LVDS test pattern generation. The mode of test pattern generation is determined by register configuration as shown in Table 2.

Table 2. VideoRegisters

Addr. bit	Register Name
0x20.7:0	CHA_ACTIVE_LINE_LENGTH_LOW
0x21.3:0	CHA_ACTIVE_LINE_LENGTH_HIGH
0x24.7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW
0x25.3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH
0x2C.7:0	CHA_HSYNC_PULSE_WIDTH_LOW
0x2D.1:0	CHA_HSYNC_PULSE_WIDTH_HIGH
0x30.7:0	CHA_VSYNC_PULSE_WIDTH_LOW
0x31.1:0	CHA_VSYNC_PULSE_WIDTH_HIGH
0x34.7:0	CHA_HORIZONTAL_BACK_PORCH
0x36.7:0	CHA_VERTICAL_BACK_PORCH
0x38.7:0	CHA_HORIZONTAL_FRONT_PORCH
0x3A.7:0	CHA_VERTICAL_FRONT_PORCH

Local I^2C Interface Overview

The SN65DSI84 local I^2C interface is enabled when EN is input high, access to the CSR registers is supported during ultra-low power state (ULPS). The SCL and SDA terminals are used for I^2C clock and I^2C data respectively. The SN65DSI84 I^2C interface conforms to the two-wire serial interface defined by the I^2C Bus Specification, Version 2.1 (January 2000), and supports fast mode transfers up to 400 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN65DSI84 is factory preset to 010110X with the least significant bit being determined by the ADDR control input. Table 3 clarifies the SN65DSI84 target address.

Table 3. SN65DSI84 I^2C Target Address Description (1) (2)

SN65DSI84 I2C TARGET ADDRESS							
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	1	0	1	1	0	ADDR	0/1

(1) When ADDR=1, Address Cycle is 0x5A (Write) and 0x5B (Read)
(2) When ADDR=0, Address Cycle is 0x58 (Write) and 0x59 (Read)

The following procedure is followed to write to the SN65DSI84 I^2C registers.

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI84 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The SN65DSI84 acknowledges the address cycle.
3. The master presents the sub-address (I2C register within SN65DSI84) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI84 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^2C register.
6. The SN65DSI84 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN65DSI84.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the SN65DSI84 I^2C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN65DSI84 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The SN65DSI84 acknowledges the address cycle.
3. The SN65DSI84 transmit the contents of the memory registers MSB-first starting at register 00h. If a write to the SN65DSI84 I2C register occurred prior to the read, then the SN65DSI84 will start at the sub-address specified in the write.
4. The SN65DSI84 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I2C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the SN65DSI84 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure is followed for setting a starting sub-address for I^2C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI84 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The SN65DSI84 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within SN65DSI84) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI84 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

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Control and Status Registers Overview

Many of the SN65DSI84 functions are controlled by the Control and Status Registers (CSR). All CSR registers are accessible through the local I^2C interface.

See the following tables for the SN65DSI84 CSR descriptions. Reserved or undefined bit fields should not be modified. Otherwise, the device may operate incorrectly.

Table 4. CSR Bit Field Definitions – ID Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS(1)
0x00 – 0x08	7:0	Reserved Addresses 0x08 - 0x00 = {0x01, 0x20, 0x20, 0x20, 0x44, 0x53, 0x49, 0x38, 0x35}	Reserved	RO

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)

Table 5. CSR Bit Field Definitions – Reset and Clock Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x09	0	SOFT_RESET This bit automatically clears when set to '1' and returns zeros when read. This bit must be set after the CSR's are updated. This bit must also be set after making any changes to the DIS clock rate or after changing between DSI burst and non-burst modes. 0 – No action (default) 1 – Reset device to default condition excluding the CSR bits.	0	WO
0x0A	7	PLL_LOCK 0 – PLL not locked (default) 1 – PLL locked	0	RO
	3:1	LVDS_CLK_RANGE This field selects the frequency range of the LVDS output clock. 000 – 25 MHz ≤ LVDS_CLK < 37.5 MHz 001 – 37.5 MHz ≤ LVDS_CLK < 62.5 MHz 010 – 62.5 MHz ≤ LVDS_CLK < 87.5 MHz 011 – 87.5 MHz ≤ LVDS_CLK < 112.5 MHz 100 – 112.5 MHz ≤ LVDS_CLK < 137.5 MHz 101 – 137.5 MHz ≤ LVDS_CLK ≤ 154 MHz (default) 110 – Reserved 111 – Reserved	101	RW
	0	HS_CLK_SRC 0 – LVDS pixel clock derived from input REFCLK (default) 1 – LVDS pixel clock derived from MIPI D-PHY channel A HS continuous clock	0	RW
0x0B	7:3	DSI_CLK_DIVIDER When CSR 0x0A.0 = '1', this field controls the divider used to generate the LVDS output clock from the MIPI D-PHY Channel A HS continuous clock. When CSR 0x0A.0 = '0', this field must be programmed to 00000. 00000 – LVDS clock = source clock (default) 00001 – Divide by 2 00010 – Divide by 3 00011 – Divide by 4 • • • 10111 – Divide by 24 11000 – Divide by 25 11001 through 11111 – Reserved	00000	RW
	1:0	REFCLK_MULTIPLIER When CSR 0x0A.0 = '0', this field controls the multiplier used to generate the LVDS output clock from the input REFCLK. When CSR 0x0A.0 = '1', this field must be programmed to 00. 00 – LVDS clock = source clock (default) 01 – Multiply by 2 10 – Multiply by 3 11 – Multiply by 4	00	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)

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Table 5. CSR Bit Field Definitions – Reset and Clock Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x0D	0	PLL_EN When this bit is set, the PLL is enabled with the settings programmed into CSR 0x0A and CSR 0x0B. The PLL should be disabled before changing any of the settings in CSR 0x0A and CSR 0x0B. The input clock source must be active and stable before the PLL is enabled. 0 – PLL disabled (default) 1 – PLL enabled	0	RW

Table 6. CSR Bit Field Definitions – DSI Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x10	4:3	CHA_DSI_LANES This field controls the number of lanes that are enabled for DSI Channel A. 00 – Four lanes are enabled 01 – Three lanes are enabled 10 – Two lanes are enabled 11 – One lane is enabled (default) Note: Unused DSI input pins on the SN65DSI84 should be left unconnected.	11	RW
	0	SOT_ERR_TOL_DIS 0 – Single bit errors are tolerated for the start of transaction SoT leader sequence (default) 1 – No SoT bit errors are tolerated	0	RW
0x11	7:6	CHA_DSI_DATA_EQ This field controls the equalization for the DSI Channel A Data Lanes 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	RW
	3:2	CHA_DSI_CLK_EQ This field controls the equalization for the DSI Channel A Clock 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	RW
0x12	7:0	CHA_DSI_CLK_RANGE This field specifies the DSI Clock frequency range in 5 MHz increments for the DSI Channel A Clock 0x00 through 0x07 – Reserved 0x08 – 40 ≤ frequency < 45 MHz 0x09 – 45 ≤ frequency < 50 MHz • • • 0x63 – 495 ≤ frequency < 500 MHz 0x64 – 500 MHz 0x65 through 0xFF – Reserved	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)

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Table 7. CSR Bit Field Definitions – LVDS Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x18	7	DE_NEG_POLARITY 0 – DE is positive polarity driven ‘1’ during active pixel transmission on LVDS (default) 1 – DE is negative polarity driven ‘0’ during active pixel transmission on LVDS	0	RW
	6	HS_NEG_POLARITY 0 – HS is positive polarity driven ‘1’ during corresponding sync conditions 1 – HS is negative polarity driven ‘0’ during corresponding sync (default)	1	RW
	5	VS_NEG_POLARITY 0 – VS is positive polarity driven ‘1’ during corresponding sync conditions 1 – VS is negative polarity driven ‘0’ during corresponding sync (default)	1	RW
	4	LVDS_LINK_CFG 0 – LVDS Channel A and Channel B outputs enabled When CSR 0x10.6:5 = ’00’ or ‘01’, the LVDS is in Dual-Link configuration When CSR 0x10.6:5 = ‘10’, the LVDS is in two Single-Link configuration 1 – LVDS Single-Link configuration; Channel A output enabled and Channel B output disabled (default)	1	RW
	3	CHA_24BPP_MODE 0 – Force 18bpp; LVDS channel A lane 4 (A_Y3P/N) is disabled (default) 1 – Force 24bpp; LVDS channel B lane 4 (B_Y3P/N) is enabled	0	RW
	2	CHB_24BPP_MODE 0 – Force 18bpp; LVDS channel A lane 4 (A_Y3P/N) is disabled (default) 1 – Force 24bpp; LVDS channel B lane 4 (B_Y3P/N) is enabled	0	RW
	1	CHA_24BPP_FORMAT1 This field selects the 24bpp data format 0 – LVDS channel A lane A_Y3P/N transmits the 2 most significant bits (MSB) per color; Format 2 (default) 1 – LVDS channel B lane B_Y3P/N transmits the 2 least significant bits (LSB) per color; Format 1 Note1: This field must be ‘0’ when 18bpp data is received from DSI. Note2: If this field is set to ‘1’ and CHA_24BPP_MODE is ‘0’, the SN65DSI84 will convert 24bpp data to 18bpp data for transmission to an 18bpp panel. In this configuration, the SN65DSI84 will not transmit the 2 LSB per color on LVDS channel A, since LVDS channel A lane 4 is disabled.	0	RW
	0	CHB_24BPP_FORMAT1 This field selects the 24bpp data format 0 – Data lane 4 transmits the 2 most significant bits (MSB) per color; Format 2 (default) 1 – Data lane 4 transmits the 2 least significant bits (LSB) per color; Format 1 Note1: This field must be ‘0’ when 18bpp data is received from DSI. Note2: If this field is set to ‘1’ and CHB_24BPP_MODE is ‘0’, the SN65DSI84 will convert 24bpp data to 18bpp data for transmission to an 18bpp panel. In this configuration, the SN65DSI84 will not transmit the 2 LSB per color on LVDS channel B, since LVDS channel B lane 4 is disabled.	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write ‘1’ to Clear; WO = Write Only (reads return undetermined values)

Table 7. CSR Bit Field Definitions – LVDS Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x19	6	CHA_LVDS_VOCM This field controls the common mode output voltage for LVDS Channel A 0 – 1.2V (default) 1 – 0.9V (CSR 0x1B.5:4 CHA_LVDS_CM_ADJUST must be set to '01b')	0	RW
	4	CHB_LVDS_VOCM This field controls the common mode output voltage for LVDS Channel B 0 – 1.2V (default) 1 – 0.9V (CSR 0x1B.1:0 CHB_LVDS_CM_ADJUST must be set to '01b')	0	RW
	3:2	CHA_LVDS_VOD_SWING This field controls the differential output voltage for LVDS Channel A. See the Electrical Characteristics table for $\|V_{OD}\|$ for each setting: 00, 01 (default), 10, 11.	01	RW
	1:0	CHB_LVDS_VOD_SWING This field controls the differential output voltage for LVDS Channel B. See the Electrical Characteristics table for $\|V_{OD}\|$ for each setting: 00, 01 (default), 10, 11.	01	RW

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Table 7. CSR Bit Field Definitions – LVDS Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x1A	6	EVEN_ODD_SWAP 0 – Odd pixels routed to LVDS Channel A and Even pixels routed to LVDS Channel B (default) 1 – Odd pixels routed to LVDS Channel B and Even pixels routed to LVDS Channel A Note: When the SN65DSI84 is in two stream mode (CSR 0x10.6:5 = '10'), setting this bit to '1' will cause the video stream from DSI Channel A to be routed to LVDS Channel B and the video stream from DSI Channel B to be routed to LVDS Channel A.	0	RW
	5	CHA_REVERSE_LVDS This bit controls the order of the LVDS pins for Channel A. 0 – Normal LVDS Channel A pin order. LVDS Channel A pin order is the same as listed in the Terminal Assignments Section. (default) 1 – Reversed LVDS Channel A pin order. LVDS Channel A pin order is remapped as follows: • A_Y0P → A_Y3P • A_Y0N → A_Y3N • A_Y1P → A_CLKP • A_Y1N → A_CLKN • A_Y2P → A_Y2P • A_Y2N → A_Y2N • A_CLKP → A_Y1P • A_CLKN → A_Y1N • A_Y3P → A_Y0P • A_Y3N → A_Y0N	0	RW
	4	CHB_REVERSE_LVDS This bit controls the order of the LVDS pins for Channel B. 0 – Normal LVDS Channel B pin order. LVDS Channel B pin order is the same as listed in the Terminal Assignments Section. (default) 1 – Reversed LVDS Channel B pin order. LVDS Channel B pin order is remapped as follows: • B_Y0P → B_Y3P • B_Y0N → B_Y3N • B_Y1P → B_CLKP • B_Y1N → B_CLKN • B_Y2P → B_Y2P • B_Y2N → B_Y2N • B_CLKP → B_Y1P • B_CLKN → B_Y1N • B_Y3P → B_Y0P • B_Y3N → B_Y0N	0	RW
	1	CHA_LVDS_TERM This bit controls the near end differential termination for LVDS Channel A. This bit also affects the output voltage for LVDS Channel A. 0 – 100Ω differential termination 1 – 200Ω differential termination (default)	1	RW
	0	CHB_LVDS_TERM This bit controls the near end differential termination for LVDS Channel B. This bit also affects the output voltage for LVDS Channel B. 0 – 100Ω differential termination 1 – 200Ω differential termination (default)	1	RW

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Table 7. CSR Bit Field Definitions – LVDS Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0x1B	5:4	CHA_LVDS_CM_ADJUST This field can be used to adjust the common mode output voltage for LVDS Channel A. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%	00	RW
	1:0	CHB_LVDS_CM_ADJUST This field can be used to adjust the common mode output voltage for LVDS Channel B. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%	00	RW

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Note for all video registers:

1. TEST PATTERN GENERATION PURPOSE ONLY registers are for test pattern generation use only. Others are for normal operation unless the test pattern generation feature is enabled.

Table 8. CSR Bit Field Definitions – Video Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS(1)
0x20	7:0	CHA_ACTIVE_LINE_LENGTH_LOW This field controls the length in pixels of the active horizontal line line that are received on DSI Channel A and output to LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length.	0	RW
0x21	3:0	CHA_ACTIVE_LINE_LENGTH_HIGH This field controls the length in pixels of the active horizontal line that are received on DSI Channel A and output to LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length.	0	RW
0x24	7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size.	0	RW
0x25	3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 4 bits of the 12-bit value for the vertical display size	0	RW
0x28	7:0	CHA_SYNC_DELAY_LOW This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI84. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 8 bits of the 12-bit value for the Sync delay.	0	RW
0x29	3:0	CHA_SYNC_DELAY_HIGH This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI84. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the upper 4 bits of the 12-bit value for the Sync delay.	0	RW
0x2C	7:0	CHA_HSYNC_PULSE_WIDTH_LOW This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 10-bit value for the HSync Pulse Width.	0	RW
0x2D	1:0	CHA_HSYNC_PULSE_WIDTH_HIGH This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 2 bits of the 10-bit value for the HSync Pulse Width.	0	RW
0x30	7:0	CHA_VSYNC_PULSE_WIDTH_LOW This field controls the length in lines of the VSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 10-bit value for the VSync Pulse Width.	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)

Table 8. CSR Bit Field Definitions – Video Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS(1)
0x31	1:0	CHA_VSYNC_PULSE_WIDTH_HIGH This field controls the length in lines of the VSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 2 bits of the 10-bit value for the VSync Pulse Width.	0	RW
0x34	7:0	CHA_HORIZONTAL_BACK_PORCH This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW
0x36	7:0	CHA_VERTICAL_BACK_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW
0x38	7:0	CHA_HORIZONTAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW
0x3A	7:0	CHA_VERTICAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW
0x3C	4	CHA_TEST_PATTERN TEST PATTERN GENERATION PURPOSE ONLY. When this bit is set, the SN65DSI84 will generate a video test pattern based on the values programmed into the Video Registers for LDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW

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Table 9. CSR Bit Field Definitions – IRQ Registers

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS (1)
0xE0	0	IRQ_EN When enabled by this field, the IRQ output is driven high to communicate IRQ events. 0 – IRQ output is high-impedance (default) 1 – IRQ output is driven high when a bit is set in registers 0xE5 that also has the corresponding IRQ_EN bit set to enable the interrupt condition	0	RW
0xE1	7	CHA_SYNCH_ERR_EN 0 – CHA_SYNCH_ERR is masked 1 – CHA_SYNCH_ERR is enabled to generate IRQ events	0	RW
	6	CHA_CRC_ERR_EN 0 – CHA_CRC_ERR is masked 1 – CHA_CRC_ERR is enabled to generate IRQ events	0	RW
	5	CHA_UNC_ECC_ERR_EN 0 – CHA_UNC_ECC_ERR is masked 1 – CHA_UNC_ECC_ERR is enabled to generate IRQ events	0	RW
	4	CHA_COR_ECC_ERR_EN 0 – CHA_COR_ECC_ERR is masked 1 – CHA_COR_ECC_ERR is enabled to generate IRQ events	0	RW
	3	CHA_LLP_ERR_EN 0 – CHA_LLP_ERR is masked 1 – CHA_ LLP_ERR is enabled to generate IRQ events	0	RW
	2	CHA_SOT_BIT_ERR_EN 0 – CHA_SOT_BIT_ERR is masked 1 – CHA_SOT_BIT_ERR is enabled to generate IRQ events	0	RW
	0	PLL_UNLOCK_EN 0 – PLL_UNLOCK is masked 1 – PLL_UNLOCK is enabled to generate IRQ events	0	RW
0xE5	7	CHA_SYNCH_ERR When the DSI channel A packet processor detects an HS or VS synchronization error, that is, an unexpected sync packet; this bit is set; this bit is cleared by writing a ‘1’ value.	0	RW1C
	6	CHA_CRC_ERR When the DSI channel A packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a ‘1’ value.	0	RW1C
	5	CHA_UNC_ECC_ERR When the DSI channel A packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a ‘1’ value.	0	RW1C
	4	CHA_COR_ECC_ERR When the DSI channel A packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a ‘1’ value.	0	RW1C
	3	CHA_LLP_ERR When the DSI channel A packet processor detects a low level protocol error, this bit is set; this bit is cleared by writing a ‘1’ value. Low level protocol errors include SoT and EoT sync errors, Escape Mode entry command errors, LP transmission sync errors, and false control errors. Lane merge errors are reported by this status condition.	0	RW1C
	2	CHA_SOT_BIT_ERR When the DSI channel A packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a ‘1’ value.	0	RW1C
	0	PLL_UNLOCK This bit is set whenever the PLL Lock status transitions from LOCK to UNLOCK.	1	RW1C

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write ‘1’ to Clear; WO = Write Only (reads return undetermined values)

APPLICATION INFORMATION

Video STOP and Restart sequence

When the system requires to stop outputting video to the display, it is recommended to use the following sequence for the SN65DSI84:

1. Clear the PLL_EN bit to 0(CSR 0x0A.7
2. Stop video streaming on DSI inputs
3. Drive all DSI input lanes including DSI CLK lane to LP11.

When the system is ready to restart the video streaming.

1. Start video streaming on DSI inputs.
2. Set the PLL_EN bit to 1(CSR 0x0D.0).
3. Wait for the PLL_LOCK bit to be set(CSR 0x0A.7).
4. Set the SOFT_RESET bit(0x09.0).

Reverse LVDS Pin Order Option

For ease of PCB routing, the SN65DSI84 supports swapping/reversing the channel or pin order via configuration register programming. The order of the LVDS pin for LVDS Channel A or Channel B can be reversed by setting the address 0x1A bit 5 CHA_REVERSE_LVDS or bit 4 CHB_REVERSE_LVDS. The LVDS Channel A and Channel B can be swapped by setting the 0x1A.6 EVEM_ODD_SWAP bit. See the corresponding register bit definition for details.

IRQ Usage

The SN65DSI84 provides an IRQ pin that can be used to indicate when certain errors occur on DSI. The IRQ output is enabled through the IRQ_EN bit (CSR 0xE0.0). The IRQ pin will be asserted when an error occurs on DSI, the corresponding error enable bit is set, and the IRQ_EN bit is set. An error is cleared by writing a '1' to the corresponding error status bit.

NOTE

If the SOFT_RESET bit is set while the DSI video stream is active, some of the error status bits may be set.

NOTE

If the DSI video stream is stopped, some of the error status bits may be set. These error status bits should be cleared before restarting the video stream.

NOTE

If the DSI video stream starts before the device is configured, some of the error status bits may be set. It is recommended to start streaming after the device is correctly configured as recommended in the initialization sequence in the Recommended Initialization Sequence section.

PRODUCT PREVIEW

Typical WUXGA 18 bpp Application

Figure 19 illustrates a typical application using the SN65DSI84 for a single channel DSI receiver to interface a single-channel DSI application processor to an LVDS Dual-Link 18 bit-per-pixel panel supporting 1920 x 1200 WUXGA resolutions at 60 frames per second.

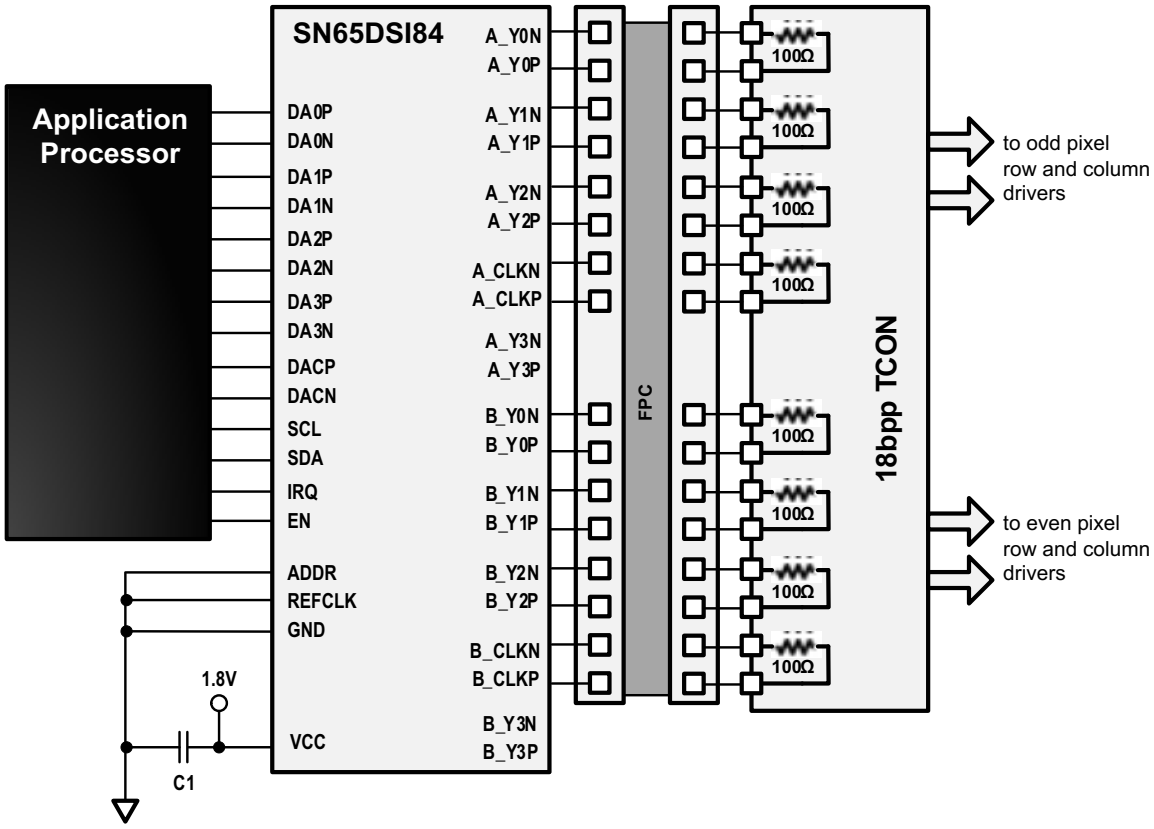


Figure 19. Typical WUXGA 18bpp Panel Application

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65DSI84ZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	64	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

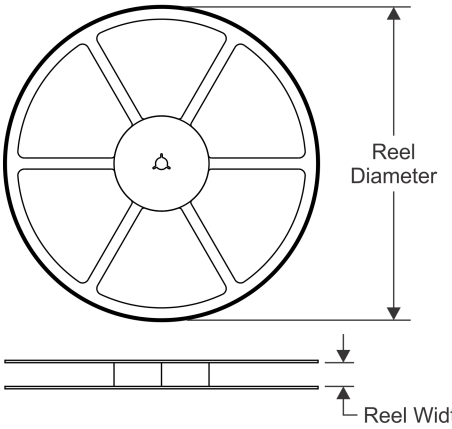
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

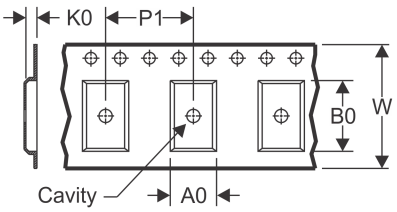
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

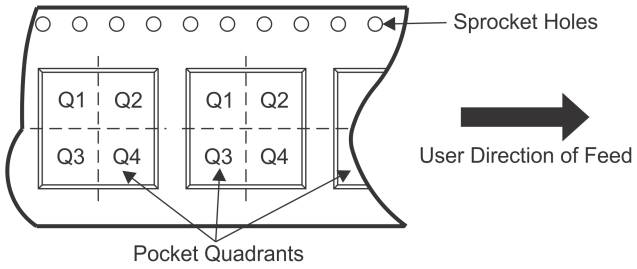


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

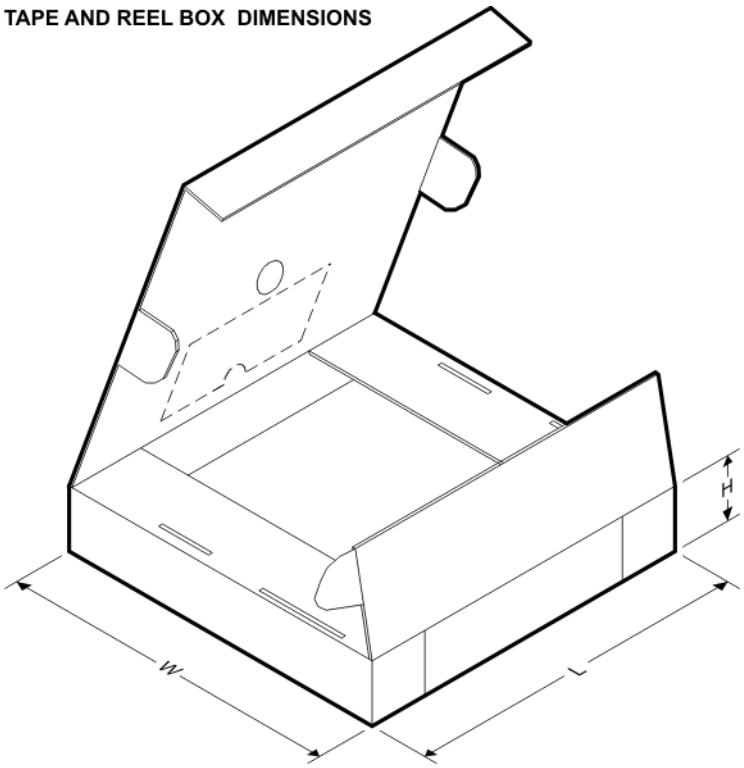
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65DSI84ZQER	BGA MICROSTAR JUNIOR	ZQE	64	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

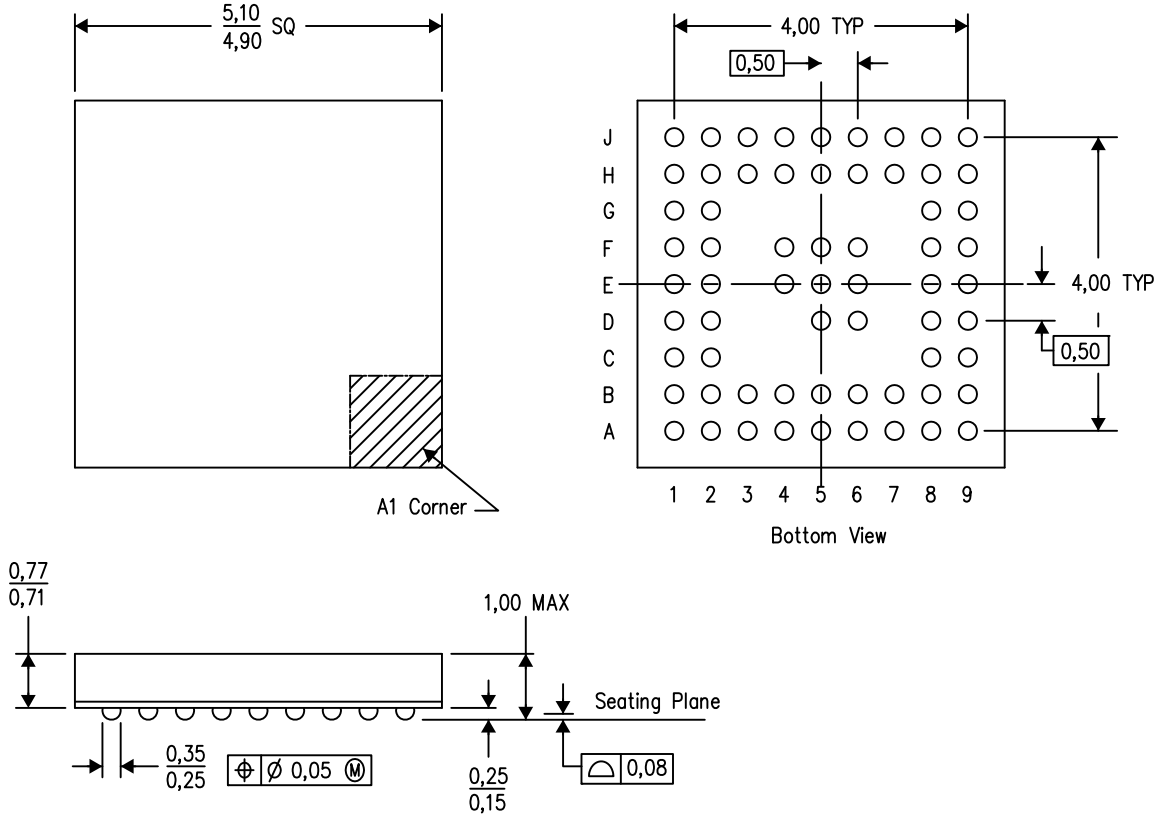
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65DSI84ZQER	BGA MICROSTAR JUNIOR	ZQE	64	2500	336.6	336.6	31.8

ZQE (S–PBGA–N64) PLASTIC BALL GRID ARRAY



4204334–3/G 09/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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