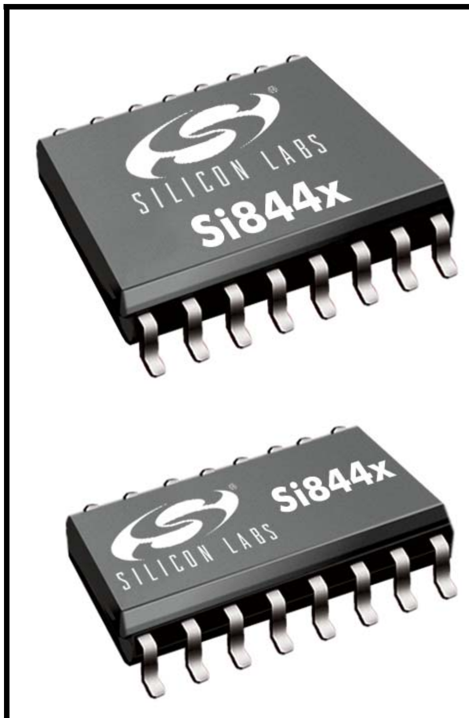
Si8440/41/42/45

LOW-POWER QUAD-CHANNEL DIGITAL ISOLATOR

Features

- High-speed operation
  - DC to 150 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage: 2.70–5.5 V
- Wide Operating Supply Voltage: 2.70–5.5V
- Ultra low power (typical)
  5 V Operation:
  - < 1.6 mA per channel at 1 Mbps
  - < 6 mA per channel at 100 Mbps

  2.70 V Operation:
  - < 1.4 mA per channel at 1 Mbps
  - < 4 mA per channel at 100 Mbps
- High electromagnetic immunity
- Up to 2500 V_{RMS} isolation
- 60-year life at rated working voltage
- Precise timing (typical)
  - <10 ns worst case
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
  - 6 ns minimum pulse width
- Transient Immunity 25 kV/µs
- AEC-Q100 qualified
- Wide temperature range
  - –40 to 125 °C at 150 Mbps
- RoHS-compliant packages
  - SOIC-16 wide body
  - SOIC-16 narrow body



Ordering Information:
See page 27.

Applications

- Industrial automation systems
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Description

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages when compared to legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges throughout their service life. For ease of design, only VDD bypass capacitors are required.

Data rates up to 150 Mbps are supported, and all devices achieve worst-case propagation delays of less than 10 ns. All products are safety certified by UL, CSA, and VDE and support withstand voltages of up to 2.5 kVrms. These devices are available in 16-pin wide- and narrow-body SOIC packages.

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125	ºC
Supply Voltage	V_{DD1}		2.70	—	5.5	V
	V_{DD2}		2.70	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	ºC
Ambient Temperature Under Bias	T_A	–40	—	125	ºC
Supply Voltage (Revision C)[3]	V_{DD1}, V_{DD2}	–0.5	—	5.75	V
Supply Voltage (Revision D)[3]	V_{DD1}, V_{DD2}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	ºC
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may degrade performance.
2. VDE certifies storage temperature from –40 to 150 °C.
3. See "5. Ordering Guide" on page 27 for more information.

Table 3. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	loh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	lol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at Supply)						
Si8440Ax, Bx and Si8445Bx						
V_{DD1}		All inputs 0 DC	—	1.5	2.3	mA
V_{DD2}		All inputs 0 DC	—	2.5	3.8	
V_{DD1}		All inputs 1 DC	—	5.7	8.6	
V_{DD2}		All inputs 1 DC	—	2.6	3.9	
Si8441Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.8	2.7	mA
V_{DD2}		All inputs 0 DC	—	2.5	3.8	
V_{DD1}		All inputs 1 DC	—	4.9	7.4	
V_{DD2}		All inputs 1 DC	—	3.6	5.4	
Si8442Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2.3	3.5	mA
V_{DD2}		All inputs 0 DC	—	2.3	3.5	
V_{DD1}		All inputs 1 DC	—	4.5	6.8	
V_{DD2}		All inputs 1 DC	—	4.5	6.8	
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8440Ax, Bx and Si8445Bx						
V_{DD1}			—	3.6	5.4	mA
V_{DD2}			—	3.0	3.9	
Si8441Ax, Bx						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	3.4	5.1	
Si8442Ax, Bx						
V_{DD1}			—	3.6	5.4	mA
V_{DD2}			—	3.6	5.4	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8440Bx, Si8445Bx V_{DD1} V_{DD2}			— —	3.6 4.0	5.4 5.6	mA
Si8441Bx V_{DD1} V_{DD2}			— —	3.7 4.1	5.5 5.7	mA
Si8442Bx V_{DD1} V_{DD2}			— —	4.2 4.2	5.9 5.9	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8440Bx, Si8445Bx V_{DD1} V_{DD2}			— —	3.8 19.4	5.7 24.3	mA
Si8441Bx V_{DD1} V_{DD2}			— —	8.0 15.8	10 19.8	mA
Si8442Bx V_{DD1} V_{DD2}			— —	11.8 11.8	14.8 14.8	mA
Timing Characteristics						
Si844xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si844xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	3.8	5.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.8	3.7	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Enable to Data Valid[3]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[3]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[3,4]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

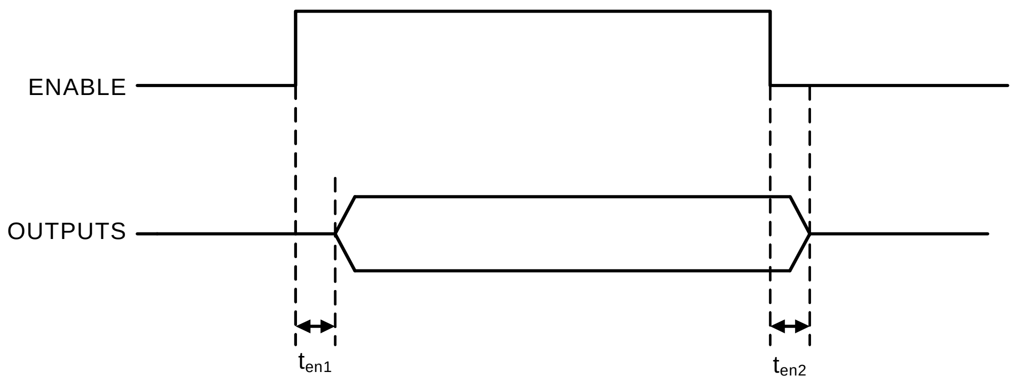


Figure 1. ENABLE Timing Diagram

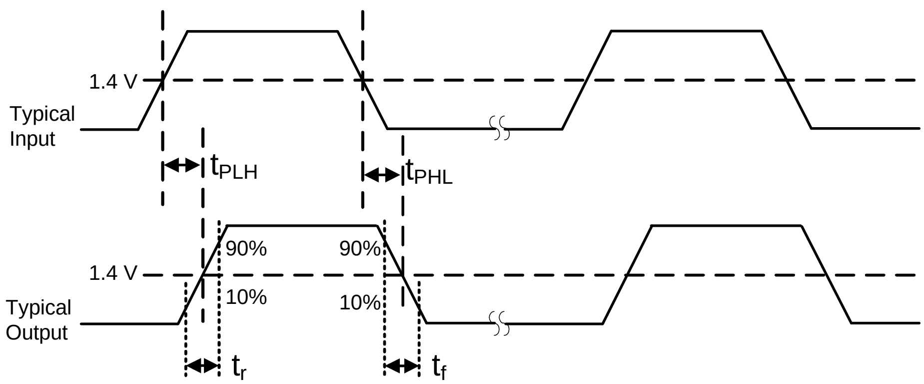


Figure 2. Propagation Delay Timing

Table 4. Electrical Characteristics

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8440Ax, Bx and Si8445Bx						
V_{DD1}		All inputs 0 DC	—	1.5	2.3	mA
V_{DD2}		All inputs 0 DC	—	2.5	3.8	
V_{DD1}		All inputs 1 DC	—	5.7	8.6	
V_{DD2}		All inputs 1 DC	—	2.6	3.9	
Si8441Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.8	2.7	mA
V_{DD2}		All inputs 0 DC	—	2.5	3.8	
V_{DD1}		All inputs 1 DC	—	4.9	7.4	
V_{DD2}		All inputs 1 DC	—	3.6	5.4	
Si8442Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2.3	3.5	mA
V_{DD2}		All inputs 0 DC	—	2.3	3.5	
V_{DD1}		All inputs 1 DC	—	4.5	6.8	
V_{DD2}		All inputs 1 DC	—	4.5	6.8	
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8440Ax, Bx and Si8445Bx						
V_{DD1}			—	3.6	5.4	mA
V_{DD2}			—	3.0	3.9	
Si8441Ax, Bx						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	3.4	5.1	
Si8442Ax, Bx						
V_{DD1}			—	3.6	5.4	mA
V_{DD2}			—	3.6	5.4	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8440Bx, Si8445Bx V_{DD1} V_{DD2}			— —	3.6 4.0	5.4 5.6	mA
Si8441Bx V_{DD1} V_{DD2}			— —	3.7 4.1	5.5 5.7	mA
Si8442Bx V_{DD1} V_{DD2}			— —	4.2 4.2	5.9 5.9	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8440Bx, Si8445Bx V_{DD1} V_{DD2}			— —	3.6 14	5.5 17.5	mA
Si8441Bx V_{DD1} V_{DD2}			— —	6.4 11.4	8.0 14.5	mA
Si8442Bx V_{DD1} V_{DD2}			— —	8.6 8.6	10.8 10.8	mA
Timing Characteristics						
Si844xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL},t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si844xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	4.3	6.1	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	3.0	4.3	ns
Common Mode Transient Immunity at Logic Low Output	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Enable to Data Valid[3]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[3]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[3,4]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1]
(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8440Ax, Bx and Si8445Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 1.5 2.5 5.7 2.6	 2.3 3.8 8.6 3.9	 mA
Si8441Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 1.8 2.5 4.9 3.6	 2.7 3.8 7.4 5.4	 mA
Si8442Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 2.3 2.3 4.5 4.5	 3.5 3.5 6.8 6.8	 mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8440Ax, Bx and Si8445Bx V_{DD1} V_{DD2}			 — —	 3.6 3.0	 5.4 3.9	 mA
Si8441Ax, Bx V_{DD1} V_{DD2}			 — —	 3.5 3.4	 5.3 5.1	 mA
Si8442Ax, Bx V_{DD1} V_{DD2}			 — —	 3.6 3.6	 5.4 5.4	 mA

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
5. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)
(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8440Bx, Si8445Bx V_{DD1} V_{DD2}			— —	3.6 4.0	5.4 5.6	mA
Si8441Bx V_{DD1} V_{DD2}			— —	3.7 4.1	5.5 5.7	mA
Si8442Bx V_{DD1} V_{DD2}			— —	4.2 4.2	5.9 5.9	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8440Bx, Si8445Bx V_{DD1} V_{DD2}			— —	3.6 10.8	5.5 13.5	mA
Si8441Bx V_{DD1} V_{DD2}			— —	5.6 9.3	7.0 11.6	mA
Si8442Bx V_{DD1} V_{DD2}			— —	7.2 7.2	9.0 9.0	mA
Timing Characteristics						
Si844xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
5. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)
(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si844xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	4.8	6.5	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	3.2	4.6	ns
Common Mode Transient Immunity at Logic Low Output	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Enable to Data Valid[4]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[4]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[4,5]	t_{SU}		—	15	40	µs

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. See "3. Errata and Design Migration Guidelines" on page 25 for more details.
5. Start-up time is the time period from the application of power to valid data at the output.

Table 6. Regulatory Information*

CSA
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 130 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 560 V_{peak} for basic insulation working voltage.
UL
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V_{RMS} isolation voltage for basic insulation.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. For more information, see "5. Ordering Guide" on page 27.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB SOIC-16	NB SOIC-16	
Nominal Air Gap (Clearance)[1]	L(IO1)		8.0	4.9	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		8.0	4.01	mm
Minimum Internal Gap (Internal Clearance)			0.008	0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	V_{RMS}
Erosion Depth	ED		0.040	0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in “6. Package Outline: 16-Pin Wide Body SOIC” and “8. Package Outline: 16-Pin Narrow Body SOIC”. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 package and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16 package and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Condition	Specification
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max		Unit
					WB SOIC-16	NB SOIC-16	
Case Temperature	T_S		—	—	150	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	220	210	mA
Device Power Dissipation[2]	P_D		—	—	275	275	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 3 and 4.
2. The Si844x is tested with VDD1 = VDD2 = 5.5 V, TJ = 150 ºC, CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ		Max	Unit
				WB SOIC-16	NB SOIC-16		
IC Junction-to-Air Thermal Resistance	θ_{JA}		—	100	105	—	ºC/W

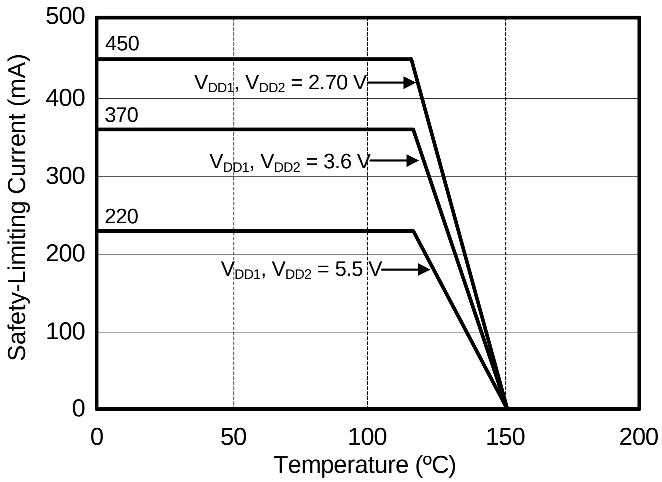


Figure 3. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

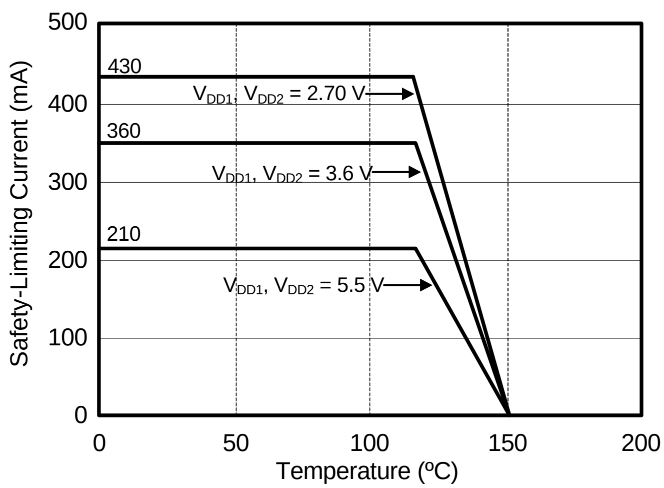


Figure 4. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Functional Description

2.1. Theory of Operation

The operation of an Si844x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si844x channel is shown in Figure 5.

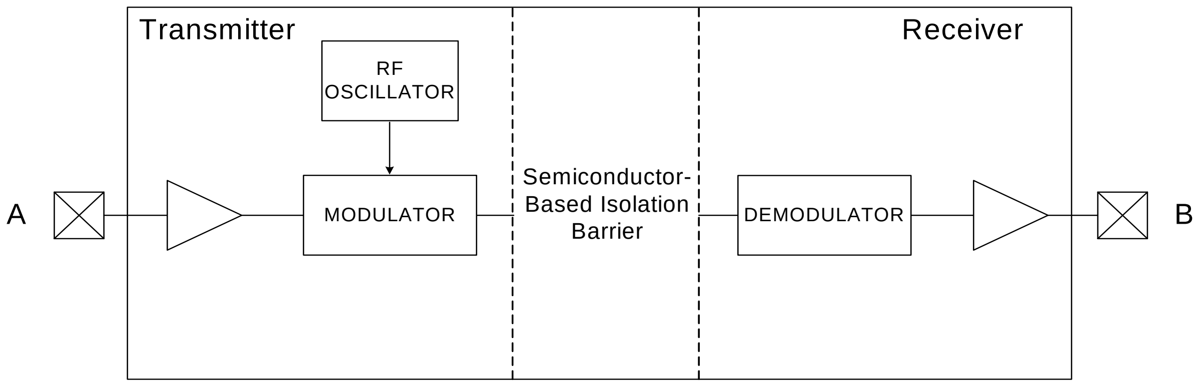


Figure 5. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 6 for more details.

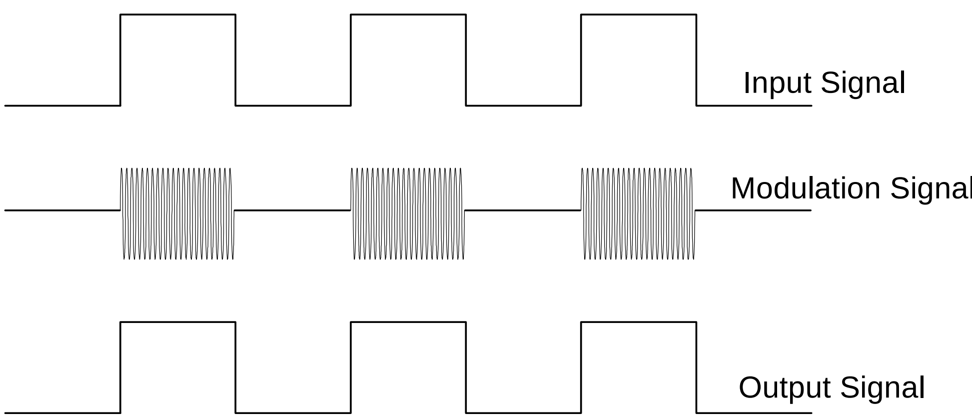


Figure 6. Modulation Scheme

2.2. Eye Diagram

Figure 7 illustrates an eye-diagram taken on an Si8440. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8440 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 250 ps peak jitter were exhibited.

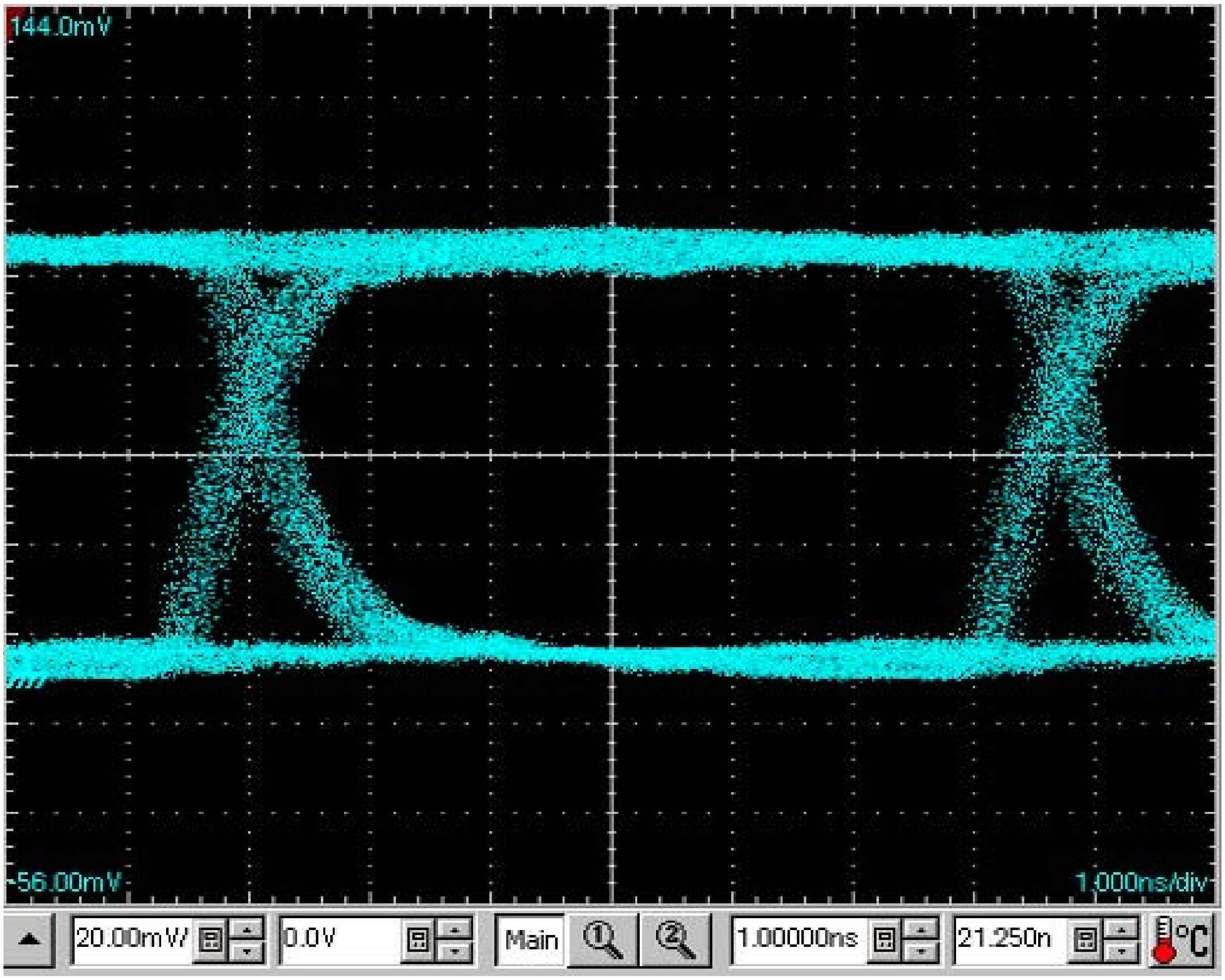


Figure 7. Eye Diagram

2.3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Table 12. Table 13 provides an overview of the output states when the Enable pins are active.

Table 12. Si84xx Logic Operation Table

V_I Input[1,2]	EN Input[1,2,3,4]	VDDI State[1,5,6]	VDDO State[1,5,6]	V_O Output[1,2]	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X[7]	L	P	P	Hi-Z or L[8]	Disabled.
X[7]	H or NC	UP	P	L	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[7]	L	UP	P	Hi-Z or L[8]	Disabled.
X[7]	X[7]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V_O returns to Hi-Z within 1 µs if EN is L.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si84xx is operating in noisy environments.
4. No Connect (NC) replaces EN1 on Si8440/45. No Connect replaces EN2 on the Si8445. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. "Powered" state (P) is defined as 2.70 V < VDD < 5.5 V.
6. "Unpowered" state (UP) is defined as VDD = 0 V.
7. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
8. When using the enable pin (EN) function, the output pin state is driven to a logic low state when the EN pin is disabled (EN = 0) in Revision C. Revision D outputs go into a high-impedance state when the EN pin is disabled (EN = 0). See "3. Errata and Design Migration Guidelines" on page 25 for more details.

Table 13. Enable Input Truth Table[1]

P/N	EN1[1,2]	EN2[1,2]	Operation
Si8440	—	H	Outputs B1, B2, B3, B4 are enabled and follow the input state.
	—	L	Outputs B1, B2, B3, B4 are disabled and Logic Low or in high impedance state.[3]
Si8441	H	X	Output A4 enabled and follows the input state.
	L	X	Output A4 disabled and Logic Low or in high impedance state.[3]
	X	H	Outputs B1, B2, B3 are enabled and follow the input state.
	X	L	Outputs B1, B2, B3 are disabled and Logic Low or in high impedance state.[3]
Si8442	H	X	Outputs A3 and A4 are enabled and follow the input state.
	L	X	Outputs A3 and A4 are disabled and Logic Low or in high impedance state.[3]
	X	H	Outputs B1 and B2 are enabled and follow the input state.
	X	L	Outputs B1 and B2 are disabled and Logic Low or in high impedance state.[3]
Si8445	—	—	Outputs B1, B2, B3, B4 are enabled and follow the input state.

Notes:

1. Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. EN1, EN2 logic operation is summarized for each isolator product in Table 13. These inputs are internally pulled-up to local VDD by a 3 µA current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the Si84xx is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state is driven to a logic low state when the EN pin is disabled (EN = 0) in Revision C. Revision D outputs go into a high-impedance state when the EN pin is disabled (EN = 0). See "3. Errata and Design Migration Guidelines" on page 25 for more details.

2.4. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 6 on page 15 and Table 7 on page 15 detail the working voltage and creepage/clearance capabilities of the Si84xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, etc.) requirements before starting any design that uses a digital isolator.

The following sections detail the recommended bypass and decoupling components necessary to ensure robust overall performance and reliability for systems using the Si84xx digital isolators.

2.4.1. Supply Bypass

Digital integrated circuit components typically require 0.1 µF (100 nF) bypass capacitors when used in electrically quiet environments. However, digital isolators are commonly used in hazardous environments with excessively noisy power supplies. To counteract these harsh conditions, it is recommended that an additional 1 µF bypass capacitor be added between VDD and GND on both sides of the package. The capacitors should be placed as close as possible to the package to minimize stray inductance. If the system is excessively noisy, it is recommended that the designer add 50 to 100 Ω resistors in series with the VDD supply voltage source and 50 to 300 Ω resistors in series with the digital inputs/outputs (see Figure 8). For more details, see "3. Errata and Design Migration Guidelines" on page 25.

All components upstream or downstream of the isolator should be properly decoupled as well. If these components are not properly decoupled, their supply noise can couple to the isolator inputs and outputs, potentially causing damage if spikes exceed the maximum ratings of the isolator (6 V). In this case, the 50 to 300 Ω resistors protect the isolator's inputs/outputs (note that permanent device damage may occur if the absolute maximum ratings are exceeded). Functional operation should be restricted to the conditions specified in Table 1, “Recommended Operating Conditions,” on page 4.

2.4.2. Pin Connections

No connect pins are not internally connected. They can be left floating, tied to V_{DD}, or tied to GND.

2.4.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. The series termination resistor values should be scaled appropriately while keeping in mind the recommendations described in “2.4.1. Supply Bypass” above.

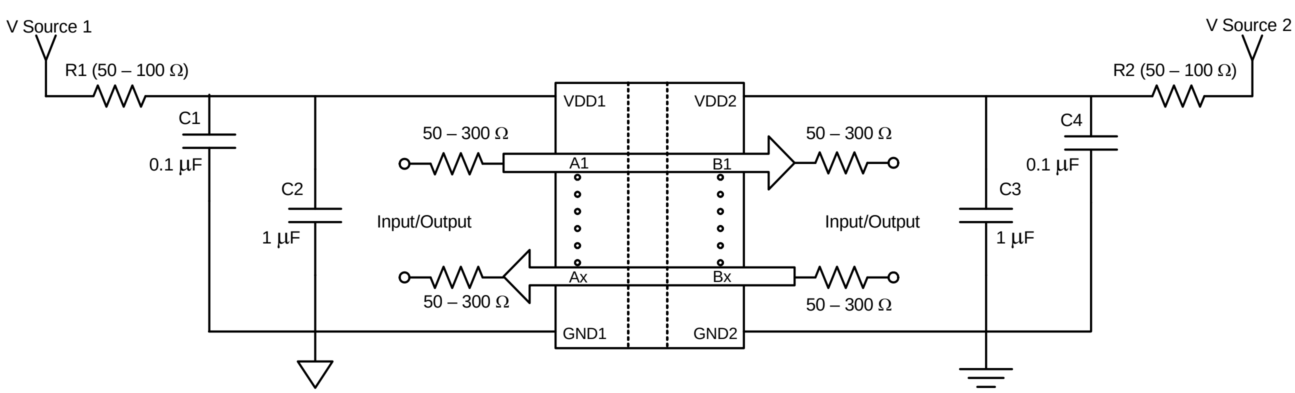


Figure 8. Recommended Bypass Components for the Si84xx Digital Isolator Family

2.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 3, 4, and 5 for actual specification limits.

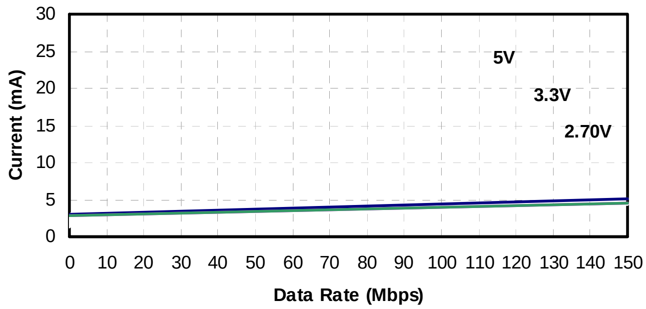


Figure 9. Si8440/45 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

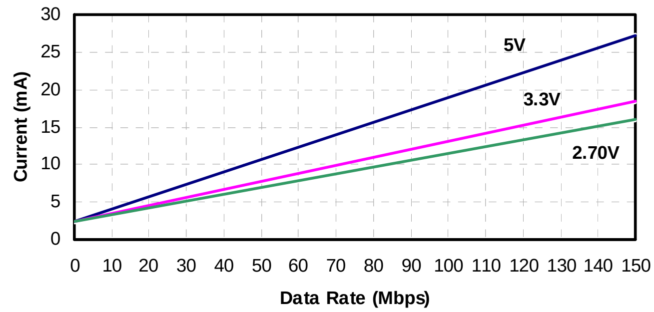


Figure 12. Si8440/45 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V

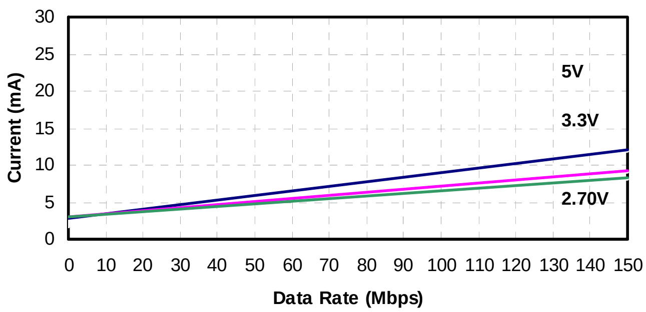


Figure 10. Si8441 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

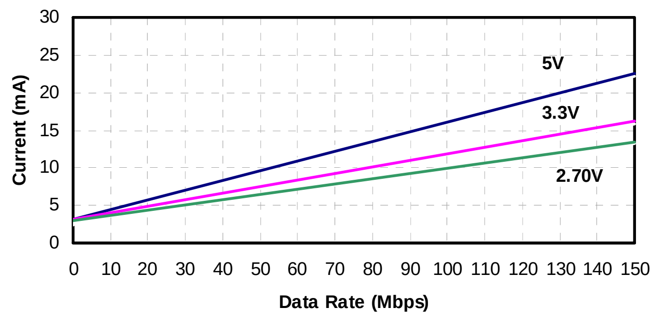


Figure 13. Si8441 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

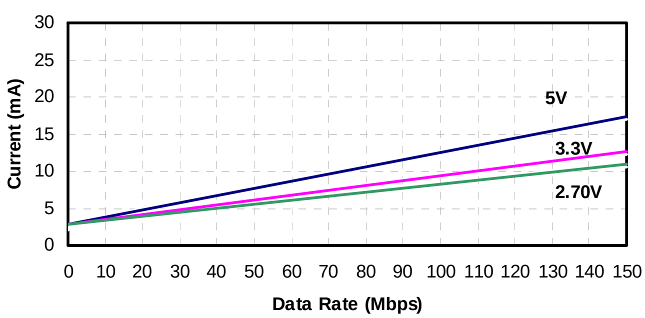


Figure 11. Si8442 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

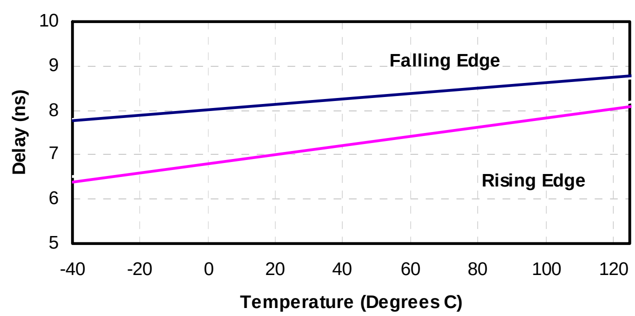


Figure 14. Propagation Delay vs. Temperature

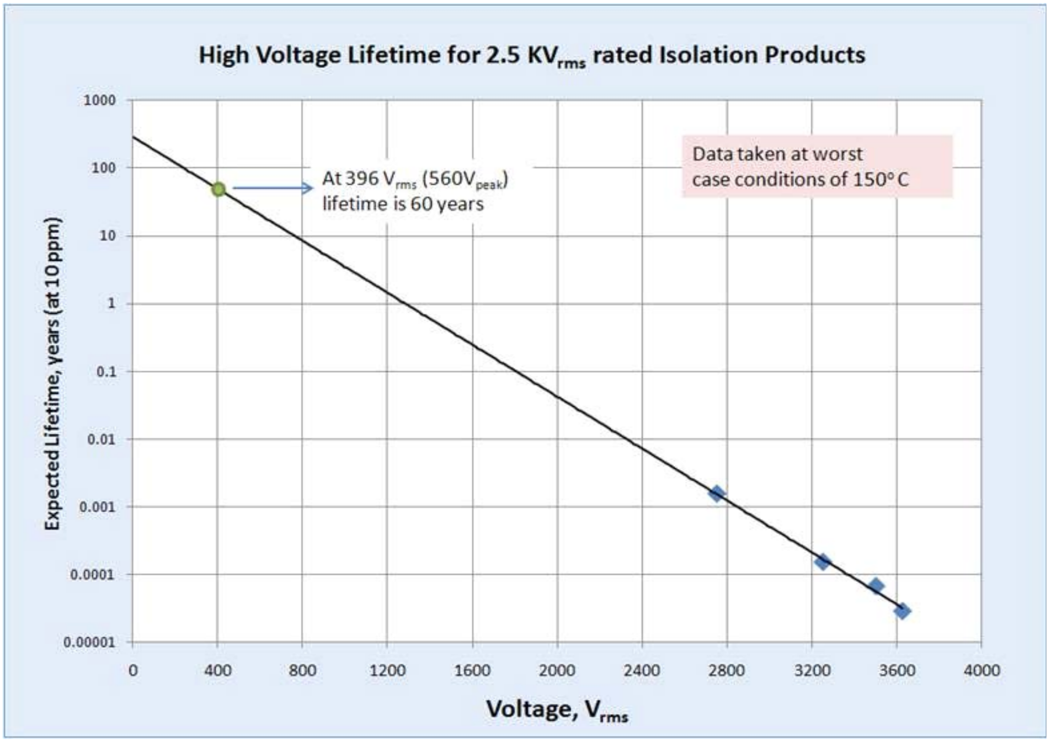


Figure 15. Si84xx Time-Dependent Dielectric Breakdown

3. Errata and Design Migration Guidelines

The following errata apply to Revision C devices only. See "5. Ordering Guide" on page 27 for more details. No errata exist for Revision D devices.

3.1. Enable Pin Causes Outputs to Go Low (Revision C Only)

When using the enable pin (EN1, EN2) function on the 4-channel (Si8440/1/2) isolators, the corresponding output pin states (pin = An, Bn, where n can be 1…4) are driven to a logic low (to ground) when the enable pin is disabled (EN1 or EN2 = 0). This functionality is different from the legacy 4-channel (Si8440/1/2) isolators. On those devices, the isolator outputs go into a high-impedance state (Hi-Z) when the enable pin is disabled (EN1 = 0 or EN2 = 0).

3.1.1. Resolution

The enable pin functionality causing the outputs to go low is supported in production for Revision C of the Si844x devices. Revision D corrects the enable pin functionality (i.e., the outputs will go into the high-impedance state to match the legacy isolator products). Refer to the Ordering Guide sections of the data sheet(s) for current ordering information.

3.2. Power Supply Bypass Capacitors (Revision C and Revision D)

When using the Si844x isolators with power supplies ≥ 4.5 V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than 0.5 V/µs (which is > 9 µs for a ≥ 4.5 V supply). Although rise time is power supply dependent, ≥ 1 µF capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

3.2.1. Resolution

For recommendations on resolving this issue, see "2.4.1. Supply Bypass" on page 22. Additionally, refer to "5. Ordering Guide" on page 27 for current ordering information.

3.3. Latch Up Immunity (Revision C Only)

Latch up immunity generally exceeds ± 200 mA per pin. Exceptions: Certain pins provide < 100 mA of latch-up immunity. To increase latch-up immunity on these pins, 100 Ω of equivalent resistance must be included in series with *all* of the pins listed in Table 14. The 100 Ω equivalent resistance can be comprised of the source driver's output resistance and a series termination resistor. The Si8441 is not affected when using power supply voltages (VDD1 and VDD2) ≤ 3.5 V.

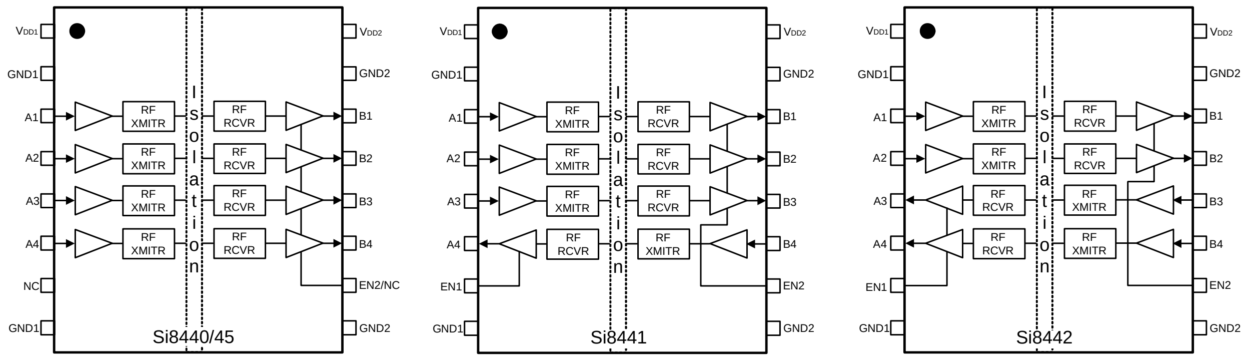
3.3.1. Resolution

This issue has been corrected with Revision D of the device. Refer to “5. Ordering Guide” for current ordering information.

Table 14. Affected Ordering Part Numbers (Revision C Only)

Affected Ordering Part Numbers*	Device Revision	Pin#	Name	Pin Type
SI8440SV-C-IS/IS1, SI8441SV-C-IS/IS1, SI8442SV-C-IS/IS1	C	6	A4	Input or Output
		10	EN2	Input
		14	B1	Output
SI8445SV-C-IS/IS1	C	6	A4	Input
		14	B1	Output
***Note:** SV = Speed Grade/Isolation Rating (AA, AB, BA, BB).				

4. Pin Descriptions



Name	SOIC-16 Pin#	Type	Description[1]
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital I/O	Side 1 digital input or output.
A4	6	Digital I/O	Side 1 digital input or output.
EN1/NC[2]	7	Digital Input	Side 1 active high enable. NC on Si8440/45.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2/NC[2]	10	Digital Input	Side 2 active high enable. NC on Si8445.
B4	11	Digital I/O	Side 2 digital input or output.
B3	12	Digital I/O	Side 2 digital input or output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.

Notes:

1. For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground.
2. No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.

5. Ordering Guide

Revision D devices are recommended for all new designs.

Table 15. Ordering Guide for Valid OPNs[1]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Temp Range	Package Type
Revision D Devices[2]						
Si8440AA-D-IS1	4	0	1			
Si8440BA-D-IS1	4	0	150			
Si8441AA-D-IS1	3	1	1			
Si8441BA-D-IS1	3	1	150	1 kVrms	–40 to 125 °C	NB SOIC-16[1]
Si8442AA-D-IS1	2	2	1			
Si8442BA-D-IS1	2	2	150			
Si8445BA-D-IS1	4	0	150			
Si8440AB-D-IS	4	0	1			
Si8440BB-D-IS	4	0	150			
Si8441AB-D-IS	3	1	1			
Si8441BB-D-IS	3	1	150	2.5 kVrms	–40 to 125 °C	WB SOIC-16[1,3]
Si8442AB-D-IS	2	2	1			
Si8442BB-D-IS	2	2	150			
Si8445BB-D-IS	4	0	150			
Si8440AB-D-IS1	4	0	1			
Si8440BB-D-IS1	4	0	150			
Si8441AB-D-IS1	3	1	1			
Si8441BB-D-IS1	3	1	150	2.5 kVrms	–40 to 125 °C	NB SOIC-16[1]
Si8442AB-D-IS1	2	2	1			
Si8442BB-D-IS1	2	2	150			
Si8445BB-D-IS1	4	0	150			

Notes:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
   Moisture sensitivity level is MSL2A for wide-body SOIC-16 packages.
   Moisture sensitivity level is MSL2A for narrow-body SOIC-16 packages.
2. Revision C devices are supported for existing designs, but Revision D is recommended for all new designs.
3. AEC-Q100 qualified.

Table 15. Ordering Guide for Valid OPNs[1] (Continued)

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Temp Range	Package Type
Revision C Devices[2]						
Si8440AA-C-IS1	4	0	1	1 kVrms	–40 to 125 °C	NB SOIC-16[1]
Si8440BA-C-IS1	4	0	150			
Si8441AA-C-IS1	3	1	1			
Si8441BA-C-IS1	3	1	150			
Si8442AA-C-IS1	2	2	1			
Si8442BA-C-IS1	2	2	150			
Si8445BA-C-IS1	4	0	150			
Si8440AB-C-IS	4	0	1	2.5 kVrms	–40 to 125 °C	WB SOIC-16[1]
Si8440BB-C-IS	4	0	150			
Si8441AB-C-IS	3	1	1			
Si8441BB-C-IS	3	1	150			
Si8442AB-C-IS	2	2	1			
Si8442BB-C-IS	2	2	150			
Si8445BB-C-IS	4	0	150			
Si8440AB-C-IS1	4	0	1	2.5 kVrms	–40 to 125 °C	NB SOIC-16[1]
Si8440BB-C-IS1	4	0	150			
Si8441AB-C-IS1	3	1	1			
Si8441BB-C-IS1	3	1	150			
Si8442AB-C-IS1	2	2	1			
Si8442BB-C-IS1	2	2	150			
Si8445BB-C-IS1	4	0	150			

Notes:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
   Moisture sensitivity level is MSL2A for wide-body SOIC-16 packages.
   Moisture sensitivity level is MSL2A for narrow-body SOIC-16 packages.
2. Revision C devices are supported for existing designs, but Revision D is recommended for all new designs.
3. AEC-Q100 qualified.

6. Package Outline: 16-Pin Wide Body SOIC

Figure 16 illustrates the package details for the Si844x Digital Isolator. Table 16 lists the values for the dimensions shown in the illustration.

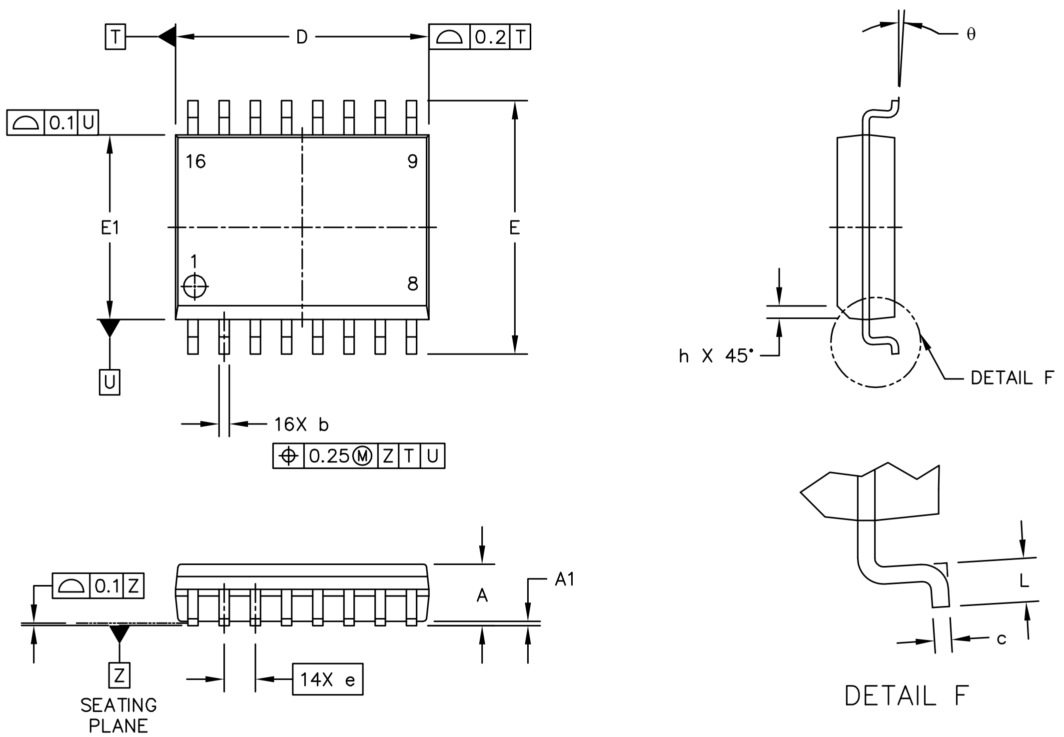


Figure 16. 16-Pin Wide Body SOIC

Table 16. Package Diagram Dimensions

Symbol	Millimeters	
	Min	**Max**
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

7. Land Pattern: 16-Pin Wide-Body SOIC

Figure 17 illustrates the recommended land pattern details for the Si844x in a 16-pin wide-body SOIC. Table 17 lists the values for the dimensions shown in the illustration.

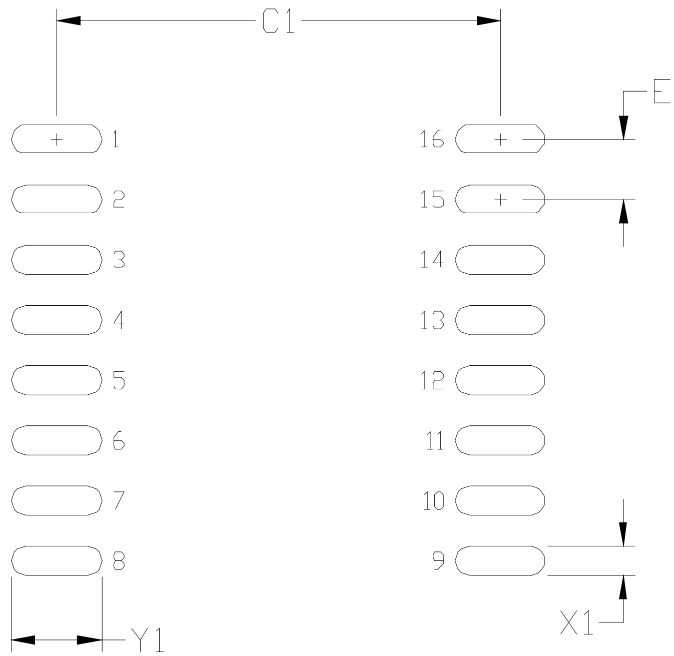


Figure 17. 16-Pin SOIC Land Pattern

Table 17. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Package Outline: 16-Pin Narrow Body SOIC

Figure 18 illustrates the package details for the Si844x in a 16-pin narrow-body SOIC (SO-16). Table 18 lists the values for the dimensions shown in the illustration.

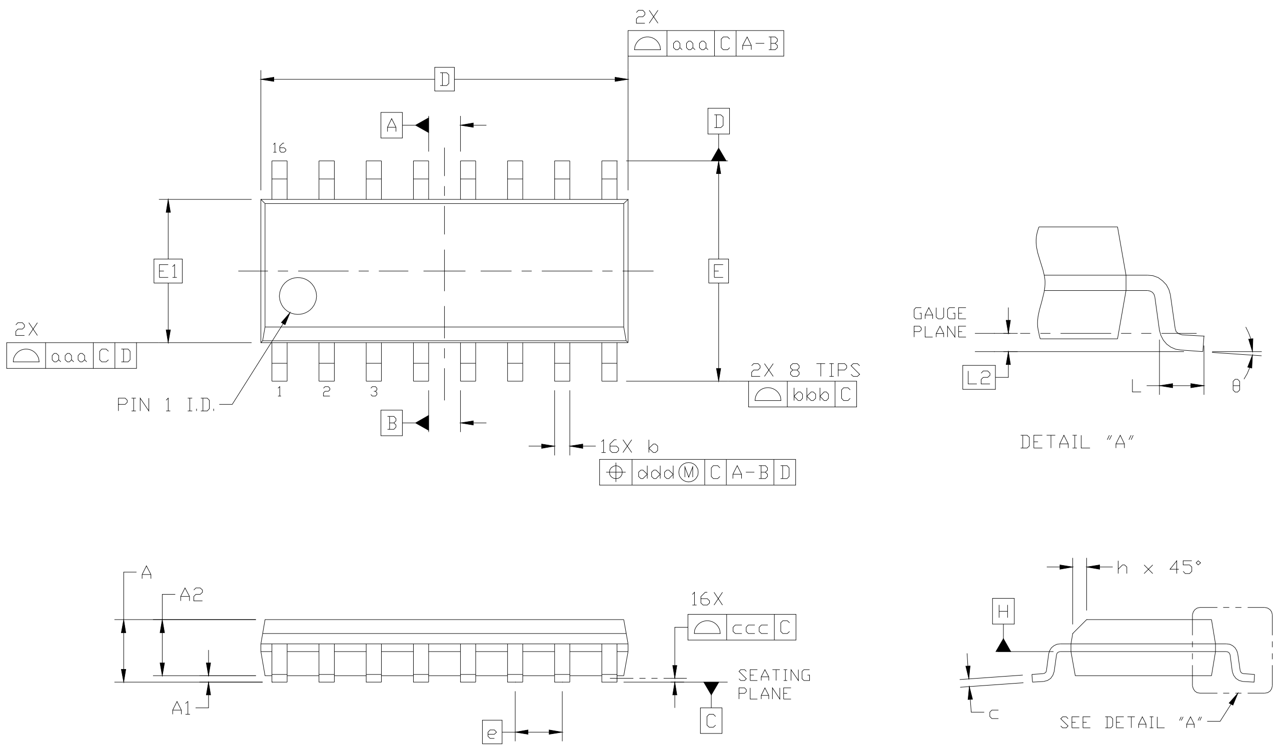


Figure 18. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 18. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

Table 18. Package Diagram Dimensions (Continued)

h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Land Pattern: 16-Pin Narrow Body SOIC

Figure 19 illustrates the recommended land pattern details for the Si844x in a 16-pin narrow-body SOIC. Table 19 lists the values for the dimensions shown in the illustration.

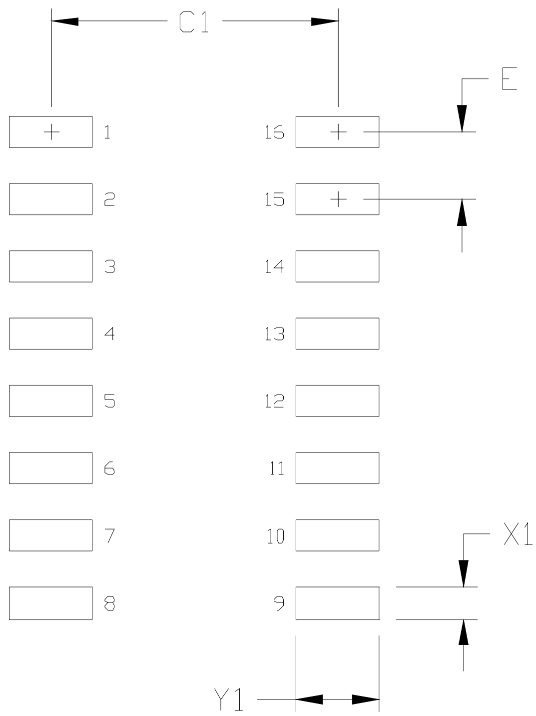


Figure 19. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 19. 16-Pin Narrow Body SOIC Land Pattern Dimensions

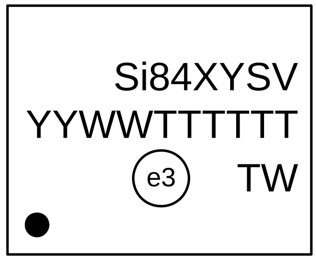
Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Marking: 16-Pin Wide Body SOIC

10.1. 16-Pin Wide Body SOIC Top Marking

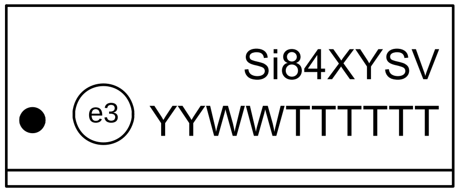


10.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (4, 3, 2, 1) Y = # of reverse channels (2, 1, 0)* S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly House
Line 3 Marking:	Circle = 1.5 mm Diameter (Center-Justified)	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan
***Note:** Si8445 has 0 reverse channels.		

11. Top Marking: 16-Pin Narrow Body SOIC

11.1. 16-Pin Narrow Body SOIC Top Marking



11.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (4, 3, 2, 1) Y = # of reverse channels (2, 1, 0)* S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.
	Circle = 1.2 mm diameter	“e3” Pb-Free Symbol.
***Note:** Si8445 has 0 reverse channels.		

Document Change List

Revision 0.62 to Revision 0.63

- Rev 0.63 is the first revision of this document that applies to the new series of ultra low power isolators featuring pinout and functional compatibility with previous isolator products.
- Updated “1. Electrical Specifications”.
- Updated “5. Ordering Guide”.
- Added “10. Top Marking: 16-Pin Wide Body SOIC”.

Revision 0.63 to Revision 0.64

- Updated all specs to reflect latest silicon.

Revision 0.64 to Revision 0.65

- Updated all specs to reflect latest silicon.
- Added "3. Errata and Design Migration Guidelines" on page 25.
- Added "11. Top Marking: 16-Pin Narrow Body SOIC" on page 35.

Revision 0.65 to Revision 1.0

- Updated document to reflect availability of Revision D silicon.
- Updated Tables 3,4, and 5.
  - Updated all supply currents and channel-channel skew.
- Updated Table 2.
  - Updated absolute maximum supply voltage.
- Updated Table 7.
  - Updated clearance and creepage dimensions.
- Updated Table 12.
  - Updated Note 7.
- Updated Table 13.
  - Updated Note 3.
- Updated "3. Errata and Design Migration Guidelines" on page 25.
- Updated "5. Ordering Guide" on page 27.

Revision 1.0 to Revision 1.1

- Updated Tables 3, 4, and 5.
  - Updated notes in both tables to reflect output impedance of 85 Ω.
  - Updated rise and fall time specifications.
  - Updated CMTI value.

Revision 1.1 to Revision 1.2

- Updated document throughout to include MSL improvements to MSL2A.
- Updated "5. Ordering Guide" on page 27.
  - Updated Note 1 in ordering guide table to reflect improvement and compliance to MSL2A moisture sensitivity level.

Revision 1.2 to Revision 1.3

- Updated " Features" on page 1.
- Moved Tables 1 and 2 to page 4.
- Updated Tables 6, 7, 8, and 9.
- Updated Table 12 footnotes.
- Added Figure 15, “Si84xx Time-Dependent Dielectric Breakdown,” on page 24.

Revision 1.3 to Revision 1.4

- Updated "2.4.1. Supply Bypass" on page 22.
- Added Figure 8, “Recommended Bypass Components for the Si84xx Digital Isolator Family,” on page 22.
- Updated "3.2. Power Supply Bypass Capacitors (Revision C and Revision D)" on page 25.

Revision 1.4 to Revision 1.5

- Updated "5. Ordering Guide" on page 27 to include MSL2A.

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.