Skyworks

Si5316

Precision Clock Jitter Attenuator

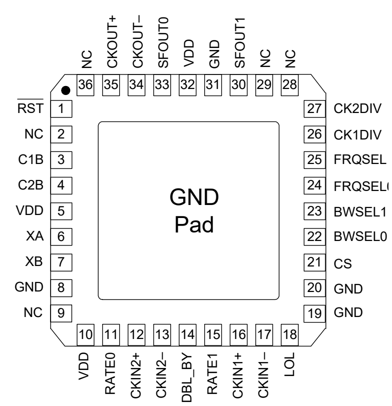
Features

- Fixed frequency jitter attenuator with selectable clock ranges at 19, 38, 77, 155, 311, and 622 MHz (710 MHz max)
- Support for SONET, 10GbE, 10GFC, and corresponding FEC rates
- Ultra-low jitter clock output with jitter generation as low as 0.3 ps_{RMS} (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (100 Hz–7.9 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Dual clock inputs with integrated clock select mux
- One clock input can be 1x, 4x, or 32x the frequency of the second clock input
- Single clock output with selectable signal format: LVPECL, LVDS, CML, CMOS
- LOL, LOS alarm outputs
- Pin programmable settings
- On-chip voltage regulator for 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10% operation
- Small size (6 x 6 mm 36-lead QFN)
- Pb-free, RoHS compliant

Ordering Information:
See page 20.

Pin Assignments

Si5316



Patents pending

Applications

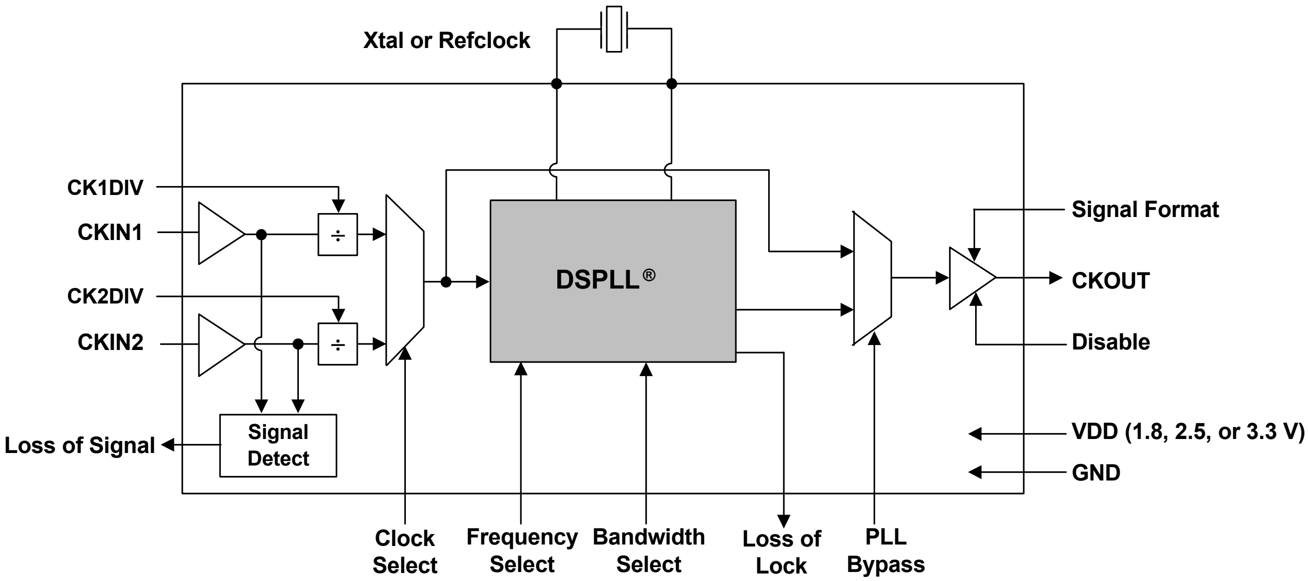
- Optical modules
- SONET/SDH OC-48/OC-192/STM-16/STM-64 line cards
- 10GbE, 10GFC line cards
- ITU G.709 line cards
- Wireless basestations
- Test and measurement
- Synchronous Ethernet

Description

The Si5316 is a low jitter, precision jitter attenuator for high-speed communication systems, including OC-48, OC-192, 10G Ethernet, and 10G Fibre Channel. The Si5316 accepts dual clock inputs in the 19, 38, 77, 155, 311, or 622 MHz frequency range and generates a jitter-attenuated clock output at the same frequency. Within each of these clock ranges, the device can be tuned approximately 15% higher than nominal SONET/SDH frequencies, up to a maximum of 710 MHz in the 622 MHz range.

The Si5316 is based on Skyworks Solutions' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5316 is ideal for providing jitter attenuation in high performance timing applications.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}	3.3 V nominal	2.97	3.3	3.63	V
		2.5 V nominal	2.25	2.5	2.75	V
		1.8 V nominal	1.71	1.8	1.89	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Current (Supply current is independent of V_{DD})	I_{DD}	LVPECL Format 622.08 MHz Out	—	217	243	mA
		CMOS Format 19.44 MHz Out	—	194	220	mA
CKIN Input Pins						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ±5%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
		3.3 V ±10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Input Voltage Level Limits	CKN_{VIN}	See note [2]	0	—	V_{DD}	V
Single-ended Input Voltage Swing	V_{ISE}	$f_{CKIN} \le$ 212.5 MHz See Figure 6.	0.2	—	—	V_{PP}
		$f_{CKIN} >$ 212.5 MHz See Figure 6.	0.25	—	—	V_{PP}
Differential Input Voltage Swing	V_{ID}	$f_{CKIN} \le$ 212.5 MHz See Figure 6.	0.2	—	—	V_{PP}
		$f_{CKIN} >$ 212.5 MHz See Figure 6.	0.25	—	—	V_{PP}

Notes:
1. LVPECL outputs require nominal $V_{DD} \ge$ 2.5 V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 10. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Clock (CKOUT)[1]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single-ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD} – 0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVDS, LVPECL	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V
Output Drive Current	CKO_{IO}	CMOS Driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally.				
		V_{DD} = 1.8 V	—	7.5	—	mA
		V_{DD} = 3.3 V	—	32	—	mA

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq 2.5$ V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 10. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V
Input Low Current	I_{IL}		—	—	50	µA
Input High Current	I_{IH}		—	—	50	µA
Weak Internal Input Pull-up Resistor	R_{PUP}		—	75	—	kΩ
Weak Internal Input Pull-down Resistor	R_{PDN}		—	75	—	kΩ
3-Level Input Pins						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}[3]		–20	—	—	µA
Input Mid Current	I_{IMM}[3]		–2	—	2	µA
Input High Current	I_{IHH}[3]		—	—	20	µA

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq 2.5$ V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 10. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	I_O = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
		I_O = 2 mA V_{DD} = 2.97 V	—	—	0.4	V
Output Voltage High	V_{OH}	I_O = –2 mA V_{DD} = 1.71 V	V_{DD} – 0.4	—	—	V
		I_O = –2 mA V_{DD} = 2.97 V	V_{DD} – 0.4	—	—	V
Disabled Leakage Current	I_{OZ}	$\overline{RST}$ = 0	–100	—	100	µA
Single-Ended Reference Clock Input Pin XA (XB with cap to gnd)						
Input Resistance	XA_{RIN}	XTAL/RefCLK RATE[1:0] = LM, ML, MH, or HM	—	12	—	kΩ
Input Voltage Level Limits	XA_{VIN}		0	—	1.2	V
Input Voltage Swing	XA_{VPP}		0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (XA/XB)						
Input Resistance	XA/XB_{RIN}	XTAL/RefCLK RATE[1:0] = LM, ML, MH, or HM	—	12	—	kΩ
Differential Input Voltage Level Limits	XA/XB_{VIN}		0	—	1.2	V
Input Voltage Swing	XA_{VPP}/XB_{VPP}		0.5	—	2.4	V_{PP}

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq 2.5$ V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 10. In most designs, an external resistor voltage divider is recommended.

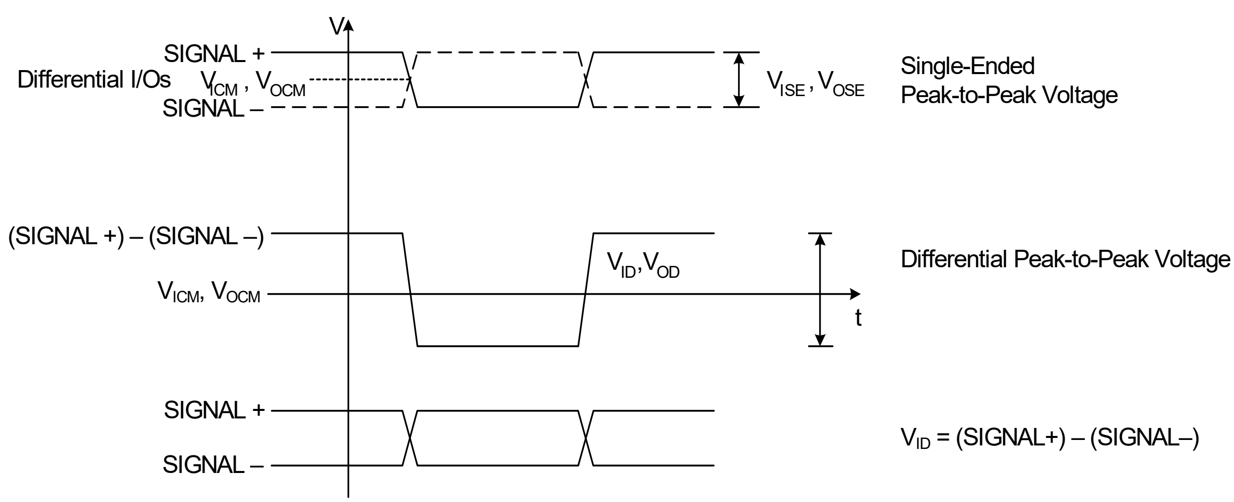


Figure 1. Voltage Characteristics

Table 3. AC Characteristics
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CKIN Input Pins						
Input/Output Clock Frequency (CKIN1, CKIN2, CKOUT)	CK_F	FRQSEL[1:0] = LL FRQSEL[1:0] = LM FRQSEL[1:0] = LH FRQSEL[1:0] = ML FRQSEL[1:0] = MM FRQSEL[1:0] = MH	19.38 38.75 77.5 155.0 310.0 620.0	— — — — — —	22.28 44.56 89.13 178.25 356.5 710.0	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40%/60% limitation applies only to high clock frequencies)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 6	—	—	11	ns
CKOUT Output Pins						
Maximum Output Frequency in CMOS Format	CKO_{FMC}		—	—	212.5	MHz
Single-ended Output Rise/Fall (20–80%)	CKO_{TRF}	CMOS Output V_{DD} = 1.71 Cload = 5 pF	—	—	8	ns
		CMOS Output V_{DD} = 2.97 Cload = 5 pF	—	—	2	ns
Differential Output Rise/Fall Time	CKO_{TRF}	20 to 80 %, f_{OUT} = 622.08	—	230	350	ps
Output Duty Cycle Differential Uncertainty	CKO_{DC}	100 Ω Load Line to Line Measured at 50% Point (not for CMOS)	—	—	±40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMIN}		1	—	—	µs
Input Capacitance	C_{IN}		—	—	3	pF
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20 pf See Figure 6	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKIN↑ to LOS↑		—	750	µs
***Note:** Input to output skew is not controlled and can assume any value.						

Table 3. AC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Time to Clear LOL after LOS Cleared	t_{CLRLOL}	f_{in} unchanged and XA/XB stable. ↓ LOS to ↓ LOL	—	10	—	ms
PLL Performance						
Lock Time	t_{LOCKHW}	Whenever $\overline{RST}$, FRQTBL, RATE, BWSEL, or FRQSEL are changed, with valid CKIN to ↓ LOL; BW = 100 Hz	—	0.035	1.2	sec
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	BW determined by BWSEL[1:0]	5000/BW	—	—	ns pk-pk
Spurious Noise	SP_{SPUR}	Max spur @ n x f3 (n ≥ 1, n x f3 < 100 MHz)	—	–93	–70	dBc
Phase Change due to Temperature Variation*	t_{TEMP}	Max phase changes from –40 to +85 ºC	—	300	500	ps

***Note:** Input to output skew is not controlled and can assume any value.

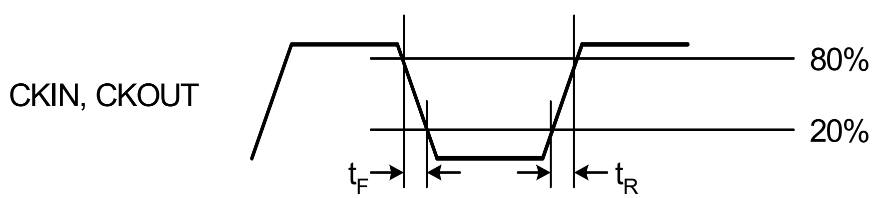


Figure 2. Rise/Fall Time Characteristics

Table 4. Three-Level Input Pins[1,2,3,4]

Parameter	Min	Max
Input Low Current	–30 µA	—
Input Mid Current	–11 µA	–11 µA
Input High Current	—	–30 µA

Notes:

1. The current parameters are the amount of leakage that the 3L inputs can tolerate from an external driver using the external resistor values indicated in this example. In most designs, an external resistor voltage divider is recommended.
2. Resistor packs are only needed if the leakage current of the external driver exceeds the current specified in Table 2. Any resistor pack may be used (e.g., Panasonic EXB-D10C183J). PCB layout is not critical.
3. If a pin is tied to ground or VDD, no resistors are needed.
4. If a pin is left open (no connect), no resistors are needed.

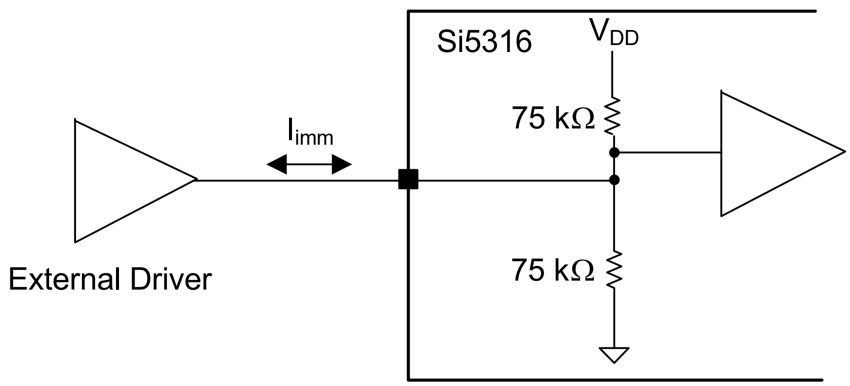


Figure 3. Three-Level (3L) Input Pins (No External Resistors)

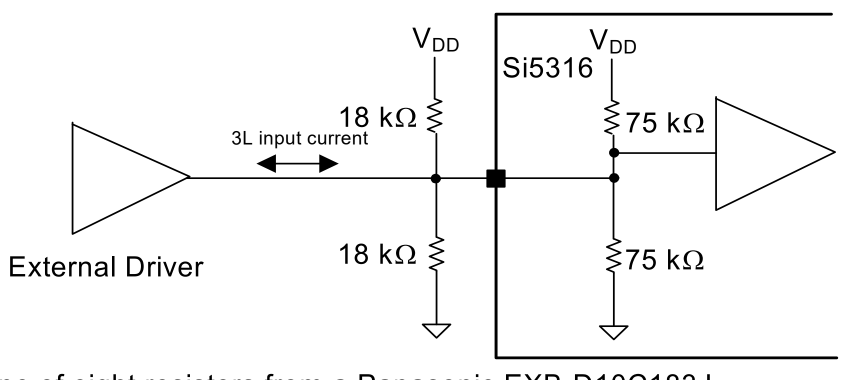


Figure 4. Three-Level Input Pins (Example with External Resistors)

Table 5. Performance Specifications[1, 2, 3, 4, 5]
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Generation f_{IN} = f_{OUT} = 622.08 MHz, LVPECL Output Format BW = 120 Hz	J_{GEN}	50 kHz–80 MHz	—	0.27	0.42	ps rms
		12 kHz–20 MHz	—	0.25	0.41	ps rms
		800 Hz–80 MHz	—	0.28	0.45	ps rms
Phase Noise f_{IN} = f_{OUT} = 622.08 MHz LVPECL Output Format	CKO_{PN}	1 kHz offset	—	–106	—	dBc/Hz
		10 kHz offset	—	–121	—	dBc/Hz
		100 kHz offset	—	–122	—	dBc/Hz
		1 MHz offset	—	–132	—	dBc/Hz

Notes:

1. BWSEL [1:0] loop bandwidth settings provided in “Si53xx-RM: Any-Frequency Precision Clocks Si53xx Family Reference Manual.”
2. 114.285 MHz 3rd OT crystal used as XA/XB input.
3. V_{DD} = 2.5 V
4. T_A = 85 °C
5. Test condition: f_{IN} = 622.08 MHz, f_{OUT} = 622.08 MHz, LVPECL clock input: 1.19 Vppd with 0.5 ns rise/fall time (20-80%), LVPECL clock output.

Table 6. Thermal Conditions
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	32	—	ºC/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	14	—	ºC/W

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.8	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
CKINn Voltage Level Limits	CKN_{VIN}	0 to V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}	0 to 1.2	V
Operating Junction Temperature	T_{JCT}	–55 to 150	C
Storage Temperature Range	T_{STG}	–55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–		2	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–		150	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–		750	V
ESD MM Tolerance; CKIN+/CKIN–		100	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

2. Typical Phase Noise Plot

The following is the typical phase noise performance of the Si5316. The clock input source was a Rohde and Schwarz model SML03 RF Generator. The phase noise analyzer was an Agilent model E5052B. The Si5316 operates at 3.3 V with an ac coupled differential PECL output and an ac coupled differential sine wave input from the RF generator at 0 dBm. Note that, as with any PLL, the output jitter that is below the loop BW is caused by the jitter at the input clock. The loop BW was 120 Hz.

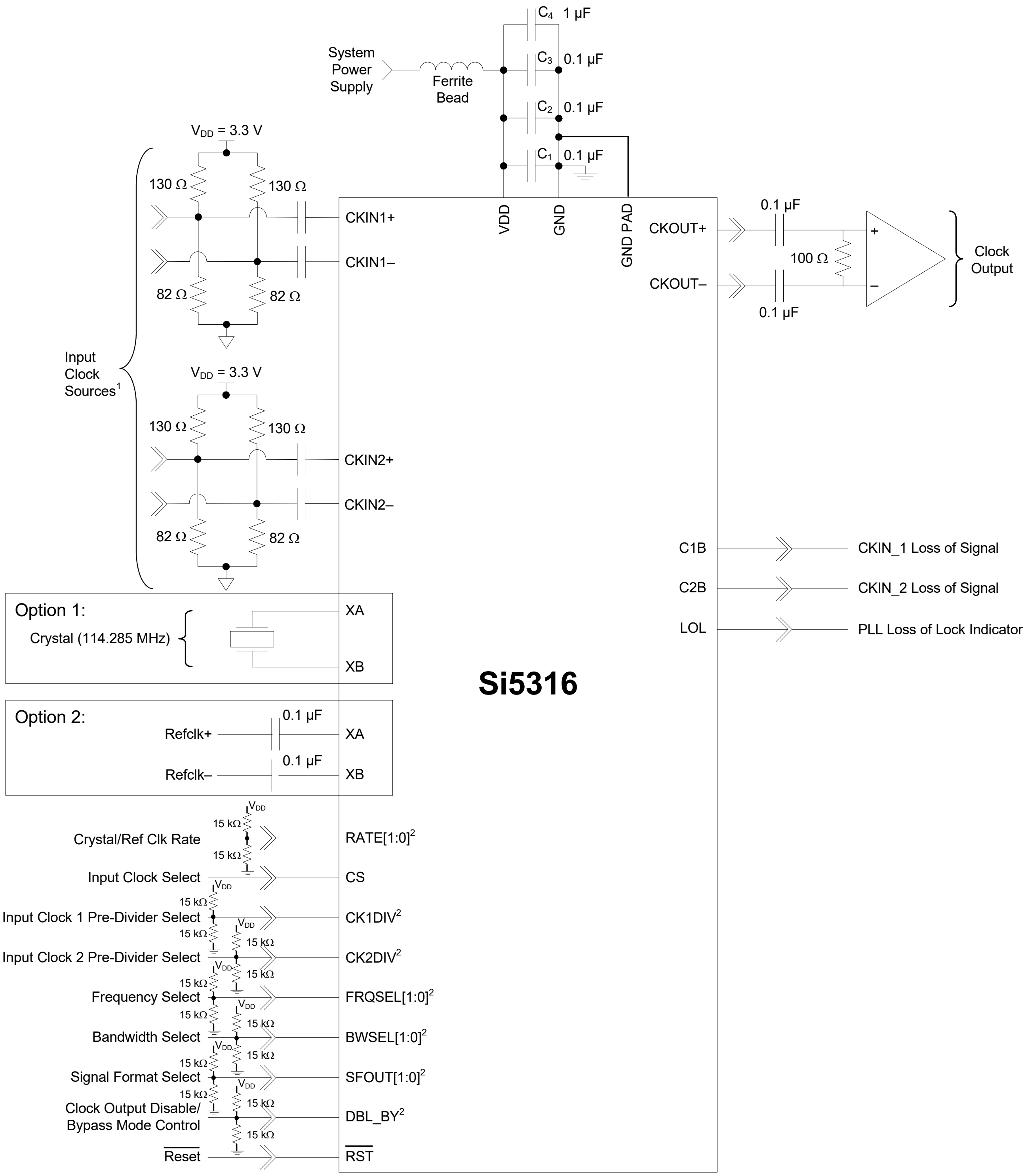
2.1. Example: SONET OC-192

Figure 5. Typical Phase Noise Plot

Jitter Band	Jitter, RMS
SONET_OC48, 12 kHz to 20 MHz	250 fs
SONET_OC192_A, 20 kHz to 80 MHz	274 fs
SONET_OC192_B, 4 to 80 MHz	166 fs
SONET_OC192_C, 50 kHz to 80 MHz	267 fs
Brick Wall, 800 Hz to 80 MHz	274 fs

Note: SONET jitter bands include the SONET skirts. The phase noise plot is brick wall integration.

3. Typical Applications Schematic



Notes:
1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes 3-level input pins with states designated as L (ground), M ($V_{DD}/2$), and H (V_{DD}).

Figure 6. Si5316 Typical Application Circuit

4. Functional Description

The Si5316 is a precision jitter attenuator for high-speed communication systems, including OC-48/STM-16, OC-192/STM-64, 10G Ethernet, and 10G Fibre Channel. The Si5316 accepts dual clock inputs in the 19, 38, 77, 155, 311, or 622 MHz frequency range and generates a jitter-attenuated clock output at the same frequency. Within each of these clock ranges, the device can be tuned approximately 15% higher than nominal SONET/SDH frequencies, up to a maximum of 710 MHz in the 622 MHz range. The Si5316 is based on Skyworks Solutions' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. For applications which require input clocks at different frequencies, the frequency of CKIN1 can be 1x, 4x, or 32x the frequency of CKIN2 as specified by the CK1DIV and CK2DIV inputs.

The Si5316 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 100 Hz to 7.9 kHz. To calculate potential loop bandwidth values for a given input/output clock frequency, Skyworks Solutions offers a PC-based software utility, DSPLL*sim*, that calculates valid loop bandwidth settings automatically. This utility can be downloaded from https://www.skyworksinc.com/en/Products/Timing.

The Si5316 supports manual active input clock selection. The Si5316 monitors both input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on either input clock. Hitless switching is not supported by the Si5316. During a clock transition, the phase of the output clock will slew at a rate defined by the PLL loop bandwidth until the original input clock phase to output clock phase is restored. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5316 has one differential clock output. The electrical format of the clock output is programmable to support LVPECL, LVDS, CML, or CMOS loads. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

4.1. External Reference

An external, 38.88 MHz clock or a low-cost 114.285 MHz 3rd overtone crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to operate. Skyworks Solutions recommends using a high quality crystal. Specific recommendations may be found in the Family Reference Manual. An external 38.88 MHz clock from a high quality OCXO or TCXO can also be used as a reference for the device.

In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

4.2. Further Documentation

Consult the Skyworks Solutions Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5316. Additional design support is available from Skyworks Solutions through your distributor.

Skyworks Solutions has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection.

The FRM and this utility can be downloaded from https://www.skyworksinc.com/en/Products/Timing.

5. Pin Descriptions: Si5316

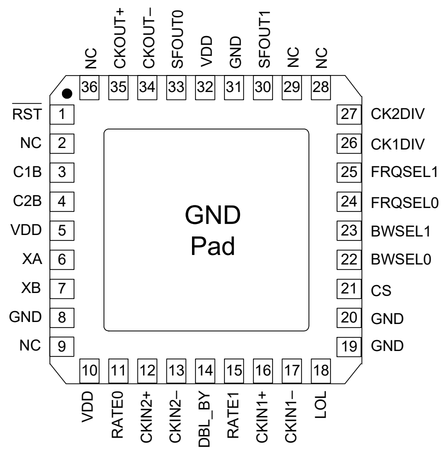


Table 8. Si5316 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5316 will perform an internal self-calibration when a valid signal is present. This pin has a weak pull-up.
2, 9, 28, 29, 36	NC			**No Connection.** Leave floating. Make no external connection to this pin for normal operation.
3	C1B	O	LVCMOS	**CKIN1 Loss of Signal.** Active high Loss-of-signal indicator for CKIN1. Once triggered, the alarm will remain active until CKIN1 is validated. 0 = CKIN1 present 1 = LOS on CKIN1
4	C2B	O	LVCMOS	**CKIN2 Loss of Signal.** Active high Loss-of-signal indicator for CKIN2. Once triggered, the alarm will remain active until CKIN2 is validated. 0 = CKIN2 present 1 = LOS on CKIN2
5, 10, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should also be placed as close to device as is practical.

***Note:** Denotes 3-Level input pin with states designated as L (ground), M (VDD/2), and H (VDD).

Table 8. Si5316 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
7 6	XB XA	I	Analog	**External Crystal or Reference Clock.** External crystal should be connected to these pins to use internal oscillator based reference. Refer to Family Reference Manual for interfacing to an external reference. External reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pins.
8, 19, 20, 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device. Grounding these pins does not eliminate the requirement to ground the GND PAD on the bottom of the package. Pins 19 and 20 may be left NC.
11 15	RATE0 RATE1	I	3-Level*	**External Crystal or Reference Clock Rate.** Three level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down; they default to M. The "HH" setting is not supported. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
12 13	CKIN2+ CKIN2–	I	Multi	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal.
14	DBL_BY	I	3-Level*	**Output Disable/Bypass Mode Control.** Controls enable of CKOUT divider/output buffer path and PLL bypass mode. L = CKOUT enabled M = CKOUT disabled H = Bypass mode with CKOUT enabled This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. Bypass mode is not supported for CMOS clock outputs.
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal.
18	LOL	O	LVCMOS	**PLL Loss of Lock Indicator.** This pin functions as the active high PLL loss of lock indicator. 0 = PLL locked 1 = PLL unlocked

***Note:** Denotes 3-Level input pin with states designated as L (ground), M (VDD/2), and H (VDD).

Table 8. Si5316 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
21	CS	I	LVCMOS	**Input Clock Select.** This pin functions as the input clock selector. This input is internally deglitched to prevent inadvertent clock switching during changes in the CKSEL input state. 0 = Select CKIN1 1 = Select CKIN2 Must be driven high or low.
23 22	BWSEL1 BWSEL0	I	3-Level*	**Bandwidth Select.** Three level inputs that select the DSPLL closed loop bandwidth. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. These pins are both pull-ups and pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
25 24	FRQSEL1 FRQSEL0	I	3-Level*	**Frequency Select.** Sets the output frequency of the device. When the frequency of CKIN1 is not equal to CKIN2, the lower frequency input clock must be equal to the output clock frequency. These pins have both weak pull-ups and weak pull-downs and default to M. For the pin settings, see Table 3 on page 8. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
26	CK1DIV	I	3-Level*	**Input Clock 1 Pre-Divider Select.** Pre-divider on CKIN1. Used with CK2DIV to divide input clock frequencies to a common value. L = CKIN1 input divider set to 1. M = CKIN1 input divider set to 4. H = CKIN1 input divider set to 32. This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
27	CK2DIV	I	3-Level*	**Input Clock 2 Pre-Divider Select.** Pre-divider on CKIN2. Used with CK1DIV to divide input clock frequencies to a common value. L = CKIN2 input divider set to 1. M = CKIN2 input divider set to 4. H = CKIN2 input divider set to 32. This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.

***Note:** Denotes 3-Level input pin with states designated as L (ground), M (VDD/2), and H (VDD).

Table 8. Si5316 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
33 30	SFOUT0 SFOUT1	I	3-Level*	**Signal Format Select.** Three level inputs that select the output signal format (common mode voltage and differential swing) for CKOUT. Valid settings include LVPECL, LVDS, and CML. Also includes selections for CMOS mode, tristate mode, and tristate/sleep mode. <table><tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr><tr><td>HH</td><td>Reserved</td></tr><tr><td>HM</td><td>LVDS</td></tr><tr><td>HL</td><td>CML</td></tr><tr><td>MH</td><td>LVPECL</td></tr><tr><td>MM</td><td>Reserved</td></tr><tr><td>ML</td><td>LVDS—low swing</td></tr><tr><td>LH</td><td>CMOS</td></tr><tr><td>LM</td><td>Disabled</td></tr><tr><td>LL</td><td>Reserved</td></tr></table>These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
34 35	CKOUT– CKOUT+	O	Multi	**Clock Output.** Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
GND PAD	GND	GND	Supply	**Ground Pad.** The ground pad must provide a low thermal and electrical impedance to a ground plane.
***Note:** Denotes 3-Level input pin with states designated as L (ground), M (VDD/2), and H (VDD).				

6. Ordering Guide

Ordering Part Number	Package	ROHS6, Pb-Free	Temperature Range
Si5316-C-GM	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Note: Add an R at the end of the device to denote tape and reel options.			

7. Package Outline: 36-Lead QFN

Figure 7 illustrates the package details for the Si5316. Table 9 lists the values for the dimensions shown in the illustration.

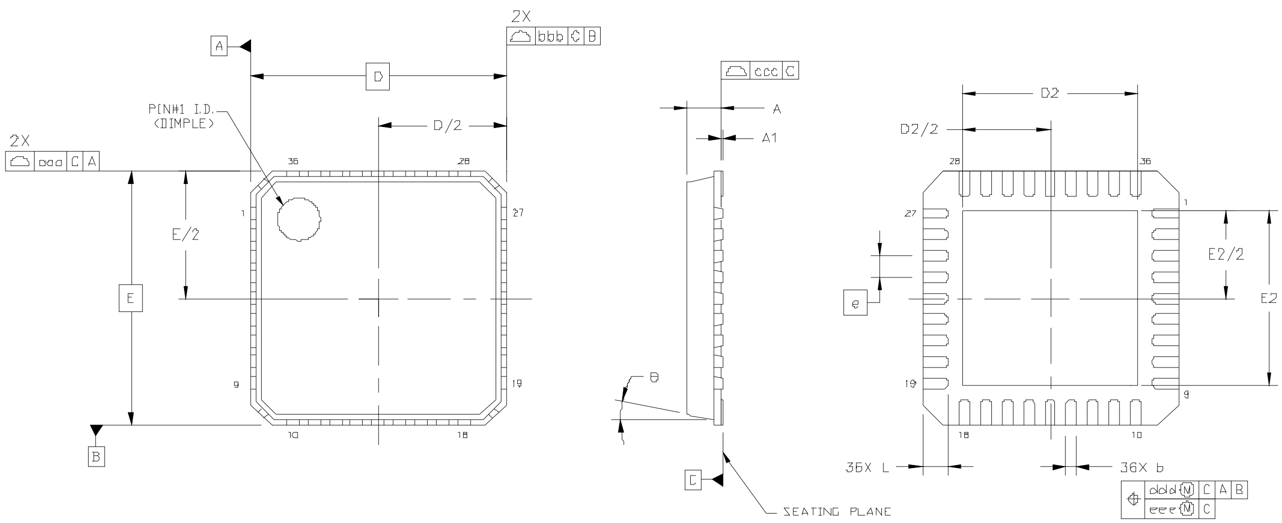


Figure 7. 36-Pin Quad Flat No-lead (QFN)

Table 9. Package Dimensions

Symbol	Millimeters			Symbol	Millimeters		
	Min	**Nom**	**Max**		**Min**	**Nom**	**Max**
A	0.80	0.85	0.90	L	0.50	0.60	0.70
A1	0.00	0.02	0.05	θ	—	—	12º
b	0.18	0.25	0.30	aaa	—	—	0.10
D	6.00 BSC			bbb	—	—	0.10
D2	3.95	4.10	4.25	ccc	—	—	0.08
e	0.50 BSC			ddd	—	—	0.10
E	6.00 BSC			eee	—	—	0.05
E2	3.95	4.10	4.25				

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Recommended PCB Layout

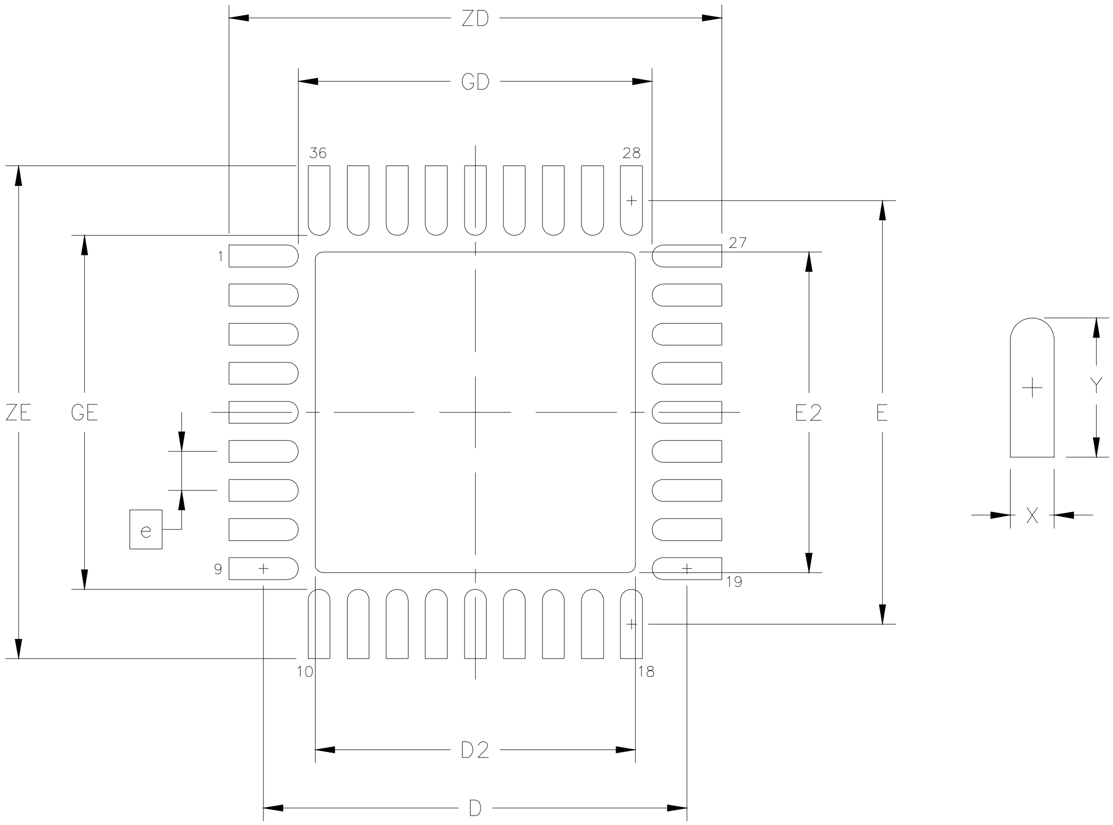


Figure 8. PCB Land Pattern Diagram

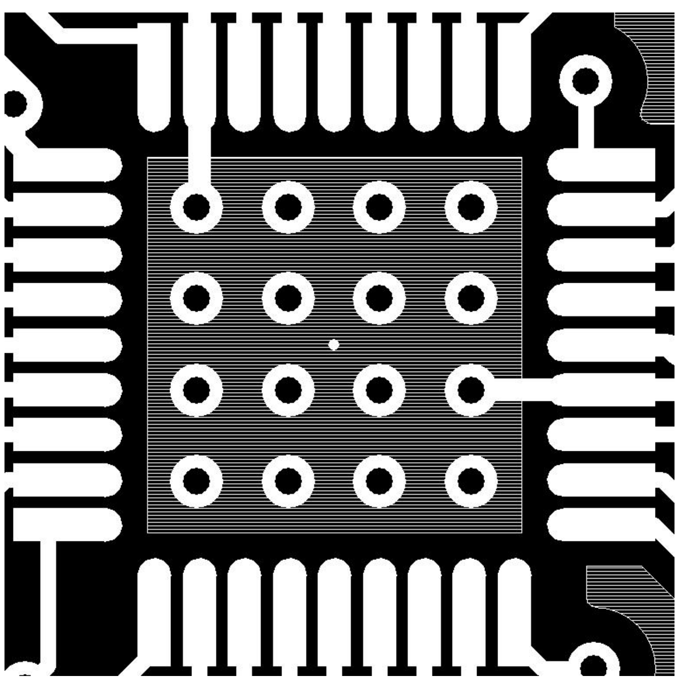


Figure 9. Ground Pad Recommended Layout

Table 10. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Marking

9.1. Si5316 Top Marking

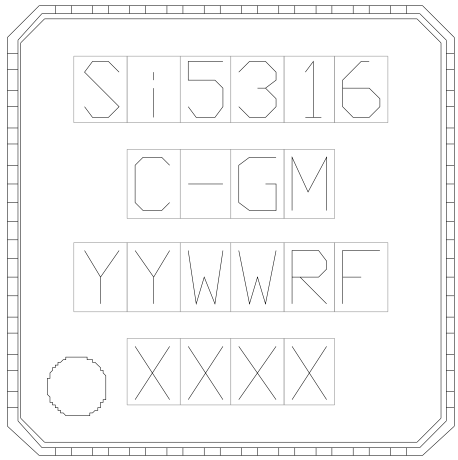


Figure 10. Si5316 Top Marking

9.2. Top Marking Explanation

Mark Method:	Laser	
Line 1 Marking:	Si5316	Customer Part Number
Line 2 Marking:	C-GM	C = Product Revision G = Temperature Range –40 to 85 °C (RoHS6) M = QFN Package
Line 3 Marking:	YYWWRF	YY = Year WW = Work Week R = Die Revision F = Internal code Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 4 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	XXXX	Internal Code

Document Change List

Revision 0.23 to 0.24

- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 5.
- Added Figure 5, “Typical Phase Noise Plot,” on page 13.
- Showed preferred interface for an external reference clock in Figure 6, “Si5316 Typical Application Circuit,” on page 14.
- Updated "3. Ordering Guide" on page 11.
- Added “5. Recommended PCB Layout” .

Revision 0.24 to Revision 0.3

- Changed 1.8 V operating range ±5%.
- Updated Table 1 on page 4.
- Updated Table 2 on page 5.
- Updated Table 8 on page 16.
- Added table under Figure 5 on page 13.
- Updated "1. Functional Description" on page 6.
- Clarified "2. Pin Descriptions: Si5316" on page 7 including pull-up/pull-down.

Revision 0.3 to Revision 0.4

- Updated Table 1, “Performance Specifications[1],” on page 4.
- Updated Table 8, “Si5316 Pin Descriptions,” on page 16.
- Updated Figure 6, “Si5316 Typical Application Circuit,” on page 14.
- Updated "4.1. External Reference" on page 15.
- Updated "2. Pin Descriptions: Si5316" on page 7.

Revision 0.4 to Revision 1.0

- Expanded and rearranged specification tables in section “1. Electrical Specifications” .
- Updated "2. Typical Phase Noise Plot" on page 13.
- Changed “any-rate” to “any-frequency” throughout.
- Added "9. Top Marking" on page 24.
- Added recommended ground pad drawing in "8. Recommended PCB Layout" on page 22.

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