

**ESD Protection Diodes with Ultra-Low Capacitance**

The UESD9L is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

**Specification Features:**

- Ultra Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:  
0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- This is a Pb-Free Device
- **Pb-Free package is available**  
RoHS product for packing code suffix "G"  
Halogen free product for packing code suffix "H"

**Mechanical Characteristics:**

**CASE:** Void-free, transfer-molded, thermosetting plastic

Epoxy Meets UL 94 V-0

**LEAD FINISH:** 100% Matte Sn (Tin)

**QUALIFIED MAX REFLOW TEMPERATURE:** 260°C

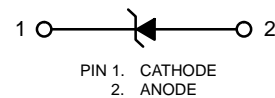
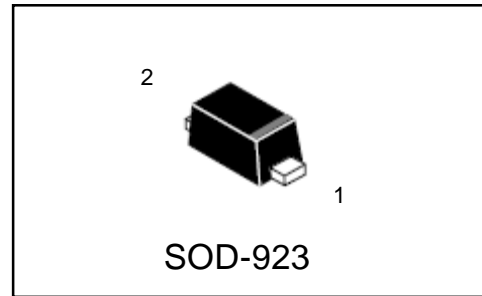
Device Meets MSL 1 Requirements

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		±10 ±15	kV
Total Power Dissipation on FR-5 Board (Note 1) @ T <sub>A</sub> = 25°C	P <sub>D</sub>	150	mW
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Lead Solder Temperature - Maximum (10 Second Duration)	T <sub>L</sub>	260	°C
Peak Pulse Current 8 x 20 μsec.	I <sub>PP</sub>	5(Max)	A
Peak Power Dissipation 8 x 20 μsec.	P <sub>pk</sub>	50(Max)	W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-5 = 1.0 x 0.75 x 0.62 in.



**Ordering information**

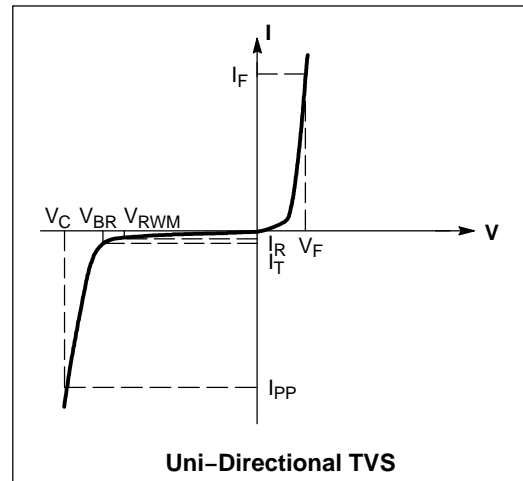
Device	Marking	Shipping
SESD9L5.0T5	D	8000/Tape&Reel

**ESD Protection Diodes with Ultra-Low Capacitance**

**ELECTRICAL CHARACTERISTICS**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$
$P_{pk}$	Peak Power Dissipation
C	Capacitance @ $V_R = 0$ and $f = 1.0$ MHz

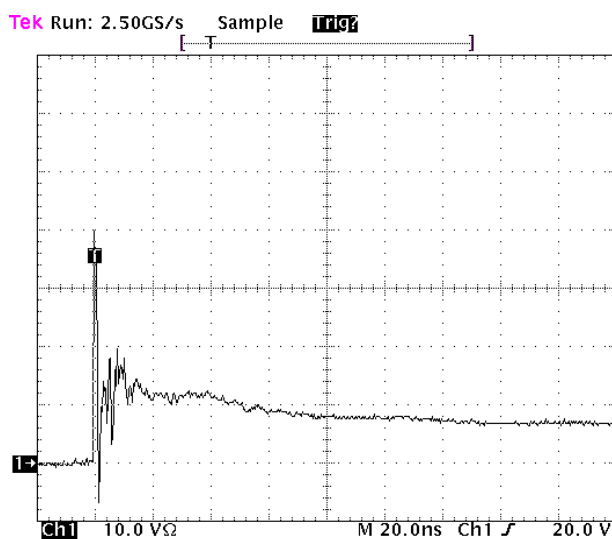


\*See Application Note AND8308/D for detailed explanations of datasheet parameters.

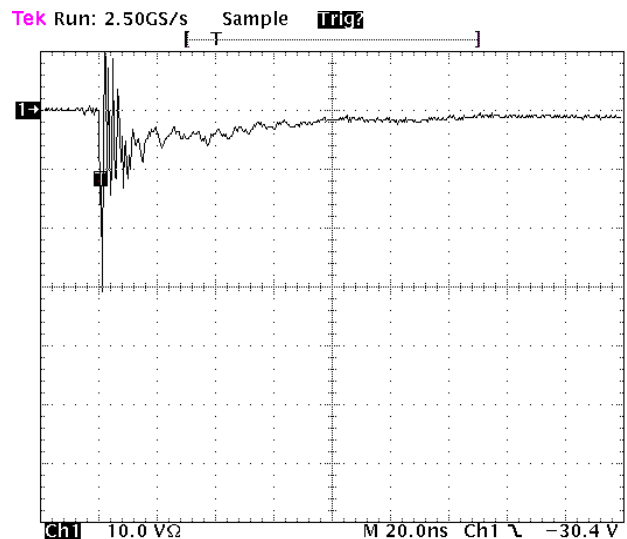
**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted,  $V_F = 1.0$  V Max. @  $I_F = 10$  mA for all types)

Device	Device Marking	$V_{RWM}$ (V)	$I_R$ ( $\mu\text{A}$ ) @ $V_{RWM}$	$V_{BR}$ (V) @ $I_T$ (Note 2)	$I_T$	C (pF)		$V_C$ (V) @ $I_{PP} = 1$ A (Note 3)	$V_C$ Per IEC61000-4-2 (Note 4)
		Max	Max	Min		mA	Typ	Max	
SESD9L5.0T5	D	5.0	1.0	5.4	1.0	0.5	0.9	9.8	Figures 1 and 2 See Below

2.  $V_{BR}$  is measured with a pulse test current  $I_T$  at an ambient temperature of  $25^\circ\text{C}$ .
3. Surge current waveform per Figure 5.
4. For test procedure see Figures 3 and 4 and Application Note AND8307/D.



**Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2**



**Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2**



### ESD Protection Diodes with Ultra-Low Capacitance

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

IEC61000-4-2 Waveform

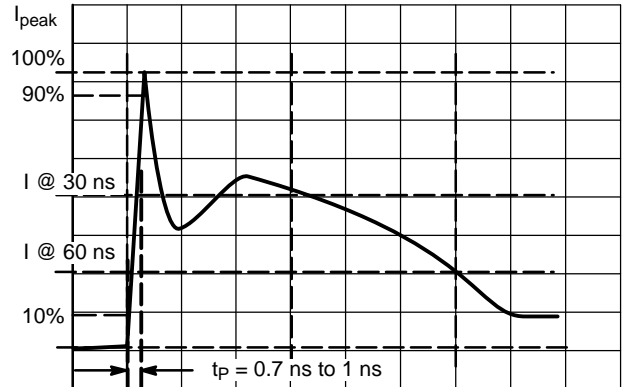


Figure 3. IEC61000-4-2 Spec

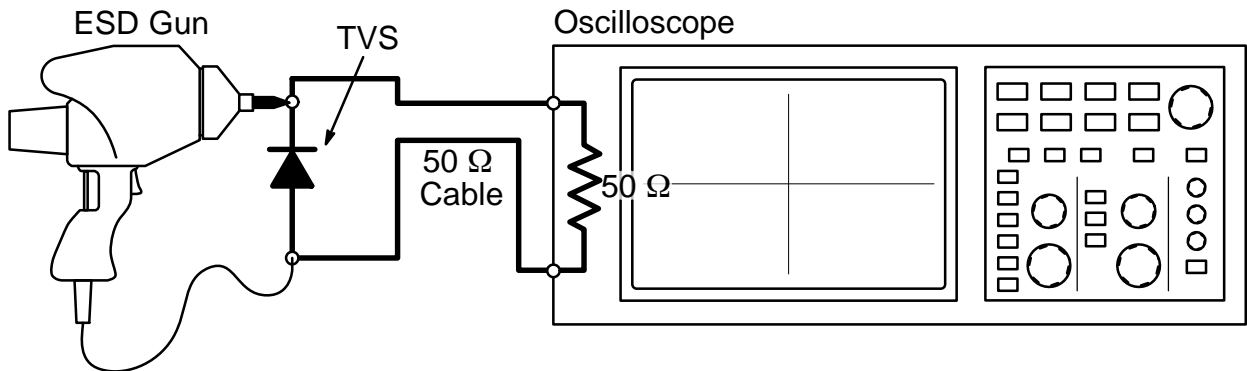


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

#### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

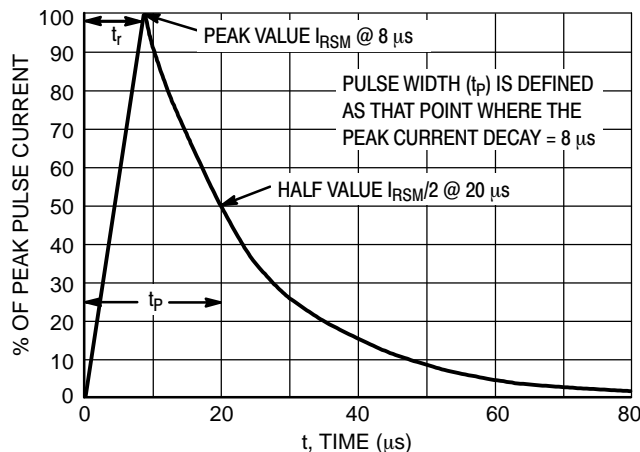
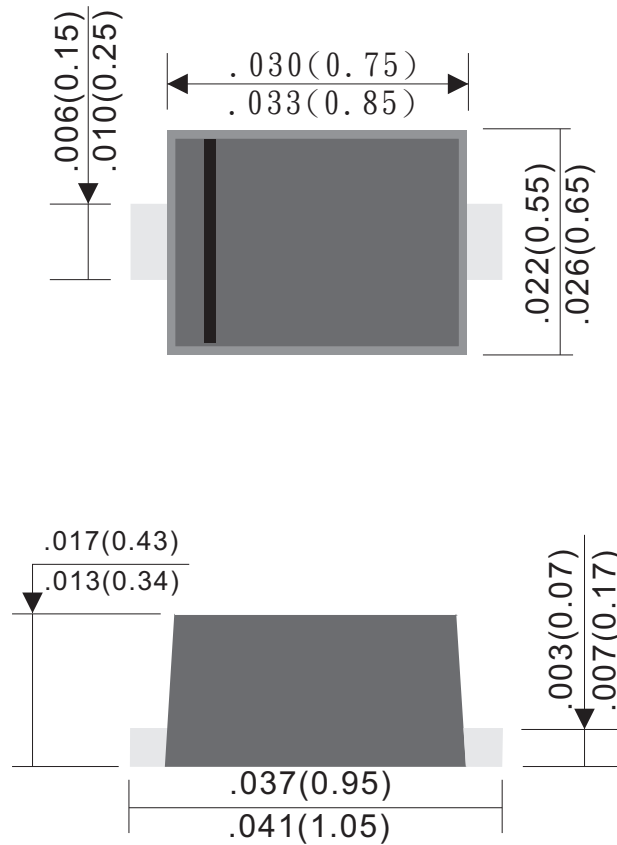


Figure 5. 8 X 20 μs Pulse Waveform



## SOD-923



Dimensions in inches and (millimeters)

### SOLDERING FOOTPRINT\*

