SAF7741HV

Dual IF car radio and audio DSP (N1F)

Rev. 05 — 09 May 2008 Objective data sheet

1. General description

The SAF7741HV is a combined Intermediate-Frequency (IF) car radio and audio Digital Signal Processor (DSP) with several powerful cores integrated onto a single device. It combines analog IF input, digital radio and audio processing, sample-rate converters and digital and analog audio output to enhance listening clarity and noise suppression while reducing multipath channel effect.

The SAF7741 offers user-specific functions which can be configured to match the software platform required by the systems of individual car-radio manufacturers, thus providing a high level of product differentiation. It is equipped to work with the TEF7000 and TEF6730 integrated tuners for analog and digital AM/FM decoding and sound processing

The SAF7741HV consists of two main processing blocks; one for radio and the other for audio. These blocks demodulate either the IF or the low-IF tuner output, delivering digital audio to internal Digital-to-Analog Converters (DACs). In addition to the main blocks there are a number of interfaces and dedicated sub-circuits.

1.1 Radio processing

The IF radio block interfaces to the front-end tuner chips and supports either a so-called low-IF frequency (of 60 kHz or 300 kHz) or an IF frequency of 10.7 MHz. Two tuner interfaces are supported, each of which is suitable for analog Frequency-Modulated/Amplitude-Modulated and Weatherband (FM/AM/WX) radio reception as well as reception of encoded digital signals such as HD Radio and Digital Radio Mondiale (DRM).

Signals received from the tuner front-end chips are digitized with integrated Intermediate-Frequency Analog-to-Digital Converters (IFADCs). The resulting digital signals are then down-sampled, error-corrected and filtered in the digital domain to be suitable for further radio and audio processing by the DSPs.

The low-IF interface to the tuner chip combined with the high level of integration allows cost-effective implementation of the entire tuner/DSP application on a main radio Printed Circuit Board (PCB).

1.2 Audio processing

The audio processing block receives either external digital signals, or analog signals which are then digitized by the integrated ADCs. Together with the internal radio audio signals these inputs are available for further audio processing such as equalization, tone control and volume control. The output signals of the audio processing block are provided in digital format on the Host IIS outputs and in analog format on the DAC outputs.

founded by Philips

2. Features

2.1 Hardware features

SAF7741HV hardware is configured by firmware and host software to meet specific customer requirements. The firmware is defined by the Read-Only Memory (ROM) code associated with each DSP.

Remark: The list below describes the maximum hardware configuration. Customers should consult with NXP to identify the best method of supporting their own particular requirements.

- Two IF data-paths of either 2 × IF 10.7 MHz or 2 × low IF 300 kHz input

  Remark: The combination of 1 x IF and 1 x low IF is not supported.
- Two 5th order Sigma-Delta (ΣΔ) IF ADCs for FM/AM/WB (Weather-band) and digital radio at either IF = 10.7 MHz or low IF = 300 kHz
- IF signal quadrature-mixing and down-sampling with signal level generation
- Automatic Gain Control (AGC) of the radio front-end chip in three steps (6 dB for each step) for the TEF6730 tuner and seven steps (6 dB for each step) for the TEF7000 tuner
- AGC control of the TEF6730 tuner front-end PIN diodes, with an analog signal via the Radio General-Purpose DAC (RGP DAC) output: one DAC for each radio data path
- Integrated IF filter with bandwidth of 100 kHz or 400 kHz
- Two wideband outputs for external digital radio decoding; one output for each data-path
- Two Radio Data System (RDS) decoders
- Five bit-stream, 3rd order audio, ΣΔ ADCs with an anti-aliasing broadband input-filter
- Eight configurable analog inputs (differential/stereo/mono) connected to any of the five ADCs using an analog switchbox
- Dedicated DSP for the Sample Rate Converter (SRC)
- Audio Host Inter-IC Sound (IIS) Input/Output (I/O) port, with eight/ten outputs and eight inputs with an option for slaving the DSP to an external master sample-rate
- Audio Host IIS Bit-Clock (BCK) and Word-Size (WS) available simultaneously at full-rate and half-rate
- Four independent IIS inputs and two independent digital Sony/Philips Digital Interface Format (SPDIF) inputs also configurable for Digital Versatile Disc/Digital Video Device (DVD) multi-channel data inputs
- Radio Host IIS master with separate data in and out lines
- IIS output with buffer for eight samples for radio applications
- WatchDog (WDOG) to monitor execution of the DSP main software loop
- Phase-Lock Loop (PLL) to generate the DSP clock from the oscillator crystal
- PLL to generate the audio reference sample-rate clock
- Internal voltage regulator for the 1.8 V supply
- I^2C (Inter-IC Communication) bus-controlled
- Possibility of powering down unused blocks to reduce power dissipation
- Qualified in accordance with AEC-Q100

2.2 Software Features

The following software features are available for the SAF7741HV:

- Improved FM weak-signal processing
- Integrated 19 kHz Multiplexed (MPX) filter and de-emphasis
- Electronic adjustment of FM/AM level and FM channel separation
- Variable IF bandwidth. This is controlled partly by the DSP software and depends on the quality of the reception
- Selective IF bandwidth for wideband FM, FM Weatherband and AM
- Variable IF bandwidth on FM, dependent on the adjacent channel interference
- Digital stereo decoder for FM and AM
- Advanced digital Interference Absorption Circuit (IAC) for FM and AM
- Digital Automatic Frequency Control (AFC)
- RDS demodulation
- Pause detection for RDS updates with audio mute during RDS updates
- Baseband audio processing (treble, bass, balance, fader and volume)
- Maximum of five audio SRCs
- Dynamic loudness or bass boost
- Audio level meter
- Compact Disc (CD) dynamics compressor/expander
- Improved AM processing with soft mute, high cut control, 6th order low-pass filtering and AM audio IAC
- Soft audio mute
- Extended chime functions
- Signal level, noise and multi-path detection for AM/FM signal quality information
- AM audio AGC
- AGC click suppression in AM mode

3. Applications

The SAF7741HV is designed for use in high-performance car radio systems.

4. Ordering information

Table 1. Ordering information

Type Number	Package		
	Name	Description	Version
SAF7741HV	HLQFP144	144 leads; plastic thermal enhanced low profile quad flat package; exposed die pad	N115F

5. Block diagram

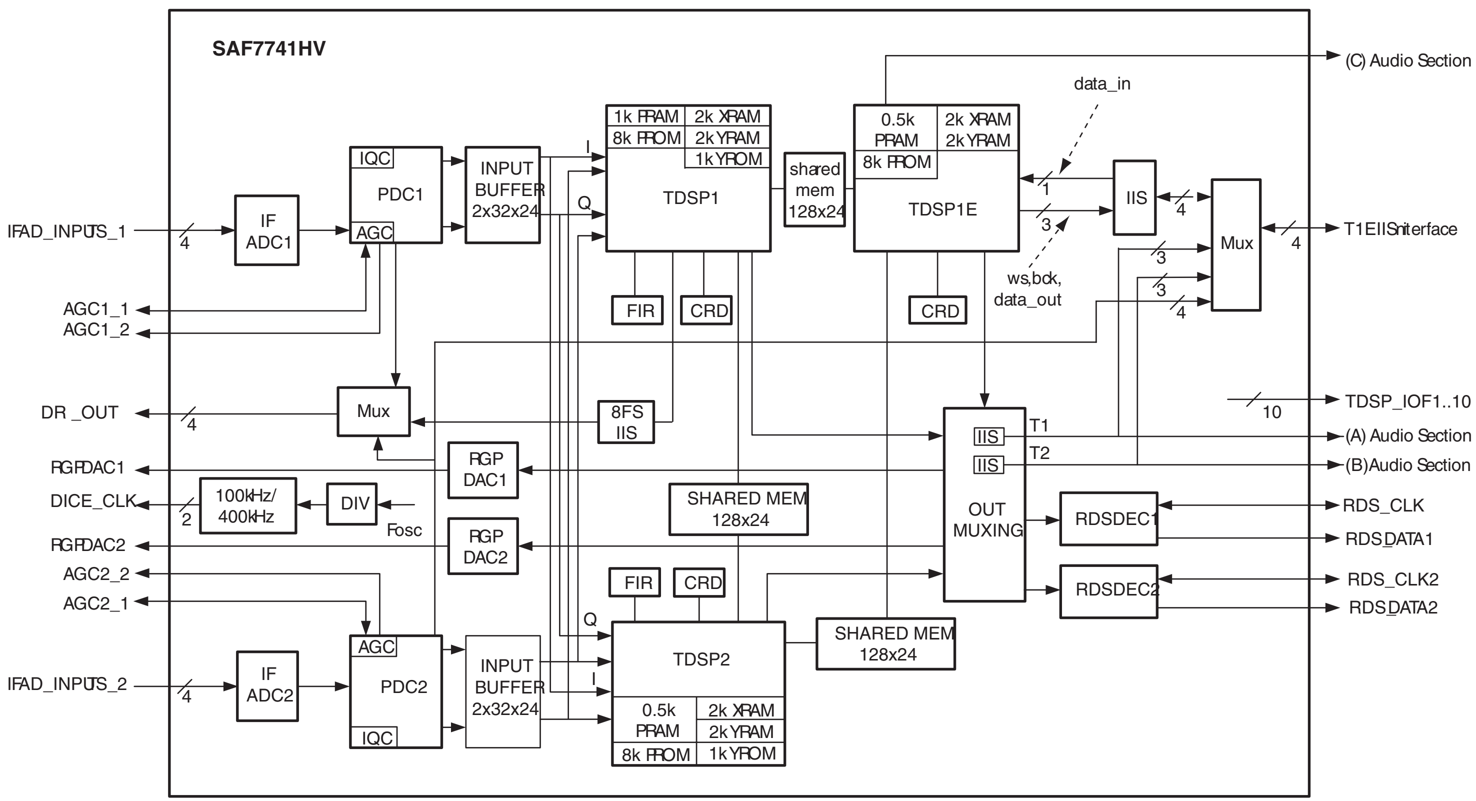


Fig 1. Block diagram of SAF7741HV radio section

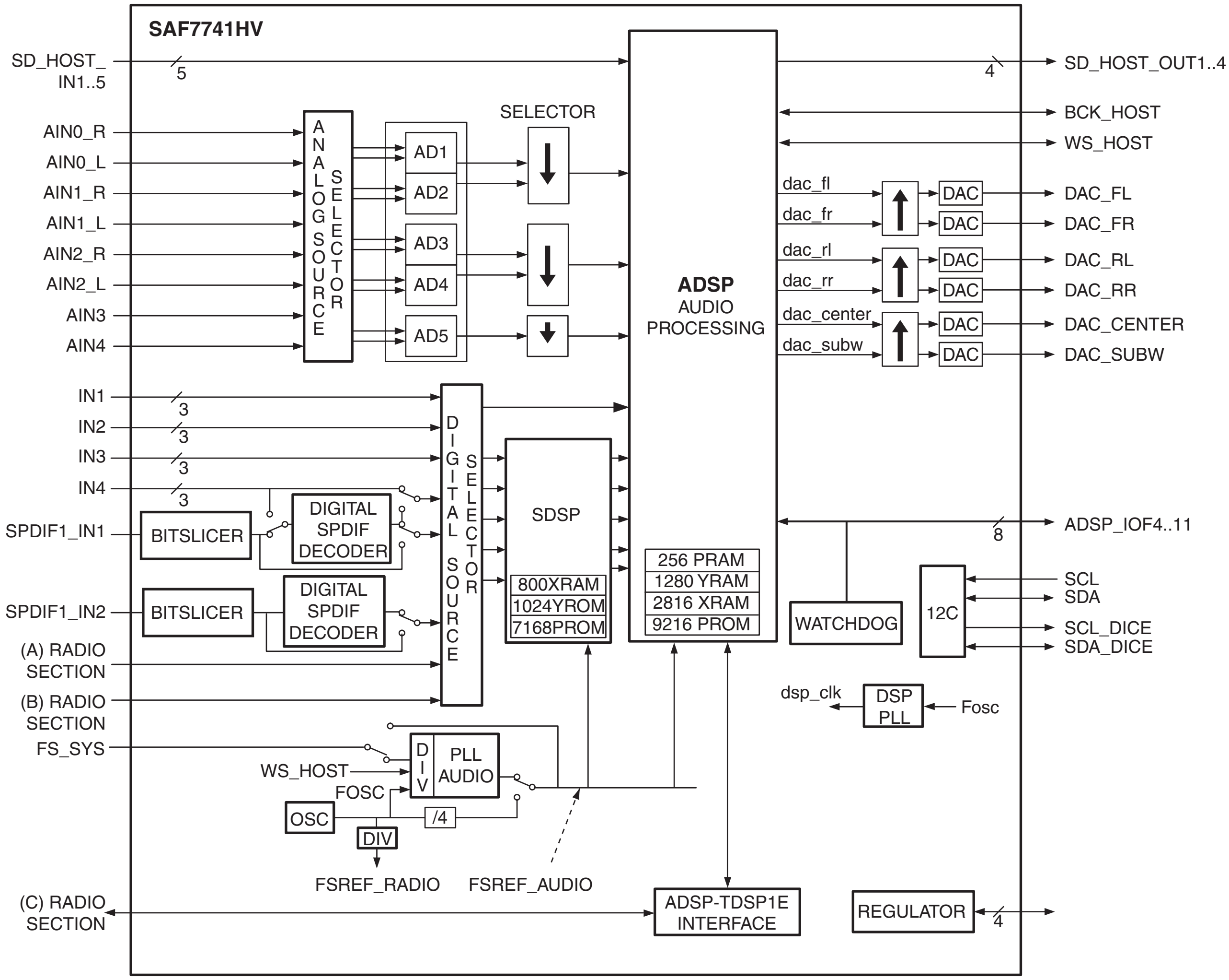


Fig 2. Block diagram of SAF7741HV audio section

6. Pinning information

6.1 Pinning

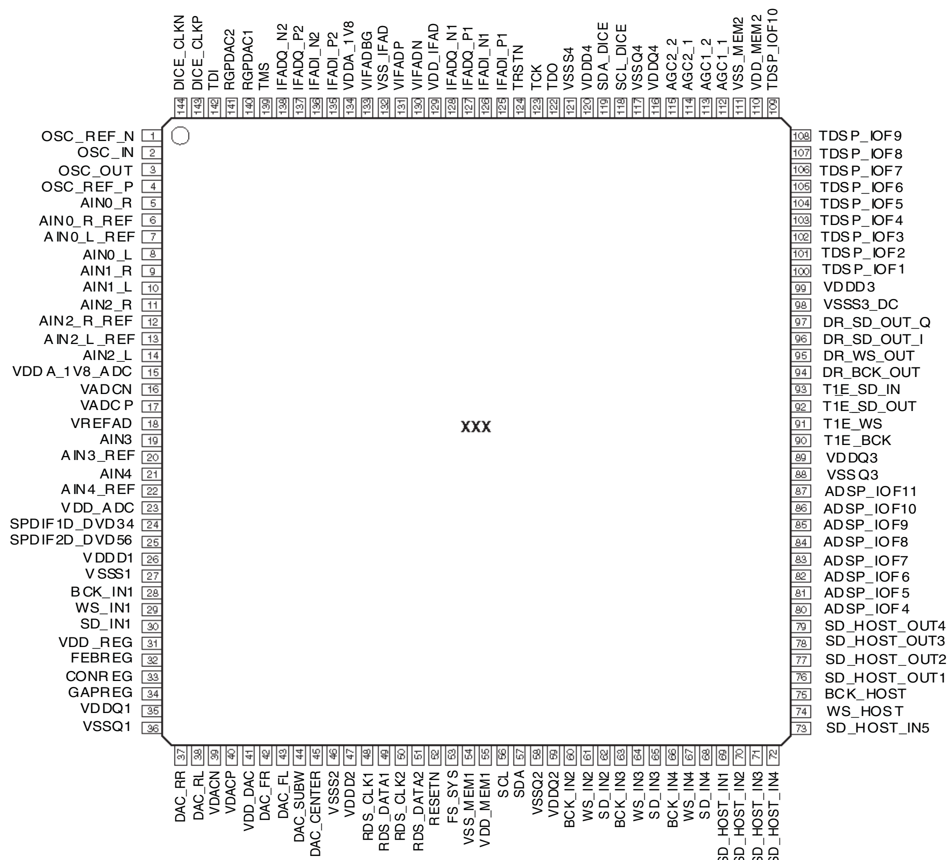


Fig 3. Pin configuration for the SAF7741HV

Table 2. Pin allocation table

Pin Name	Pin Number	Description	Pin Type
OSC_REF_N	1	Ground reference for oscillator, PLLs and tuner clock generator	vssco
OSC_IN	2	Crystal oscillator input	apio
OSC_OUT	3	Crystal oscillator output	apio
OSC_REF_P	4	1.8 V reference supply for oscillator, PLLs and tuner clock generator	vddco
AIN0_R	5	Right channel analog audio input 0	apio
AIN0_R_REF	6	Right common mode reference audio input 0	apio
AIN0_L_REF	7	Left common mode reference audio input 0	apio
AIN0_L	8	Left channel analog audio input 0	apio
AIN1_R	9	Right channel analog audio input 1	apio
AIN1_L	10	Left channel analog audio input 1	apio
AIN2_R	11	Right channel analog audio input 2	apio

Table 2. Pin allocation table *…continued*

Pin Name	Pin Number	Description	Pin Type
AIN2_R_REF	12	Right common mode reference audio input 2	apio
AIN2_L_REF	13	Left common mode reference audio input 2	apio
AIN2_L	14	Left channel analog audio input 2	apio
VDDA_1V8_ADC	15	1.8 V supply for ADC	vddco
VADCN	16	Ground reference for audio ADCs and RGPDACs	apio
VADCP	17	Positive reference voltage for Audio ADCs and RGPDACs	apio
VREFAD	18	Common mode reference voltage ADCs	apio
AIN3	19	Analog audio input 3	apio
AIN3_REF	20	Common mode reference audio input 3	apio
AIN4	21	Analog audio input 4	apio
AIN4_REF	22	Common mode reference audio input 4	apio
VDD_ADC	23	3.3 V supply for audio ADCs	vddco
SPDIF_IN1	24	Input 1 SPDIF analog / input DVD-A channels 3 and 4 [1]	apio
SPDIF_IN2	25	Input 2 SPDIF analog / input DVD-A channels 5 and 6 [1]	apio
VDDD1	26	1.8 V positive supply (digital core)	vddi
VSSS1	27	Ground supply (digital core)	vssis
BCK_IN1	28	Inter-IC Sound (I^2S) source 1 Bit Clock input	bpts5ptpht5v
WS_IN1	29	I^2S source 1 Word Select input	bpts5ptpht5v
SD_IN1	30	I^2S source 1 data input/input DVD-A channels 1 and 2	bpts5ptpht5v
VDD_REG	31	3.3 V supply for regulator	vddco
FEBREG	32	Feedback input monitoring the 1.8 V	apio
CONREG	33	Control output for external Positive-channel Metal Oxide Semiconductor (PMOS) transistor	apio
GAPREG	34	Decoupling for regulator bandgap voltage	apio
VDDQ1	35	3.3 V positive supply (peripheral cells)	vdde
VSSQ1	36	Ground supply (peripheral cells)	vsse
DAC_RR	37	Audio output for the rear-right speaker	apio
DAC_RL	38	Audio output for the rear-left speaker	apio
VDACN	39	Ground reference voltage for the Audio DACs (ADAC)	apio
VDACP	40	Positive reference voltage for the Audio DACs (ADAC)	apio
VDD_DAC	41	3.3 V supply for the Audio DACs (ADAC)	vddco
DAC_FR	42	Audio output for the front-right speaker	apio
DAC_FL	43	Audio output for the front-left speaker	apio
DAC_SUBW	44	Audio output for the sub-woofer	apio
DAC_CENTER	45	Audio output for the centre speaker	apio
VSSS2	46	Ground supply (digital core)	vssis
VDDD2	47	1.8 V positive supply (digital core)	vddi
RDS_CLK1	48	RDS bit clock (CLK) output 1/RDS external clock input 1	bpts5ptpht5v
RDS_DATA1	49	RDS data output 1	bpts5ptpht5v
RDS_CLK2	50	RDS bit clock output 2/RDS external clock input 2	bpts5ptpht5v

Table 2. Pin allocation table *...continued*

Pin Name	Pin Number	Description	Pin Type
RDS_DATA2	51	RDS data output 2	bpts5ptpht5v
RESETN	52	General reset of chip (active low)	bpts5ptpht5v
FS_SYS	53	Fs system clock in/output	bpts10thdt5v
VSS_MEM1	54	Ground supply (digital core)	vssi
VDD_MEM1	55	1.8 V positive supply (memories)	vddcobf
SCL	56	Serial clock input I^2C bus	iic3m4sclt5v
SDA	57	Serial data input/output I^2C bus	iic3m4sdat5v
VSSQ2	58	Ground supply (peripheral cells)	vsse
VDDQ2	59	3.3 V positive supply (peripheral cells)	vdde
BCK_IN2	60	IIS source 2 Bit Clock input	bpts5ptpht5v
WS_IN2	61	IIS source 2 Word Select input	bpts5ptpht5v
SD_IN2	62	IIS source 2 data input	bpts5ptpht5v
BCK_IN3	63	IIS source 3 Bit Clock input	bpts5ptpht5v
WS_IN3	64	IIS source 3 Word Select input	bpts5ptpht5v
SD_IN3	65	IIS source 3 data input	bpts5ptpht5v
BCK_IN4	66	IIS source 4 Bit Clock input	bpts5ptpht5v
WS_IN4	67	IIS source 4 Word Select input	bpts5ptpht5v
SD_IN4	68	IIS source 4 data input/input SPDIF 1 digital	bpts5ptpht5v
SD_HOST_IN1	69	Host I^2S 1 data input	bpts5ptpht5v
SD_HOST_IN2	70	Host I^2S 2 data input	bpts5ptpht5v
SD_HOST_IN3	71	Host I^2S 3 data input	bpts5ptpht5v
SD_HOST_IN4	72	Host I^2S 4 data input	bpts5ptpht5v
SD_HOST_IN5	73	Host I^2S 5 data input	bpts5ptpht5v
WS_HOST	74	Host I^2S Word Select output/input	bpts10thdt5v
BCK_HOST	75	Host I^2S Bit Clock output/input	bpts10thdt5v
SD_HOST_OUT1	76	Host I^2S 1 data output	bpts10thdt5v
SD_HOST_OUT2	77	Host I^2S 2 data output	bpts10thdt5v
SD_HOST_OUT3	78	Host I^2S 3 data output	bpts10thdt5v
SD_HOST_OUT4	79	Host I^2S 4 data output	bpts10thdt5v
ADSP_IOF4	80	Audio DSP (ADSP) general purpose I/O flag 4	bpts5ptpht5v
ADSP_IOF5	81	ADSP general purpose I/O flag 5	bpts5ptpht5v
ADSP_IOF6	82	Audio/SCR DSP general purpose I/O flag 6	bpts5ptpht5v
ADSP_IOF7	83	Audio/SRC DSP general purpose I/O flag 7	bpts5ptpht5v
ADSP_IOF8	84	Audio/SRC DSP general purpose I/O flag 8	bpts5ptpht5v
ADSP_IOF9	85	Audio/SRC DSP general purpose I/O flag 9	bpts5ptpht5v
ADSP_IOF10	86	Audio/SRC DSP general purpose I/O flag 10	bpts5ptpht5v
ADSP_IOF11	87	Audio/SRC DSP general purpose I/O flag 11	bpts5ptpht5v
VSSQ3	88	Ground supply (peripheral cells)	vsse
VDDQ3	89	3.3 V positive supply (peripheral cells)	vdde
T1E_BCK	90	Tuner I^2S BCK output / digital radio interface 2 bit clock output	bpts10thdt5v

Table 2. Pin allocation table *…continued*

Pin Name	Pin Number	Description	Pin Type
T1E_WS	91	Tuner I^{2}S WS output / digital radio interface 2 word-select output	bpts10thdt5v
T1E_SD_OUT	92	Tuner I^{2}S Serial data output / Serial data output digital radio interface 2 word select signal	bpts10thdt5v
T1E_SD_IN	93	Tuner I^{2}S Serial data input / Serial data output digital radio interface 2 Q-signal	bpts10thdt5v
DR_BCK_OUT	94	Digital radio interface 1 bit clock output	bpts10thdt5v
DR_WS_OUT	95	Digital radio interface 1 word-select output	bpts10thdt5v
DR_SD_OUT_I	96	Serial data output digital radio interface 1 I-signal	bpts10thdt5v
DR_SD_OUT_Q	97	Serial data output digital radio interface 1 Q-signal	bpts10thdt5v
VSSS3_DC	98	Digital core DC ground connection	vssis
VDDD3	99	1.8 V positive supply (digital core)	vddi
TDSP_IOF1	100	Tuner DSP (TDSP) general purpose I/O flag 1	bpts5ptpht5v
TDSP_IOF2	101	Tuner DSP general purpose I/O flag 2	bpts5ptpht5v
TDSP_IOF3	102	Tuner DSP general purpose I/O flag 3	bpts5ptpht5v
TDSP_IOF4	103	Tuner DSP general purpose I/O flag 4	bpts5ptpht5v
TDSP_IOF5	104	Tuner DSP general purpose I/O flag 5	bpts5ptpht5v
TDSP_IOF6	105	Tuner DSP general purpose I/O flag 6	bpts5ptpht5v
TDSP_IOF7	106	Tuner DSP general purpose I/O flag 7	bpts5ptpht5v
TDSP_IOF8	107	Tuner DSP general purpose I/O flag 8	bpts5ptpht5v
TDSP_IOF9	108	Tuner DSP general purpose I/O flag 9	bpts5ptpht5v
TDSP_IOF10	109	Tuner DSP general purpose I/O flag 10	bpts5ptpht5v
VDD_MEM2	110	1.8 V positive supply (memories)	vddco
VSS_MEM2	111	Ground supply (digital core)	vssi
AGC1_1	112	Command input from TEF7000 connected to IFAD1 / Least Significant Bit (LSB) gain control output to TEF6730 tuner connected to IFAD1	bpts5ptpht5v
AGC1_2	113	Request output to TEF7000 tuner connected to IFAD1 / Most Significant Bit (MSB) gain control output to TEF6730 tuner connected to IFAD1	bpts5ptpht5v
AGC2_1	114	Command input from TEF7000 connected to IFAD2 / Least Significant Bit (LSB) gain control output to TEF6730 tuner connected to IFAD2	bpts5ptpht5v
AGC2_2	115	Request output to TEF7000 tuner connected to IFAD2 / Most Significant Bit (MSB) gain control output to TEF6730 tuner connected to IFAD2	bpts5ptpht5v
VDDQ4	116	3.3 V positive supply (peripheral cells)	vdde
VSSQ4	117	Ground supply (peripheral cells)	vsse
SCL_DICE	118	SCL output of the tuner I^{2}C bus	iic3m4sclt5v
SDA_DICE	119	SDA input/output of the tuner I^{2}C bus	iic3m4sdat5v
VDDD4	120	1.8 V positive supply (digital core)	vddi
VSSS4	121	Ground supply (digital core)	vssis
TDO	122	JTAG Test control data output	bpts5ptpht5v
TCK	123	JTAG Test clock	bpts5ptpht5v
TRSTN	124	JTAG Test reset, active low	bpts5ptpht5v
IFADI_P1	125	Positive phase of the first differential IF I input	aprf3v3
IFADI_N1	126	Negative phase of the first differential IF I input	aprf3v3

Table 2. Pin allocation table *…continued*

Pin Name	Pin Number	Description	Pin Type
IFADQ_P1	127	Positive phase of the first differential IF Q input	aprf3v3
IFADQ_N1	128	Negative phase of the first differential IF Q input	aprf3v3
VDD_IFAD	129	3.3 V supply for IF ADCs and RGPDACs	vddco
VIFADN	130	Ground reference voltage for IF ADCs	apio
VIFADP	131	Decoupling for IF ADCs positive reference voltage	apio
VSS_IFAD	132	Ground supply for IF ADCs and RGPDACs	vssco
VIFADBG	133	Decoupling for IF ADCs bandgap voltage	apio
VDDA_1V8	134	1.8 V supply for IFADC and Audio ADCs	vddco
IFADI_P2	135	Positive phase of the second differential IF I input	aprf3v3
IFADI_N2	136	Negative phase of the second differential IF I input	aprf3v3
IFADQ_P2	137	Positive phase of the second differential IF Q input	aprf3v3
IFADQ_N2	138	Negative phase of the second differential IF Q input	aprf3v3
TMS	139	JTAG Test mode select	bpts5ptpht5v
RGPDAC1	140	RGP DAC 1 output	apio
RGPDAC2	141	RGP DAC 2 output	apio
TDI	142	JTAG Test control data input	bpts5ptpht5v
DICE_CLKP	143	100 kHz/400 kHz clock reference output to TEF6730/TEF7000 tuner (positive)	apio
DICE_CLKN	144	100 kHz/400 kHz clock reference output to TEF6730/TEF7000 tuner (negative)	apio

[1] The maximum input voltage is 3.3 volts.

6.2 Pin description

Table 3. Pad name description

Pad Name	Description
IICT5V	
iic3m4sdat5v	IIC pad: 5 V-tolerant; data signal
iic3m4sclt5v	IIC pad: 5 V-tolerant; clock signal
IOT5V	
bpts5ptpht5v	Bi-directional pad; plain input; 3-state output; SSO control; TTL with programmable hysteresis; programmable pull-up and pull-down, repeater; 5 V- tolerant
bpts10thdt5v	Bi-directional pad; plain input ; 3-state output; 10 ns slew-rate control; TTL with hysteresis; pull-down; 5 V-tolerant
IO3V3	
apio	Analog pad; analog input/output for RF applications; ESD diode to VDD supply
aprf	Analog pad; analog input/output for RF applications; ESD diode to VDDE supply
aprf3v3	Analog pad; analog supply for high-voltage application; high trigger-voltage ESD protection
IO3V3 (supply)	
vddco	VDD pad connected to CORE VDD
vddcobf	VDD pad connected to CORE VDD with BigFET protection
vdde	VDD pad connected to external (noisy) VDD supply rail

Table 3. Pad name description *…continued*

Pad Name	Description
vddi	VDD pad connected to CORE VDD and internal VDD supply rail in I/O ring
vssi	VSS pad connected to CORE VSS and internal VSS supply rail in I/O ring
vsse	VSS pad connected to external (noisy) VSS supply rail
vssis	VSS pad connected to CORE VSS, internal VSS supply rail in I/O ring and substrate rail in I/O ring
vssco	VSS pad connected to CORE VSS

7. Functional description

7.1 Radio subsystem

The complete radio system is able to receive FM, AM, Weatherband, RDS and FM/AM digital radio. The SAF7741HV radio section will incorporate the following features (see Figure 1):

- Two IFADCs to digitize the incoming analog IF signals from the tuner(s)
- Two Primary Decimation Chains (PDCs) for analog and digital radio reception, including digital mixing to Zero IF (ZIF)
- Software-based radio functionality running on one or more DSPs depending on the features set and dual or single tuner usage

The IFADC digitizes the incoming Near-Zero Intermediate Frequency (NZIF) signals. The IFADC is a baseband ΣΔ ADC.

The PDC decimates the incoming data stream by a factor of 128 before passing it to the software radio for processing.

For digital radio reception the PDC decimates the incoming data stream by 64 before it is forwarded to the external co-processor.

The software radio consists of three Tuner DSPs: TDSP1, TDSP2 and TDSP1E. All three TDSPs have a basically identical structure, but TDSP1 and TDSP2 are extended with:

- A Finite Impulse Response (FIR) filter
- CORDIC (COordinate Rotation DIgital Calculation) Rotate and De-rotate (CRD)

TDSP1E is extended with a CRD only. Each FIR (controlled by the TDSP) is used for variable bandwidth control and for the Polar-to-Rectangular (P->R), Rectangular-to-Polar (R->P) and DIV conversions that will be used for demodulation. Added to this block is a 2LOG(LD(x)) function.

In addition, a Radio General-Purpose DAC (RGPDAC) and an RDS decoder are included for each tuner channel.

The SAF7741HV chip is capable of handling full dual radio. Depending on the firmware, several such configurations are possible:

- Dual radio with two stereo-audio output channels. The attainable performance depends on the DSP tuner firmware. The available feature set is less than that for one-channel radio

- Dual tuner, which offers antenna, phased-array or MPX diversity
- Single tuner on the smallest possible hardware set: preferably one DSP

7.1.1 IFADCs

For each tuner path two fully differential ΣΔ IFADCs are used for the I and Q paths. For each IFADC two fully differential input nodes are fed with a 300 kHz input signal. This design provides good suppression of even harmonics. The noise is shaped by a 5th order loop filter to get sufficient resolution in the band of interest, and for complex filtering the input signal of the I and Q paths has a 90° phase shift.

The IFADCs are sampled by a 41.6 MHz clock. The output is a 1-bit bitstream signal with a frequency of 41.6 MHz (see Figure 4).

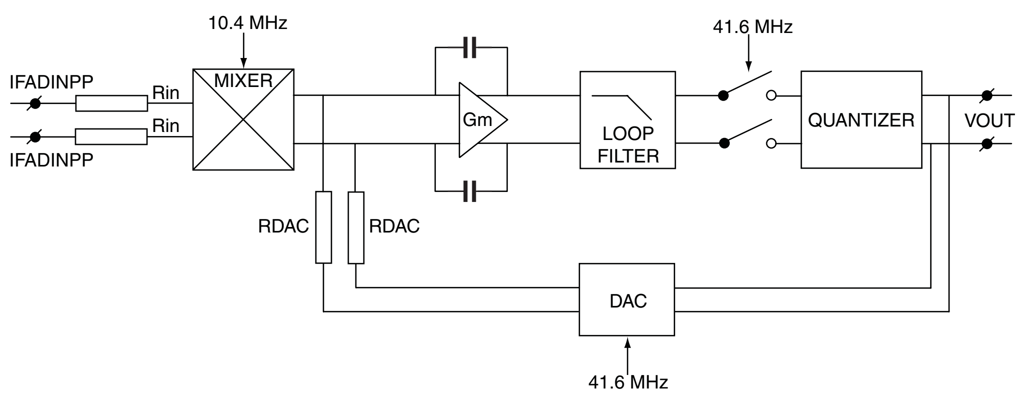


Fig 4. Simplified block diagram of an IFADC

7.1.1.1 TEF6730 tuner compatibility mode

In this mode the IF input signal is 10.7 MHz differential. The mixer is in front of the IFADC, and this converts the input signal down to 300 kHz using a quadrature 10.4 MHz square wave. The 300 kHz down-converted signal is then fed to the IFADCs as I and Q signals.

Switching to TEF6730 tuner compatibility mode is performed via the I^2C interface and is only available to the microprocessor.

7.1.2 Primary decimation chain

The PDC (see Figure 5) decimates the incoming sample rate from the IFADC, shifts the signal to baseband and applies Amplitude Gain Control (AGC) step compensation, linear AGC correction and IQ Correction (IQC).

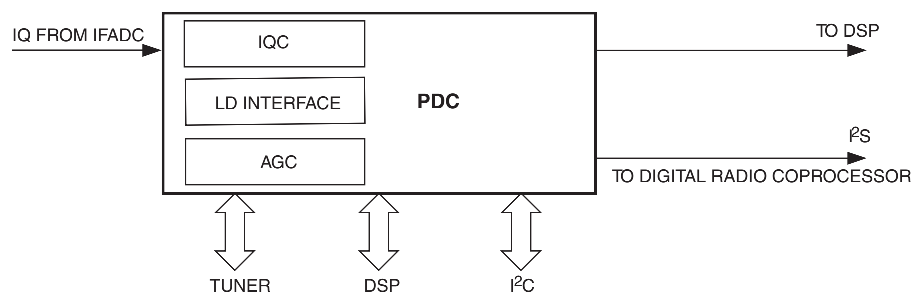


Fig 5. Block diagram of the PDC

The PDC decimates the incoming signal by 16 before shifting it to the baseband and creating two paths: ‘wanted’ and ‘image’. After another decimation by two, the AGC stage takes place to compensate for the tuner gain-reduction steps. The linear gain control stage makes sure that there is maximum use of the dynamic range. After another decimation by two the IQC stage takes place to compensate for imperfections in the analog mixer of the tuner by measuring and correcting possible aliases between the wanted and image signals. The PDC settings allow for different IF bandwidth corrections and for local oscillator swap of the TEF7000. Communication between the tuner and SAF7741HV uses the proprietary two-line LD interface for AGC, injection-mode and bandwidth settings.

The PDC has two data outputs: one parallel inteface to the TDSPs and one I^{2}S-like interface to the external digital radio co-processor.

7.1.2.1 PDC Input

The PDC input is a complex bit stream from the 5th order converter. The I and Q bit streams each have a sample rate of 41.6 MSa/s.

7.1.2.2 Input decimation

The input sample rate of 41.6 MSa/s is decimated by 16 MSa/s to 2.6 MSa/s.

7.1.2.3 Shift-to-baseband mixer

For the wanted signal, the TEF7000 tuner has an IF frequency of 300 kHz for FM and 60 kHz for AM: for the image signal these values are –300 kHz and –60 kHz respectively. The shift-to-baseband mixer shifts the wanted signal by $-f_{mix}$ to baseband and the image signal by $+f_{mix}$. The mixer has two independent registers for the wanted frequency alignment:

- fmix_0 with high-side injection
- fmix_1 with low-side injection

In TEF6730 mode fmix_0 and fmix_1 are 300 kHz for both FM and AM

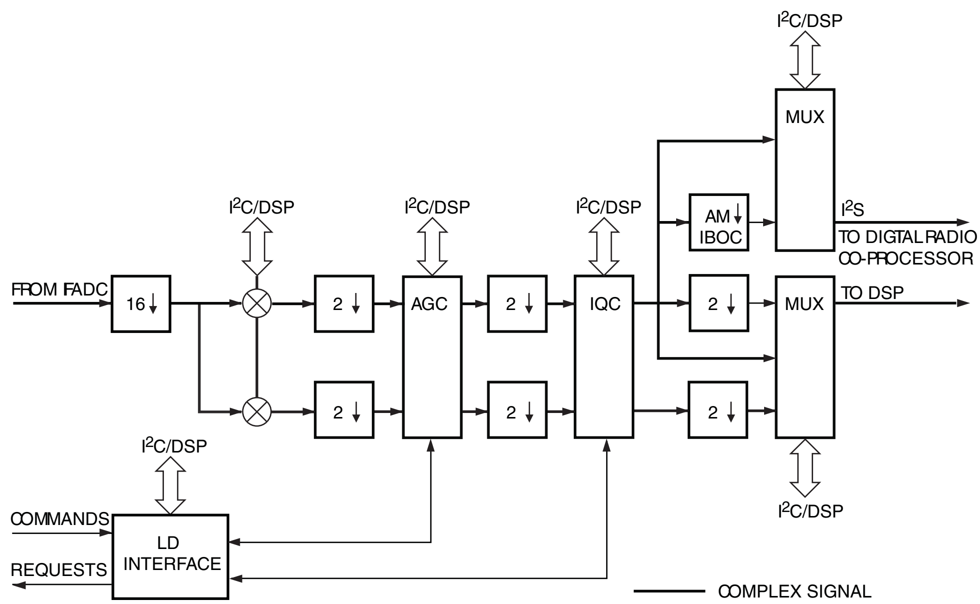


Fig 6. PDC Block diagram for one data path

7.1.2.4 Mixer output decimation

The output signal of the shift-to-baseband mixer is decimated by two to 1.3 MSa/s before it enters the AGC stage.

7.1.2.5 Gain control

Both the wanted and the image signals are gain-controlled in the AGC stage. This contains a stepped gain stage, a linear gain stage and IF signal level detection. The linear gain stage ensures that maximum use is made of the dynamic range (see Figure 7).

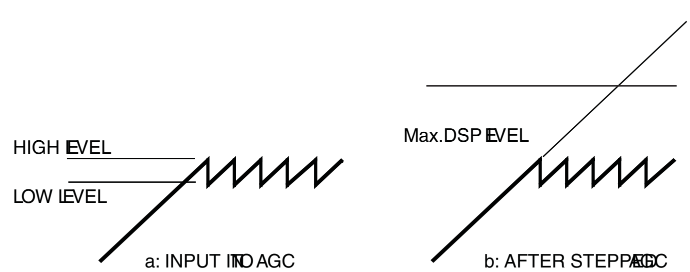


Fig 7. Stepped AGC signal levels

Various gain-step compensation controls are implemented to reduce the audible effects of the gain steps. To increase the dynamic range of the tuner, gain-step compensation takes place in the AGC block of the PDC for:

- Step-response amplitude
- Step-response waveform
- Step-response timing

7.1.2.6 Stepped gain amplitude

The tuner communicates a new gain setting to the SAF7741HV via the DL interface. The SAF7741HV has four independent and different stepped AGC banks:

- AGC_A
- AGC_B
- AGC_C
- AGC_D

The number of steps for each AGC bank and the associated resolution is listed in Table 4.

Table 4. Stepped AGC gain reduction

AGC	Function	Number of Steps	Number of Bits	Resolution
AGC_A	LNA_1	16	12	50 mdB
AGC_B	LNA_2	8	11	50 mdB
AGC_C	Mixer	4	10	50 mdB
AGC_D	IF	4	10	50 mdB

The AGC tables contain the corresponding gain reduction values of the tuner, expressed in bits. Zero gain reduction is at the top of each table. The tuner has random access to the table. The maximum single amplitude change of the AGC is 16 bits −1 LSB. This is equivalent to 96 dB. This maximum amplitude change can be made in any combination of AGC values from AGC_A up to AGC_D. The last gain reduction command from the tuner is readable by the DSP in the AGC Change registers. Found in AGC Data Out registers are:

- The total stepped gain reduction
- The linear gain reduction
- The resulting gain reduction

The TEF7000 tuner uses:

- AGC_A and AGC_B for wideband AGC (in this case LNA_1 and LNA_2)
- AGC_C for the mixer AGC
- AGC_D is used as IF_AGC

Remark: The AGC_A, AGC_B and AGC_D replace the pin-diode AGC in the TEF6730.

7.1.2.7 Step-response waveform

The compensating step-response waveform depends on the step response type to be compensated. Compensating waveforms for the LNA and the mixer gain steps are stored in ROM for both the IF response and the wideband response. The IF response is derived from the PDC response before the AGC stage.

The step-response waveform from the ROM is used when the gain change is less than 12 dB. This results in compensation which is not audible and which therefore does not require muting.

When there is a gain change of more than 12 dB this is made step-wise without running the compensation waveform. This is the case with either Alternate Frequency (AF) updates or a pre-set change. These functions are always used in a muted condition and are therefore not audible.

7.1.2.8 Step-response timing

In order to align for the bandwidth of the analog circuits, an alignment is made between the response length and the response delay. This alignment is separate for the wideband and the IF responses.

Both the delay and the response length for the IF response are dominated by the PDC response before the AGC. These values are independent of the tuner response. The wideband response is different for analog and for digital AM/FM.

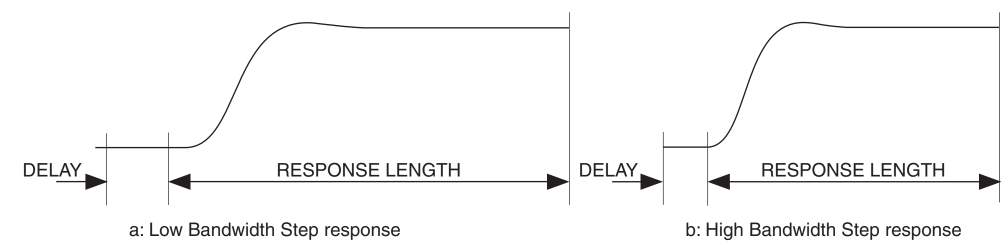


Fig 8. Step response length alignment for different tuner bandwidths

7.1.2.9 Perfect step compensation

Perfect step compensation of the tuner gain steps is made possible for signals within the IF signal band by alignments of amplitude, waveform and waveform delay. Near-perfect alignment is possible for off-centre signals within the IF signal band.

7.1.2.10 Non-perfect step compensation

Perfect compensation of the tuner gain steps is not possible for signals outside the IF signal band. In such cases the resulting interference must be suppressed. In the PDC, four signalling bits are provided for this purpose:

- AGC_A_CHANGE
- AGC_B_CHANGE
- AGC_C_CHANGE
- AGC_D_CHANGE

These bits can be read by the DSP and a soft-mute signal can be generated when required.

7.1.2.11 AGC linear gain

Data-path signals that exceed a certain level are kept constant in a linear controlled-gain stage (see Figure 9). Linear control avoids overload of the following signal stages and makes sure that maximum use is made of the data path's dynamic range. The I^2C interface sets the reference level for linear control as well as the corresponding attack and delay values.

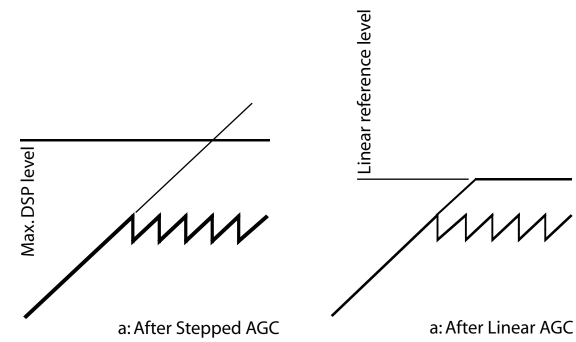


Fig 9. Linear AGC signal levels

The linear control reference level should be above the maximum uncontrolled input level of the linear control stage (See Figure 7). Settings of the reference level below the maximum uncontrolled input level will result in a distorted output signal.

7.1.2.12 IF signal level detection

Signal level detection for wideband AGC is handled in the tuner. The resulting AGC steps are then interfaced to SAF7741HV and a step compensation is made. The IF AGC is controlled by level detectors within the PDC, and by IF detector high- and low-level settings which can be set via IC. The level detectors in the PDC communicate with the tuner to increase or decrease the level of the incoming signal.

The IF detector bandwidth is shown in Figure 10.

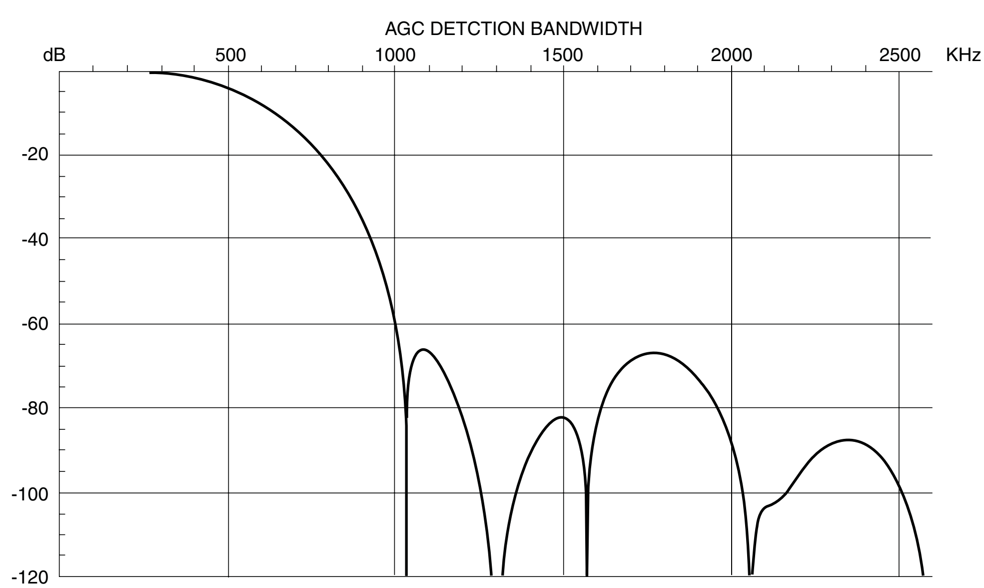


Fig 10. IF detector bandwidth

7.1.2.13 AGC output decimation

The output signal of the AGC is decimated by two to 650 kSa/s before it enters the IQC stage.

7.1.2.14 IQC stage

The IQC stage suppresses the image mirror co-channel within the wanted signal and corrects for gain and phase imperfections in the analog mixer and the subsequent analog data base. This is done by measuring and correcting possible correlations between the wanted and the image signals.

The IQC is an adaptive algorithm based on a Normalized Least Mean Square (NLMS). Normalization is performed off the data path in the Least Mean Square (LMS) adaptation engine itself, and therefore does not affect the output signals of the PDC. It takes place in steps of 6.0 dB with an associated averaging filter. Four coefficients are available to allow the IQC to manage frequency dependencies introduced by the analog IF filters. The adaptation rate parameter (mu) is controlled automatically at startup to make sure that the coefficients converge correctly.

An adaptation freeze level can be set to prevent tap drift in weak signal conditions.n TEF6730 mode the IQC stage is bypassed.

7.1.2.15 PDC output

The PDC has two outputs; one to the software radio and the other to the external pins. For the output to the software radio a choice can be made between three signals. The first of these is the wanted signal at 650 kSa/s. The bandwidth for this is shown in .Figure 11

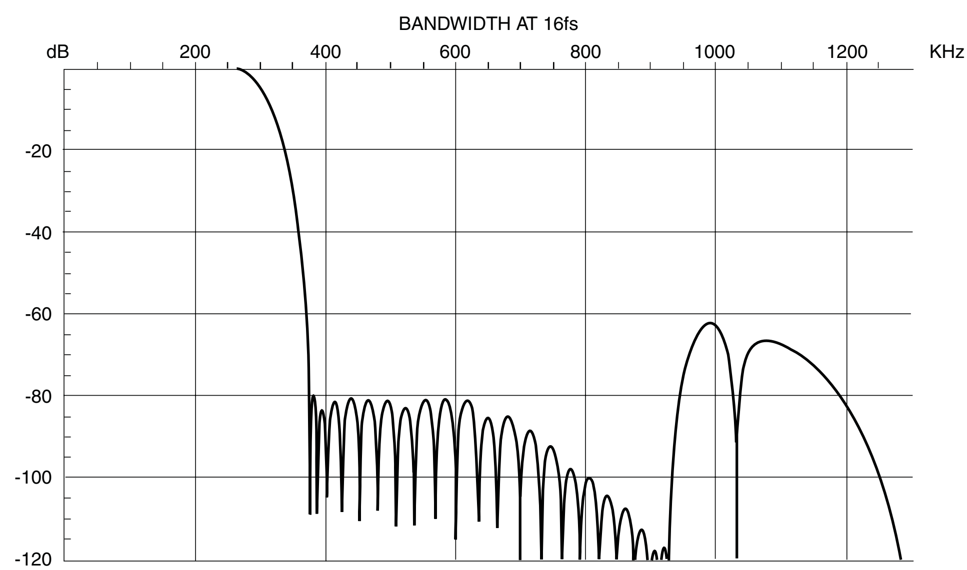


Fig 11. PDC to EPICS output bandwidth at 650 kSa/s

The second choice is the wanted signal at 325 kSa/s. This is shown in Figure 11. The third choice is the wanted/image signal pair at 325 kSa/s. The signal bandwidth for this is shown in Figure 12.

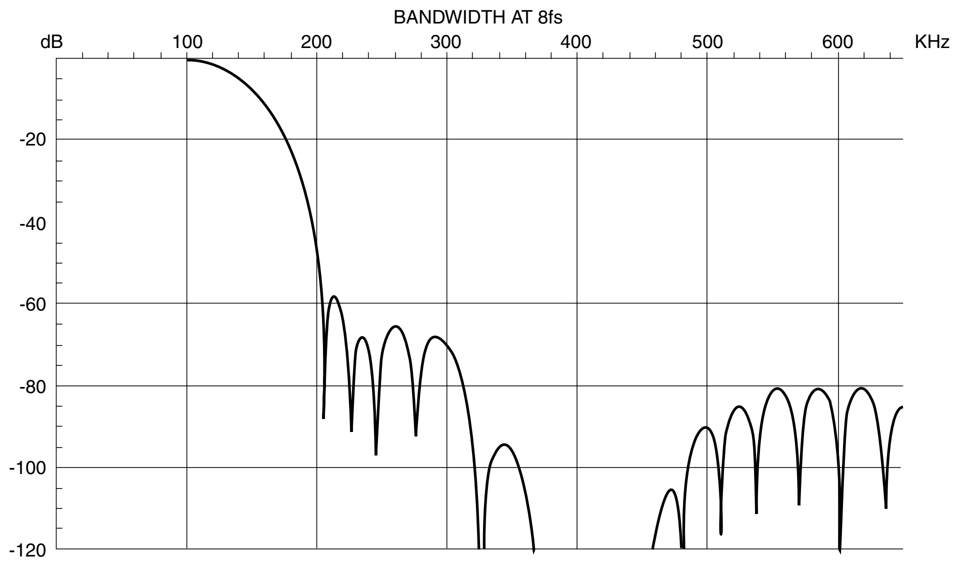


Fig 12. PDC to EPICS output bandwidth at 325 kSa/s

For the I²S external output a choice can be made between FM and AM digital radio, both at 650 kSa/s and both wanted-signal only. All PDC input and output signals are complex.

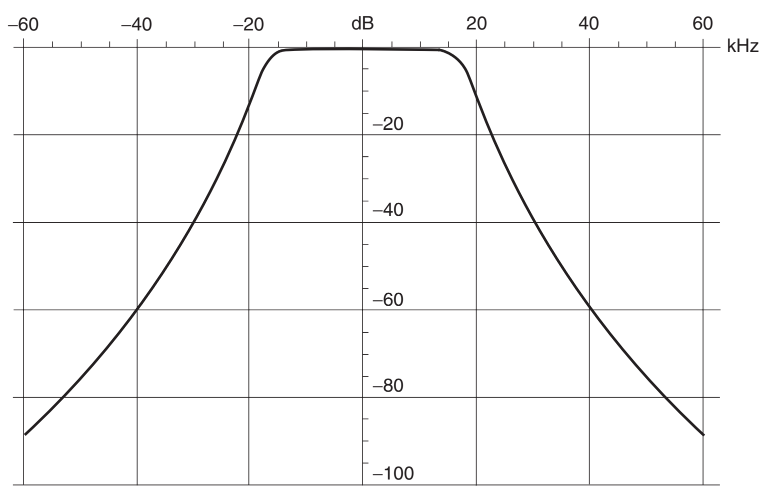


Fig 13. AM digital radio bandwidth

7.1.2.16 LD interface

The SAF7741HV is designed for a generic tuner with TEF7000 architecture. Communication between the tuner and the SAF7741HV uses the proprietary two-line LD interface for AGC, injection-mode and bandwidth settings.

The tuner sends commands to the SAF7741HV while the SAF7741HV sends requests to the tuner. A tuner command is always executed unconditionally by the SAF7741HV, but a request from the SAF7741HV to the TEF7000 may be ignored.

AGC commands define the gain compensation required to compensate for the gain change of the tuner, and can also reset detectors in the stepped and the linear AGC.

The LD interface commands and their bit allocation are listed in Table 5. Refer to the tuner data sheet for the different signal bands.

Table 5. LD interface command bit allocation

Bit	Function	Bit	Function
B22	Reserved	B10	AGC_C[1]
B21	Reserved	B09	AGC_C[0]
B20	Reserved	B08	AGC_D[1]
B19	Reserved	B07	AGC_D[0]
B18	Reserved	B06	AGC_DM
B17	AGC_A[3]	B05	RST_DET_D
B16	AGC_A[2]	B04	RST_LIN
B15	AGC_A[1]	B03	INJ
B14	AGC_A[0]	B02	INJM
B13	AGC_B[2]	B01	BW
B12	AGC_B[1]	B00	BWM
B11	AGC_B[0]	–	–

The LD interface requests from the SAF7741HV and their bit allocations are listed in Table 6.

Table 6. LD interface request bit allocation

Bit	Function
B06	Reserved
B05	Reserved
B04	Reserved
B03	DET_D[1]
B02	DET_D[0]
B01	INJ
B00	BW

In TEF6730 mode, the DL Interface is replaced by 2 IF-AGC bits.

7.1.3 Digital radio interface

For digital radio an I^{2}S output is provided for the I and Q signals (see Figure 14). A GPIO pin can be used as a blend input that makes it possible to switch from conventional FM and AM processing to digital radio processing.

There are two possible ways to get digital radio data:

- Digital radio interface 1 output, from either PDC1 or PDC2
- Digital radio interface 2 output via the T1E I^{2}S interface from PDC2

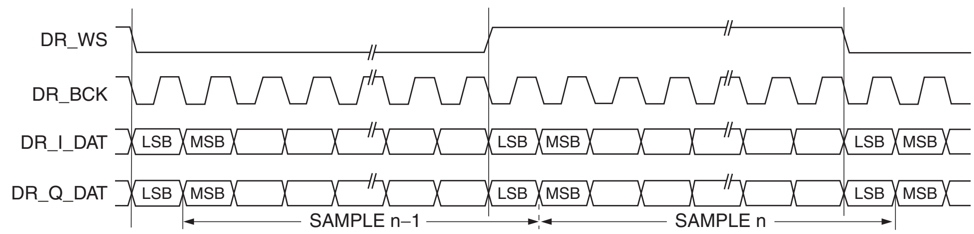


Fig 14. Digital radio I²S output format

7.1.4 RGP DAC

RGP digital-to-analog conversion is performed by a 10-bit DAC with a buffered output. This is part of the radio subsystem and can be used for various functions linked to the radio domain.

A double buffered interface is located between the DSP and the RGP DAC. The buffer is 2×8 words in length, which means that data with a maximum sample rate of 8 Fs (i.e. 325 kHz) can be transferred to the output when the DSP is running at 1 Fs (i.e. 40.625 kHz).

7.1.4.1 TEF6730 tuner compatibility

In TEF6730 tuner compatibility mode the general-purpose DAC can be used for controlling the PIN diode in front of the tuner. In addition to its digital AGC function this operates as second-level gain correction for the IFADC.

7.1.5 Radio Data System demodulator/decoder

7.1.5.1 General description

There are two Radio Data System (RDS) demodulation and decoder systems available on the SAF7741HV. The description below applies to each of them.

The RDS function recovers the additional and inaudible RDS information transmitted by FM radio broadcasting. The operational functions of the demodulator and the decoder are in accordance with EBU specification EN50067.

The function processes the RDS signal frequency-multiplexed within the stereo MultiPleX (MPX) signal to recover the information transmitted over the RDS data channel. This processing consists of band-pass filtering, demodulation and RDS/ Radio Broadcast Data System (RBDS) decoding. The RDS band-pass filter discards the audio content from the input signal and reduces the bandwidth.

The RDS demodulator regenerates the raw RDS bitstream (bit rate = 1187.5 Hz) from the modulated RDS signal. Connection to the RDS/RBDS decoder is by means of the DSP flags (see Figure 15).

Under I²C control via bit rds_clkin an internal buffer can be used to read out the raw RDS stream in bursts of 16 bits. With the I²C bit rds_clkout the RDS clock can be either enabled or switched off.

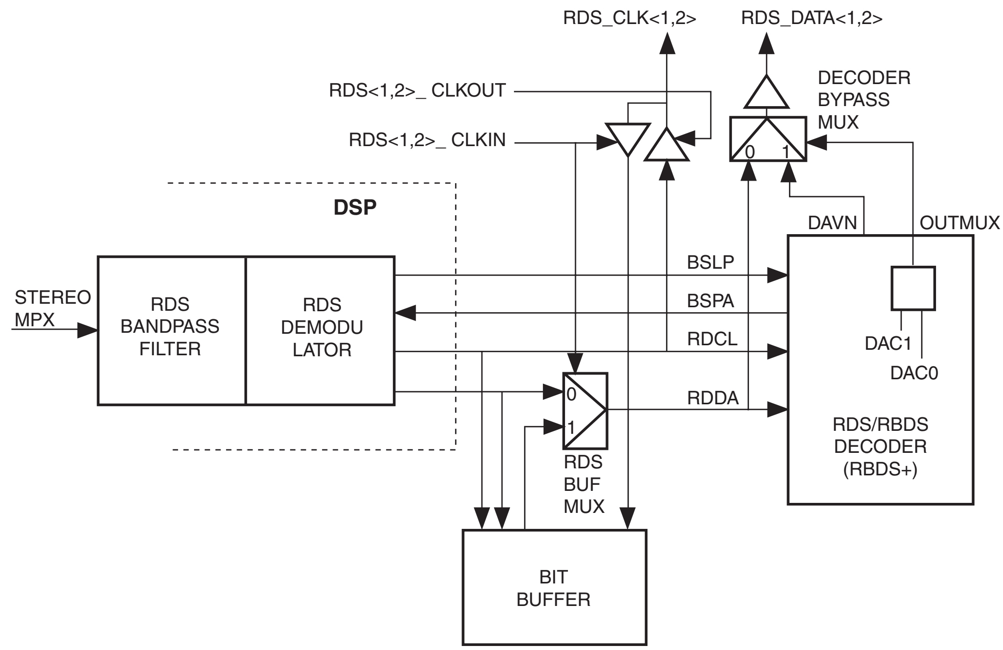


Fig 15. RDS/RBDS Functional block diagram

The RDS/RBDS decoder provides:

- Block synchronization
- Error detection
- Error correction
- Complex flywheel function
- Programmable block data output

Newly processed RDS/RBDS block information is signaled to the main microcontroller as ‘new data available’ by use of the DAVN output. The block data itself and the corresponding status information can be read out by means of an I²C bus request.

The RDS chain derives data information from the MPX signal independently of either the analog or the digital audio streams. This allows RDS updates during playback from tape or other sources.

7.1.5.2 RDS I/O modes

Apart from the control inputs and data outputs via the I²C inteface, the inputs and the outputs related to the RDS function are listed in Table 7, Table 8 and Table 9

Table 7. Unbuffered raw (direct) RDS output mode (rds<1,2>_clkin = 0, rds<1,2>_clkout = 1 and DAVD mode: dac0 = 1, dac1 = 1)

Name	Description
RDS_CLK	Clock of the raw RDS bit stream. This is extracted from the bi-phase coded baseband signal by the RDS demodulator. The clock period is 1.1875 kHz. See Ref. 1 for more details.
RDS_DATA	Raw RDS bit stream, generated by the demodulator. This allows for external receivers of the RDS data to clock the data on the RDS_CLK signal as well as on its inverse. See Ref. 1 for more details.

Table 8. Buffered raw RDS output mode (rds<1,2>_clkin = 1, rds<1,2>_clkout = 0 and DAVD mode: dac0 = 1, dac1 = 1)

Name	Description
RDS_CLK	Burst clock, generated by the multi-processor. Bursts of 17 clock cycles are expected. The average time between bursts = 13.5 ms.
RDS_DATA	Bursts of 16 raw RDS bits are put out under the control of the burst clock input. This output is high after a data burst, and is pulled low when 16 new bits are available and a new clock burst is awaited. The microprocessor has to monitor this line at least every 13.4 ms.

Table 9. DAVA, DAVB and DAVC modes (rds<1,2>_clkin = 0, rds<1,2>_clkout = 0)

Name	Description
davn	Data-available signal for synchronization of a data request between the main controller and the decoder (for further information see Ref. 2).

Remark: Rds<1,2>_clkin = 1 and rds<1,2>_clkout = 1 is NOT an allowed mode.

Depending on the mode selected, the same output is used for RDS_DATA and DAVN (see Figure 15).

7.1.5.3 RDS timing of clock and data signals in DAVD mode

The timing of the clock and data outputs is derived from the incoming data signal. Under stable conditions the data will remain valid for 400 ms after the clock transition. The timing of the data change is 100 ms before a positive clock change. This timing is well suited to positive- and negative-triggered interrupts on a microprocessor.

It is possible that phase faults will occur during poor reception, in which case the duty cycle of the clock and data signals will vary between a minimum of 0.5 and a maximum of 1.5 times the standard clock period. Faults in phase do not normally occur on a cyclical basis. See also Section 14.1.

7.1.5.4 RDS bit buffer

The repetition frequency of the RDS data is 1187.5 Hz. This results in an interrupt on the microprocessor every 842 ms, but the double 16-bit buffer allows this timing requirement to be relaxed since the two 16-bit buffers are filled alternately. If a buffer has not been read out by the time the other buffer is filled it will be overwritten and the old data will be lost. While a 16-bit buffer is being filled the RDS bit buffer keeps the data line high.

When a 16-bit buffer is full the data line is pulled down. The microprocessor has to monitor the data line at least every 13.5 ms. The data line remains low until the microprocessor pulls the clock line low. This starts reading out of the buffer, and the first bit is put on the data line. The RDS bit buffer puts a bit on the data line after every falling clock edge, and the data remains valid while the clock is high. After 16 falling and 16 rising edges the whole buffer is read out and the bits are stored by the microprocessor. After a 17th falling clock edge the data line is set high until the other 16-bit buffer is full. The microprocessor stops communication by pulling the clock line high again. See Section 14.1.

7.1.5.5 RDS demodulator

The RDS demodulator is implemented in DSP software. See Ref. 1 for details of its functionality.

Demodulator decoder interface: Communication between the RDS demodulator and decoder is provided by Economic Parameterized Integrated Cores (EPICS) flags and consists of four signals as shown in Figure 15.

Remark: Instead of the EPICS flags, the RDS decoder connection register can be used for demodulator decoder communication. For further details see Ref. 3.

Table 10. Signals provided by the demodulator

Name	Description
rdcl	Demodulator clock output. Generated by the RDS/RBDS demodulator for every RDS/RBDS clock period (1.1875 kHz). This pulse remains high for about half of an RDS/RBDS clock period (~420 μs). The rising edge of this signal is used as an input shift enable for the decoder internal data buffer (RDS Data Output [RDDA] bit input). It is assumed that the RDDA input will remain unchanged for at least one system clock (10.4 MHz) after a rising RDCL edge.
rdda	Demodulator data output. Represents the actual RDS/RBDS data bit. The RDDA is shifted into the decoder module internal data buffer by detection of a rising edge on the RDCL input signal.
bslp	Bit-Slip (BSLP) detected. This is set to high for at least one RDS/RBDS clock period (1.1875 kHz), but only when the demodulator detects a possible BSLP. The BSLP signal itself has to be reset to low after one RDS/RBDS clock period.

Table 11. Signals received by the demodulator

Name	Description
bspa	Bit-Slip Process Active (BSPA). This is set to HIGH when the RDS decoder detects a BSLP: at all other times it is LOW.

Remark: The current version of the SAF7741HV firmware does not use bslp/bspa signalling. This is implemented in the hardware, and is therefore mentioned here for information only.

7.1.6 8Fs I^{2}S interface

The 8Fs I^{2}S interface is used to transform the parallel data outputs of the TDSP1 (24 bits wide) to serial data in I^{2}S format, and then make that data available at the digital radio interface 1 (see Figure 16). The TDSP1 has the capability to write data to the interface at 1Fs, 2Fs, 4Fs and 8Fs.

Depending on the flag values, the interface can send data in I^{2}S format at 1Fs, 2Fs, 4Fs, 8Fs and 16Fs.

Table 12 gives all possible combinations of speeds at which the interface receives and sends data.

Table 12. TDSP1/I^{2}S interface receive and send data speeds

TDSP1 Speed	I^{2}S Speed
1Fs	1Fs, 2Fs, 4Fs, 8Fs
2Fs	1Fs,2Fs, 4Fs, 8Fs, 16Fs
4Fs	1Fs,2Fs,4Fs, 8Fs,16Fs
8Fs	1Fs,2Fs,4Fs,8Fs, 16Fs

The size of the buffer is determined by the largest factor between the speeds of the TDSP1 and the IIS, which is the case when the TDSP1 runs at either 1Fs and the IIS at 8Fs or when the TDSP1 runs at 2Fs and the IIS at 16Fs. In the first case the TDSP1 has to be able to write two words of 24 bits - i.e. left data and right data for stereo samples at 1Fs speed - and the speed at which the read should be performed by the IIS interface is 8Fs. Therefore the required buffer size is 16×24 bits. Moreover, the buffer is required to support double buffering; i.e. it can be written to and read from at the same time. This makes the total size of the buffer 32×24 bits.

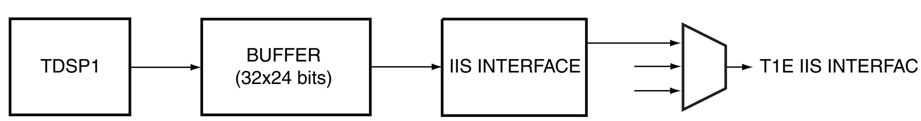


Fig 16. Top-level diagram of 8Fs I^{2}S interface

7.1.7 Tuner I^{2}S interface

The Tuner I^{2}S interface provides a connection between the output multiplexer and TDSP1E. There are two data converters, one converting parallel data (24 bits wide) to IIS format and the second converting from I^{2}S format to parallel. The two converters both run at the TDSP1E sample rate. The format of the I^{2}S data can be configured by setting the applicable registers, and the internal I^{2}S generator and I^{2}S receiver both work as masters. The result is that the signals ‘word select’ and ‘serial clock’ are always generated internally.

7.1.8 Output multiplexer

The output multiplexer behind the tuner I^{2}S interface maps four different serial data streams to and from the pins:

- Data going to or coming from the tuner I^{2}S interface (I^{2}S in/out)
- Data T1 coming from the software radio and going to the SRC DSP (SDSP) (I^{2}S out)
- Data T2 coming from the software radio and going to the SDSP (I^{2}S out)
- Data coming from PDC2 (digital radio format out)

7.1.9 Software radio user flags

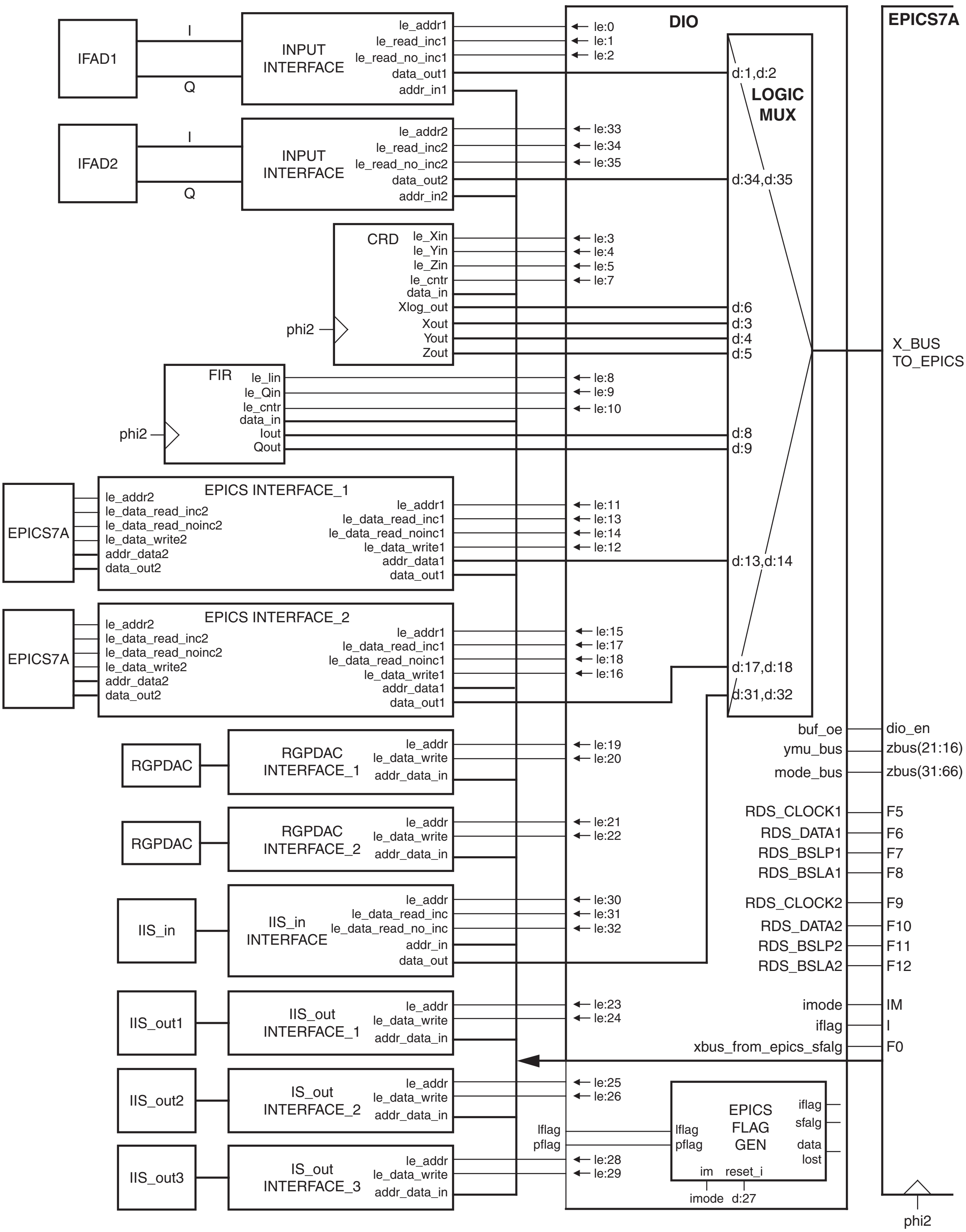


Fig 17. Software radio TDSP1 DIO block diagram (superset of all TDSP DIOs)

The user flags of the TDSPs can be programmed for various functions described below. Every TDSP has 13 I/O flags available. Table 13 shows all the possibilities for each user flag.

Table 13. TDSP user flags

User Flag	Chip Pin Name	Function	Mode[1]	
			I/O	Stretch
F0	–	SFLAG input from EPICS flag generator	IN	OFF
F1	TDSP_IOF1	User-defined in or out	IN/OUT	ON/OFF
F2	TDSP_IOF2	User-defined in or out	IN/OUT	ON/OFF
F3	TDSP_IOF3	User-defined in or out	IN/OUT	ON/OFF
F4	TDSP_IOF4	User-defined in or out	IN/OUT	ON/OFF
F5	TDSP_IOF5	User-defined in or out/clock output to RDS decoder1	IN/OUT	ON/OFF
F6	TDSP_IOF6	User-defined in or out/data output to RDS decoder1	IN/OUT	ON/OFF
F7	TDSP_IOF7	User-defined in or out/BSLP output to RDS decoder1	IN/OUT	ON/OFF
F8	TDSP_IOF8	User-defined in or out/bspa input from RDS decoder1	IN/OUT	ON/OFF
F9	TDSP_IOF9	User-defined in or out/clock output to RDS decoder2	IN/OUT	ON/OFF
F10	TDSP_IOF10	User-defined in or out/data output to RDS decoder2	IN/OUT	ON/OFF
F11	–	ADSP TDSP1E interface/RDS decoder	IN	ON/OFF
F12	–	Out flag to the WDOG value registers/ADSP TDSP1E interface/RDS decoder	IN	ON/OFF

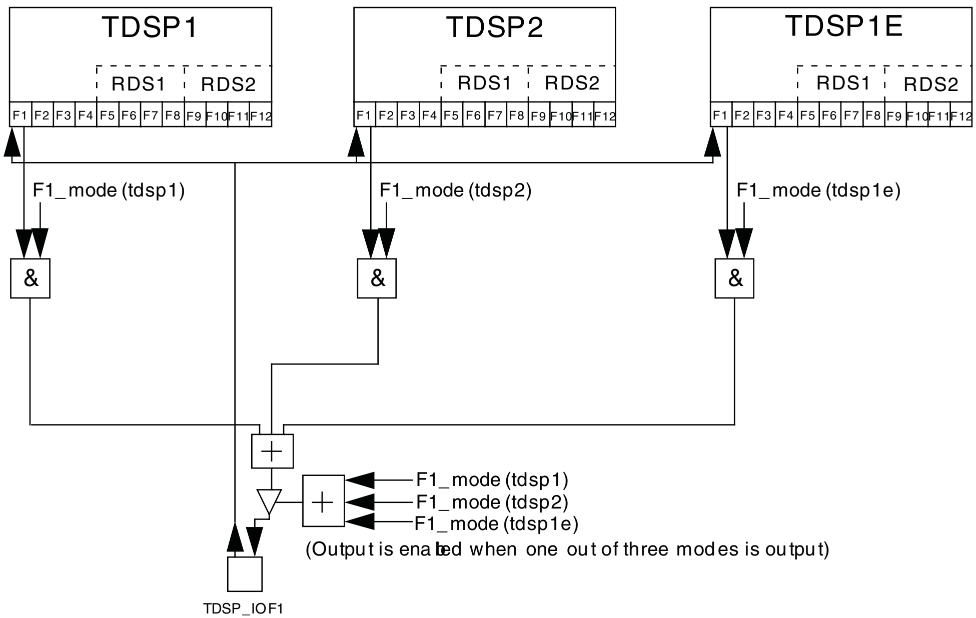
[1] All I^{2}C-controllable

There are 10 general purpose I/O pins available for the software radio. These have to be shared between the available TDSPs as shown in Figure 18. In this diagram only TDSP_IOF1 is depicted since all the other flags are connected the same way.

In the description that follows the value of ‘n’ can be 1 to 10.

1. Pin TDSP_IOFn is wired directly to the input flag ‘n’ of each TDSP.
2. The output flags ‘n’ of all the TDSPs are OR-ed together and the resulting signal is wired to TDSP_IOFn.
3. All the flags on all the separate TDSPs can be set to input or output in the I^{2}C registers. The pad of TDSP_IOFn is input when all TDSP flags ‘n’ are set to input: otherwise it is used as an output.
4. All the flags on all separate TDSPs can be set to stretch mode or non-stretch mode in the I^{2}C registers.

There are exceptions to the above description. On the chip there are two RDS decoders that can be connected to either of the TDSPs, using predefined pins on the DSP when connected. The corresponding TDSP pins connected to the RDS decoder are then fixed as RDS pins and are no longer available as user-defined. The stretch mode of the corresponding pins is switched off. Which RDS decoder is connected to which TDSP is controlled in the I²C registers. Table 13 shows which flags are used for RDS when connected.



Remark: F11 and F12 are not available outside of the chip.

Fig 18. Overview of RDS user-defined flag configuration

7.1.9.1 EPICS flag generator

The EPICS flag generator generates two flags: IFLAG and the Sync Flag (SFLAG). IFLAG is connected to the ‘I’ input flag of the EPICS and SFLAG is connected to the user flag 0. SFLAG indicates that the EPICS should use page0 of the EPICS interface memories to avoid read and/or write errors and conflicts.

The normal duration of IFLAG is four EPICS clock periods. The SFLAG is set until the next IFLAG is generated.

The EPICS can stretch (IMODE) IFLAG via the IM input.

7.1.9.2 Flag overview

When IFLAG is in stretch mode (IM is high) the flag is set at every rising edge of LFLAG. IFLAG can be reset only with the RESET_I input connected to a DIO address. When this address is read by the EPICS, RESET_I is pulsed. SFLAG is not stretched. If IFLAG is not cleared before the next LFLAG the LOST_DATA flag is set.

When IFLAG is not in stretch mode (IM is low) then an IFLAG is generated at every rising edge of the LFLAG . If at this point PFLAG is high, then SFLAG is set until the next rising edge of LFLAG (see Figure 19). LFLAG and PFLAG are generated in the software radio flag generator.

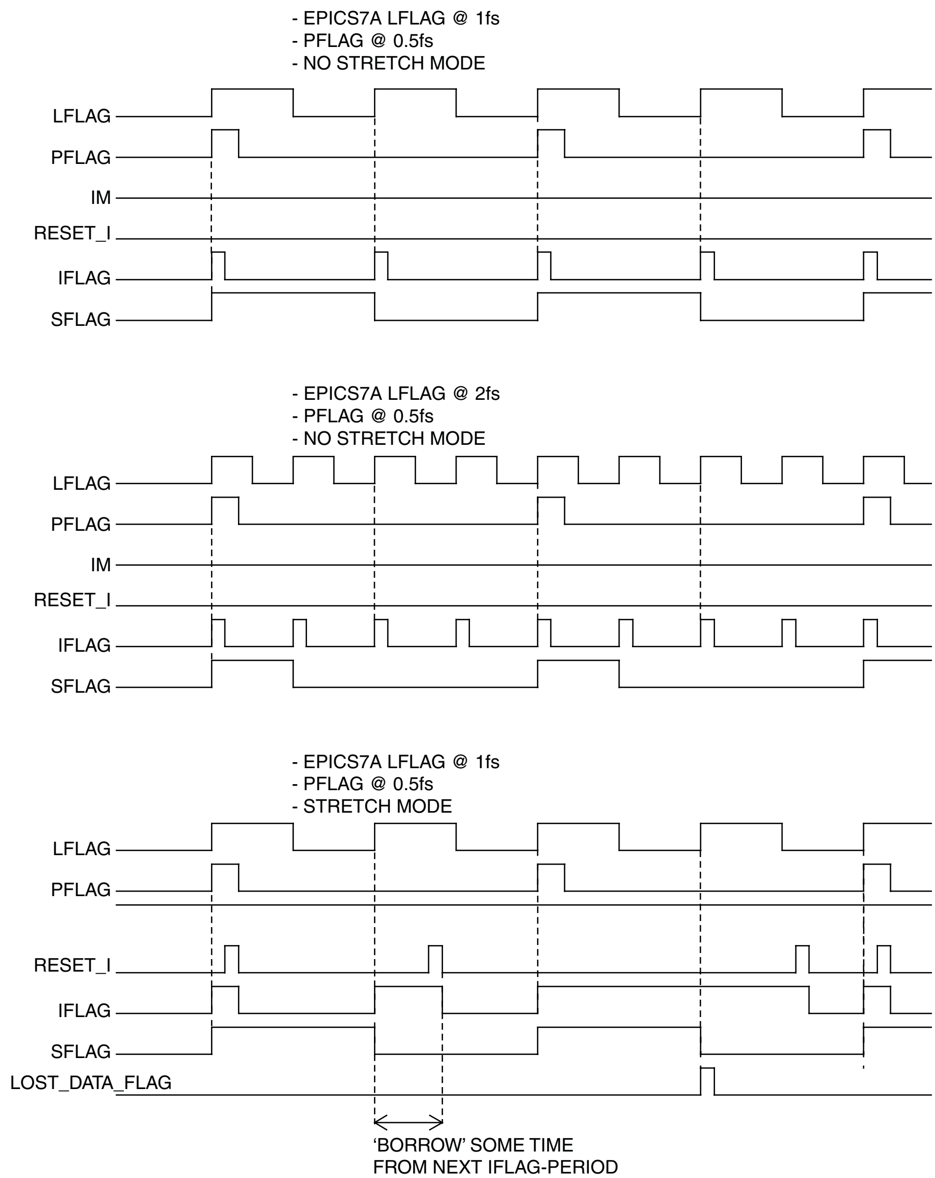


Fig 19. Overview of the user defined flag configuration

7.2 Audio subsystem

The audio subsystem (see Figure 2) consists mainly of four sequential sections:

- Input section (analog and digital)
- SRC section
- Audio processing section
- Audio output section

7.2.1 Input section

The audio input section is split into an analog and a digital input.

7.2.1.1 Analog audio input paths

The analog input section consists of an analog source selector and five ADCs. The outputs of the ADCs are connected to the ADSP. The audio sample rate of these inputs can be a maximum of 55 kHz. When the ADSP runs at a higher rate the inputs need to be routed via a software up-sampler.

7.2.2 Signal flow of the analog audio input

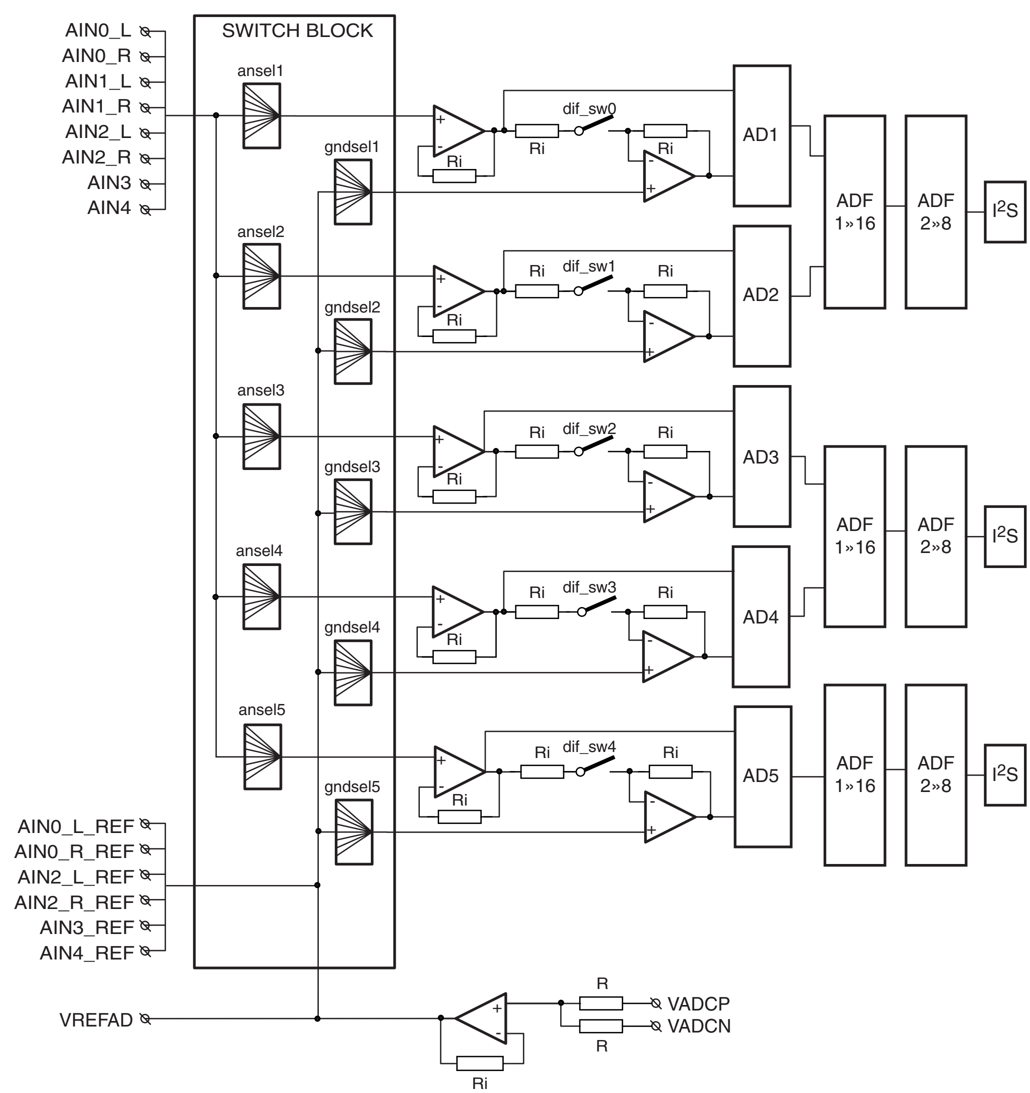


Fig 20. Analog audio input switching block diagram

The input switching for the five possible analog channel setups is very flexible. Using the switches gndsel0 to gndsel4 (see) and ansel0 to ansel4 all combinations can be made either for normal inputs or for high common-mode inputs with a ground connection (see Figure 20)

In principle, any signal input can be connected to any ADC. However, it is possible to make the stereo signals use the even-numbered ADCs (ADC0, ADC 2 and ADC4) for the left channels and the odd-numbered ones (ADC 1 and ADC 3) for the right channels. The only conditions are that:

- When the input signals do not have a ground pin the minus input of the second Op-amp in the signal chain must be connected by means of the gndsel switches to the VREFAD line.
- When there is a high common-mode input with ground input pin the associated gndsel switch must be connected to this pin.
- Some connections to the switching matrix are 'reserved'. These must not be used.

Table 14 and Table 15 show the possible connections.

Table 14. Selection of analog signal switches

Position	ANSEL1 to ANSEL5
000	AIN0_L
001	AIN0_R
010	AIN2_L
011	AIN2_R
100	AIN3
101	AIN4
110	AIN1_L
111	AIN1_R

Table 15. Selection of the analog ground switches

Position	ANSEL1 to ANSEL5
000	AIN0_L_REF
001	AIN0_R_REF
010	AIN2_L_REF
011	AIN2_R_REF
100	AIN3_REF
101	AIN4_REF
110	VREFAD
111	Reserved

7.2.3 Realization of the common mode inputs

A high Common-Mode Rejection Ratio (CMRR) can be created for all the analog inputs by use of the ground pins. To create a signal input, connect the ground pin that is to be used to the second Op-amp in the signal path by using the gndsel switch. This ensures that the two signal lines that go to the ADC will contain the common-mode signal. The ADC itself will suppress the signal very effectively, so in this way good common-mode signal suppression will be achieved.

An example of a high common-mode stereo input with two ground shielding lines is shown in Figure 21.

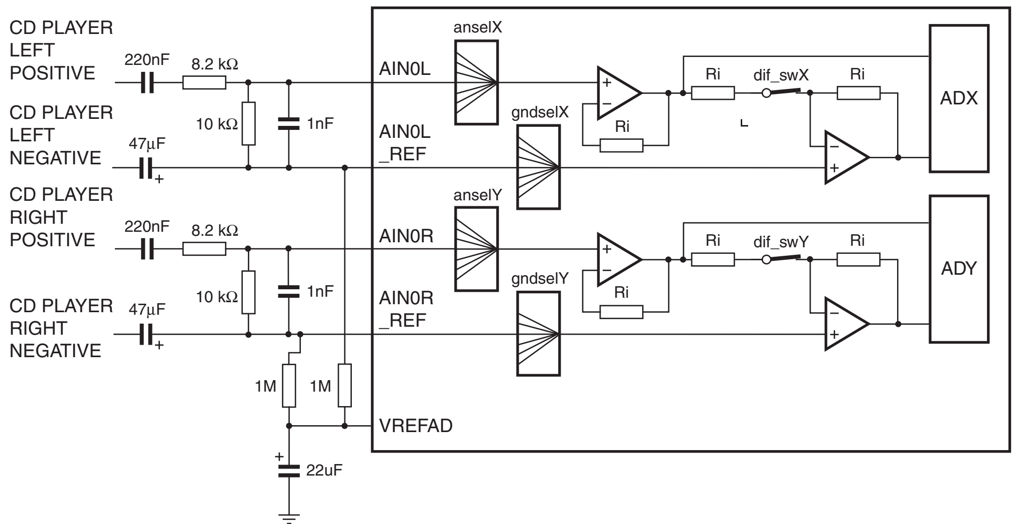


Fig 21. High common-mode stereo input with two ground lines

In this example input voltage reduction is accomplished by the external 8.2 kΩ to 10 kΩ resistor divider. The rather low-value resistor divider is necessary because in this case the parasitic capacitance on pins AIN0_L and AIN0_R will reduce the common-mode signal on them. The CMRR can be guaranteed when the source and cable impedance do not exceed the specified value as stated in the conditions column of Table 35.This leads to a reduction of the CMRR when the source impedance is too high. Half of the supply voltage is provided as reference by connecting the negative inputs of the second operational amplifier to VREFAD by means of the gnd_sel switches and the external 1.0 MΩ resistor. The 1.0 nF capacitors are used for anti-aliasing.

An example of a high common-mode input with only one ground-shielding line is shown in Figure 22.

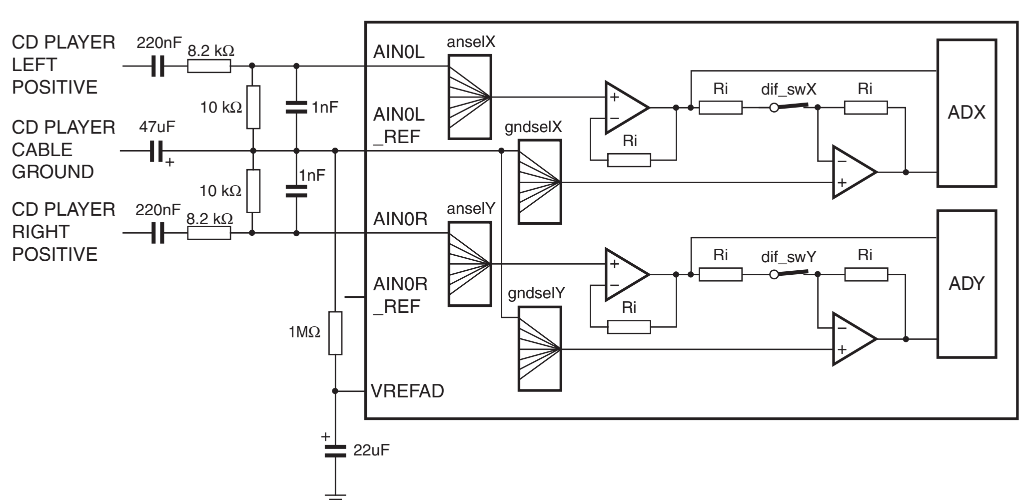


Fig 22. High common-mode stereo input with one ground line

A full-stereo differential input of a CD changer is shown in Figure 23. The switches dif_sw are shown open, and only when signals on the inputs (marked POS and NEG) are different will analog-to-digital conversion take place. Common-mode signals on the inputs will also appear as common-mode signals on the ADC inputs and will not be converted to the digital data stream.

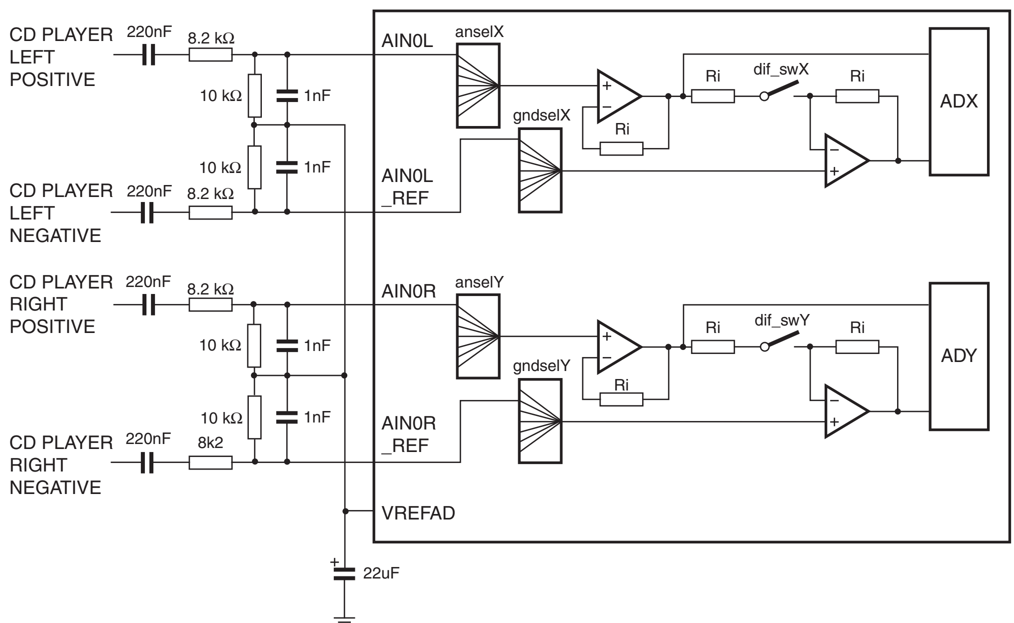


Fig 23. Differential stereo input

The differential-mode application of a single-ended input is shown in Figure 24. In this case the input voltage is reduced symmetrically with two 82 kΩ resistors and one100 kΩ resistor. This neutralizes the effect of parasitic capacitance on the AIN3 input and the AIN3_GND input to permit a relative high-ohmic resistor divider to be used. In this example common-mode signals which have not been reduced in value are applied to the ADC. The ADC itself has a very good CMRR, so this input also has a high CMRR.

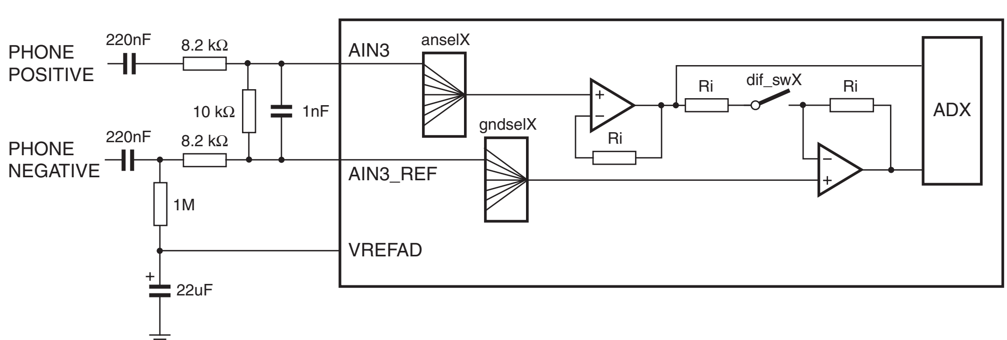


Fig 24. Differential mono input

In Figure 25 a single-ended input is shown. The reference here is VREFAD which is connected internally, so no common-mode rejection can be expected.

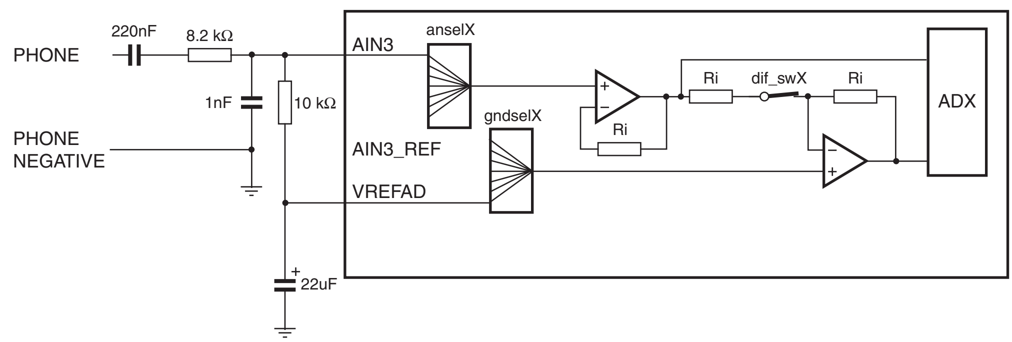


Fig 25. Single-ended input

7.2.4 Audio ADC decimator paths (DAD)

7.2.4.1 Functional description

Decimation of the audio ADC signals is completed in a block called DAD. This block can handle the signals from two ADCs, so a stereo signal can be processed.

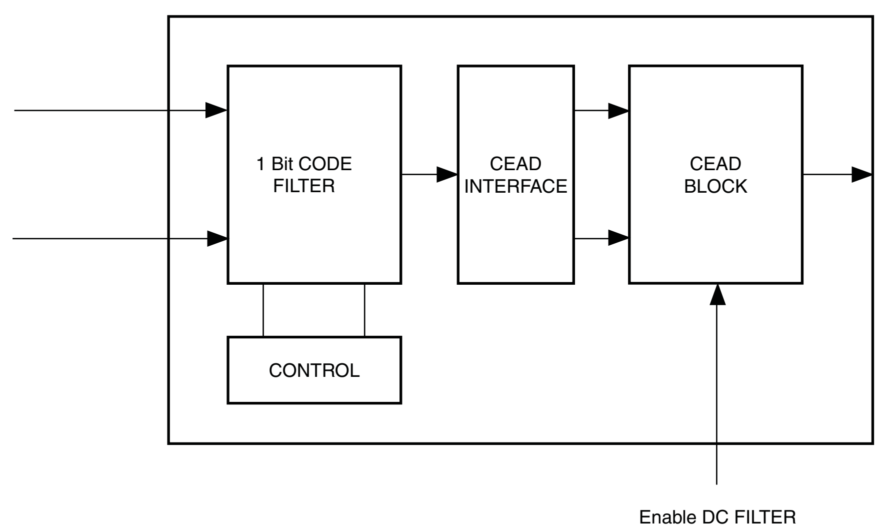


Fig 26. DAD block diagram

The input signal has a sample frequency of $128 \times$ fs and comes from a third-order $\Sigma\Delta$ ADC. The first step in the decimation process is done by the 1-bit code Cascaded Integrator Comb (CIC) filter and Audio Decimation Filter 1 (ADF1) filter. See Figure 26. The CIC filter decimates the input sample rate by a factor of 16 and thus results in a sample rate of $8 \times$ fs.

After the 1-bit code filter, sample reworking is necessary to enter the CEAD block and the ADF2. The CEAD block further decimates the audio samples by 8, giving a sample rate of $1 \times$ fs. The overall gain in the pass band of the decimation filter (including the CIC filter and the CEAD block) becomes 4.85 dB. A nominal input level of –8.45 dB comes from the ADC and results in a –3.6 dB level after decimation.

The DC filter in the CEAD block is controlled by an I^2C bit that can be found in Ref. 3. Power-on reset circuitry is not implemented, which means that after power-up all filters will go through a brief transient phase before they reach their steady-state behavior.

7.3 Audio Digital-to-Analog (ADAC) conversion

The ADAC module consists of a DAC, an interpolation filter and a noise shaper for the audio. Both the analog and the digital functions are described here.

The digital part consists of an interpolation filter which increases the sample rate from 1 fs to 128 fs and a third-order noise shaper that runs at 128 fs.

The analog part consists of six single-ended DAC modules for the left, the right, the centre and the sub-woofer channels.

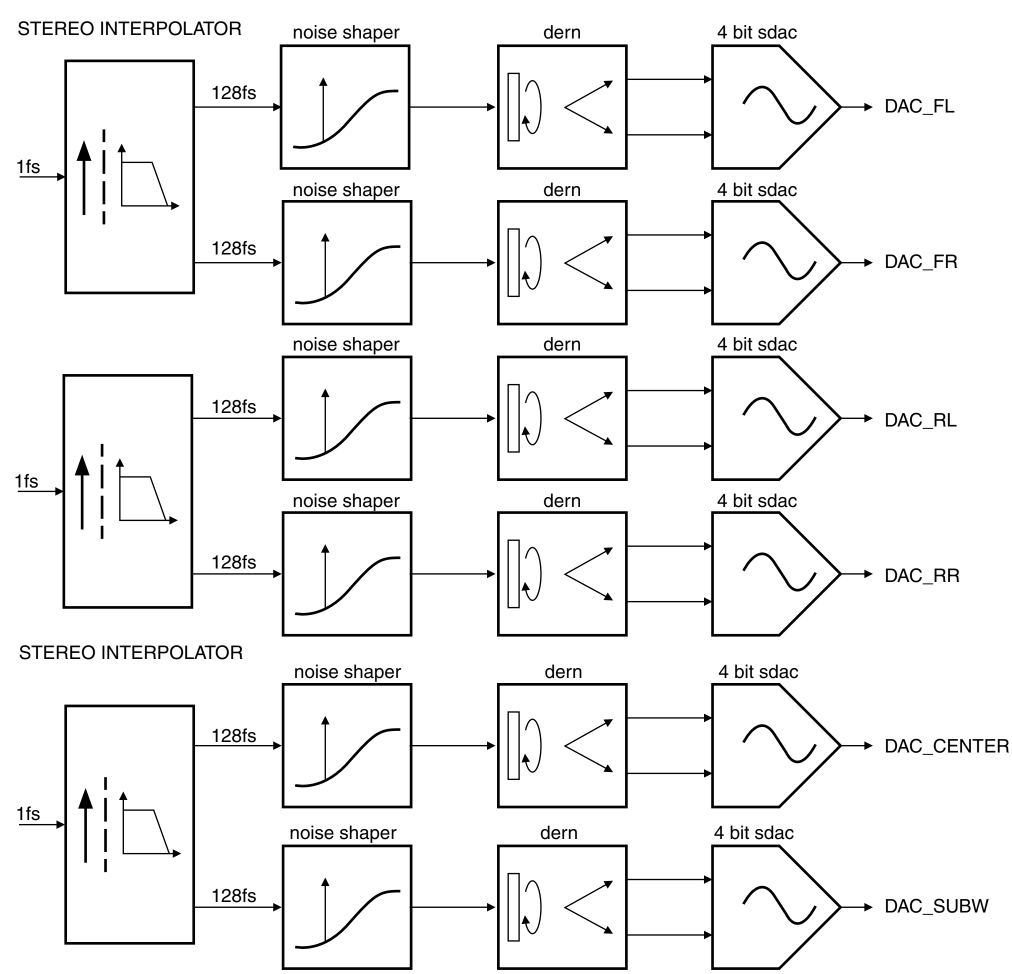


Fig 27. Audio DAC block diagram

7.3.1 Functional description

The audio DAC comprises these functions:

- Digital up-sampling filter

- 3rd order noise shaper
- DAC including Compensations and the DEM algorithm

7.3.2 Digital filters

The interpolation from 1 fs to 128 fs is done in four stages:

- The first stage is a 99 tap Half-Band (HB) filter that increases the sample rate from 1 fs to 2 fs. It has a steep transition band to correct for the missing inherent filter function of the DAC used
- The second stage is a 31-tap FIR filter that increases the data rate from 2 fs to 8 fs. It compensates for the roll-off caused by the Sample and Hold (SH) function prior to the noise shaper
- The third stage is a simple hardware Linear Interpolator (LIN) function that increases the sample rate from 8 fs to 16 fs. It removes the 8 fs component in the output spectrum
- The fourth and last stage is a SH function increasing the sample rate from 16 fs to 128 fs.

The overall transfer characteristics can be found in Table 16.

Table 16. Digital filter characteristics

Characteristics	Condition	Value (dB)
Passband ripple	0 Fs to 0.4535 Fs	+0.02
Stop band	>0.5465 Fs	–72
Dynamic range	0 Fs to 0.4535 Fs	>143

7.3.3 Noise shaper

The 3rd-order noise shaper operates at 128 fs, shifting the in-band quantization noise to frequencies well above the audio band. This noise-shaping technique enables high signal-to-noise ratios to be achieved at low frequencies. The noise-shaper output is converted into an analog signal using a 4-bit Switched Resistor Digital-to-Analog Converter (SDAC).

7.3.4 DAC (4-bit SDAC)

The 4-bit DAC is based on a switched resistor architecture which forms a controlled voltage divider between the positive (VDACP) and the negative (VDACN) reference supplies. The 4-bit input data from the noise shaper is decoded first to a 13-level thermometer code to control the 15 taps of the converter. Data-Weighted Averaging (DWA) is added to the decoding to guarantee that there is no correlation between the input signal and the resistors used for that input signal.

After decoding and DWA the buffers connect the resistors to either the VDACP or the VDACN pin so that the reference voltage will be divided depending on the input signal. The result is an analog output voltage with a rail-to-rail maximum output swing. The output impedance of this DAC is approximately 1.0 kΩ. By applying an external capacitor of 3.3 nF to the output pin a 1st order low-pass post-filter is introduced with a –3.0 dB roll-off at 48 kHz (dimensioned for fs = 44.1 kHz). This will reduce the 3rd-order noise-shaped output spectrum of the DAC to a spectrum that increases with 2nd order.

Remark: The value of this capacitor depends on the actual sample frequency used.

7.4 Digital audio I/O

Two groups of digital inputs to the audio subsystem can be distinguished:

- Inputs (I^2S, SPDIF, I^2S from radio subsystem) that run at their own sample frequency
- Inputs (HOST I^2S) that run at a sample rate equal to that of the ADSP

At the output side only the HOST I^2S outputs are available, also running at a sample rate equal to that of the ADSP.

There are provisions to enable I^2S input 4 as a digital SPDIF input and to configure I^2S input 1 and the SPDIF inputs as a six-channel DVD input, where the SPDIF inputs carry the serial data for the four additional channels.

There is provision to enable I^2S input 4 as a digital SPDIF input, and to configure I^2S input 1 and the SPDIF inputs as a six-channel DVD input where the SPDIF inputs carry the serial data for the four additional channels.

The I^2S inputs (both primary and from the radio subsystem) and the SPDIF inputs are sample-rate converted by the SRC implemented on an EPICS7A core. The SDSP software supports three different modes:

- Stereo mode (maximum of five stereo SRCs)
- Multi-channel mode 1 (maximum of one six-channel SRC plus two stereo SRCs)
- Multi-channel mode 2 (one six-channel SRC)

The actual number of SRCs that can be active depends on the DSP clock frequency and the required sample rate. An additional stereo SRC is possible on the platform device in the ADSP and will depend on the code present in this DSP.

7.4.1 I^2S inputs

An I^2S digital interface bus can be used for communication with external digital sources. This is a serial three-line bus that has:

- One line for data
- One line for the clock
- One line for word-select

For external digital sources the SAF7741HV can act as a slave so the external source is master and supplies the clock.

Remark: The digital audio input is capable of handling multiple formats, so for simplicity the serial digital audio inputs and outputs are referred to as I^2S. However, this does not mean that the format always conforms exactly to the published Philips I^2S standard (see Ref. 5).

The I^2S input is capable of handling Philips I^2S- and LSB-justified formats of 16-bit, 18-bit, 20-bit and 24-bit word sizes. See Figure 28.

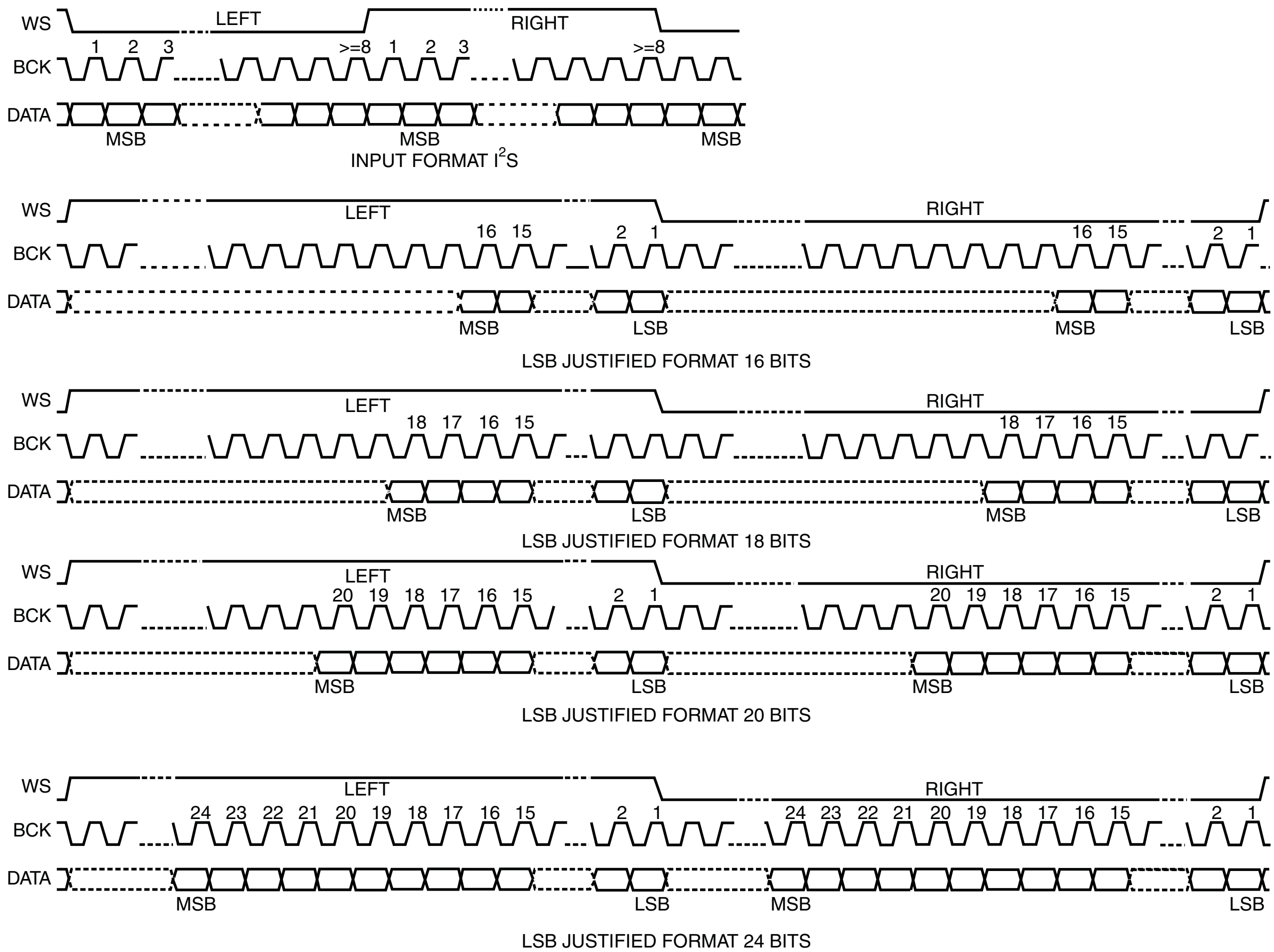


Fig 28. IIS formats

See Ref. 3 for the bits that must be programmed and for details of how to select the required I^{2}S format.

The number of BCK pulses may vary in the application. When the applied word length exceeds 24 bits the LSBs are not used. The input circuitry cannot handle an unlimited number of BCK pulses per WS period, so the maximum allowable number of BCKs per period is 256.

It is not necessary for the WS to have a 50% duty cycle in Philips I^{2}S standard format. This means that the number of BCKs during high or low may be different. However this is not allowed for LSB-justified formats.

External IIS sources with a wide sample-rate range are supported: from 8 kHz up to 192 kHz. This does not mean, however, that any sample rate can be applied to the inputs and be handled simultaneously by the sample-rate conversion DSP. The audio bandwidth after sample-rate conversion is of course always limited to half of the master sample rate Fs.

7.4.1.1 General description of the SPDIF inputs

The design fulfils the requirements of the IEC60958 Digital Audio Interface specification (see Ref. 6) except for the input voltage, which is required to have a digital level. The interface is compliant with the electrical limitations of the pins (see Table 23).

There are two SPDIF independent input pins with their own SPDIF receivers. This means that two SPDIF signals can be processed in parallel.

The SPDIF receiver is not fitted with an analog PLL. The incoming SPDIF stream is sampled at a high frequency in the digital domain. From the SPDIF signal a 3-wire (I^2S-like) serial bus is made consisting of word-select, data and bitclock lines. The Fs frequency depends solely on the accuracy of the SPDIF signal input.

This design does not handle the user data bits of the SPDIF stream. The audio field of up to 24 bits is available at its output. The audio bits are always decoded regardless of any status bits; e.g. copy-protected, professional mode or data mode. However, a subset of the channel status bits is decoded and made available to the ADSP and the SDSP. In addition, the 'validity' bit is available. This means that the ADSP can prevent non-PCM audio or data being processed as audio. See the relevant tables in Ref. 3 for the exact channel status bits supported. The supported bits are extracted from the left channel only.

SPDIF format: The SPDIF format was conceived to transport 2-channel PCM audio for distances of up to several hundred metres over a 3-wire balanced line. Alternatively the signal could be carried for shorter distances over a 2-wire pair.

The SPDIF format can be partitioned into two main layers:

- The abstract model of frames and blocks
- The channel modulation

SPDIF channel modulation: The digital signal is coded using Bi-phase Mark Coding (BMC), which is a type of phase modulation. In this scheme a logical 1 in the data corresponds to two zero crossings in the coded signal and a logical 0 to one zero crossing.

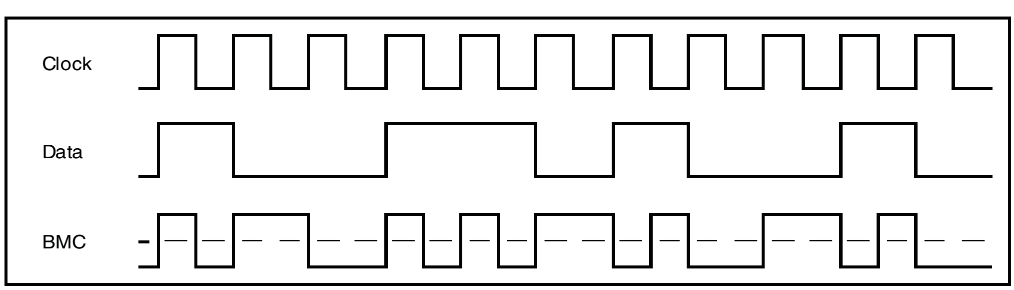


Fig 29. Bi-phase mark coding

Since a logic 1 implies two transitions in the BMC signal, a clock at twice the bit rate assumes the use of all rising signal edges.

SPDIF sample rates: The IEC60958 specification allows the use of sample rates from 22.05 kHz to 192 kHz. The SAF7741HV is designed to support a very wide range of sample rates, but there are restrictions with respect to the processing power of the SDSP and the actual contained bandwidth of the audio information. Any product derivative with a fixed SDSP ROM code will have clear restrictions. The code for the SAF7741HV platform can be chosen for different implementations.

Table 17. Examples of the most common SPDIF sample frequencies

Sample frequency (kHz)	Data rate (Mbits)	Channel rate (Mbits)
44.1	2.8224	5.6448
48.0	3.0720	6.1440
32.0	2.0480	4.0960

7.5 Host I^{2}S I/O

A HOST I^{2}S interface is available that features five inputs and four outputs. Configuration of the HOST I^{2}S interface can be done via the I^{2}C registers . Details can be found in Ref. 3.

7.6 ADSP

The ADSP processes audio features on five stereo audio channels coming from the SDSP, two stereo channels and one mono channel from the ADCs and eight stereo HOST inputs. In addition to this the ADSP can be used to sample-rate convert one additional stereo input to the same reference sample rate as all the other inputs. On the output side there are eight to 10 HOST outputs. The ADSP will control the switches in SwitchBox2 of the SDSP and SwitchBox1 in front of the ADC.

7.6.1 ADSP user flags

Eight user flags can be used to control several settings in the ADSP. The stretch mode as well as I/O direction of those flags is user-definable. Furthermore, there are two flags that are used as sample indicators for the SRC software and two flags that support an interface towards the TDSP1E in the radio subsystem (fixed input flags). Finally there is one flag that is connected to the WDOG status register. When this is used it must be configured as an output. The table below shows the function of each flag.

Table 18. ADSP user flags

Pin name	Flag	Function	Mode [1]	
			I/O	Stretch
–	F0	Internal divided sample rate flag (pflag)	IN	OFF
–	F1	Internal source sample rate flag	IN	ON
–	F2	ADSP TDSP1E interface	IN	OFF
–	F3	ADSP TDSP1E interface	IN	OFF
ADSP_IOF4	F4	User-defined input or output	IN/OUT	ON/OFF
ADSP_IOF5	F5	User-defined input or output	IN/OUT	ON/OFF
ADSP_IOF6	F6	User-defined input or output	IN/OUT	ON/OFF
ADSP_IOF7	F7	User-defined input or output	IN/OUT	ON/OFF
ADSP_IOF8	F8	User-defined input or output	IN/OUT	ON/OFF
ADSP_IOF9	F9	User-defined input or output	IN/OUT	ON/OFF

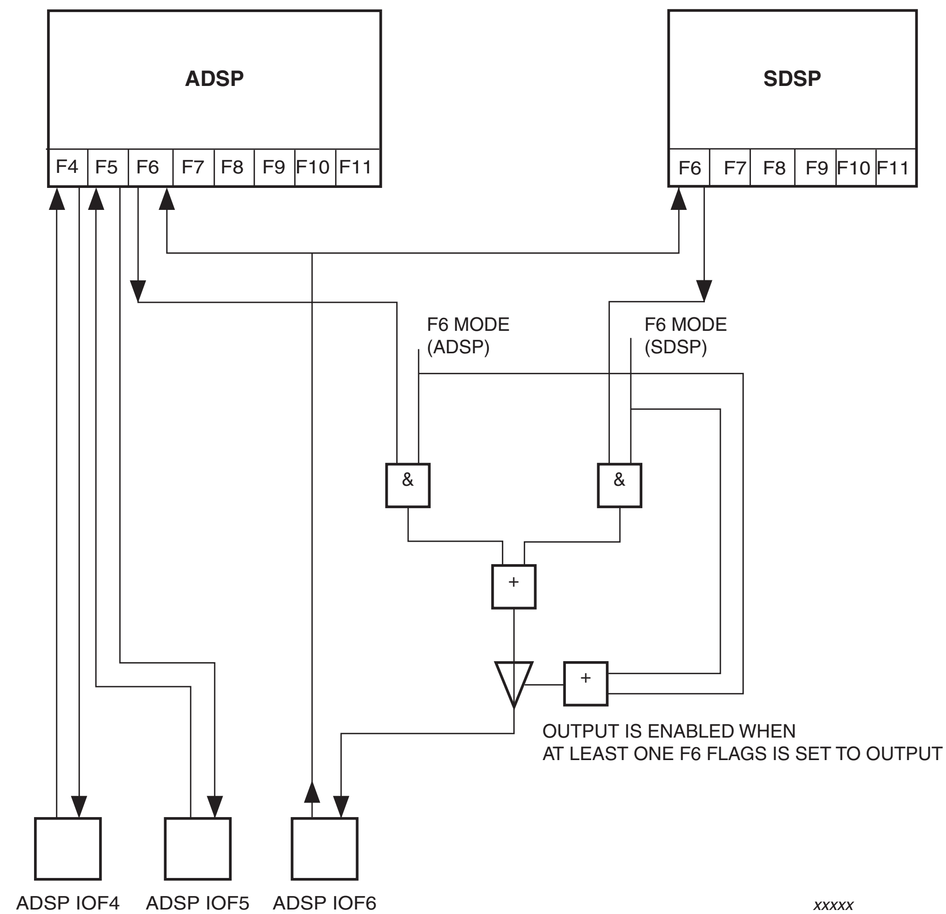
Table 18. ADSP user flags

Pin name	Flag	Function	Mode [1]	
			I/O	Stretch
ADSP_IOF10	F10	User-defined input or output	IN/OUT	ON/OFF
ADSP_IOF11	F11	User-defined input or output	IN/OUT	ON/OFF
–	F12	Output flag to the WDOG status register	IN/OUT	ON/OFF

[1] All I^2C controllable

In the description that follows, ‘n’ can be any value from 6 to11. See Figure 30 for details.

- The output flags ‘n’ of all the ADSPs or SDSPs are made to be OR-ed together, and the resulting signal is wired to ADSP_IOFn
- All flags on all the individual ADSPs and SDSPs can be set to either ‘input’ or ‘output’ in the I^2C registers. The pad of ADSP_IOFn is an input when the two ADSP/SDSP flags ‘n’ are set to input: otherwise it is used as an output.
- All flags on the two separate ADSPs or SDSPs can be set to either stretch mode or non-stretch mode in the I^2C registers
- User flags 4 and 5 of the ADSP are always connected to pads ADSP_IOF4 and ADSP_IOF5
- User flag ADSP_IOF11 is shared with the output wd_flag of the Watchdog (WDOG) module. This is configured by the IIC control register WD_CTRL ($000090). Details can be found in Ref. 3.



(1) User flag 4 and user flag 5 of the ADSP are connected always to pad ADSP_IOF4 and ADSP_IOF5 (respectively)

Fig 30. Schematic overview of the ADSP user-defined flag configuration

7.6.2 ADSP digital I/O inteface

The digital I/O interface (DIO) of the ADSP is realized via the XBUS. For the inputs a LOGIC_MUX is placed in front of the XBUS of the DSP. Mux selection is decoded from the instruction bus. For the SRC input, extra inputs are provided for the timestamp registers of the reference sample rate and the to-be-converted input. For the other inputs with the same sample rate but different arrival times, some extra buffering and scheduling of the sample valid pulse is calculated by an ASFTIM block. For each output a buffer is connected to the XBUS from the DSP and its latch-enable signal is decoded from the instruction bus as well. For an overview see Figure 31.

For further information on DIO mapping of the registers, see Ref. 4.

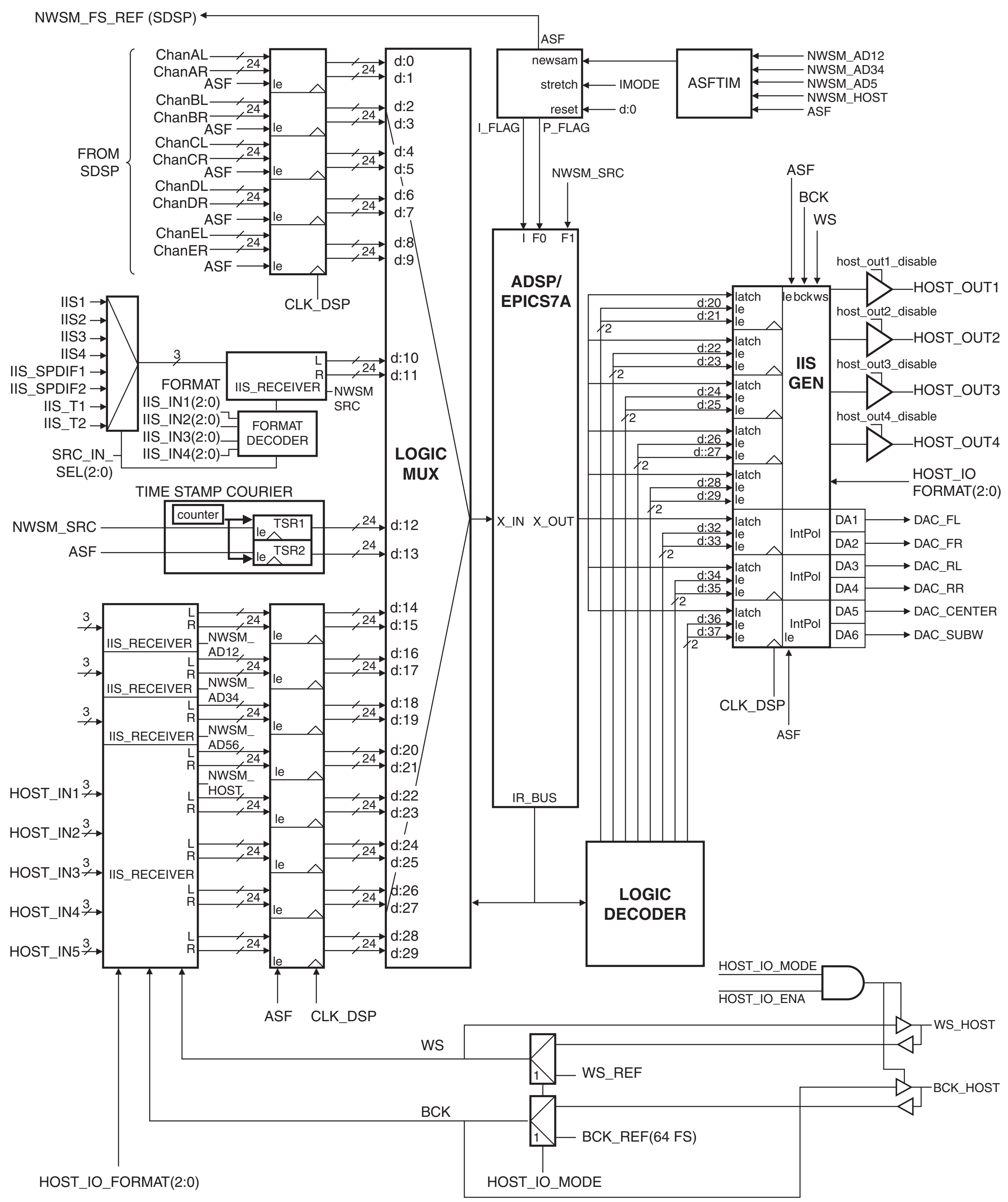


Fig 31. ADSP digital I/O interface diagram

The input format of HOST_IN, HOST_OUT and SRC INPUT can be selected via an I^2C register. The source that will be sample-rate converted is also selected by I^2C register bits (see Ref. 3). Control of these I^2C bits will be maintained by the ADSP and the MicroProcessor Interface (MPI).

Extra DIO inputs are provided for registers that contain new sample time-stamps for the stereo input and one extra register for the reference sample rate. Combined with the new sample flags from the input and the reference flags, these time-stamps allow the DSP program to convert the sample rate to the reference on the output.

7.6.3 ADSP-TDSP1E interface

The ADSP TDSP1E communication interface provides two general-purpose communication channels between the ADSP and the TDSP1E, one for each direction. Each channel has two registers of 24 bits each:

- For the channel from the ADSP to the TDSP1E, the ADSP writes the data to the registers and the TDSP1E then reads this data
- For the channel from the TDSP1E to the ADSP, the TDSP1E writes the data to the registers and the ADSP then reads this data

A full handshake mechanism is provided In addition to the communication channel, but the communication channels can be used either with or without handshaking.

When the communication between the two DSPs requires a handshake, the software can test the input flags. The flags are either cleared or set by hardware under the condition of either reading from the second register or writing to the second register. See Figure 32 for a block diagram of the communication interface.

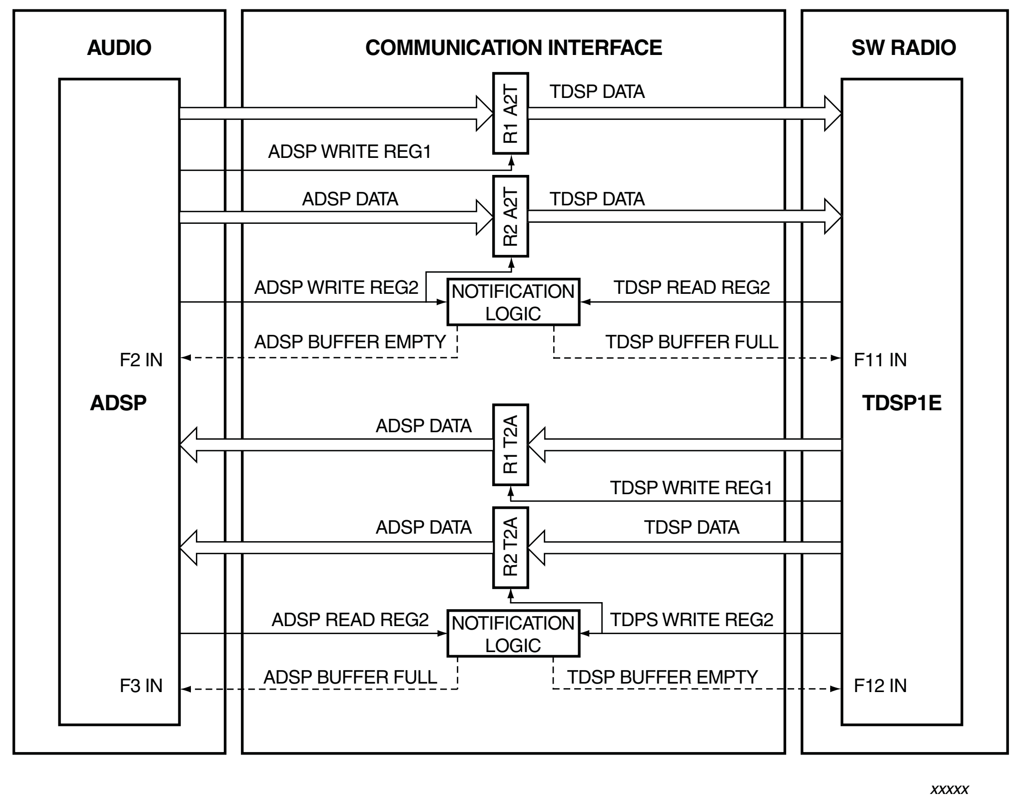


Fig 32. ADSP TDSP communication channel

7.6.3.1 Communication protocol example

Figure 33 is an example of the handshake protocol for one direction. The signal adsp_write_reg2 is equal to the ADSP DIO write signal for register R2_A2T (see Ref. 4). The signal 'tdsp_read_reg2' is equal to the TDSP1E DIO read signal for register R2_A2T. These two signals are used to generate the flags 'adsp_buffer_empty' and 'tdsp_buffer_full'.

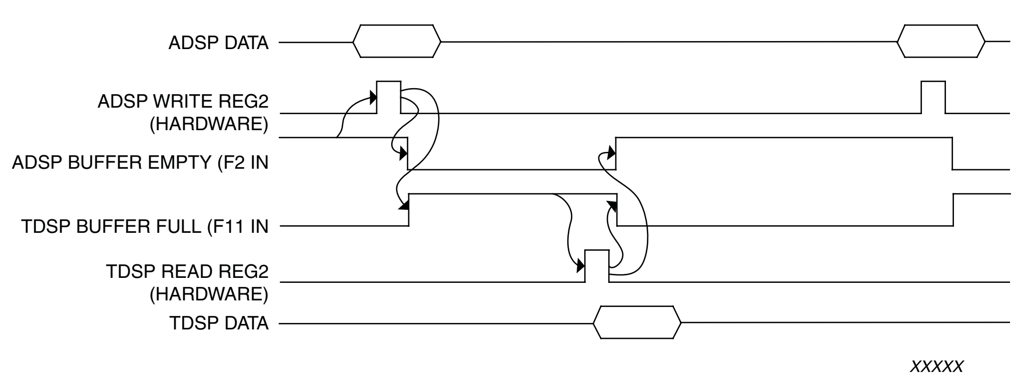


Fig 33. Handshake example: ADSP to TDSP1E

7.6.3.2 Software interface description

The flag update is the result of either a 'write R2_A2T' or a 'write R2_T2A' instruction. For this reason checking these flags at the next instruction after writing to a communication interface register should be avoided because the flags will not have been updated yet. For correct behavior there has to be at least one instruction (nop) between the write to either R2_A2T or R2_T2A and the flag check. However, in practical programming terms this should not be a restriction.

7.7 Sample-rate convertor DSP (SDSP)

7.7.1 Function

This SDSP is used solely for sample-rate conversion of five separate inputs to one master output sample rate. The hardware supports five stereo inputs and outputs, the possible input and output sample-rate combinations depending on the DSP clock frequency.

The digital inputs are grouped into four independent I^{2}S inputs, two SPDIF digital inputs and two I^{2}S-like inputs from the TDSPs. All of these are stereo channels. Of these inputs, five can be routed through the SDSP and one can be selected directly as input for the ADSP. This means that six digital channels can be processed at the same time by the ADSP where the sixth direct input on the ADSP needs to be sample-rate converted in the ADSP. When a six-channel - i.e. three I^{2}S channels - DVD source needs to be processed, I^{2}S input 1, SPDIF1D_DVD34 and SPDIF2D_56 are used to cover all three stereo channels.

7.7.2 Flags

Six user flags are available for the software running in the SDSP, the stretch mode as well as the I/O direction of these flags being user-definable. A further six ‘newsam’ flags are used as sample indicators for the SRC software. These flags have stretch mode pre-set and are hard-wire coded, and therefore cannot be changed; only disabled or enabled using the corresponding I^{2}C control bits. The function of each SDSP user flag is shown in Table 19.

Table 19. SDSP user flag function

Chip pin name	Flag	Function	Mode	
			I/O	Stretch
-	F0	Reference sample rate flag	IN	ON
-	F1	Source 1 sample rate flag	IN	ON
-	F2	Source 2 sample rate flag	IN	ON
-	F3	Source 3 sample rate flag	IN	ON
-	F4	Source 4 sample rate flag	IN	ON
-	F5	Source 5 sample rate flag	IN	ON
ADSP_IOF6	F6	User-defined input or output	IN/OUT [1]	ON/OFF [1]
ASDP_IOF7	F7	User-defined input or output	IN/OUT [1]	ON/OFF [1]
ADSP_IOF8	F8	User-defined input or output	IN/OUT [1]	ON/OFF [1]
ADSP_IOF9	F9	User-defined input or output	IN/OUT [1]	ON/OFF [1]

Table 19. SDSP user flag function

Chip pin name	Flag	Function	Mode	
			I/O	Stretch
ADSP_IOF10	F10	User-defined input or output	IN/OUT [1]	ON/OFF [1]
ADSP_IOF11	F11	User-defined input or output	IN/OUT [1]	ON/OFF [1]
-	F12	Out flag to the WDOG status register	IN/OUT [1]	ON/OFF [1]

[1] I^2C-controllable

7.7.3 DIO of the SDSP

For each stereo input one out of eight available stereo sources can be selected via a switchbox. The input format of each stereo DIO input can then be selected via an I^2C register. For the location of these bits see Ref. 3.

The I^2C bits are controlled by the ADSP and the MPI. DIO inputs are also available for the registers that contain new sample timestamps of the five individual stereo inputs, and there is one extra register for the reference sample rate. Combined with the new-sample flags of the inputs and the reference flags, these timestamps allow the DSP program to convert the five sample rates to the reference on the output (see Figure 34).

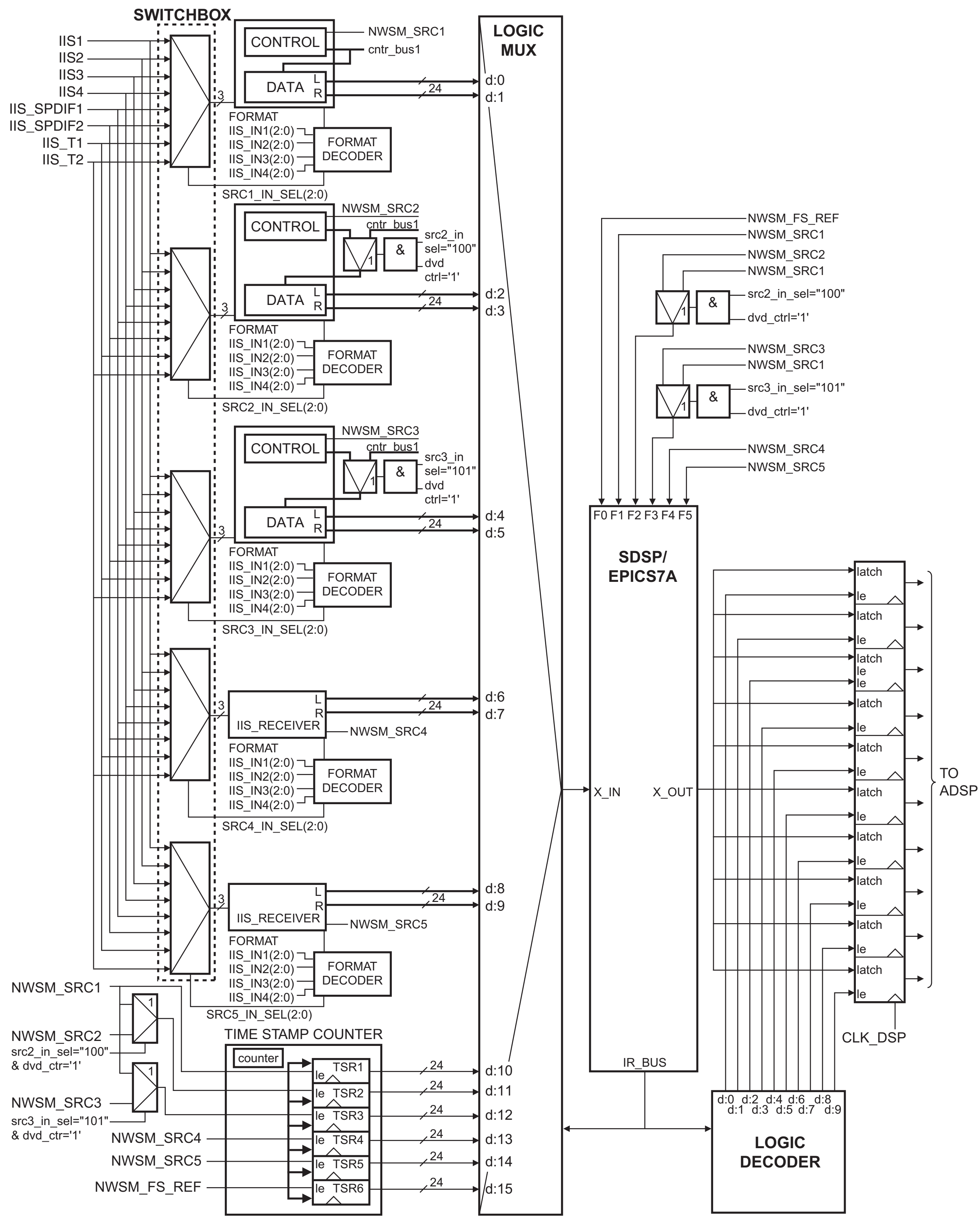


Fig 34. Digital inputs/outputs of the SDSP

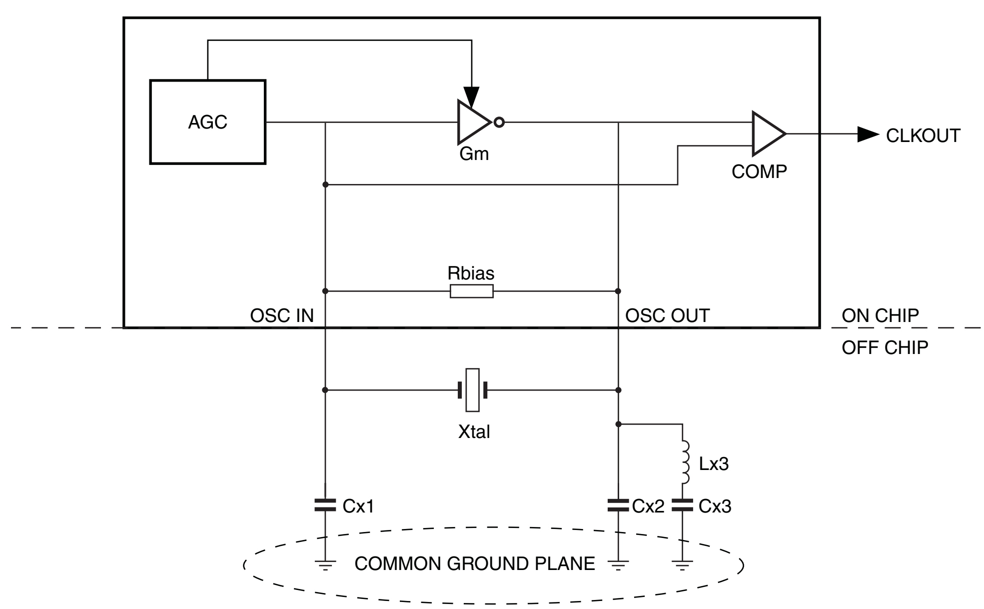
7.8 Common system descriptions

This section provides descriptions of certain functions and blocks that are not exclusively related to either the radio or the audio part of the SAF7741HV.

7.8.1 Oscillator

The SAF7741HV has a low-power Pierce oscillator with amplitude control and an inverter for the gain stage. The inverter biasing together with capacitive input coupling gives the gain stage Class C operation. When the circuit is oscillating there are sine waves at the input (osc_in) and at the output (osc_out) with V_{pp} close to the 1.8 V oscillator supply V_{dd}. The sine wave at the input and the output is converted by a low-jitter comparator into a CMOS-compatible clock.

The oscillator block diagram is shown in Figure 35. The crystal should be connected to the PCB as close as possible to the oscillator input and output pins of the chip. Care must also be taken to make sure that the load capacitors Cx1 and Cx2 and OSC_REF_N have a common ground plain. Loops must be made as small as possible in order to minimize noise coupling to the crystal nodes, and in addition parasitics should be kept as small as possible.



Lx3 and Cx3 should be connected only in combination with 3rd overtone crystals

Fig 35. Oscillator block diagram

Lx3 and Cx3 have to be added when the crystal is used at the third overtone frequency. Table 20 gives specifications for fundamental and third-overtone frequency crystals. C_L is the typical load capacitance of the crystal and is usually specified by the manufacturer. The actual C_L influences the oscillation frequency. Using a crystal manufactured for a different load capacitance will cause the circuit to oscillate at a slightly different frequency (dependent on the quality of the crystal) from the specified one. Therefore, to obtain an accurate time reference, it is advisable to use the load capacitors specified in Table 20. In addition to start-up problems, the use of values other than those quoted can lead to performance degradation due to an unstable clock reference.

Table 20. Crystal parameters and external components

Name	Value	
	Third overtone	Fundamental
Maximum parallel capacitance (C_p)	7 pF	7 pF
Load capacitance (C_l)	10 pF	10 pF
Series resistance (R_s)	<60 Ω	<60 Ω
C_{x1}	≥12 pF	≥8 pF
C_{x2}	≥12 pF	≥8 pF
C_{x3}	10 nF	-
L_{x3}	2.2 μH	-

7.8.2 Voltage regulator

A voltage regulator controls all the 1.8 V supplies of the chip, with input from the 3.3 V supply. An external PMOS power transistor is used to handle power. The regulated 1.8 V supply is derived from a band-gap voltage AC-decoupled by an external capacitor so that a very accurate output voltage is obtained.

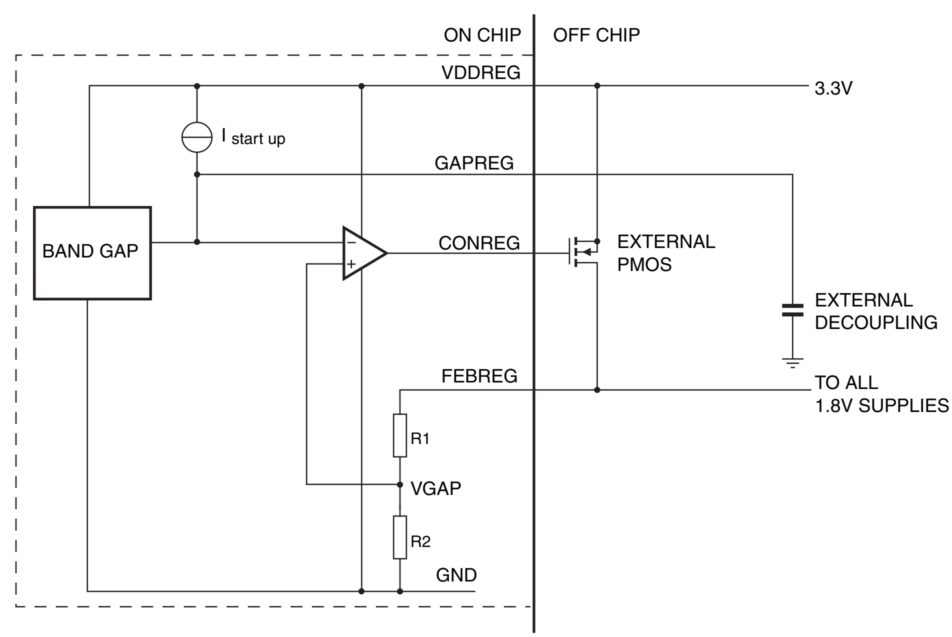


Fig 36. Voltage regulator block diagram

To speed up the settling time of the regulated supply voltage the external capacitor is charged with a larger current during start-up. When the voltage across the capacitor is close to the internal reference voltage this current is then switched off. A build in hysteresis makes sure that this current stays switched off during normal operation.

7.8.2.1 Power dissipation of the external transistor

Under worst-case conditions the total power dissipation of the external PMOS transistor is about the same as the power consumption of all the 1.8 V supplies. The application diagram in Section 9 shows the voltage regulator application with the recommended PHK04P02T power transistor.

7.8.3 Clocking strategy

The overall clocking diagram is shown in Figure 37. The main clock source of the generated clock frequencies is the crystal oscillator running at 41.6 MHz. This generates the reference frequency for the:

- IFADC
- PDC
- DSP_PLL
- Audio PLL

The Audio PLL can also use either the FS_SYS pin or the WS_HOST pin as reference when the SAF7741HV is in slave mode.

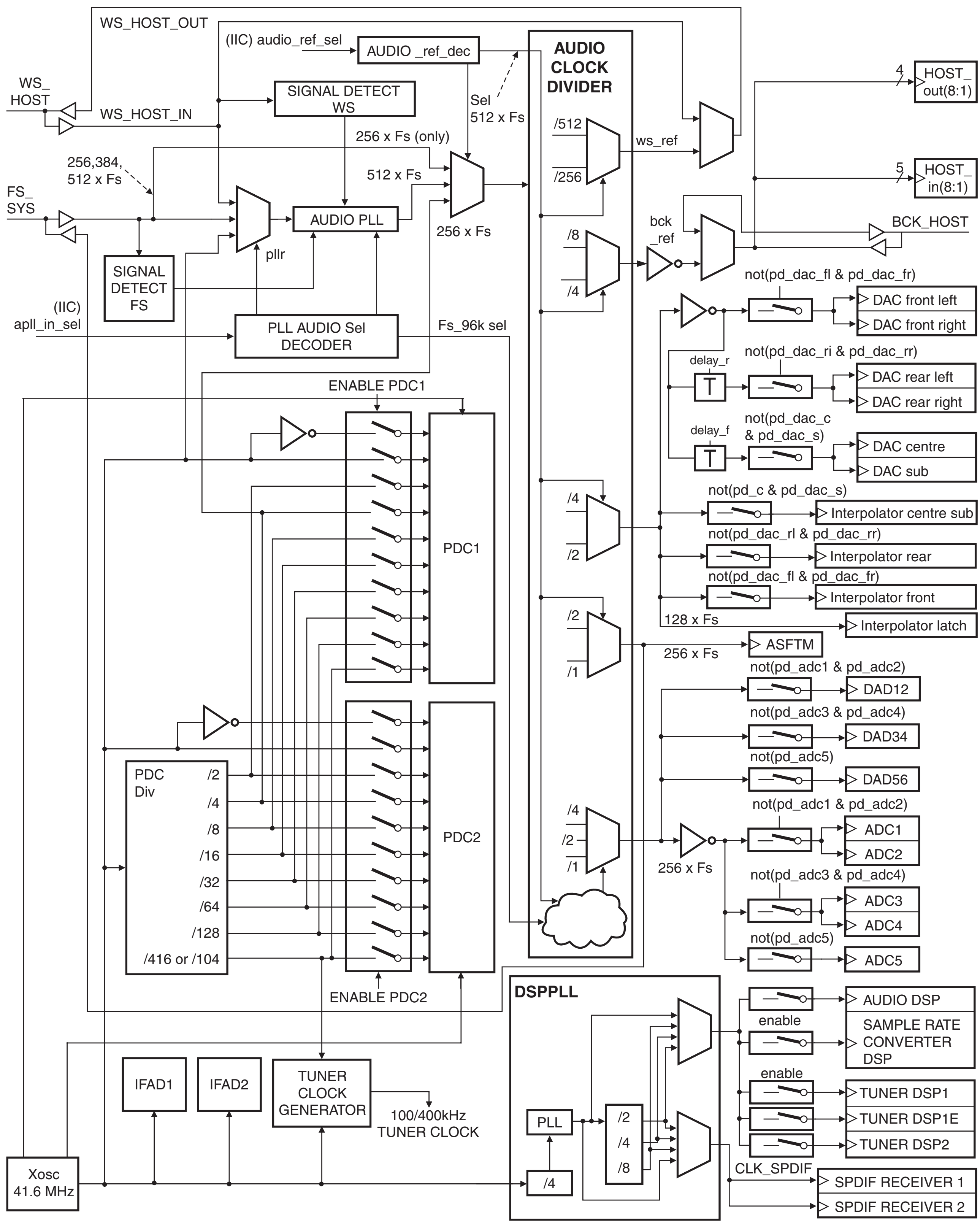


Fig 37. Clock strategy overview

Generation of the DSP and other clocks

The SAF7741HV has two PLL circuits: one (DSP PLL) to generate the system clock for the DSPs and SPDIF receiver; the other (audio PLL) to generate the audio reference clocks. The crystal oscillator (radio rate), FS_SYS (external rate) or WS_HOST (audio rate) can be used as an input for the generation of the audio clocks. For the full setting ranges of the two PLLs see Ref. 3.

The DSP PLL is used to generate the clock to the DSPs and the SPDIF block.

The clock frequency of the SPDIF block should be chosen so that its relation to the sample rate of the incoming SPDIF Fs is 660 × Fs < SPDIF CLOCK < 2480 × Fs.

For reasons of power reduction the clock to major blocks can be stopped separately. Exact bit definitions can be found in the CLK_EN register ($000050) and APD_CTRL1 register ($000040) of Ref. 3.

Audio clock generation is constructed in such a way that the ADSP can simultaneously process audio samples of 48 kHz and 96 kHz (i.e. double the sample rate frequency). These samples can be provided to the ADSP via the host inputs and received from the ADSP via the host outputs. For each host input or output a selection can be made between Fs or ½ × Fs. Exact bit definitions can be found in Ref. 3.

When the SAF7741HV is in master mode the audio PLL is used to generate Fs from the crystal oscillator frequency of 41.6 MHz. Fs can be 44.1 kHz, 48 kHz or 96 kHz. When the SAF7741HV is in the slave mode the AUDIO_PLL can lock onto either WS_HOST or FS_SYS. If WS_HOST is used as an input its frequency can be 44.1 kHz, 48 kHz or 96 kHz. If FS_SYS pin is selected as the direct source for the internal audio clocks the maximum sample rate is limited to 48 kHz.

For the PDC blocks (PDC1 and PDC2) the clocks are derived digitally from the crystal oscillator frequency. The communication clock between SAF7741HV and the tuner IC can be either 100 kHz or 400 kHz. To reduce noise this tuner clock signal is sent to the tuner IC via a complementary current source. Frequency selection depends on the type of tuner connected to the SAF7741HV.

7.8.4 DSP PLL description

The oscillator frequency of 41.6 MHz is first divided by four, then fed to the DSP PLL. The DSP PLL output can be further divided by two, four or eight (depending on the I^2C settings) before being fed as the clock frequency to the DSP cores and the SPDIF block. A partial overview of the available frequencies is given in Table 21. The DSP PLL frequency is controlled via I^2C registers.

The output frequency of DSP PLL can be calculated with the formula:

$$F_{out} = 65 \times 10^4 \times (212 + MSEL) / 2^{(3 - \mathrm{DSP\_SEL})} \mathrm{Hz} \quad (1)$$

Where:

- MSEL = the decimal value of the dsp_pll_msel bits of the I^2C CLKPLL_CTR register
- DSP_SEL = the decimal value of the dsp_sel bits of the I^2C CLKPLL_CTR register

The default output frequency of the DSP PLL is 130 MHz.

Figure 38 shows a simplified block diagram of the DSP PLL and the generation of the DSP and SPDIF clocks.

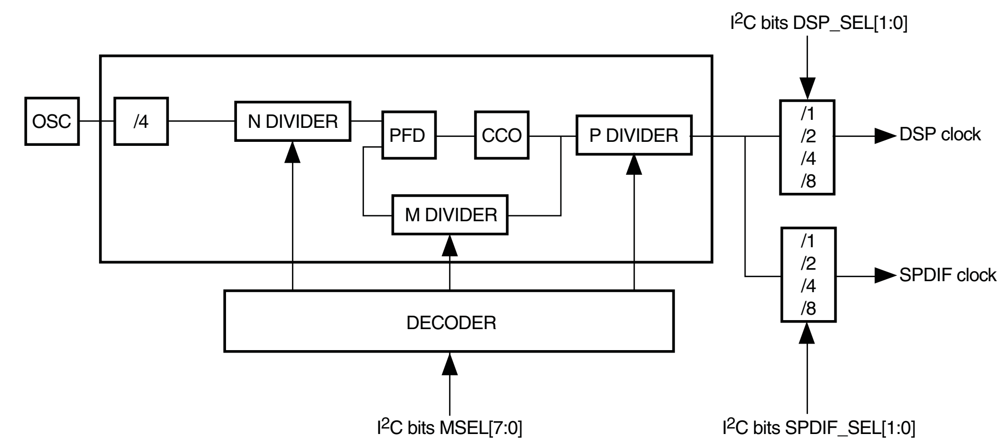


Fig 38. DSP PLL Diagram

Table 21. Example of DSP PLL setting

M-divider ratio	MSEL[7:0]	Clock frequency (MHz)			
		SPDIF_SEL=00	SPDIF_SEL=01	SPDIF_SEL=10	SPDIF_SEL=11
		DSP_SEL=00	DSP_SEL=01	DSP_SEL=10	DSP_SEL=11
		= M-divider ratio × 81.25 kHz	= M-divider ratio × 162.50 kHz	= M-divider ratio × 325.00 kHz	= M-divider ratio × 650.00 kHz
212	0(0x00)	17.225	34.450	68.900	137.800
213	1(0x02)	17.306	34.612	69.225	138.450
214	2(0x03)	17.387	34.775	69.550	139.100
390	178(0xB2)	31.687	63.375	126.750	253.500
400	188(0xBC)	32.50	65.00	130.00	260.00
420	208(0xD0)	34.125	68.250	136.500	273.000
421	209(0xD1)	34.206	68.412	136.825	273.650
422	210(0xD2)	34.287	68.575	137.150	274.300

7.8.5 Audio PLL details

The audio PLL block is responsible for the generation of 512 × Fs where Fs is the master sampling frequency. The audio PLL has three different inputs:

- Crystal oscillator input at 41.6 MHz. The audio PLL is preset automatically to the targeted frequencies of 512 × Fs for Fs = 44.1 kHz, Fs = 48 kHz and Fs = 96 kHz
- WS_HOST input. This is used to generate the 512 × Fs output frequencies for the following input sampling frequencies: Fs = 44.1 kHz, Fs = 48 kHz and Fs = 96 kHz
- FS_SYS input. This is used to generate the 512 × Fs output frequencies for the following input frequencies: 256 × Fs, 384 × Fs and 512 × Fs where Fs can be either 44.1 kHz or 48 kHz

To prevent the system from locking up when the WS_HOST or FS_SYS input drops out, the audio PLL switches automatically to the crystal oscillator input for generating the appropriate frequency. For example, if the WS_HOST input for Fs = 48 kHz drops out the audio PLL selects the crystal oscillator as input and generates the 512 × Fs output frequency with Fs = 48 kHz.

Table 22 lists all the targeted output frequencies. The first column in the table gives the three possible inputs of the audio PLL while the second column lists the corresponding input frequencies. The third column shows the targeted sampling frequencies that are used to derive the output frequency of the PLL as shown in the last column of the table, i.e. 512 × Fs.

Table 22. List of frequencies generated by audio PLL

Input signal	Input signal frequency	Targeted Fs (kHz)	Targeted output frequency = 512 × Fs
Osc: Oscillator (41.6 Mhz)	41.6 MHz	44.1	22.583 MHz
	41.6 MHz	48	24.576 MHz
	41.6 MHz	96	49.152 MHz
WS_HOST	44.1 kHz	44.1	22.579 MHz
	48 kHz	48	24.576 MHz
	96 kHz	96	49.152 MHz
FS_SYS	256 × Fs	44.1	22.579 MHz
	384 × Fs	44.1	22.579 MHz
	512 × Fs	44.1	22.579 MHz
	256 × Fs	48	24.576 MHz
	384 × Fs	48	24.576 MHz
	512 × Fs	48	24.576 MHz

Remark: When the audio PLL is set to lock onto either WS_HOST or FS_SYS the actual frequency of the input signal is allowed to deviate by up to 20% from the target Fs. However, optimum audio performance of the SAF7741HV is guaranteed only at 44.1 kHz and 48 kHz.

7.8.6 Tuner clock generation circuit

To decrease total system cost, the crystal oscillator of SAF7741HV can also be used as reference clock for the tuner so that the external components of the the tuner's own crystal oscillator can be omitted. The technical advantage here is that the tuner and SAF7741HV clock frequencies are coupled, which prevents performance deterioration as a result of mismatched frequency domains.

The tuner clock generation circuit uses a differential output current to provide a 100 kHz/400 kHz reference clock. The reference frequency is derived from the crystal oscillator. To get rid of the disturbances introduced by the digital dividers, the clock for the current drivers is synchronized by the clean crystal oscillator clock. The differential output current ensures that the interface between the tuner and SAF7741HV will not interfere with the application. The output current depends on the number of connected tuners and needs to be controlled by I^{2}C. See Figure 39 for the dual tuner application.

For the TEF6730 the reference clock frequency can be set to 100 kHz.

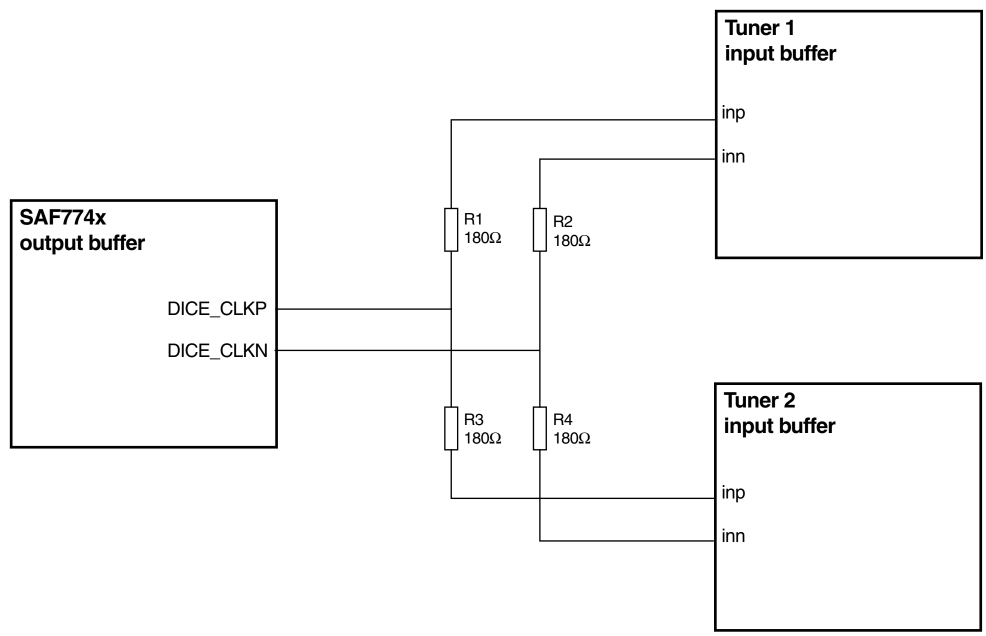


Fig 39. Dual tuner mode SAF7741HV

7.8.7 RESET sequence

The reset sequence is initiated by the RESETN pin going low, and will finish approximately 1.0 ms after the pin goes high again.

For a correct reset sequence initialization, the oscillator must be running and the oscillation must be stable. For small-pulse immunity the RESETN pin must be low during at least forty oscillator clock periods for a valid reset.

The total time between the RESETN pin going high and the reset sequence finishing is called the reset time, or tRESET, and is determined by the locking time of the PLLs. Once both PLLs are in lock the internal reset will stay active for another 2047 oscillator clock periods before the reset sequence completes. A reset will cause the chip to go into the initialization state.

When there is a reset the following actions are performed:

- All the bits of the I^{2}C registers are set to their default values
- The DSP’s program counter is reset to zero and kept there until the microprocessor writes the correct values to the DSP_CTR register ($000010)
- The DSP’s status registers are reset
- All DSP I/O flags are set to their default modes
- The IF processor block is reset
- The RDS decoder is reset
- The RS and I^{2}C interfaces are reset
- The WDOG is reset

The RESETN pin is active low and has an internal pull-up function.

7.8.8 I²C interface

The I²C bus is for two-way, two-line-plus-ground communication between different ICs or modules. The two lines are the Serial Data Line (SDA) and the Serial Clock Line (SCL). The I²C interface allows access to:

- Radio settings
- PLL settings
- AD volume control
- DSP settings
- All DSP registers and memories

The chip acts as an I²C slave, so the SCL clock is input only while the SDA is a bi-directional line. Both standard-mode I²C (up to 100 kHz) and fast-mode I²C (up to 400 kHz) are supported.

7.8.8.1 I²C switch

The I²C switch enables communication with a secondary I²C bus connecting modules that are sensitive to digital noise. The switch is bi-directional and is controlled by the I²C block of the SAF7741HV. It has been designed specifically for an IF front-end chip for FM/AM reception that works with low voltages delivered by the antenna, and which is therefore easily disturbed by digital switching.

7.8.9 Watchdog (WDOG)

A Watchdog (WDOG) function has been added to each DSP to detect and signal operating faults. This feature increases the overall robustness of the system, but it cannot detect all DSP-related problems. The basic principle is that an instruction (mvi #FFFFFF, rmy0;) that will certainly not occur elsewhere is added to the DSP program. This instruction is inserted into the main software loop and will therefore be executed at regular intervals. To detect whether or not a DSP is running correctly an external circuit will check that the watchdog instruction has executed within a certain time slot. This slot is I2C-programmable to a maximum of 12.6 ms, and is therefore more than sufficient to accomodate the longest software loop.

The watchdog is disabled when the clock of a particular DSP is stopped or when a DSP is in reset.

The watchdog function offers a neat way of interrupting the external microcontroller. The function can also be used to allow the DSPs to interrupt the microcontroller under software control by means of output flag F12.

The interrupt output pad ADSP_IOF11 is connected to the WDOG logic and is combined with the ADSP I/O flag F11.

8. I²C memory map and bit definitions

The separate I²C Memory Map and Bit Definitions (Ref. 3) contains all the defined I²C bits and provides access to the memories of all the DSPs and the various registers throughout the whole system. It also provides access to the secondary I²C bus for communicating with the tuner.

To prevent EMC problems at the high-sensitivity tuner, normal I^2C transmissions are not applied to the I^2C bus that is connected to the tuner. Instead the SAF7741HV has a built-in I^2C switch that becomes active the moment the so-called ‘secondary I^2C bus switch’ address is written to, and which de-activates again the moment an I^2C stop code is detected.

9. Application diagrams

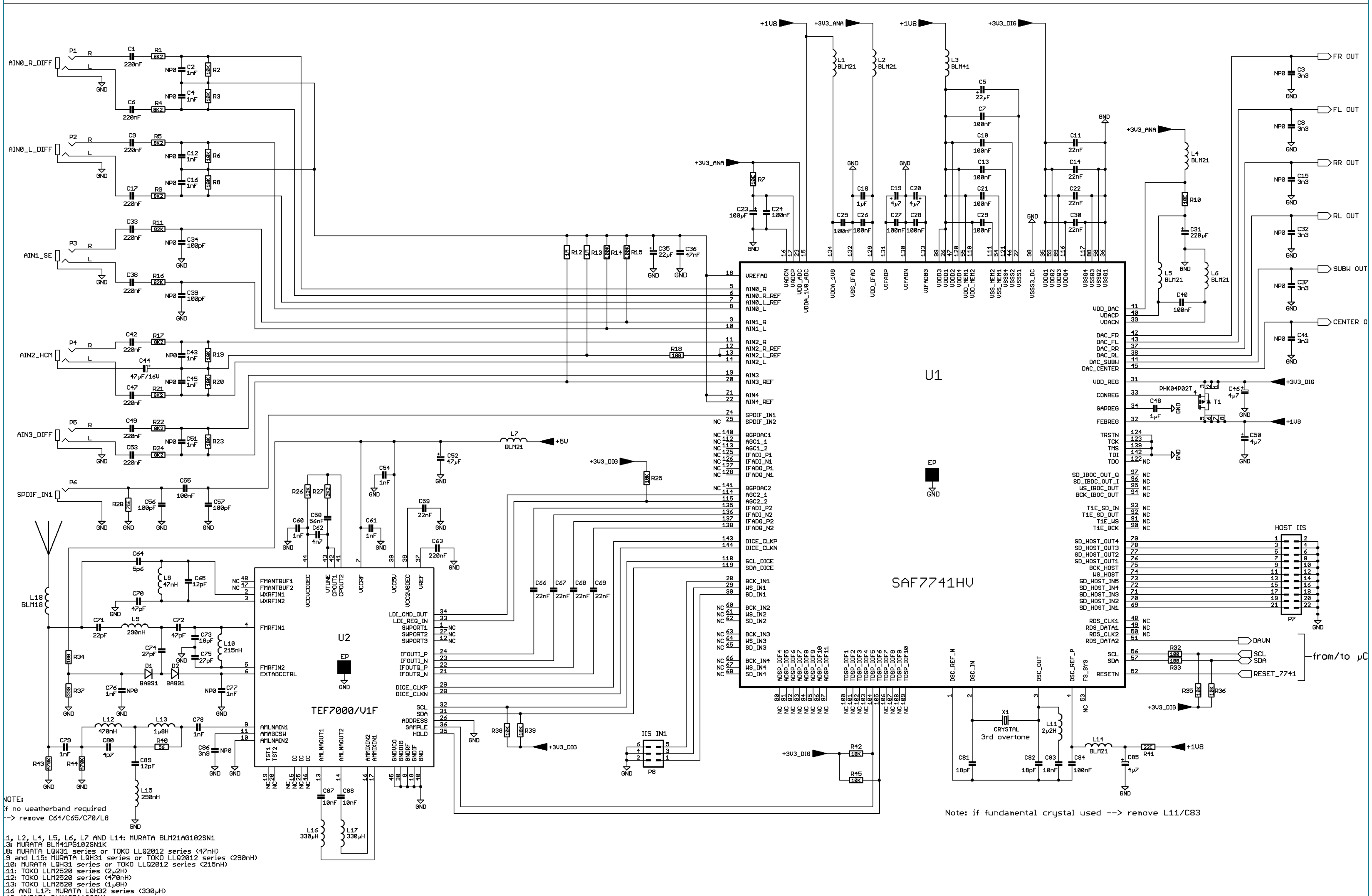


Fig 40. Single-tuner SAF7741 and TEF7000 application diagram

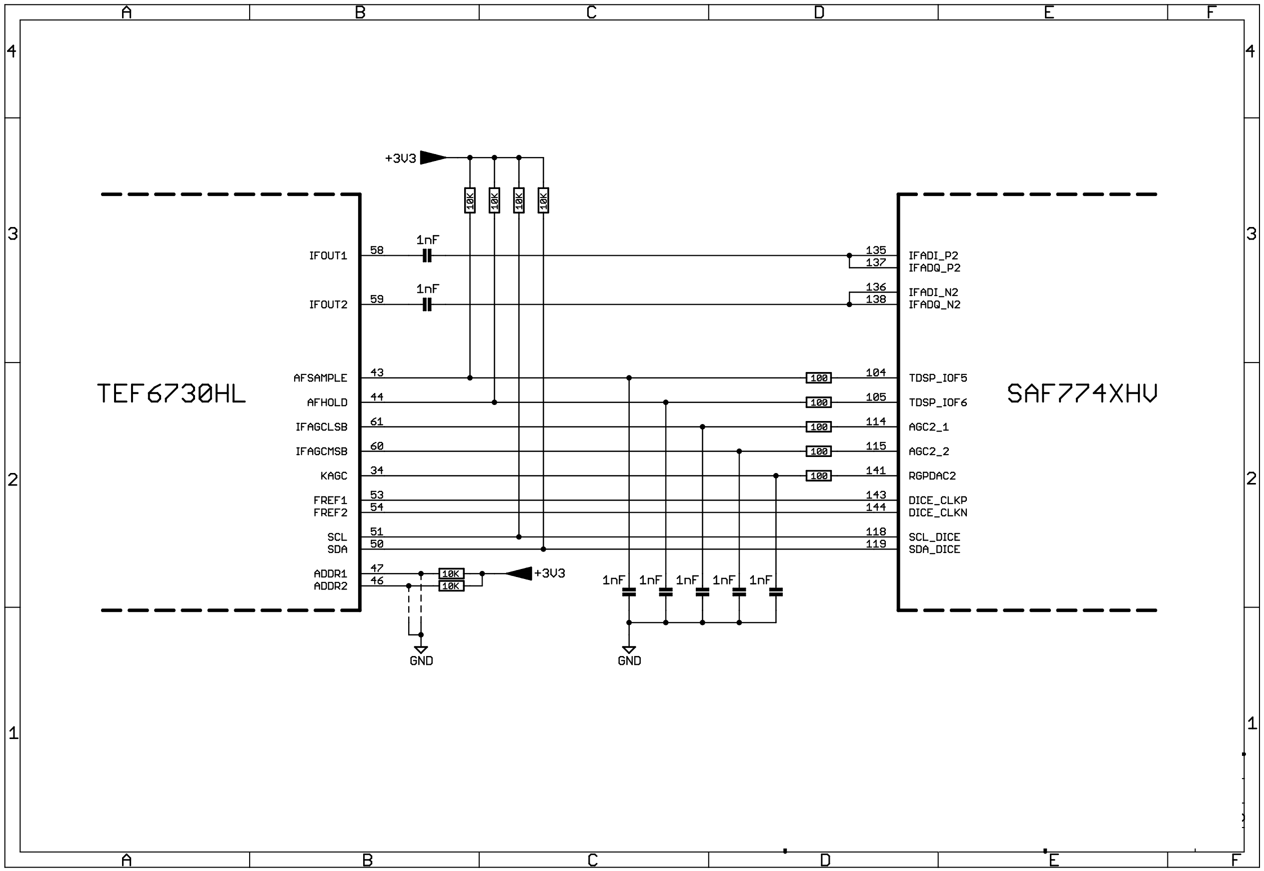


Fig 41. SAF774x and TEF6730 connections

10. Limiting values

10.1 Electrical limiting values

Table 23. Electrical limiting values (in accordance with the Absolute Maximum Continuous Ratings system IEC134)

Symbol	Parameter	Conditions	Min	Max	Unit
VDDD	Supply voltage, internal rail		–0.5	+2.5	V
VDDQ	Supply voltage, external rail		–0.5	+4.6	V
V_i	DC input voltage	All inputs, except for IFAD inputs	–0.5	(VDDQ + 2.5) or 5.5	V
V_{i_ifad}	DC input voltage pins IFAD	IFAD pins only	–0.5	VDDQ	V
I_{sup}	DC supply current per supply pin		-	100	mA
I_{gnd}	DC ground current per ground pin		-	100	mA
T_{amb}	Ambient operating temperature		–40	+85	C
T_{stg}	Storage temperature		–40	+125	C
ESDS	ESD sensitivity				
	Human body model pass voltage level	AEC - Q100-002 - REV-D	2000	-	V
	Charged device model pass voltage level	AEC - Q100-011 - REV-B	C4	-	Class
LU	Latch Up I-O trigger current	JESD78A	-	100	mA
	Latch Up VDD trigger voltage	JESD78A	-	$1.5 \times VDD_{max}$	V
P_{tot}	Total power dissipation		-	1600	mW

11. Recommended operating conditions

Table 24. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDD	Supply voltage, internal rail		1.73	1.8	1.95	V
VDDQ	Supply voltage, external rail		3.0	3.3	3.6	V
T_{amb}	Ambient temperature		–40	-	+85	C

12. Thermal characteristics

Table 25. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient	Jedec 2S2P board with EPAD connection	24	K/W

12.1 Thermal considerations in choosing a package

According to the worst-case simulations of the chip speed, the maximum allowable junction temperature is 125 °C. Reducing the thermal resistance of the system is therefore required, and a relatively effective way of doing this is to design an HLQFP144 with an exposed die-pad. The metal of the die-pad is exposed at the bottom of the package and must be soldered onto a thermal land pattern. The exposed die-pad is used as extra ground pin in connection with the Kelvin capacitors (see Hardware description manual for details). The exposed dip-pad is connected with two types of copper plated PCB vias to a ground plane (see Figure 47). Soldering the die-pad onto the land pattern ensures that there is good thermal conductivity between the chip and the PCB, but there is little improvement to the thermal conductivity overall because power dissipation largely depends upon:

- The heat-radiating area
- The exposure of this area to the environment
- The thermal conductivity of heat-radiating/convecting material

That is why the thermal land pattern must be connected to a large ground plane by a number of vias that act as heat pipes. It is best to place the vias directly under the exposed die-pad as they are only 12 mil to 13 mil wide at a 1.2 mm pitch. These vias are exposed to the solder between the die-pad and the thermal land pattern. Making these vias only 12 mil to 13 mil wide will prevent solder wicking through the holes during reflow.

The solder mask is not one large mask with the same size as the exposed die-pad, but is sub-divided into 1.0 mm $\times$ 1.0 mm large squares at a pitch of 1.2 mm. However, making vias of only 12 mil to 13 mil is expensive and here it is proposed to have the vias outside the solder area. These vias can be larger than 12 mil to 13 mil because these are not on a solder mask and are depicted here as 25 mil vias.

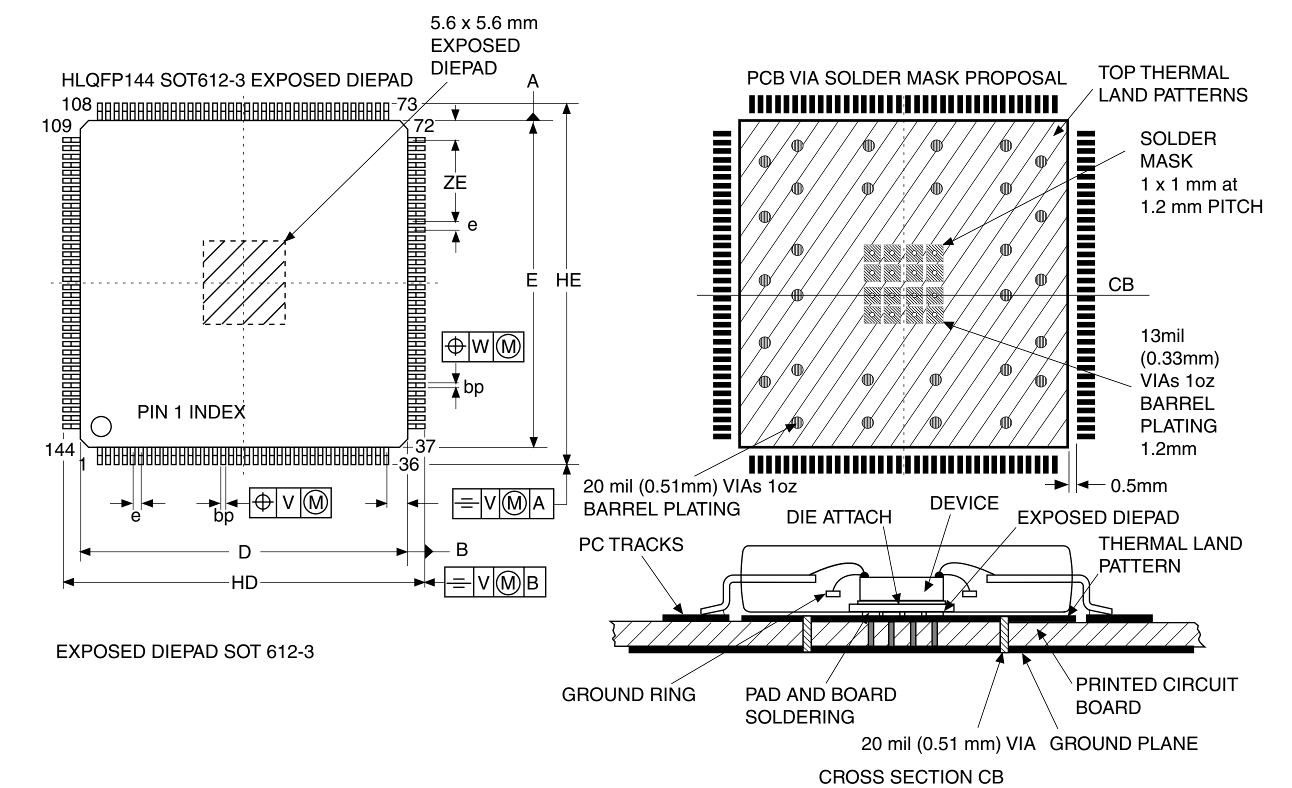
Thermally speaking, this is not the best solution but results in an acceptable thermal resistance. Taking the above mentioned considerations into account, it can be stated that the $R_{thj\text{-}a}$ (thermal conductivity junction-to-ambient) of this package mounted on a particular PCB (with a specific ground plane area and plating thickness) will be known only after measuring the $R_{thj\text{-}a}$. The quality of the soldering of the die-pad to the land pattern, determines largely the $R_{thj\text{-}a}$, and some testing by the set maker needs to be done to be sure that in the production process automotive quality is guaranteed.

The following determine the total $R_{thj\text{-}a}$ of this set-up:

- The thickness of the PCB (equal to the length of the plugged VIAs)
- The PCB material
- The number of conductive layers in the PCB
- The number of layers used to connect to the thermal VIAs
- The thickness of the copper plating
- The copper area exposed to the outside world

Normally, 70% of the IC power is dissipated via the PCB. This could increase to 90% by using the exposed soldered die-pad solution.

12.2 Thermal considerations in choosing a package for the SAF7741HV production chip



The package dimensions are indicated in Figure 47.

Fig 42. Thermal considerations for package choice

13. Static characteristics

13.1 Supply currents

Table 26. Current for each supply pin or pin group

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IP_DIG	DC supply current of the digital core, pins $VDDD_x$. Supply voltage 1.8 V (typical), 1.95 V (max)	High activity of the DSPs at 135.2 MHz DSP frequency	-	220	290	mA
IP_MEM	DC supply current of the memories, pins VDD_MEM_x. Supply voltage 1.8 V (typical), 1.95 V (max)	High activity of the DSPs at 135.2 MHz DSP frequency	-	100	120	mA
IP_IO	DC supply current of the periphery, pins $VDDQ_x$. Supply voltage 3.3 V (typical), 3.6 V (max)	Without an external load to ground	-	2.5	8.0	mA
IP_ANA18	Supply current of the analog 1.8 V of IFADC, pin VDDA_1V8. Supply voltage 1.8 V (typical), 1.95 V (max)		-	1.6	4.0	mA
IP_ADC18	Supply current of the analog 1.8 V of audio ADC, pin VDDA_1V8_ADC. Supply voltage 1.8 V (typical), 1.95 V (max)		-	15	19	mA

Table 26. Current for each supply pin or pin group *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IP_AD	Supply current of the audio ADCs and SPDIF bitslicer, pin VDD_ADC. Supply voltage 3.3 V (typical) 3.6 V (max)	At zero input signal and zero output signal	-	18	23	mA
IP_VADCP	Supply current of the audio ADCs and RGP DAC, pin VADCP. Supply voltage 3.3 V (typical), 3.6 V (max)		-	0.5	0.7	mA
IP_IFADC	Supply current of the IFADCs and RGP DAC, pin VDD_IFADC. Supply voltage 3.3 V (typical), 3.6 V (max)		-	27	35	mA
IP_VDDDAC	Supply current of the DAC, pin VDD_DAC. Supply voltage 3.3 V (typical)	At zero input and output signal	-	0.7	1.2	mA
IP_VDACP	Supply current of the DAC, pin VDACP. Supply voltage 3.3 V (typical), 3.6 V (max)	At zero input and output signal	-	5.6	7.3	mA
IP_XTAL	Supply current XTAL oscillator, tuner clock generator and PLLs, pin OSC_REF. Supply voltage 1.8 V (typical), 1.95 V (max)	OSC functional mode at 41.6 MHz and a C_{load} = 10 pF. PLLs at default settings.	-	3.2	4.1	mA
IP_REG	Supply current regulator, pin VDD_REG. Supply voltage 3.3 V (typical), 3.6 V (max)	Functional mode	-	0.4	0.52	mA
P_{tot}	Total power dissipation	High activity of the DSPs at 135.2 MHz	-	800	1125	mW

13.2 DC characteristics

Table 27. DC characteristics digital I/O (at T_{amb} = –40°C to +85 °C, V_{DDQ} = 3.3 V unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDD	Operating supply voltage 1.8 V analog and digital	All VDD pins with respect to V_{SS} all parts	1.73	1.8	1.95	V
VDDQ	Operating supply voltage 3.3 V peripheral	All VDDQ pins with respect to V_{SS} all parts	3.0	3.3	3.6	V
VIH	High level, input voltage	All digital inputs and I/Os	2.0	-	-	V
VIL	Low level, input voltage	All digital inputs and I/Os	-	-	0.8	V
V_{hyst}	Input hysteresis voltage	All digital inputs and I/Os	0.4	-	-	V
VOH	Static output, high voltage	All digital inputs and I/Os	VDDQ – 0.4	-	-	V
VOL	Static output, low voltage	All digital inputs and I/Os	-	-	0.4	V
IOZ	3-state leakage current towards either VSSQ or VDDQ	Input voltage < VIL	-	–1	-	µA
		Input voltage > VIH	-	1	-	µA
		VIL < input voltage < VIH	-	20	-	µA
IOSH	Short circuit current, output high	Drive high. Pad connected to ground	-	-	40	mA
IOSL	Short circuit current, output low	Drive low. Pad connected to VDDQ	-	-	45	mA
I_{PU}	Pull-up current	V_i = 0.0 V	-	–50	-	µA
I_{PD}	Pull-down current	V_i = 3.3 V	-	50	-	µA
C_{IN}	Input capacitance	Including bond pads	-	-	3	pF
I^2C pads						

Table 27. DC characteristics digital I/O (at T_{amb} = –40°C to +85 °C, V_{DDQ} = 3.3 V unless otherwise stated) *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Low level input voltage		–0.5	-	0.3 × VDDQ	V
VIH	High level input voltage		0.7 × VDDQ	-	VDDQ + 0.5	V
V_{hys}	Hysteresis voltage		0.1 × VDDQ	-	-	V
IOL	Low level output current	At V_{OL} = 0.4V	3	-	-	mA
IOH	High level output current	0.3 × VDDQ <V_{OH} < 0.7 × VDDQ	3	-	12	mA
Miscellaneous						
t_{RESET}	Time when the device is ready for use after the rising edge of the RESETN pin	All power supply voltages are within the specified values	-	0.6	2	ms
I_{ddq}	Digital quiescent (not active) current	VDDD = 1.95 V VDDQ = 3.6 V	-	-	1000	µA

14. Dynamic characteristics

Table 28. Digital pins timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RF}	Output rise/fall time digital pads non slew-rate controlled	[1]	2.5	-	5.5	ns
t_{RF_SC}	Output rise/fall time digital pads slew-rate controlled	[1]		10		ns
F_{MAX}	Maximum operating frequency	[1]	-	-	50	MHz

[1] Output load = 30 pF. Measurement criteria is 10% to 90%.

14.1 RDS electrical specification

Remark: Refer to Ref. 1 for the timing figure in Direct Output mode.

Figure 43 shows the timing of the interface signals in buffer mode.

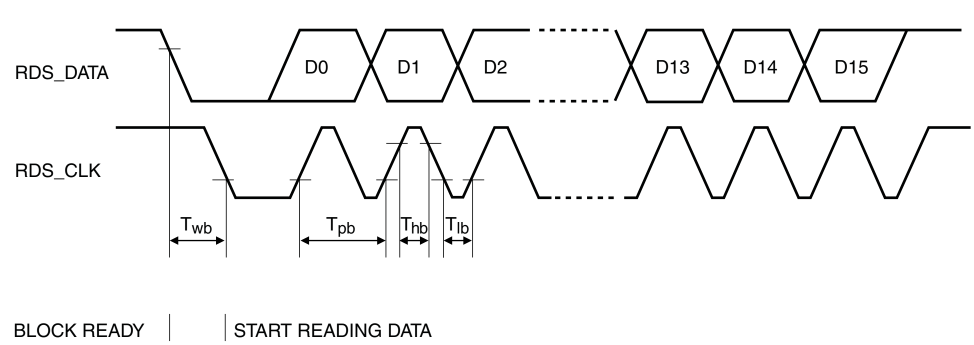


Fig 43. RDS Timing in buffer mode

Table 29. Timing of the RDS interface (see Figure 43)

Symbol	Parameter	Min	Typ	Max	Unit
F_{rdscl}	Nominal clock frequency of the RDS clock	-	1187.5	-	Hz
T_{wb}	Wait time	1	-	-	µs
T_{pb}	Periodic time	2	-	-	µs
T_{hb}	Clock high-time	1	-	-	µs
T_{lb}	Clock low-time	1	-	-	µs
F_{excl}	Input frequency External RDSA Clock	-	-	10	MHz

14.2 Digital radio output

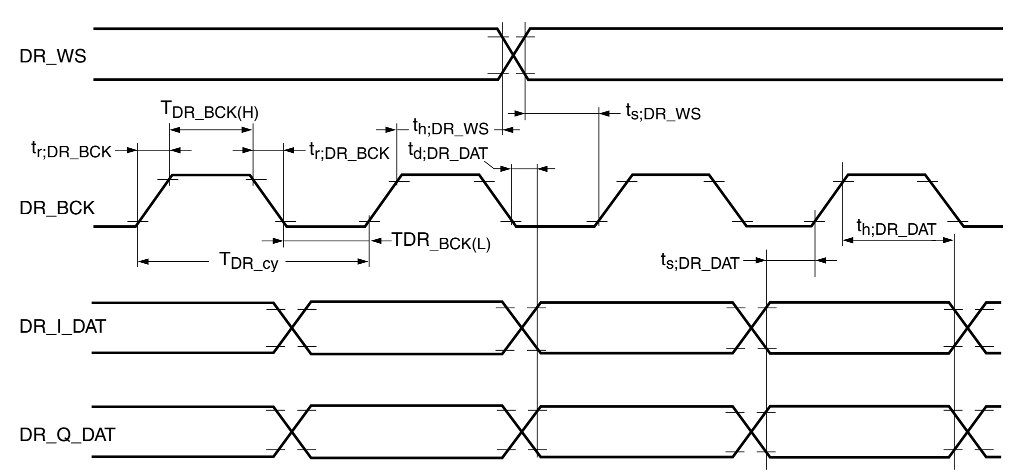


Fig 44. Digital radio I²S timing format

Table 30. Timing digital radio outputs

Symbol	Parameter	Min	Typ	Max	Unit
T_{DR_cy}	Bitclock cycle time	-	96.15	-	ns
$t_{r;DR\_BCK}$	Rise time	-	-	14	ns
$t_{r;DR\_BCK}$	Fall time	-	-	-	ns
$T_{DR\_BCK(H)}$	Bitclock time HIGH	34	-	-	ns
$T_{DR\_BCK(L)}$	Bitclock time LOW	34	-	-	ns
$t_{s;DR\_DAT}$	Data setup time	19	-	-	ns
$t_{h;DR\_DAT}$	Data hold time	19	-	-	ns
$t_{d;DR\_DAT}$	Data delay time	-	-	14	ns
$t_{s;DR\_WS}$	Word select setup time	19	-	-	ns
$t_{h;DR\_WS}$	Word select hold time	19	-	-	ns

14.3 IIS timing specification

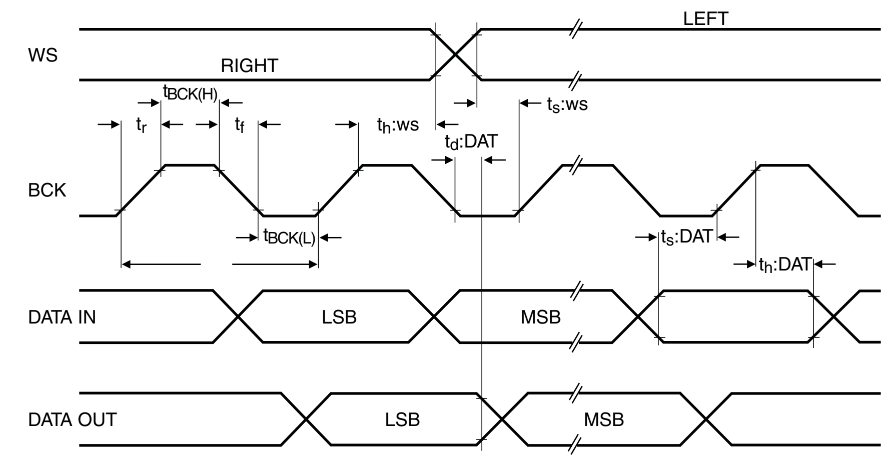


Fig 45. Input timing of the digital audio data inputs and the digital audio data outputs

Table 31. Timing digital audio inputs and outputs (see Figure 45)

Symbol	Parameter	Min	Max	Unit
T_{cy}	Bitclock cycle time	162	-	ns
t_r	Rise time	-	$0.15 \times T_{cy}$	ns
t_f	Fall time	-	$0.15 \times T_{cy}$	ns
$t_{BCK(H)}$	Bitclock time HIGH	$0.35 \times T_{cy}$	-	ns
$t_{BCK(L)}$	Bitclock time LOW	$0.35 \times T_{cy}$	-	ns
$t_{s;DAT}$	Data set-up time	$0.2 \times T_{cy}$	-	ns
$t_{h;DAT}$	Data hold time	$0.2 \times T_{cy}$	-	ns
$t_{d;DAT}$	Data delay time	-	$0.15 \times T_{cy}$	ns
$t_{s;WS}$	Word select set-up time	$0.2 \times T_{cy}$	-	ns
$t_{h;WS}$	Word select hold time	$0.2 \times T_{cy}$	-	ns

14.4 I²C electrical specifications

14.4.1 I²C timing

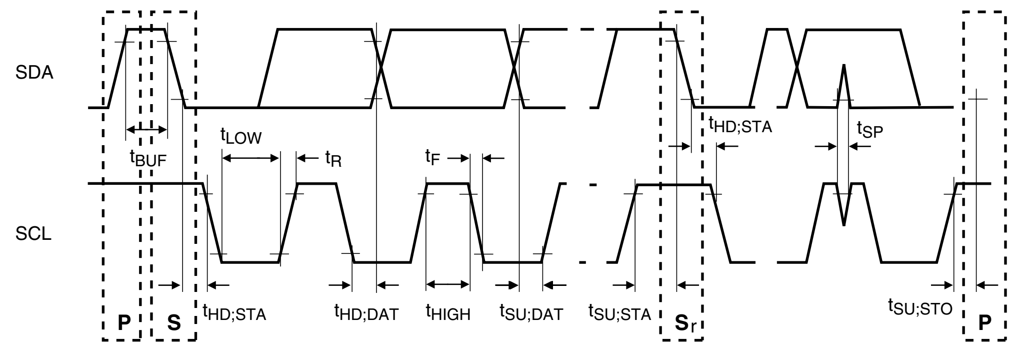


Fig 46. Definition of timing on the I²C bus

Table 32. Timing I²C bus, see Figure 46

Symbol	Parameter	Conditions	Standard Mode I²C Bus		Fast Mode I²C Bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	Bus free between a STOP and a START condition		4.7	-	1.3	-	µs
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
$t_{SU:STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{HD:DAT}$	DATA hold-time		0	-	0	0.9	µs
$t_{SU:DAT}$	DATA set-up time		250	-	100	-	ns
t_r	Rise time of both SDA and SCL signals [1]	C_b in pF	20 + $0.1C_b$	300	20 + $0.1C_b$	300	ns
t_f	Fall time of both SDA and SCL signals [1]	C_b in pF	20 + $0.1C_b$	300	20 + $0.1C_b$	300	ns
$t_{SU;STO}$	Set-up time for the STOP condition		4.0	-	0.6	-	µs
C_b	Capacitive load for each bus line		-	400	-	400	pF
t_{SB}	Pulse width of the spikes to be suppressed by the input filter		0	80	0	80	ns

[1] Measurement criteria is 30% to 70%.

14.5 SPDIF

Table 33. Analog SPDIF characteristics (conditions: Tamb = 25°C, unless otherwise stated)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VDD_SPDIF	Supply voltage for the SPDIF		3.0	3.3	3.6	V
SPVL	AC input level		0.2	-	3.6	V_{pp}
SPIR	Input resistance	f_i = 1.0 kHz	5.5	8.5	14	kΩ
SPIC	Input capacity		-	50	-	pF
SPHYS	Hysteresis input		30	40	55	mV
SPCIN	Input couple capacitor		-	10	-	nF

14.6 Audio ADC

Table 34. Audio ADC DC characteristics (conditions: T_{amb} = 25°C, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA_1v8_ADC	Supply voltage analog part ADCs		1.73	1.80	1.95	V
VDD_ADC	Supply voltage analog part ADCs		3.0	3.3	3.6	V
VREFAD	Common mode output reference voltage ADCs	With respect to VADCP/VADCN	47	50	53	%VADCP
ZOUT	Output impedance VREFAD	I_{out} <2 mA	-	10	100	Ω
VADCP	Positive input reference voltage ADCs and RGPDAC		3.0	3.3	3.6	V
VADCN	Negative input reference voltage ADCs and RGPDAC		–0.3	0	0.3	V
IVADCN	Negative input reference current ADCs and RGPDAC		-	370	-	µA

Table 35. Audio ADC AC characteristics (conditions: T_{amb} = 25°C, VDD_ADC = 3.3 V, VDDA_1v8 = 1.8 V, VADCP/VADCN = 3.3 V, Fs = 44.1 kHz, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AILVL	Conversion input level at ADC input	<1% Total Harmonic Distortion (THD)	-	-	0.7	Vrms
AIIRG	Input resistance AIN0 to AIN4		1	-	-	MΩ
AITHDC	THD+N AIN0 to AIN4 inputs	1 kHz, 0.5 V_{rms}, BW = 20 kHz	-	–82	–76	dB
AISNRC	SNR AIN0 to AIN4 inputs	1 kHz, BW = 20 kHz, 0 dB ref. = 0.5 V_{rms}	85	92	-	dBA

Table 35. Audio ADC AC characteristics (conditions: T_{amb} = 25°C, VDD_ADC = 3.3 V, VDDA_1v8 = 1.8 V, VADCP/VADCN = 3.3 V, Fs = 44.1 kHz, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AICRI	Crosstalk between inputs	1 kHz, 0.5 V_{rms}, measured input ac grounded	65	-	-	dB
		15 kHz, 0.5 V_{rms}, measured input ac grounded	50	-	-	dB
CMRRCD	CMRR high common mode	AIN0_R_GND = 1 MΩ, RCD Player GND cable = <1 kΩ, F_{in} = 1 kHz, 100 mV_{rms}	60	-	-	dB
B_ADC	Audio input frequency response	–3 dB roll-off, Fs = 44.1 kHz	20	-	-	kHz

14.7 IFADC

Table 36. IFADC DC Characteristics (conditions: T_{amb} = 25°C, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA_1v8	Supply voltage analog part IFADC		1.73	1.80	1.95	V
VDD_IFADC	Supply voltage analog part IFADC and RGPDAC		3.0	3.3	3.6	V
VIFADCP	Positive output reference voltage IFADC		2.65	-	3.0	V
VIFADCN	Negative input reference voltage IFADC		–0.3	0	+0.3	V
VIFADCBG	Band gap output reference voltage IFADC		1.15	1.26	1.30	V
IF_INPR	Single ended input resistance IFADC in low IF mode	TEF7000 tuner application	16.5	20.9	25	kΩ
	Single ended input resistance IFADC in normal IF mode	TEF6730 tuner application	50	62.2	75	kΩ

Table 37. IFADC AC Characteristics in low IF mode (conditions: T_{amb} = 25°C, VDD_IFADC = 3.3 V, VDDA_1v8 = 1.8 V, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIF_CNR3k	Carrier-to-Noise ratio total IF	1.4 V_{pp} input IFADC, bandwidth 3 kHz, typical application running	90	100	-	dB
LIF_DNR	Dynamic range IF	V_{dif} = 0.5 V_{rms} BW = 3.0 kHz	95	102	-	dB
LIF_IM_–6	Third order inter-modulation with –6 dB signals IF	Two –6 dB signals at 300 kHz and 305 kHz, with respect to 0.0 dB level	-	–88	–	dB
LIF_IM_–9	Third order inter-modulation with –9 dB signals IF	Two –9 dB signals at 300 kHz and 305 kHz, with respect to 0.0 dB level	-	–92	–	dB
LIF_IR	Image rejection IF	Two input signals that have a 90° phase shift and equal gain	45	50	-	dB

Table 38. IFADC AC Characteristics in normal IF mode (conditions: T_{amb} = 25°C, VDD_IFADC = 3.3 V, VDDA_1v8 = 1.8 V, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF_CNR3k	Carrier-to-Noise ratio total IF	1.4 V_{pp} input IFADC,bandwidth 3 kHz; typical application running	-	95	-	dB
IF_DNR	Dynamic range IF	V_{dif} = 0.5 V_{rms} BW = 3.0 kHz	-	97	-	dB
IF_IM_-6	Third order inter-modulation with -6 dB signals IF	Two -6 dB signals [1] at 10.71MHz and 10.705MHz, with respect to 0.0 dB level	-	–81	-	dB
IF_IM_-9	Third order inter-modulation with -9 dB signals IF	Two -9 dB signals [1] at 10.71MHz and 10.705MHz, with respect to 0.0 dB level	-	–89	-	dB
IF_IR	Image rejection IF	Two input signals that have a 90° phase shift and equal gain	45	50	-	dB

[1] The two signals are at 10.700 MHz and 10.705 MHz.

14.8 Voltage regulator

Table 39. Analog regulator characteristics (conditions: T_{amb} = 25°C, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD_REG	Supply voltage regulator		3.0	3.3	3.6	V
GAPREG	Band gap output reference voltage regulator		-	1.246	-	V
VFEBREG	Voltage at the pins FEBREG	PMOST PHK04P02T in application	1.82	1.91	1.95	V
VCONREG	Regulator control range	VDD_REG = 3.3 V	0.5	-	VDD_REG – 0.3	V
REGSU	Start-up time regulator		-	0.5	see [1]	ms

[1] Dependent on the external components.

14.9 Audio DAC (ADAC)

Table 40. Audio DAC DC characteristics (conditions: T_{amb} = 25°C, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD_DAC	DAC digital power supply		3.0	3.3	3.6	V
VDACP	Positive input reference voltage DAC		3.0	3.3	3.6	V
VDACN	Negative input reference voltage DAC		–0.3	0	+0.3	V
VOUT_DC	Average DC output voltage	R_{load} >20 kΩ AC coupled only	-	VDACP / 2	-	V
ROUTDA	DAC output resistance		0.7	1.0	1.3	kΩ
RREFDA	Resistance between VDACP and VDACN		-	0.66	-	kΩ
ISCDA	Output short-circuit current DAC		-	-	5.2	mA
B	Bandwidth DA (Roll-off due to internal DA source resistance and external capacitor / load)	At -3.0 dB, C_{fil} = 3.3 nF NPO	-	48	-	kHz

Table 40. Audio DAC DC characteristics (conditions: T_{amb} = 25°C, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
B_DAC	Roll-off due to internal DAC filter	At -3.0 dB, Fs = 44.1 kHz	20	-	-	kHz
DAC-CFIL	Filter capacitance on DAC outputs	NPO capacitor used	-	3.3	-	nF
DAC-RL	Allowed load resistor on DAC voltage outputs	AC coupled only	20	-	-	kΩ

Table 41. Audio DAC AC characteristics (conditions: T_{amb} = 25°C, VDD_DAC = 3.3 V, VDACP / VDACCN = 3.3 V, Rload AC = 20 kΩ, Fs = 44.1 kHz, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOUT_AC	Output voltage AC of Op-Amp outputs at full I^2S signal		0.95	1.0	1.10	V_{rms}
PSRRDA	Reference power supply Ripple Rejection DACs	F_{ripple} = 1.0 kHz, V_{ripple} = 100 mV_{peak}, CVDACP = 220 µF	3	6	-	dB
UNBAL	Deviation in output level of one of the six DAC outputs with respect to the average of the six outputs	Full-scale output	-	-	0.2	dB
XT	Channel separation between the outputs in the audio band. Front or Rear outputs digital silence, others maximum volume	f_i = 1.0 kHz	74	86	-	dB
THD and N/S	DAC total harmonic distortion plus noise, versus Output signal DAC	f_i = 1.0 kHz, –0.2 dB C_{fil} = 3.3 nF NPO	-	–78	–70	dB
THD and N/S 60	DAC total harmonic distortion plus noise, versus Output signal DAC at -60 dB	f_i = 1.0 kHz, –60 dB, C_{fil} = 3.3 nF NPO	-	–45	–40	dBA
SNR	Signal-to-Noise ratio. This is the dB ratio between the full I^2S signal and the I^2S digital silence noise		100	106	-	dBA
IM	Intermodulation distortion	f_i = 60 Hz and 7 kHz, ratio = 4:1	-	-70	-55	dB

14.10 RGPDAC

Table 42. RGPDAC DC Characteristics (conditions: T_{amb} = 25°C, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD_IFADC	Supply voltage analog part IFADC and RGPDAC [1]		3.0	3.3	3.6	V
VADCP	Positive output reference voltage Audio ADC [2]		3.0	3.3	3.6	V
VADCN	Negative input reference voltage Audio ADC [2]		-0.3	0	0.3	V
DCR_RDA	DC output voltage range RGPDAC		VSS_IFADC + 0.3	-	VDD_IFADC – 0.3	V

Table 42. RGPDAC DC Characteristics (conditions: T_{amb} = 25°C, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ISC_RDA	Output short circuit current RGPDAC	Output short circuit current to ground at maximum positive output DC voltage	-	-	120	mA
RL_RDA	Resistive load RGPDAC		50	-	-	kΩ
CL_RDA	Capacitive load RGPDAC		-	-	200	pF

[1] These are the same values as those given in Table 36. They have been added here because the same supply pins are connected to the Audio AD and to the RGPDAC.

[2] These are the same values as those given in Table 34. They have been added here because the same supply pins are connected to the Audio ADC and to the RGPDAC.

Table 43. RGPDAC AC Characteristics (conditions: T_{amb} = 25°C, VDD_IFADC = 3.3 V, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_RDA	Resolution of RGPDAC		-	10	-	bits
INL_RDA	Integral non-linearity RGPDAC	F = 1.0 kHz, Sampling rate = 400 kHz	-	2.5	7	LSB levels
DNL_RDA	Differential non-linearity RGPDAC	F = 1.0 kHz, Sampling rate = 400 kHz	-	1.25	2.5	LSB levels
PSRR_RDA	Power supply Ripple Rejection RGPDAC	F_{ripple} = 1.0 kHz, V_{ripple} = 100 mV_{peak} peak	43	48	-	dB
FS_RDA	Sample rate of RGPDAC		-	-	400	kHz

14.11 Tuner clock generator

Table 44. Tuner clock generator characteristics (conditions: T_{amb} = 25°C, VDD_1V8 = 1.8 V, unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tcg_Clock	Clock output frequency		-	400/100 [1]	-	kHz
Tcg_Cur	Output current sourcing/sinking	Single tuner mode	200	300	400	µA
		Dual tuner mode	400	600	800	µA
Tcg_ICM	Common mode output current	From each pin to ground	–50	-	50	µA
Tcg_V_{out}	DC level at the outputs	DC level will be determined by the load current	1.0	1.2	1.4	V
Tcg_Load	Load impedance		-	180	-	Ω

[1] Depends on the type of the tuner connected to the SAF774x

14.12 Oscillator

Table 45. Oscillator characteristics (conditions: T_{amb} = 25°C [1], unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD_XTAL	Supply voltage crystal oscillator and PLL		1.73	1.8	1.95	V

Table 45. Oscillator characteristics (conditions: T_{amb} = 25°C [1], unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
XTFREQ	Crystal frequency	C_{load} = 10 pF, 3rd overtone	-	41.6	-	MHz
	Adjustment tolerance	T_{amb} = 25°C	–50	-	+50	ppm
	Temperature drift for WX applications		–30	-	+30	ppm
	Temperature drift AM/FM applications		–50	-	+50	ppm
	Aging drift (all applications)		–5	-	+5	ppm
XLOAD	Load capacitance		-	10	-	pF
RXTAL	Allowed loss resistor of the crystal	C_{load} = 10 pF	-	-	60	Ω
CPXTAL	Parallel package capacitance		-	-	7	pF
XROUT	Oscillator output impedance	AC method: V_{im} = 20 mV_{rms} @ 1.0 MHz	600	-	1100	Ω
		DC method: V_{im} = 600 mV_{rms} @ DC	1350	-	3150	W
XGM	Oscillator trans conductance	AC method: V_{im} = 20 mV_{rms} @ 1.0 MHz	13	24	35	mA/V
		DC method: V_{im} = 600 mV_{rms} @ DC	13	-	22	mA/V

[1] The oscillator can operate within a temperature range of –40°C to 85°C.

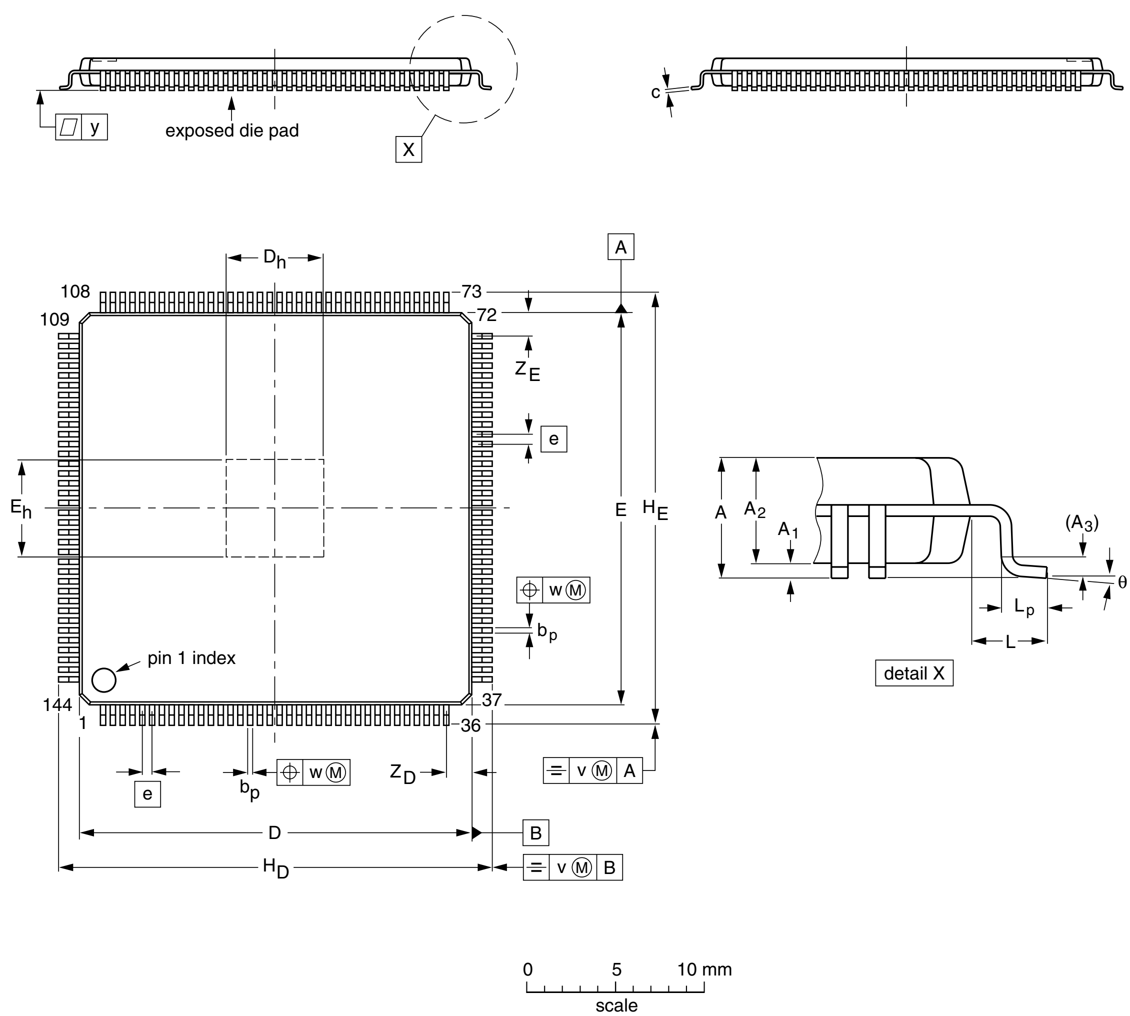
15. Package outline

The package outline for the SAF7741HV is a SOT612-3 (HLQFP144). The outer dimensions are 20 mm × 20 mm × 1.4 mm (see Figure 47).

The sub-package has a double down set with an exposed die-pad of 5.6 mm × 5.6 mm and a ground ring at a higher level that is connected mechanically to the exposed die-pad. Lead number 98 is a fused lead to this ground ring.

HLQFP144: plastic thermal enhanced low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm; exposed die pad

SOT612-3



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.12 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	5.7 5.5	20.1 19.9	5.7 5.5	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT612-3		MS-026				~~02-07-12~~ 04-07-05

Fig 47. SOT612-3 (HLQFP144) package outline

16. Abbreviations

Table 46. Abbreviations

Acronym	Description
ADC	Analog–to–Digital Converter
ADF	Audio Decimation Filter
ADSP	Audio DSP
AF	Alternate Frequency
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AM	Amplitude Modulation
A/S–DSP	Audio/Sampled DSP
BCK	Bit-Clock
BSLP	Bit–Slip
BSPA	Bit–Slip Process Active
CD	Compact Disc
CIC	Cascaded Integrator Comb filter Carrier Identification Code
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CRD	Cordic Rate and De–rotate
DAC	Digital–to–Analog Converter
DAD	Audio DAC Decimation
DAVB	Digital Audio and Video Broadcasting
DAVN	Data Available Signal (on RDS)
Dice	Digital In Car Entertainment
DIO	Digital I/O (on EPICS7A)
DIV	Divide Divider
DL	DiRaNa2 LeafDice
DRM	Digital Radio Mondiale
DSP	Digital Signal Processor
DVD	Digital Video Disc Digital Versatile Disc
EBU	European Broadcasting Union
EPICS	Economic Parameterized Integrated CoreS
ESD	Electrostatic Discharge
FIR	Finite Impulse Response
FM	Frequency Modulation
GPIO	General Purpose I/O
I/O	Input/Output
I^2C	Inter–IC Communication

Table 46. Abbreviations *…continued*

Acronym	Description
I^2S	Inter–IC Sound (a Philips standard)
IAC	Interference Absorption Circuit
IBOC	In–Band On–Channel
IF	Intermediate Frequency
IFADC	Intermediate Frequency Analog–to–Digital Converter
IFFC	IF Filter Compensation
IFLAG	I Flag (EPICS7A flag)
IIS	Inter–IC Sound (any data format)
IMODE	Input Flag Mode of EPICS7A
IQ	Quadra–tone Signals I and Q
IQC	IQ Correction
JTAG	Joint Test Action Group
kSa/s	kilo Samples per second
LFLAG	L Flag (EPICS7A flag)
LMS	Least Mean Square
LSB	Least Significant Bit
MPI	MicroProcessor Interface
MPX	Frequency MultiPleXed signal (audio/data)
MSa/s	Mega Samples per second
MSB	Most Significant Bit
MSEL	Selection for the M–divider
NSEL	Selection for the N–divider
NLMS	Normalized Least Mean Square
NZIF	Near Zero IF
PCB	Printed Circuit Board
PDC	Primary Decimation Chain
PLL	Phase Lock Loop
PMOS	Positive channel Metal Oxide Semiconductor
RBDS	Radio Broadcast Data System Radio Broadcast Data Signals
RDS	Radio Data System
RDDA	RDS Data Output Radio Digital DAta
RDCL	RDS CLock output (master mode) RDS CLock input (slave mode)
RGP	Radio General Purpose
RGP DAC	Radio General Purpose Digital–to–Analog Converter
ROM	Read Only Memory
SCL	Serial Clock (I^2C line)
SDA	Serial Data (I^2C line)
SDSP	Sample Rate Converter DSP

Table 46. Abbreviations *…continued*

Acronym	Description
SFLAG	Sync Flag
SPDIF	Sony/Philips Digital Interface Format
SRC	Sample Rate Converter
TDSP	Tuner DSP
THD	Total Harmonic Distortion
TTL	Transistor-Transistor Logic
VDD	Positive supply voltage
VDDA	Positive supply voltage (analog)
VDDE	Positive supply (peripheral cells)
VIA	A link between two layers of a PCB
VREFAD	Reference voltage for ADC
VSS	Negative supply voltage
VSSA	Negative supply voltage (analog)
VSSE	Ground supply (peripheral cells)
WB	Weather Band
WDOG	WatchDog
WS	Word–Size
XRAM	X (typically for DSP data) Random Access Memory
YRAM	Y (typically for DSP coefficients) Random Access Memory
YROM	Y (typically for DSP coefficients) Read Only Memory
ZIF	Zero IF

17. References

[1] SAF7741HV Radio User Manual

[2] SAF7741HV User Manual

[3] SAF7741HV I^2C Memory Map

[4] SAF7741HV DIO Map

[5] Official Philips I^2S Standard Document (available from NXP Semiconductors, International Marketing and Sales)

[6] Digital Audio Interface specification (IEC60958-1 Edition 2, Part 1: General Part and IEC60958-3 Edition 2, Part 3: Consumer Applications)

18. Revision history

Table 47. Revision history

Document ID	Release Date	Data Sheet Status	Change Notice	Document Number	Supersedes
SAV7741HV_5	20080509	Objective data sheet	N/A	9397 750	SAV7741HV_4
Modifications • Some minor updates and corrections.					
SAV7741HV_4	20080214	Objective data sheet	N/A	9397 750	SAV7741HV_3
Modifications • Updated the single-tuner SAF7741 and TEF7000 application diagram (Figure 40).					
SAV7741HV_3	20080125	Objective data sheet	N/A	9397 750	SAV7741HV_2
Modifications • Some minor corrections.					
SAV7741HV_2	20080117	Objective data sheet	N/A	9397 750	SAV7741HV_1
Modifications • The format of this user manual has been redesigned to comply with the new identity guidelines of NXP Semiconductors • Legal texts have been adapted to the new company name where appropriate • Updated to incorporate changes since initial release.					
SAV7741HV_1	20061031	Objective data sheet	N/A	9397 750	-

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19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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