SA630

Single-Pole Double-Throw (SPDT) switch

Rev. 3 — 23 July 2014 Product data sheet

1. General description

The SA630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC to 1 GHz from one 50 Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

The extremely low current consumption makes the SA630 ideal for portable applications. The excellent isolation and low loss makes this device a suitable replacement for PIN diodes.

The SA630 is available in an 8-pin SO (surface-mounted miniature) package.

2. Features and benefits

- Wideband (DC to 1 GHz)
- Low through loss (1 dB typical at 200 MHz)
- Unused input is terminated internally in 50 Ω
- Excellent overload capability (1 dB gain compression point +18 dBm at 300 MHz)
- Low DC power (170 μA from 5 V supply)
- Fast switching (20 ns typical)
- Good isolation (off channel isolation 60 dB at 100 MHz)
- Low distortion (IP3 intercept +33 dBm)
- Good 50 Ω match (return loss 18 dB at 400 MHz)
- Full ESD protection
- Bidirectional operation

3. Applications

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
SA630D/01	SA630D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SA630D/01	SA630D/01,112	SO8	Standard marking *IC's tube - DSC bulk pack	2000	T_{amb} = –40 °C to +85 °C
	SA630D/01,118	SO8	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = –40 °C to +85 °C

5. Block diagram

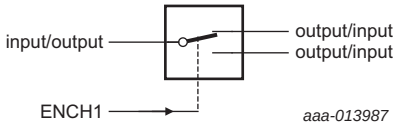


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

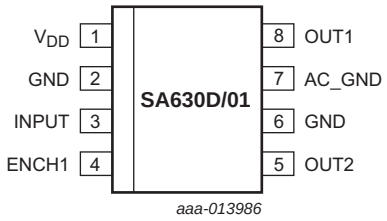


Fig 2. Pin configuration for SO8

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V_{DD}	1	supply voltage
GND	2, 6	ground
INPUT	3	input
ENCH1	4	enable channel 1
OUT2	5	output
AC_GND	7	AC ground
OUT1	8	output

7. Equivalent circuit

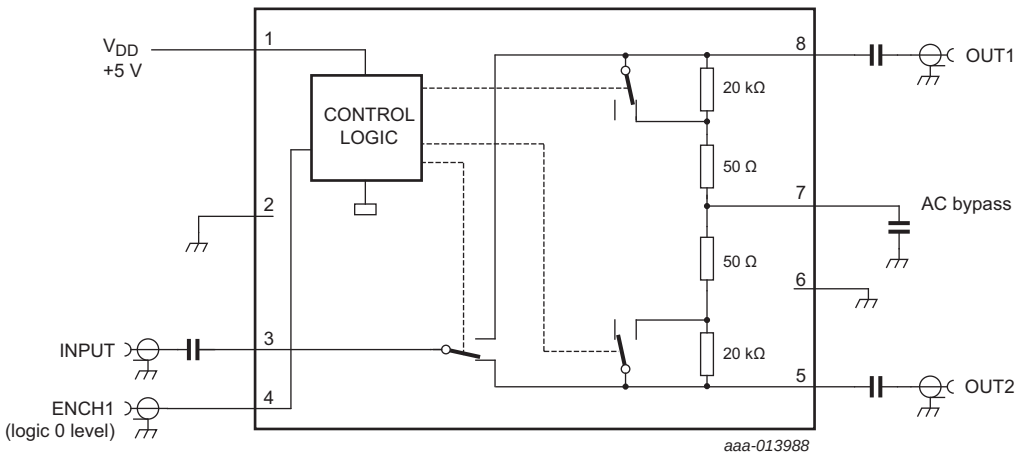


Fig 3. Equivalent circuit

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+5.5	V
P	power dissipation	T_{amb} = 25 °C (still air) [1]	-	780	mW
$T_{j(max)}$	maximum junction temperature		-	150	°C
$P_{i(max)}$	maximum input power		-	+20	dBm
$P_{o(max)}$	maximum output power		-	+20	dBm
T_{stg}	storage temperature		−65	+150	°C

[1] Maximum dissipation is determined by the operating ambient temperature and the thermal resistance $R_{th(j-a)}$.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3.0	5.5	V
T_{amb}	ambient temperature	operating	−40	+85	°C
T_j	junction temperature	operating	−40	+105	°C

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8 package	158	°C/W

11. Static characteristics

Table 7. Static characteristics

V_{DD} = +5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current		40	170	300	µA
V_{th}	threshold voltage	TTL/CMOS logic [1]	1.1	1.25	1.4	V
V_{IH}	HIGH-level input voltage	logic 1 level; enable channel 1	2.0	-	V_{DD}	V
V_{IL}	LOW-level input voltage	logic 0 level; enable channel 2	–0.3	-	+0.8	V
$I_{IL(ENCH1)}$	LOW-level input current on pin ENCH1	ENCH1 = 0.4 V	–1	0	+1	µA
$I_{IH(ENCH1)}$	HIGH-level input current on pin ENCH1	ENCH1 = 2.4 V	–1	0	+1	µA

[1] The ENCH1 input must be connected to a valid logic level for proper operation of the SA630.

12. Dynamic characteristics

Table 8. Dynamic characteristics

All measurements include the effects of the SA630 evaluation board (Figure 19). Measurement system impedance is 50 Ω.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
s_{21}, s_{12}	insertion loss (ON channel)	DC to 100 MHz	-	1	-	dB
		500 MHz	-	1.4	-	dB
		900 MHz	-	2	2.8	dB
s_{21}, s_{12}	isolation (OFF channel)[1]	10 MHz	70	80	-	dB
		100 MHz	-	60	-	dB
		500 MHz	-	50	-	dB
		900 MHz	24	30	-	dB
s_{11}, s_{22}	return loss (ON channel)	DC to 400 MHz	-	20	-	dB
		900 MHz	-	12	-	dB
s_{11}, s_{22}	return loss (OFF channel)	DC to 400 MHz	-	17	-	dB
		900 MHz	-	13	-	dB
$t_{d(off)}$	turn-off delay time	50 % TTL to (90 % to 10 %) RF	-	20	-	ns
$t_{f(off)}$	turn-off fall time	90 % to 10 % RF	-	5	-	ns
$t_{r(on)}$	turn-on rise time	10 % to 90 % RF	-	5	-	ns
$V_{trt(p-p)}$	peak-to-peak transient voltage	switching transients	-	165	-	mV
$P_{L(1dB)}$	output power at 1 dB gain compression	DC to 1 GHz	-	+18	-	dBm
IP3	third-order intercept point	100 MHz	-	+33	-	dBm
IP2	second-order intercept point	100 MHz	-	+52	-	dBm
NF	noise figure	Z_o = 50 Ω				
		100 MHz	-	1.0	-	dB
		900 MHz	-	2.0	-	dB

[1] The placement of the AC bypass capacitor is critical to achieve these specifications. See Section 14 for more details.

13. Performance curves

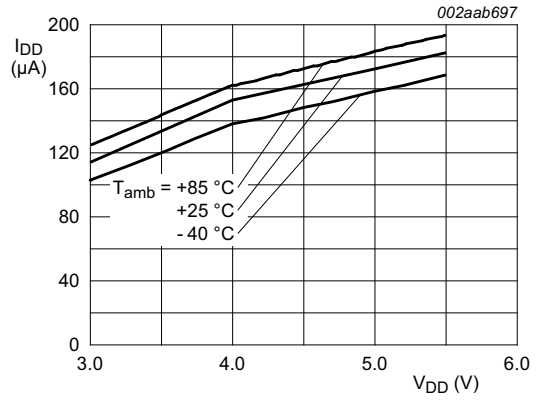
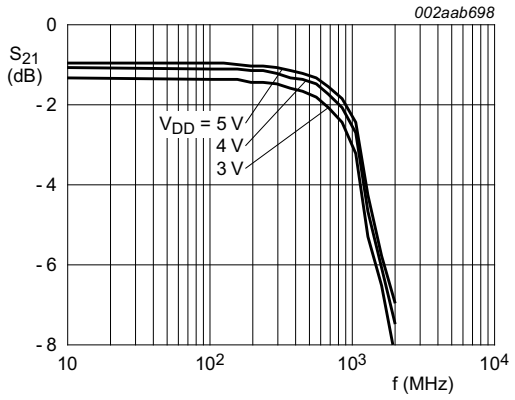
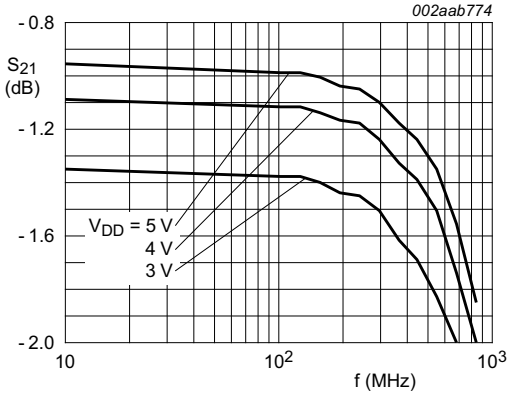


Fig 4. Supply current versus V_{DD} and temperature



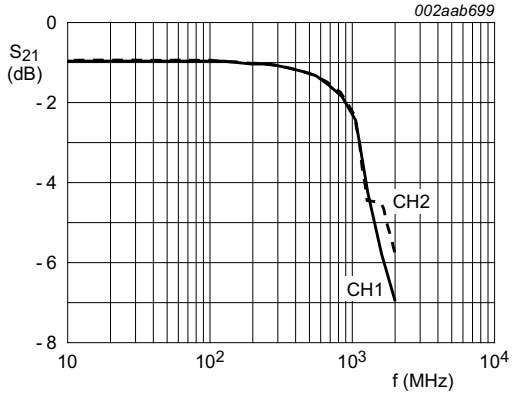
T_{amb} = +25 °C

Fig 5. Loss versus frequency and V_{DD}



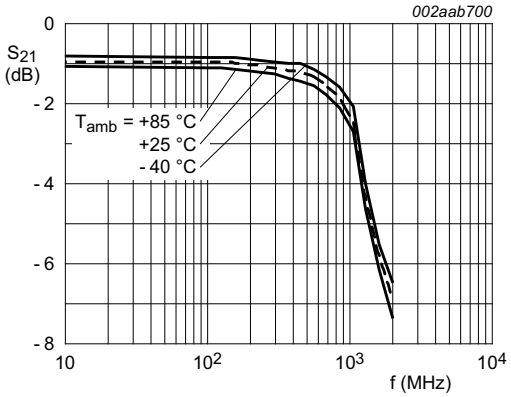
T_{amb} = +25 °C

Fig 6. Loss versus frequency and V_{DD}



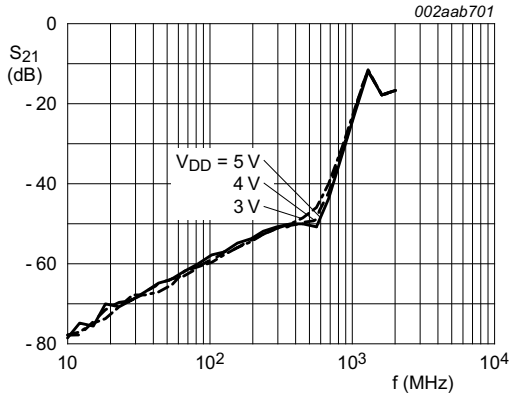
T_{amb} = +25 °C; V_{DD} = 5 V

Fig 7. Loss matching versus frequency; CH1 versus CH2



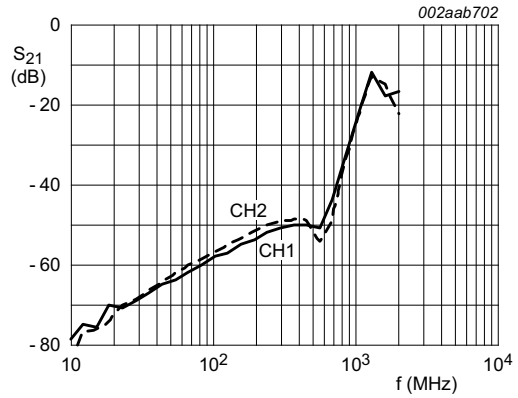
V_{DD} = 5 V

Fig 8. Loss versus frequency and temperature



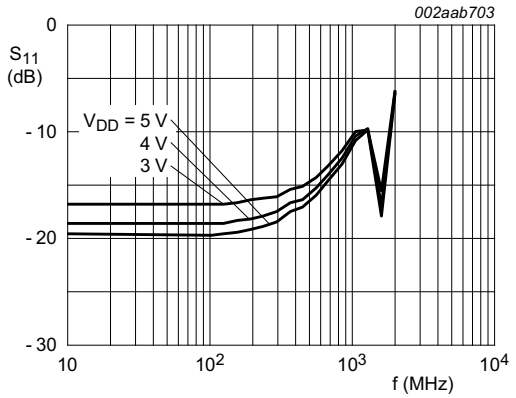
T_{amb} = +25 °C

Fig 9. Isolation versus frequency and V_{DD}



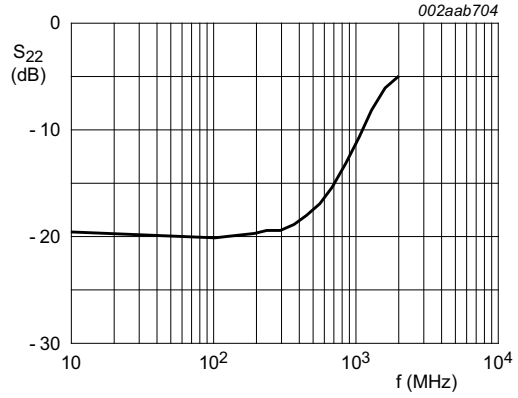
T_{amb} = +25 °C; V_{DD} = 5 V

Fig 10. Isolation matching versus frequency; CH1 versus CH2



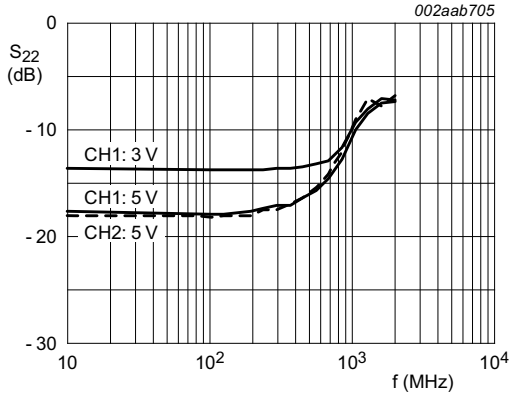
T_{amb} = +25 °C

Fig 11. Input match ON-channel versus frequency and V_{DD}



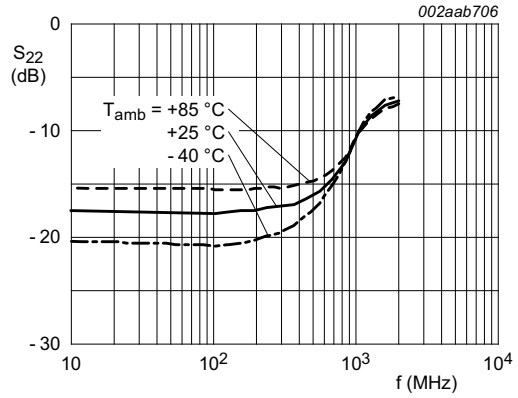
T_{amb} = +25 °C; V_{DD} = 5 V

Fig 12. Output match ON-channel versus frequency



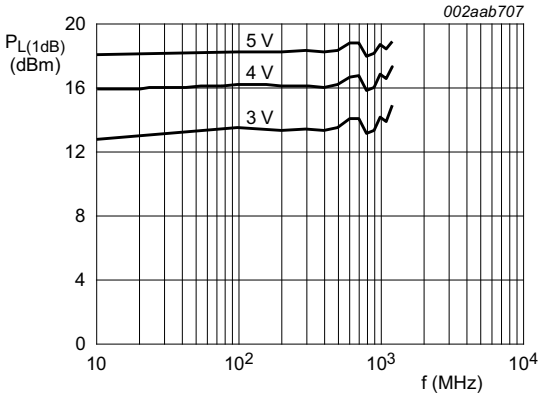
T_{amb} = +25 °C

Fig 13. OFF-channel match versus frequency and V_{DD}



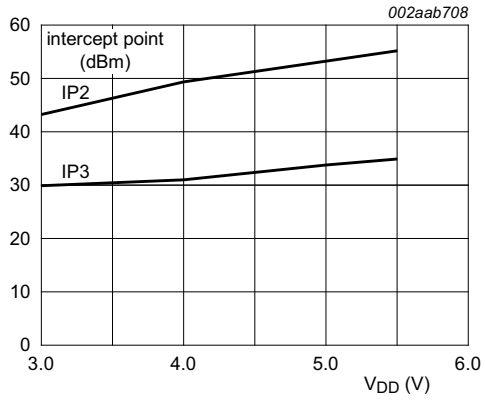
V_{DD} = 5 V

Fig 14. OFF-channel match versus frequency and temperature



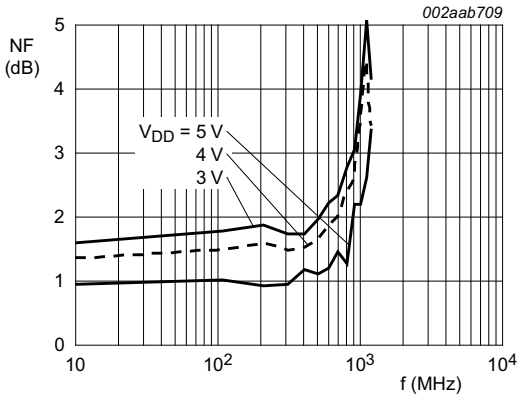
T_{amb} = +25 °C

Fig 15. $P_{L(1dB)}$ versus frequency and V_{DD}



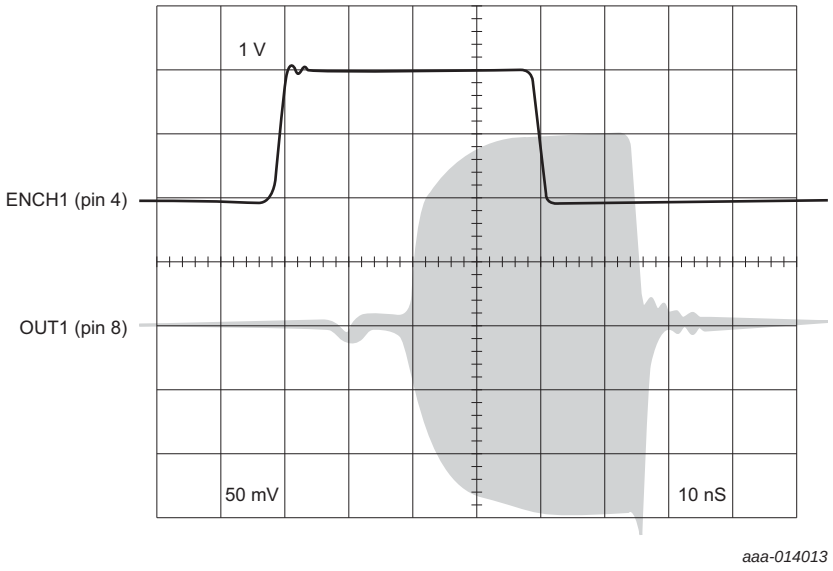
T_{amb} = +25 °C

Fig 16. Intercept points versus V_{DD}



T_{amb} = +25 °C; Z_o = 50 Ω

Fig 17. Noise Figure versus frequency and V_{DD}



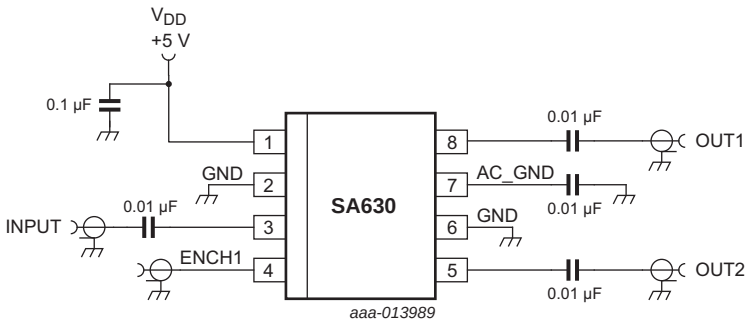
f_i = 100 MHz at −6 dBm; V_{DD} = 5 V

Fig 18. Switching speed

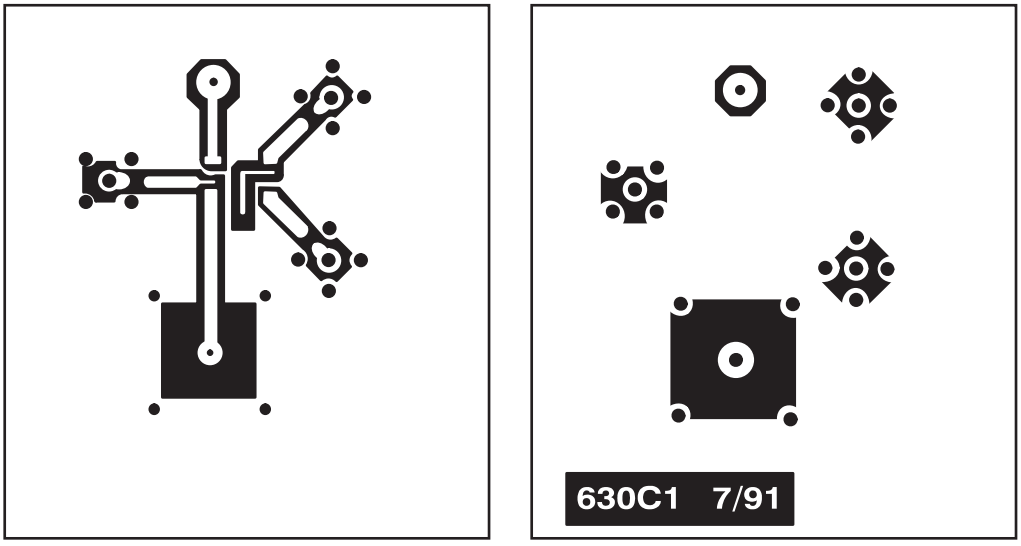
14. Application information

The typical application schematic and printed-circuit board layout of the SA630 evaluation board is shown in Figure 19. The layout of the board is simple, but a few cautions must be observed. The input and output traces should be 50 Ω. If a symmetric isolation between the two channels is desired, then the placement of the AC bypass capacitor is **extremely critical**. The trace from AC_GND (pin 7) should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical.

For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This arrangement also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 5 shows the frequency response of the SA630. The loss matching between the two channels is excellent to 1.2 GHz, as shown in Figure 7.



a. Evaluation board schematic



b. SA630 board layout

Fig 19. Evaluation board and layout

The isolation and matching of the two channels over frequency is shown in Figure 9 and Figure 10, respectively.

The SA630 is a very versatile part and can be used in many applications. Figure 20 shows a block diagram of a typical digital RF transceiver front-end. In this application, the SA630 replaces the duplexer, which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The SA630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figure 21 and Figure 22, respectively.

For applications that require a higher isolation at 1 GHz than obtained from a single SA630, several SA630s can be cascaded as shown in Figure 23. The cascaded configuration has a higher loss, but greater than 35 dB of isolation at 1 GHz and greater than 65 dB at 500 MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/demultiplexer or antenna selector can be constructed. The simplicity of SA630 coupled with its ease of use and high performance lends itself to many innovative applications.

The SA630 switch terminates the OFF channel in 50 Ω. The 50 Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50 Ω can be achieved by adding a resistor in series with the AC bypass capacitor (for example, 25 Ω additional to match to a 75 Ω environment).

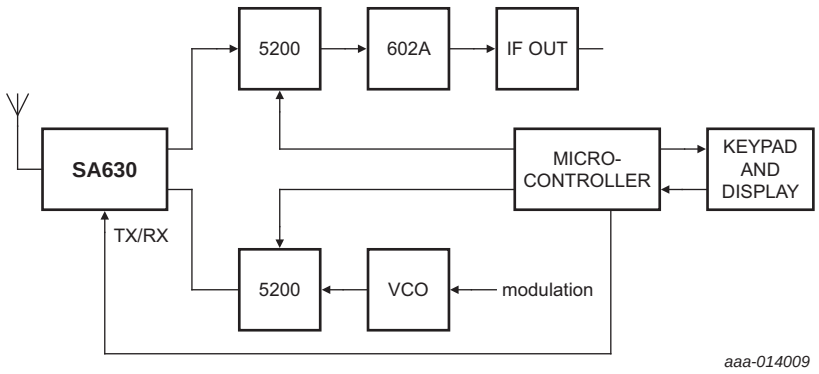


Fig 20. A typical TDMA/digital RF transceiver system front-end

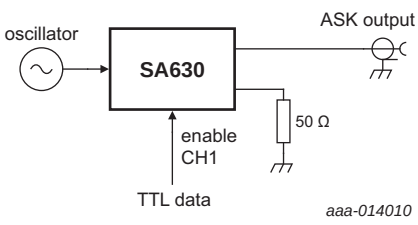


Fig 21. Amplitude Shift Keying (ASK) generator

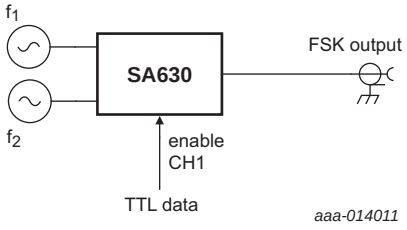


Fig 22. Frequency Shift Keying (FSK) generator

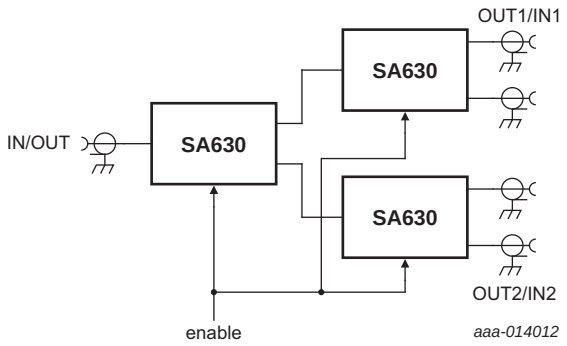
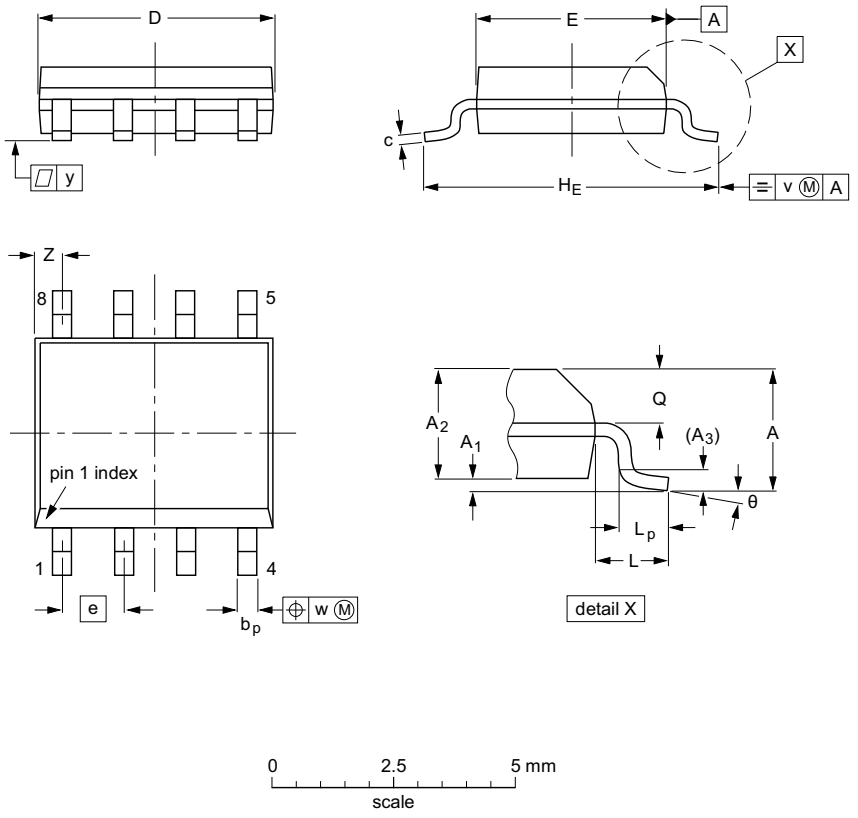


Fig 23. Cascaded configuration

15. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 24. Package outline SOT96-1 (SO8)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020D)

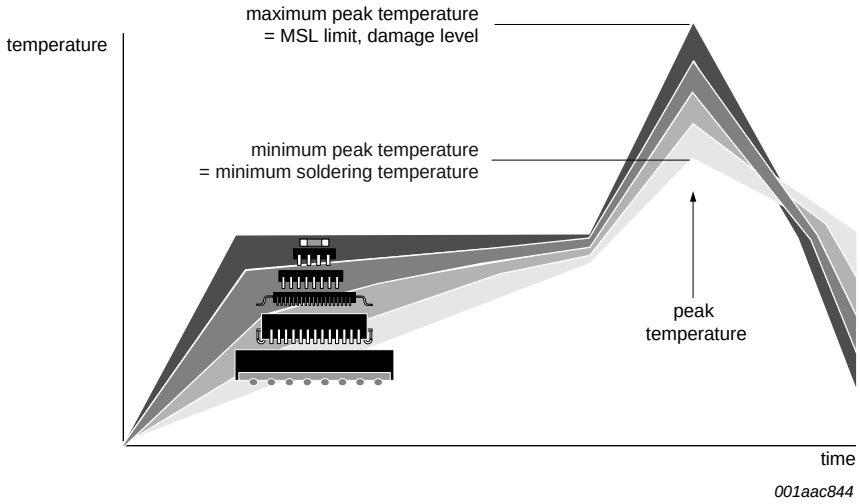
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Soldering: PCB footprints

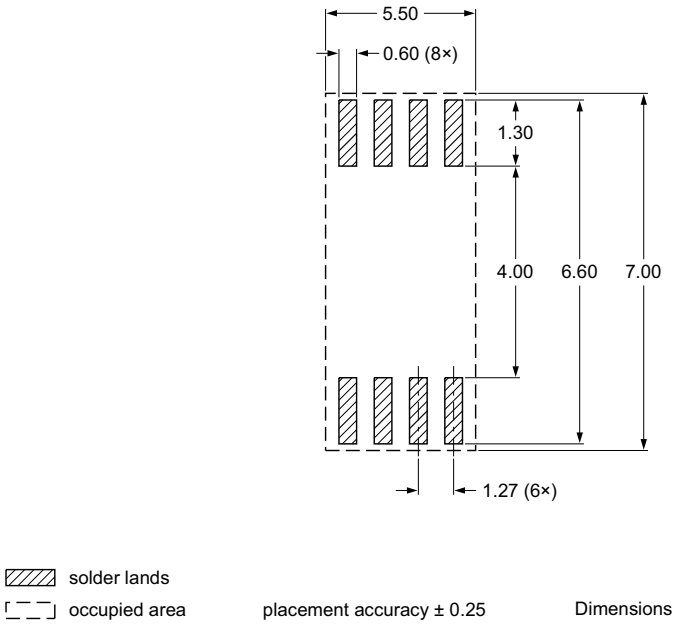


Fig 26. PCB footprint for SOT96-1; reflow soldering

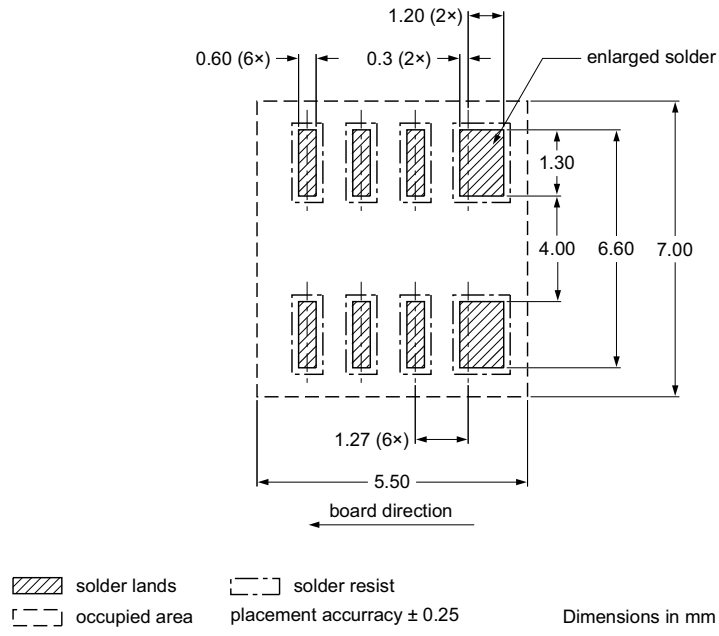


Fig 27. PCB footprint for SOT96-1; wave soldering

18. Abbreviations

Table 11. Abbreviations

Acronym	Description
ASK	Amplitude Shift Keying
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
FSK	Frequency Shift Keying
OOK	On-Off Keying
PCB	Printed-Circuit Board
PIN	Positive-doped/Intrinsic/Negative-doped diode
RF	Radio Frequency
SPDT	Single-Pole Double-Throw
TTL	Transistor-Transistor Logic

19. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA630 v.3	20140723	Product data sheet	-	SA630 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number SA630N is discontinued and removed from this data sheet • Type number SA630D is discontinued and removed from this data sheet • Type number SA630D/01 is added to this data sheet • Added Section 4.1 “Ordering options” • Added Section 6.2 “Pin description” • Added Section 10 “Thermal characteristics” • Deleted (old) “AC ELECTRICAL CHARACTERISTICS - N PACKAGE” • Deleted (old) Figure 4c, “630 N-Package Board Layout” • Deleted (old) Figure 12, “Loss Matching vs. Frequency for N-Package (DIP)” • Deleted (old) Figure 16, “Isolation Matching vs. Frequency for N-Package (DIP)” • Deleted (old) package outline drawing SOT97-1 (DIP8) • Added Section 16 “Soldering of SMD packages” • Added Section 17 “Soldering: PCB footprints” • Added Section 18 “Abbreviations”			
SA630 v.2	19971107	Product specification	ECN 853-1577 18666	NE/SA630 v.1
NE/SA630 v.1	19911010	Product specification	ECN 853-1577 04269	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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