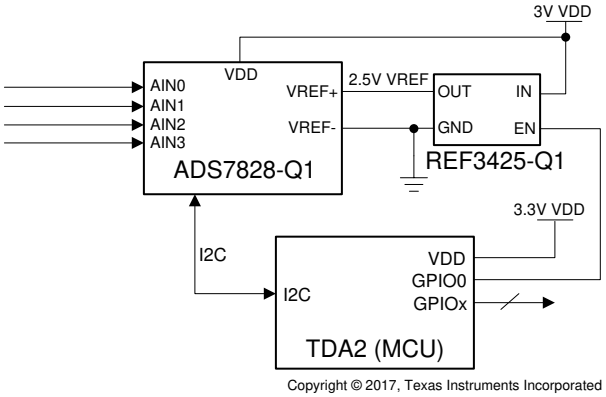
REF34-Q1 Low-Drift, Low-Power, Small-Footprint Series Voltage References

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- Initial accuracy: ±0.05% (maximum)
- Temperature coefficient : 6 ppm/°C (maximum)
- Operating temperature range: −40°C to +125°C
- Output voltage options: 2.5V, 3.0V, 3.3V, 4.096V, 5.0V
- Output current: ±10 mA
- Low quiescent current: 95 µA (maximum)
- Low shutdown mode current: 3 µA (maximum)
- Wide input voltage: 12 V
- Output 1/f noise (0.1 Hz to 10 Hz): 3.8 μV_{PP}/V
- Excellent long-term stability 25 ppm/1000 hrs
- Available in 6-pin and 5-Pin SOT-23 package and 8-pin MSOP package

2 Applications

- Body control modules
- On board chargers
- Traction inverters
- Battery management systems
- Advanced driver assistance systems



Simplified Schematic

3 Description

The REF34-Q1 devices are low-temperature-drift (6 ppm/°C), low-power, high-precision CMOS voltage references. The devices have ±0.05% initial accuracy and low operating current with power consumption less than 95 µA. These devices also offer very low output noise of 3.8 μV_{PP}/V, which enable the devices to maintain high signal integrity with high-resolution data converters and noise critical systems.

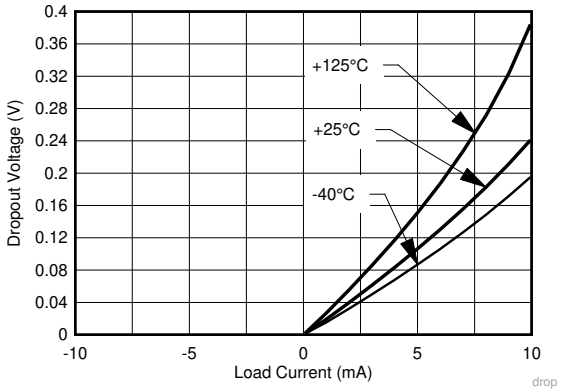
Stability and system reliability are further improved by the low output-voltage hysteresis of these devices and low long-term output voltage drift. Furthermore, the small size and low operating current of the devices (95 µA) make them an excellent choise for battery-powered applications. The REF34-Q1 features an enable pin that can set the device into shutdown where it consumes a low stand by current (3 µA) to help with overall system power during standby.

The REF34-Q1 family is specified for the wide temperature range of −40°C to +125°C. Contact the TI sales representative for additional voltage options.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
REF34xx-Q1	SOT-23 (6)	2.90 mm × 1.60 mm
REF34xxS-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
REF34xx-Q1	VSSOP (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Dropout vs Current Load Over Temperature

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2020) to Revision C (October 2020)	Page
• Added information for REF34-Q1 DGK Package	3
• Added information for REF34xx-Q1 DGK package pin functions	3

Changes from Revision A (September 2018) to Revision B (August 2020)	Page
• Added information for REF34xxS-Q1	3
• Added information for REF34xxS-Q1	3

Changes from Revision * (July 2018) to Revision A (September 2018)	Page
• Changed Advance Information to Production Data	1

5 Device Comparison Table

PRODUCT(1)		V_{OUT}
REF3425-Q1	REF3425S-Q1	2.5 V
REF3430-Q1	REF3430S-Q1	3.0 V
REF3433-Q1	REF3433S-Q1	3.3 V
REF3440-Q1	REF3440S-Q1	4.096 V
REF3450-Q1	REF3450S-Q1	5.0 V

(1) For full orderable part number please refer to Section 15.

6 Pin Configuration and Functions

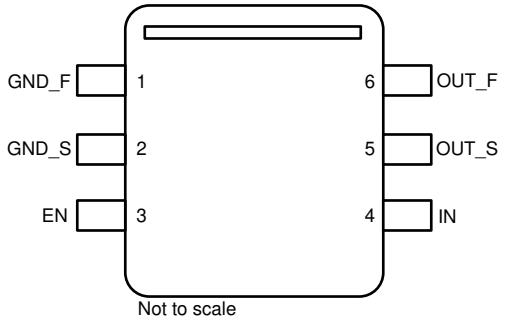


Figure 6-1. DBV Package 6-Pin SOT-23 (Top View)

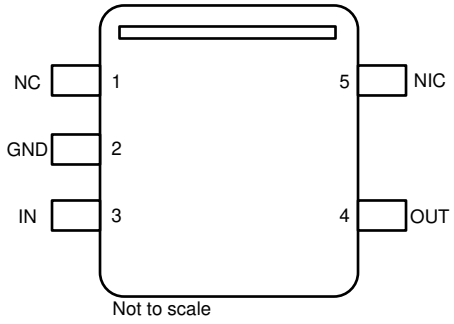


Figure 6-2. DBV Package 5-Pin SOT-23 (Top View)

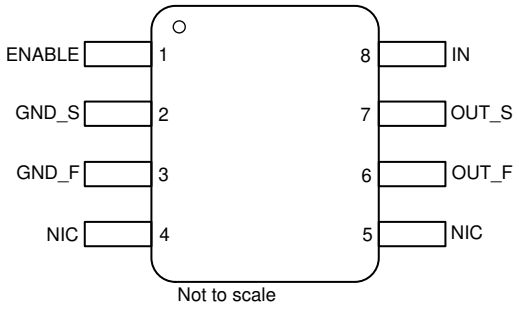


Figure 6-3. DGK Package 8-Pin VSSOP (Top View)

6.1 Pin Functions

PIN				TYPE	DESCRIPTION
NAME	REF34xx-Q1 (DBV)	REF34xxS-Q1 (DBV)	REF34xx-Q1 (DGK)		
GND_F	1	-	3	Ground	Ground force connection
GND_S	2	-	2	Ground	Ground sense connection
GND	-	2	-	Ground	Ground connection
ENABLE	3	-	1	Input	Enable connection. Enables or disables the device.
IN	4	3	8	Power	Input supply voltage connection
OUT_S	5	-	7	Output	Reference voltage output sense connection
OUT_F	6	-	6	Output	Reference voltage output force connection
OUT	-	4	-	Output	Reference voltage output connection
NC	-	1	-	-	Test pin, connect from 0V to 18V
NIC	-	5	4,5	-	No internal connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	13	V
	EN	–0.3	IN + 0.3	V
Output voltage	V_{OUT}	–0.3	5.5	V
Output short circuit current			20	mA
Operating temperature range, T_A		–55	150	°C
Storage temperature range, T_{stg}		–65	170	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Input Voltage	V_{OUT} + V_{DO} (1)		12	V
EN	Enable Voltage	0		IN	V
I_L	Output Current	–10		10	mA
T_A	Operating Temperature	–40	25	125	°C

(1) V_{DO} = Dropout voltage

7.4 Thermal Information

THERMAL METRIC(1)		REF34-Q1			UNIT
		DBV	DBV	DGK	
		5 PINS	6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.6	122.6	174.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.2	80.2	61.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42	42	95.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23.2	23.2	8.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.9	41.9	93.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At V_{IN} = V_{OUT} + V_{DO}, C_{OUT} = 10 µF, C_{IN} = 0.1 µF, I_L = 0 mA, minimum and maximum specifications at T_A = –40°C to 125°C; Typical specifications at T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.05		0.05	%
	Output voltage temperature coefficient (1)				2.5	6	ppm/°C
LINE & LOAD REGULATION							
$\Delta V_O/\Delta V_{IN}$	Line Regulation	V_{IN} = V_{OUT} + V_{DO} (2) to 12 V			2		ppm/V
		V_{IN} = V_{OUT} + V_{DO} (2) to 12 V				15	
$\Delta V_O/\Delta I_L$	Load Regulation	I_L = 0 mA to 10mA, V_{IN} = V_{OUT}+ V_{DO} (3)	Sourcing		20		ppm/mA
			Sourcing			30	
		I_L = 0 mA to –10mA, V_{IN} = V_{OUT}+ V_{DO} (3)	Sinking, REF3425-Q1		40		
			Sinking, REF3430-Q1		43		
			Sinking, REF3433-Q1		48		
			Sinking, REF3440-Q1		60		
			Sinking, REF3450-Q1		70		
			Sinking, REF3425-Q1			70	
			Sinking, REF3430-Q1			75	
			Sinking, REF3433-Q1			84	
			Sinking, REF3440-Q1			98	
			Sinking, REF3450-Q1			140	
NOISE							
e_{np-p}	Low frequency noise (4)	0.1Hz ≤ f ≤ 10Hz			5		µV p–p/V
		0.1Hz ≤ f ≤ 10Hz (REF3440–Q1 and REF3450–Q1)			3.8		
e_n	Integrated wide band noise	10Hz ≤ f ≤ 10kHz			24		µVrms
e_n	Output voltage noise density	f = 1kHz			0.25		ppm/√Hz
		f = 1kHz (REF3440–Q1 and REF3450–Q1)			0.2		
LONG TERM STABILITY AND HYSTERESIS							
	Long-term stability (5)	DBV Package	0 to 1000h at 35°C		25		ppm
			1000h to 2000h at 35°C		10		
	Long-term stability (5)	DGK Package	0 to 1000h at 35°C		17		
	Output voltage thermal hysteresis (6)	DBV Package	25°C, –40°C,125°C, 25°C Cycle 1		30		ppm
			25°C, –40°C,125°C, 25°C Cycle 2		10		
		DGK Package	25°C, –40°C,125°C, 25°C Cycle 1		20		
			25°C, –40°C,125°C, 25°C Cycle 2		10		
TURN-ON TIME							
t_{ON}	Turn-on time	0.1% of output voltage settling, C_L = 10 µF, REF3425–Q1			2.5		ms
CAPACITIVE LOAD							
C_L	Stable output capacitor range			0.1		10	µF

At V_{IN} = V_{OUT} + V_{DO}, C_{OUT} = 10 µF, C_{IN} = 0.1 µF, I_L = 0 mA, minimum and maximum specifications at T_A = –40°C to 125°C; Typical specifications at T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE						
V_{OUT}	Output voltage	REF3425Q1		2.5		V
		REF3430Q1		3.0		
		REF3433Q1		3.3		
		REF3440Q1		4.096		
		REF3450Q1		5.0		
POWER SUPPLY						
V_{IN}	Input voltage		V_{OUT} + V_{DO}		12	V
I_L	Output current capacity	V_{IN} = V_{OUT} + V_{DO} to 12 V	–10		10	mA
I_Q	Quiescent current	Active mode		72	95	µA
		Shutdown mode (7)		2.5	3	
V_{DO}	Dropout voltage	I_L = 0 mA		50		mV
		I_L = 0 mA			100	
		I_L = 10 mA			500	
V_{EN}	ENABLE pin voltage (7)	Voltage reference in active mode (EN = 1)	1.6			V
		Voltage reference in shutdown mode (EN = 0)			0.5	
I_{EN}	ENABLE pin leakage current (7)	V_{EN} = V_{IN} = 12V		1	2	µA
I_{SC}	Short circuit current	V_{OUT} = 0 V at T_A = 25°C		18	22	mA

(1) Temperature drift is specified according to the box method. See Low Temperature Drift section for more details.
(2) V_{DO} for line regulation test is 50 mV.
(3) V_{DO} for load regulation test is 500 mV.
(4) The peak-to-peak noise measurement is explained in more detail in section Noise Performance.
(5) Long-term stability measurement procedure is explained in more detail in section Long–Term Stability.
(6) Thermal hysteresis measurement procedure is explained in more detail in section Thermal Hysteresis.
(7) Not applicable for REF34S device (DBV - 5 pin package)

8 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

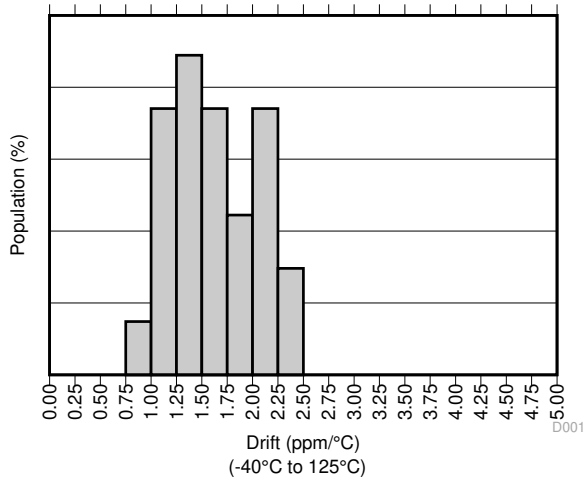


Figure 8-1. Temperature Drift

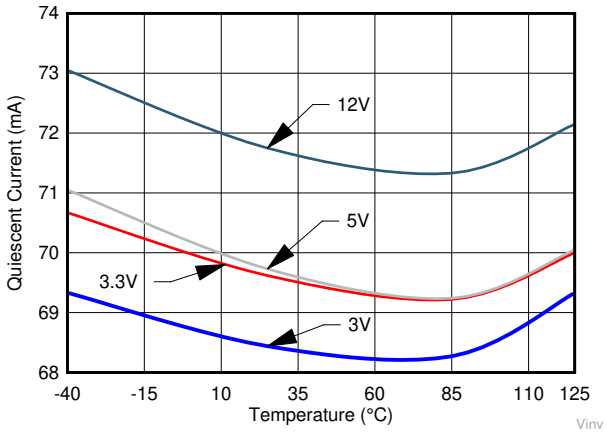


Figure 8-2. V_{IN} vs I_Q Over Temperature

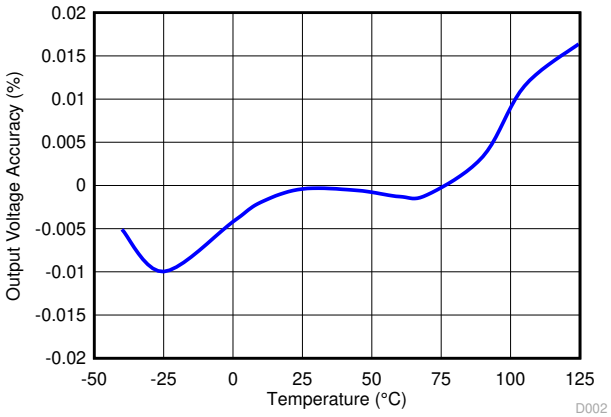


Figure 8-3. Output Voltage Accuracy vs Temperature

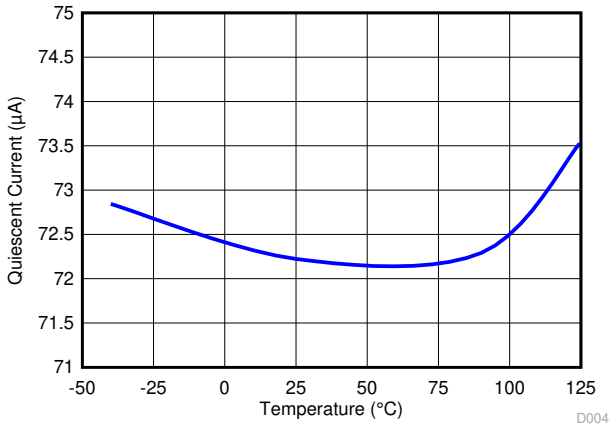


Figure 8-4. Quiescent Current vs Temperature

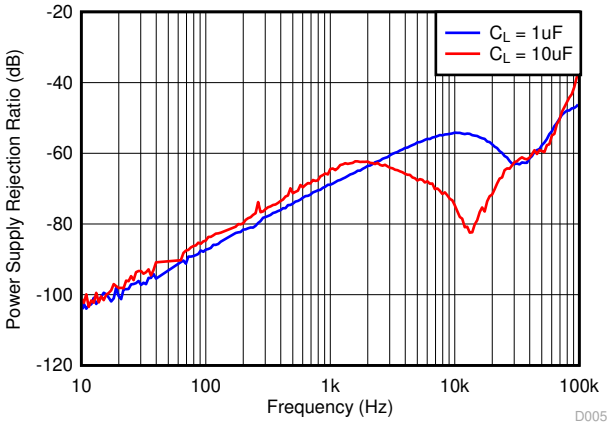


Figure 8-5. Power-Supply Rejection Ratio vs Frequency

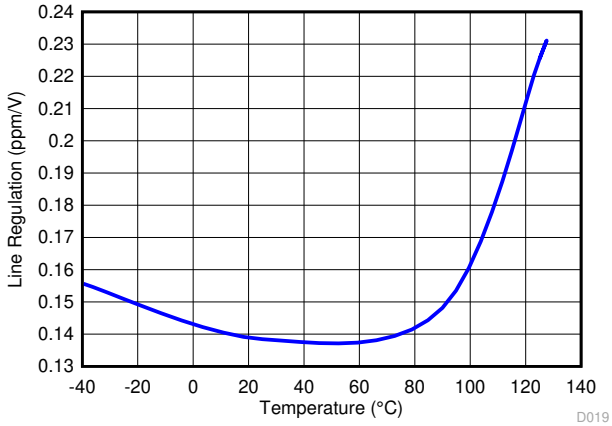


Figure 8-6. Line Regulation

8 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

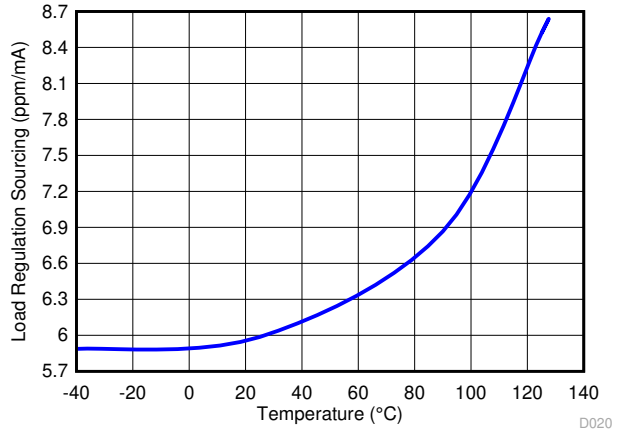


Figure 8-7. Load Regulation Sourcing

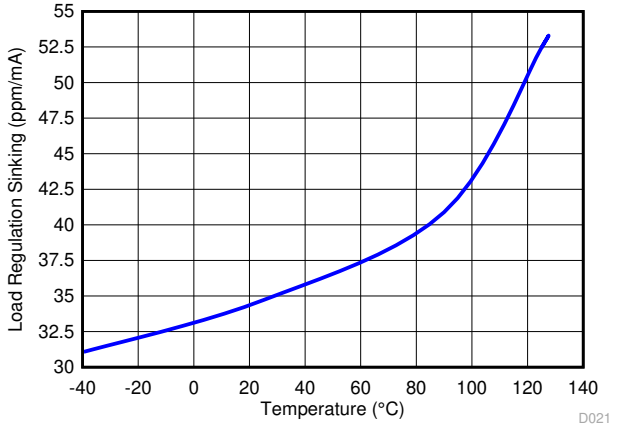


Figure 8-8. Load Regulation Sinking

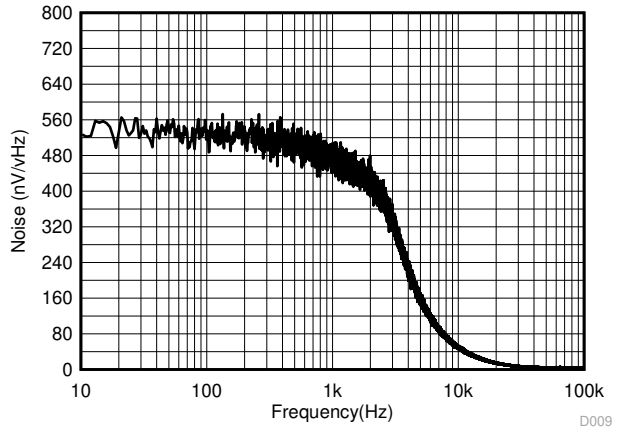


Figure 8-9. Noise Performance 10 Hz to 10 kHz

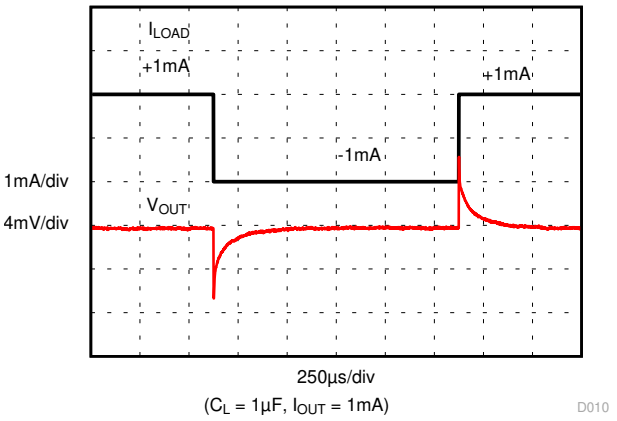


Figure 8-10. Load Transient

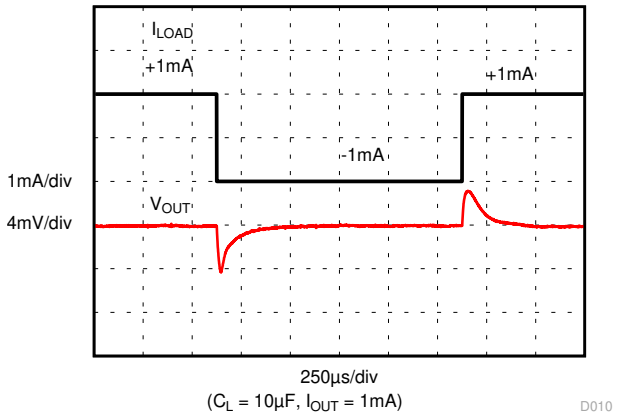


Figure 8-11. Load Transient

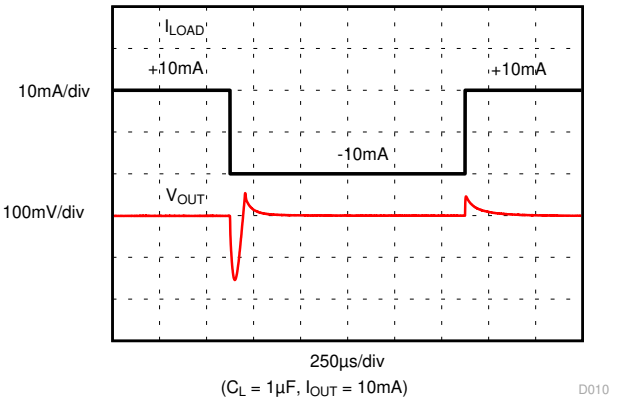


Figure 8-12. Load Transient

8 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

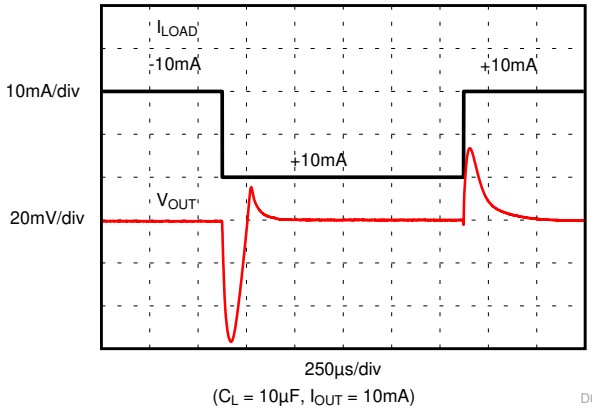


Figure 8-13. Load Transient

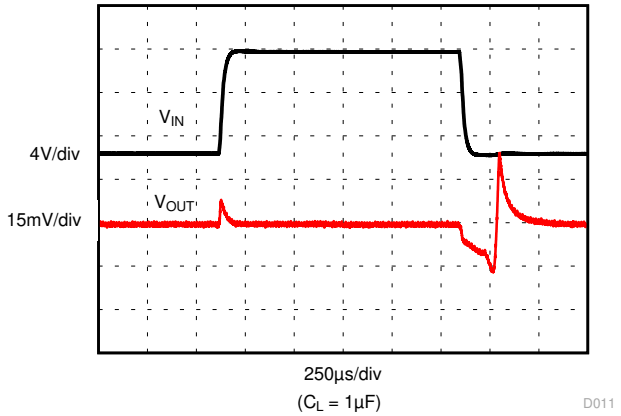


Figure 8-14. Line Transient

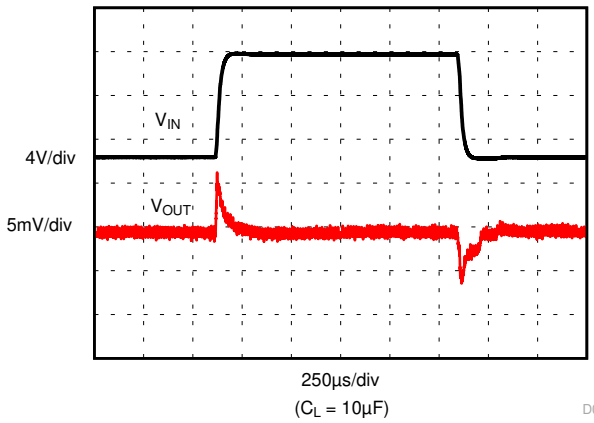


Figure 8-15. Line Transient

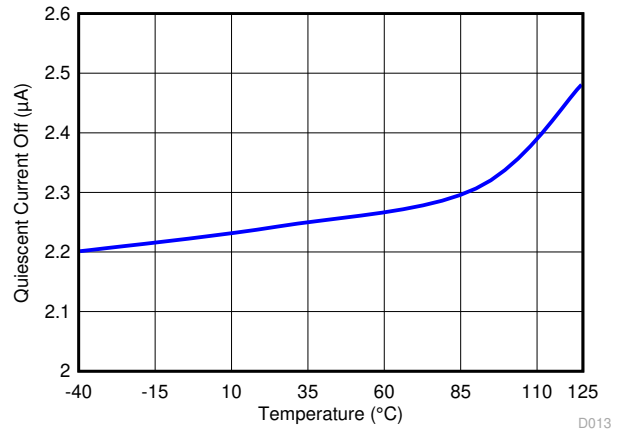


Figure 8-16. Quiescent Current Shutdown Mode

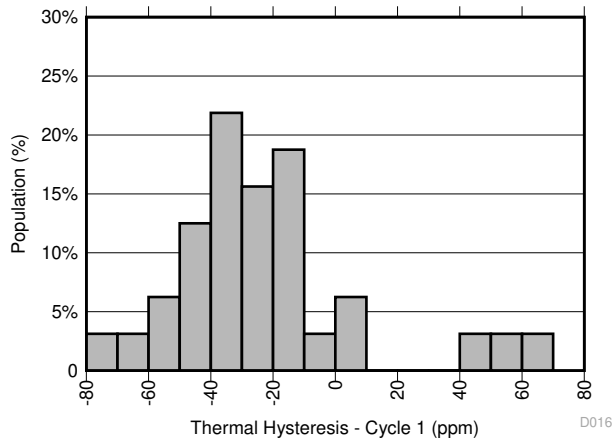


Figure 8-17. Thermal Hysteresis Distribution (Cycle 1) - DBV Package

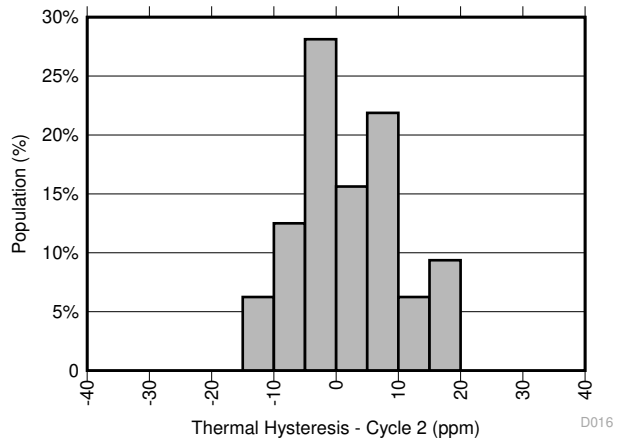


Figure 8-18. Thermal Hysteresis Distribution (Cycle 2) - DBV Package

8 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

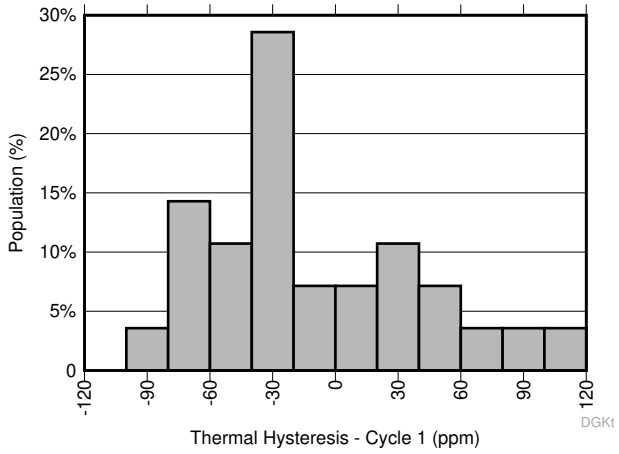


Figure 8-19. Thermal Hysteresis Distribution (Cycle 1) - DGK Package

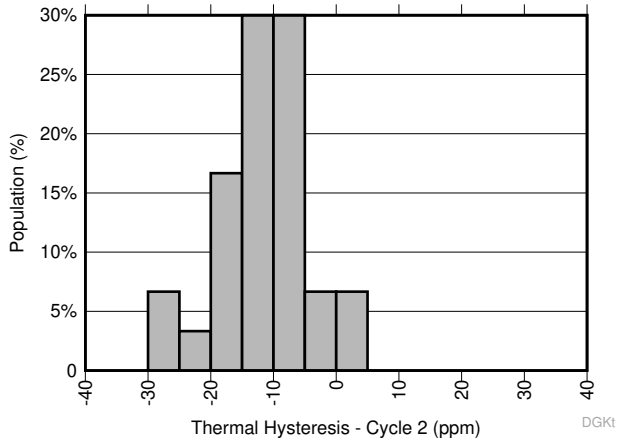


Figure 8-20. Thermal Hysteresis Distribution (Cycle 2) - DGK Package

Refer to *Section 9.1* for more information

Figure 8-21. Solder Heat Shift Distribution - DBV Package

Refer to *Section 9.1* for more information

Figure 8-22. Solder Heat Shift Distribution - DGK Package

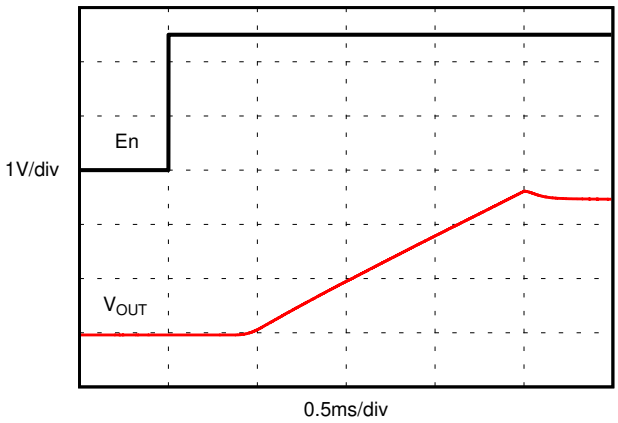


Figure 8-23. Turnon Time (Enable)

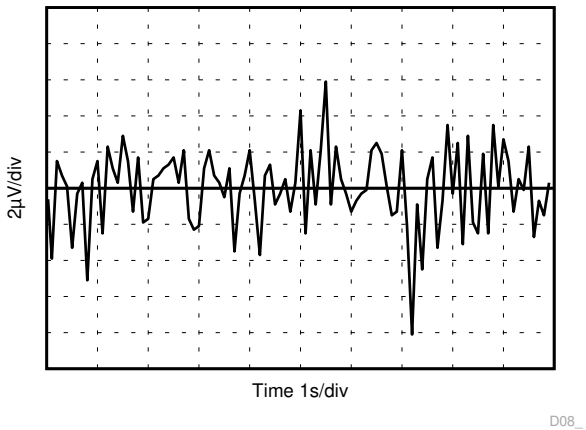


Figure 8-24. 0.1-Hz to 10-Hz Noise (V_{REF})

8 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

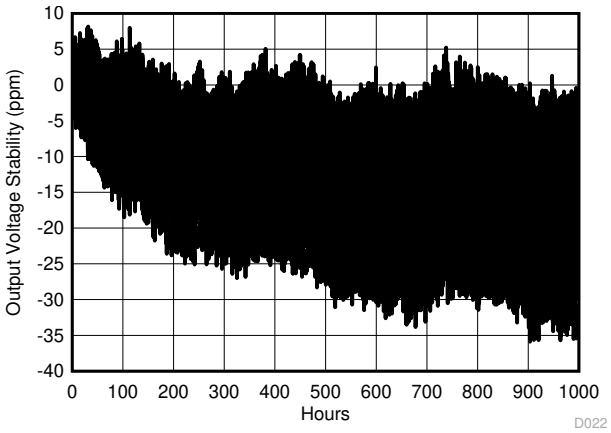


Figure 8-25. Long Term Stability - 1000 hours (V_{REF}) - DBV Package

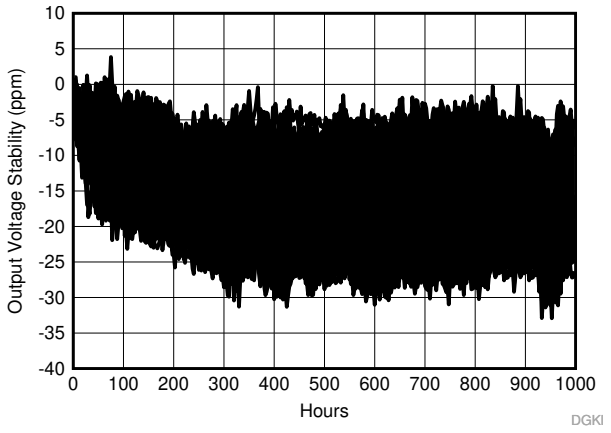


Figure 8-26. Long Term Stability - 1000 hours (V_{REF}) - DGK Package

9 Parameter Measurement Information

9.1 Solder Heat Shift

The materials used in the manufacture of the REF34-Q1 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 32 devices were soldered on four printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 9-1. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm. All measurements were taken after baking at 150°C.

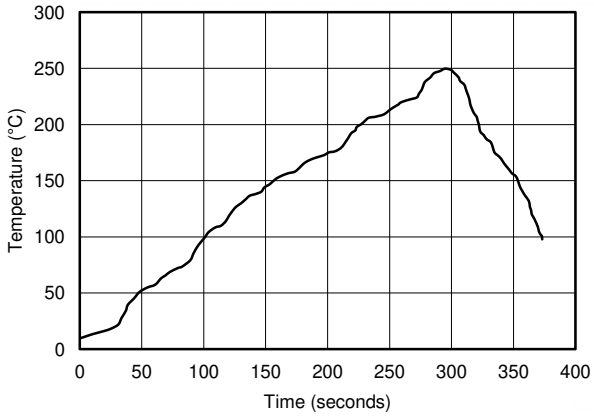


Figure 9-1. Reflow Profile

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in Figure 9-2. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the second pass to minimize its exposure to thermal stress.

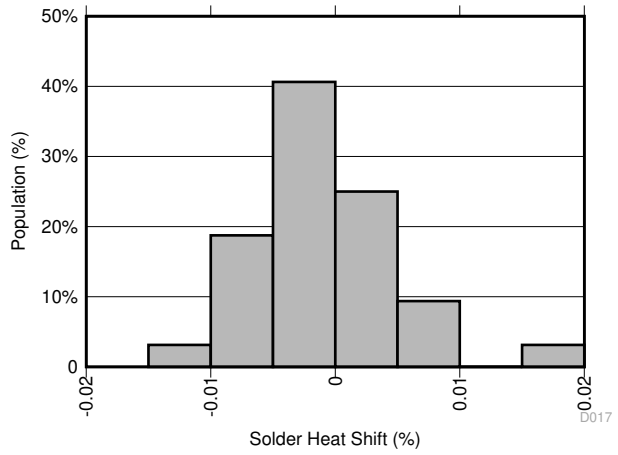


Figure 9-2. Solder Heat Shift Distribution, V_{REF} (%) - DBV Package

Figure 9-3. Solder Heat Shift Distribution, V_{REF} (%) - DGK Package

9.2 Long-Term Stability

One of the key parameters of the REF34-Q1 references is long-term stability. Typical characteristic expressed as: curves shows the typical drift value for the REF34-Q1 is 25 ppm from 0 to 1000 hours. This parameter is characterized by measuring 32 units at regular intervals for a period of 1000 hours. It is important to understand that long-term stability is not ensured by design and that the output from the device may shift beyond the typical 25 ppm specification at any time. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time

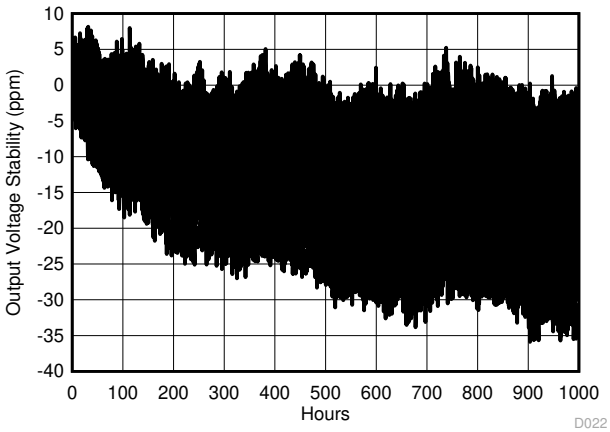


Figure 9-4. Long Term Stability - 1000 hours (V_{REF}) - DBV Package

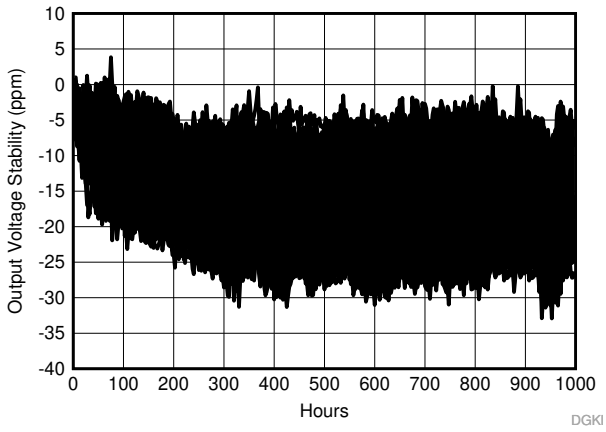


Figure 9-5. Long Term Stability - 1000 hours (V_{REF}) - DGK Package

9.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF34-Q1 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by Equation 1:

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C.

Typical thermal hysteresis distribution is as shown in Figure 9-6.

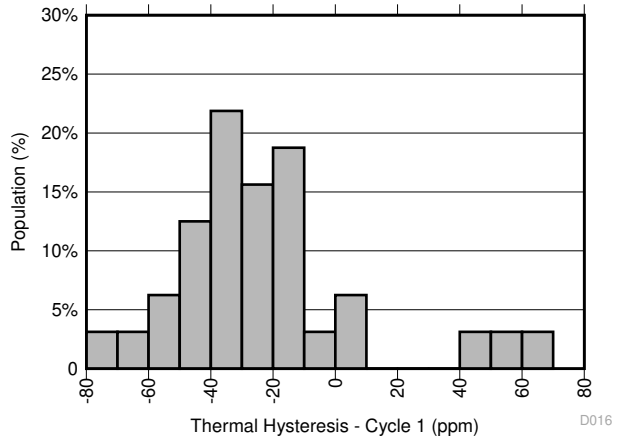


Figure 9-6. Thermal Hysteresis Distribution (V_{REF}) - DBV Package (Cycle 1)

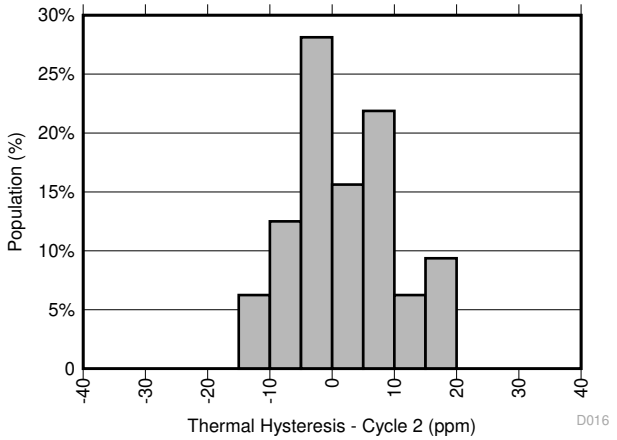


Figure 9-7. Thermal Hysteresis Distribution (V_{REF}) - DBV Package (Cycle 2)

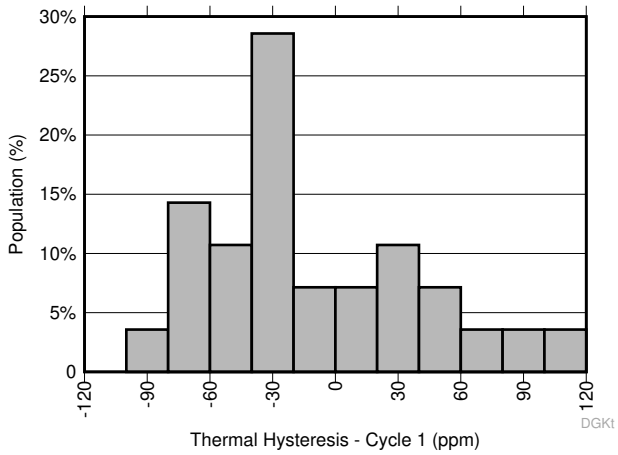


Figure 9-8. Thermal Hysteresis Distribution (V_{REF}) - DGK Package (Cycle 1)

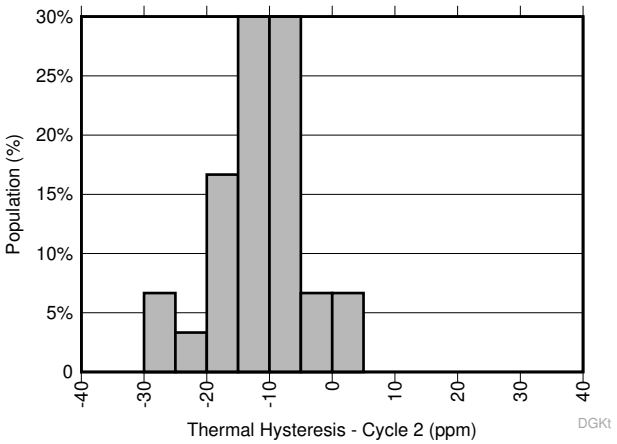


Figure 9-9. Thermal Hysteresis Distribution (V_{REF}) - DGK Package (Cycle 2)

9.4 Power Dissipation

The REF34-Q1 voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with Equation 2:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (2)$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

9.5 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in Figure 9-10 . Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in Figure 9-10.

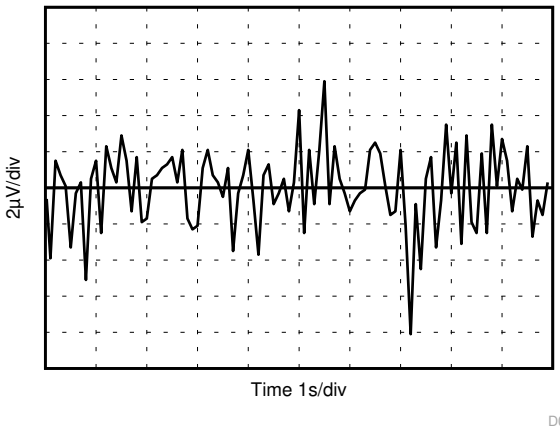


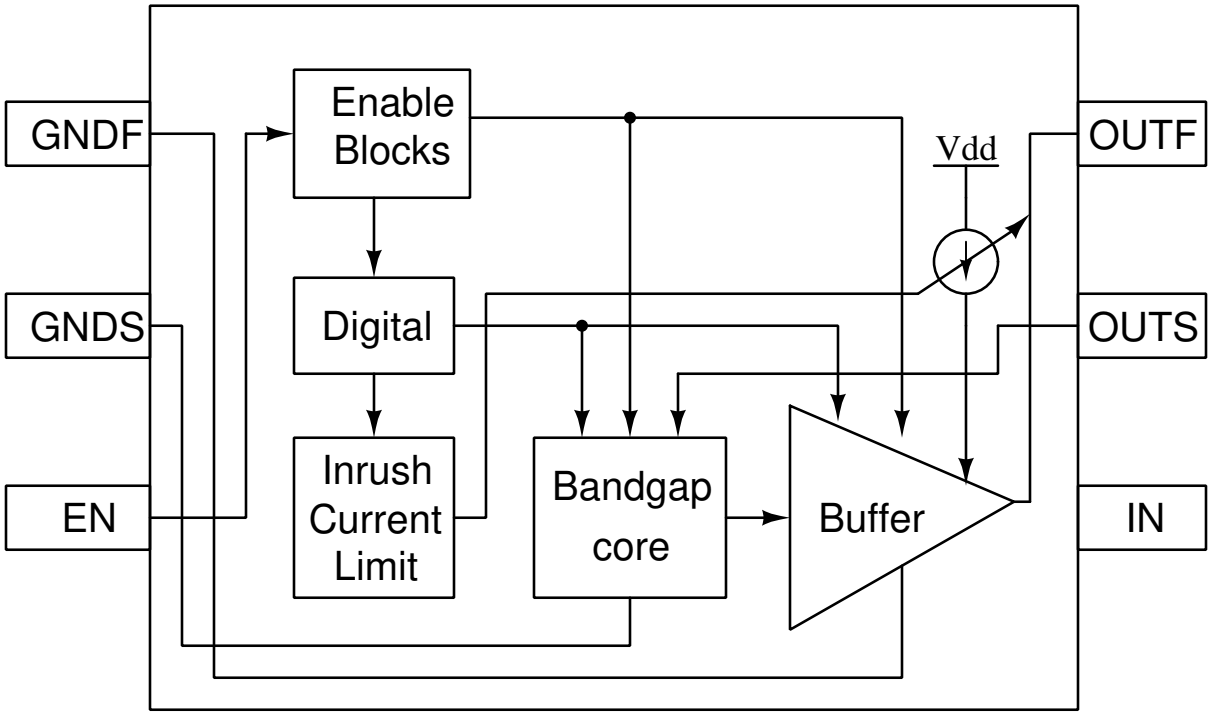
Figure 9-10. 0.1-Hz to 10-Hz Noise (V_{REF})

10 Detailed Description

10.1 Overview

The REF34-Q1 devices are a family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The *Section 10.2* is a simplified block diagram of the REF34-Q1 showing basic band-gap topology.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Supply Voltage

The REF34-Q1 family of references features an extremely low dropout voltage. For loaded conditions, a typical dropout voltage versus load is shown on the front page. The REF34-Q1 family features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 72 µA, and the maximum quiescent current over temperature is just 95 µA. Supply voltages below the specified levels can cause the REF34-Q1 to momentarily draw currents greater than the typical quiescent current. Use a power supply with a fast rising edge and low output impedance to easily prevent this issue.

10.3.2 Low Temperature Drift

The REF34-Q1 devices are designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 3:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \times \text{Temperature Range}} \right) \times 10^6 \quad (3)$$

10.3.3 Load Current

The REF34-Q1 family is specified to deliver a current load of ±10 mA per output. The V_{REF} output of the device are protected from short circuits by limiting the output short-circuit current to 18 mA. The device temperature increases according to Equation 4:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (4)$$

where

- T_J = junction temperature (°C),
- T_A = ambient temperature (°C),
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF34-Q1 maximum junction temperature must not exceed the absolute maximum rating of 150°C.

10.4 Device Functional Modes

10.4.1 EN Pin

When the EN pin of the REF34-Q1 is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF34-Q1 can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 2 µA in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See Thermal Information for logic high and logic low voltage levels.

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

As the REF34-Q1 devices have many applications and setups, there are many situations that this data sheet can not characterize in detail. Basic applications includes positive/negative voltage reference and data acquisition systems.

Table 11-1. Typical Applications and Companion ADC/DAC

APPLICATIONS	ADC/DAC/CONTROLLER
ADAS	ADS7828-Q1
HEV/EV	ADS7951-Q1, ADS1120-Q1, ADS1258, BQ76PL455A-Q1

11.2 Typical Applications

11.2.1 Basic Voltage Reference Connection

The circuit shown in Figure 11-1 shows the basic configuration for the REF34-Q1 references. Connect bypass capacitors according to the guidelines in *Section 11.2.1.2.1*.

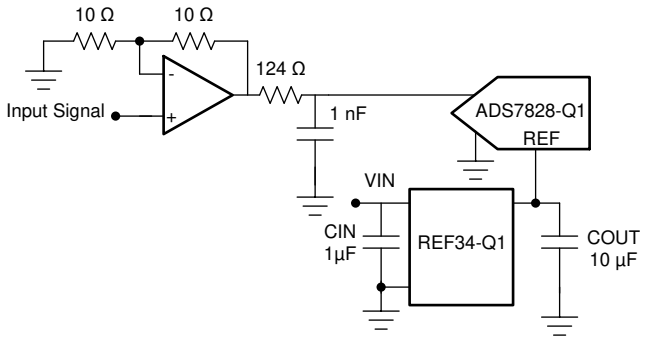


Figure 11-1. Basic Reference Connection

11.2.1.1 Design Requirements

A detailed design procedure is based on a design example. For this design example, use the parameters listed in Table 11-2 as the input parameters.

Table 11-2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	12 V
Output voltage V_{OUT}	5 V
REF3450-Q1 input capacitor	1 µF
REF3450-Q1 output capacitor	10 µF

11.2.1.2 Detailed Design Procedure

11.2.1.2.1 Input and Output Capacitors

A 1-µF to 10-µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1-µF ceramic capacitor in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least a 0.1 µF must be connected to the output to improve stability and help filter out high frequency noise. An additional 1-µF to 10-µF electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the turnon time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1-µF ceramic capacitor in parallel to reduce overall ESR on the output.

11.2.1.2.2 4-Wire Kelvin Connections

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this drop can reach several millivolts or more, introducing a considerable error into the output voltage of the reference. A 1-inch long, 5-millimeter wide trace of 1-ounce copper has a resistance of approximately 100 mΩ at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error. In an ideal board layout, the reference must be mounted as close as possible to the load to minimize the length of the output traces, and, therefore, the error introduced by voltage drop. However, in applications where this is not possible or convenient, force and sense connections (sometimes referred to as Kelvin sensing connections) are provided as a means of minimizing the IR drop and improving accuracy.

Kelvin connections work by providing a set of high impedance voltage-sensing lines to the output and ground nodes. Because very little current flows through these connections, the IR drop across their traces is negligible, and the output and ground.

It is always advantageous to use Kelvin connections whenever possible. However, in applications where the IR drop is negligible or an extra set of traces cannot be routed to the load, the force and sense pins for both V_{OUT} and GND can simply be tied together, and the device can be used in the same fashion as a normal 3-terminal reference (as shown in Figure 9-6).

11.2.1.2.3 V_{IN} Slew Rate Considerations

In applications with slow-rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

To avoid such conditions, ensure that the input voltage wave-form has both a rising and falling slew rate close to 6 V/ms.

11.2.1.2.4 Shutdown/Enable Feature

The REF34-Q1 references can be switched to a low power shut-down mode when a voltage of 0.5 V or lower is input to the ENABLE pin. Likewise, the reference becomes operational for ENABLE voltages of 1.6 V or higher. During shutdown, the supply current drops to less than 2 µA, useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the ENABLE pin voltage does not fall between 0.5 V and 1.6 V because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly. If not using the shutdown feature, however, the ENABLE pin can simply be tied to the IN pin, and the reference remains operational continuously.

11.2.1.3 Application Curves

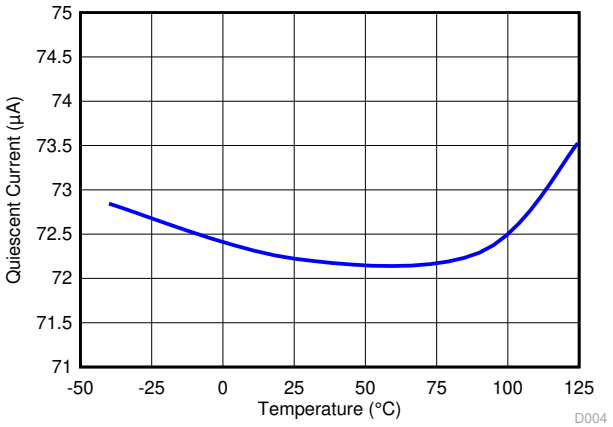


Figure 11-2. Quiescent Current vs Temperature

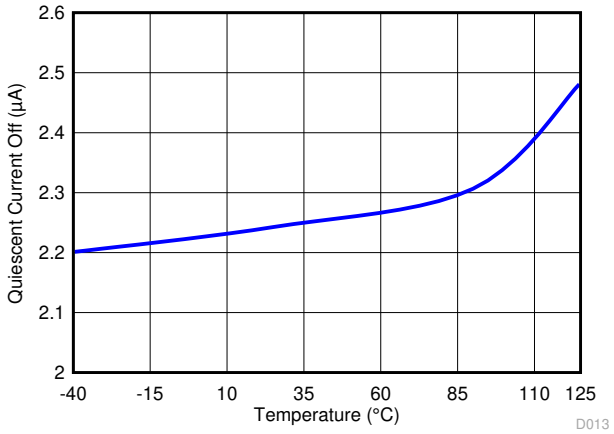


Figure 11-3. Quiescent Current Shutdown Mode

11.2.2 Advanced Driver Assistance Systems (ADAS) Microcontroller Connection

11.2.2.1 Basic Voltage Reference Connection

The circuit shown in Figure 11-4 shows the basic configuration for the REF34-Q1 references.

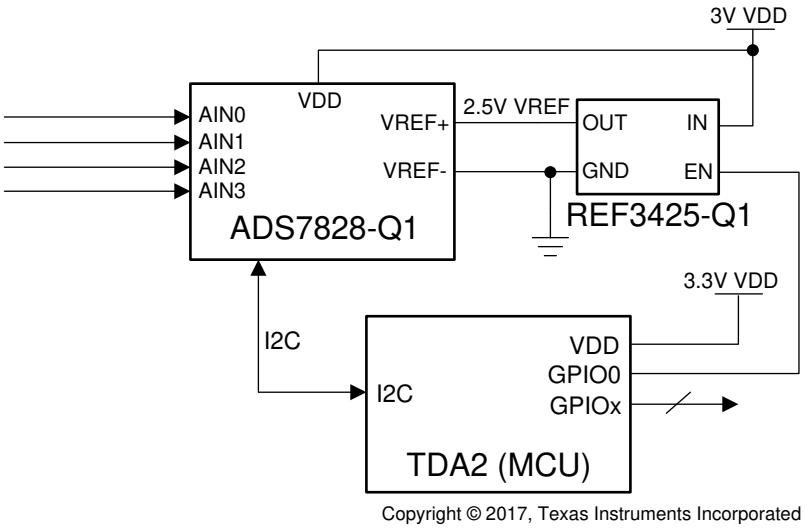


Figure 11-4. ADAS Microcontroller Application

11.2.2.2 Design Requirements

In ADAS applications it is common to use an ADC with a MCU to monitor the voltage rails to the MCU/DSP/FPGAs. In figure Figure 11-4 the automotive TI Jacinto™ TDA2 MCU is using a ADS7828-Q1 to monitor several analog input signals and in ADAS these signals will be the system power rails. It is important to monitor these power rails because tighter rail requirements allow for further system monitoring and optimization. The REF3425-Q1 is used in this application to provide the precise voltage reference signal. In these systems it is not typical to have calibration and such the most precise low power voltage reference is necessary to be able to measure down to 1% accuracy on key power rails.

For this design example, use the parameters listed in Table 11-3 as the input parameters and desired output parameters.

Table 11-3. Typical Core Voltage Rail Monitoring

SPECIFICATION	REQUIREMENT
Input Voltage V_{IN}	3V
Output Voltage	2.5V
Voltage Power Rail	1V
Max Error on Voltage Power Rail	1%
Temperature Range	-40°C to 125°C

11.2.2.3 Detailed Design Procedure

It is important to keep track of the error margin in this system to make sure that the total error of the voltage reference and ADC are less than the maximum 1% error allowed. To calculate the total RSS error of a voltage reference use Equation 5.

$$\text{Error}_{\text{VREF}}\big|_{\text{Total}} = \sqrt{(\text{Accuracy})^2 + (\text{TempCo})^2 + (\text{TempHyst})^2 + (\text{Long Term Drift})^2 + (1/f\ \text{Noise})^2} \quad (5)$$

With the RSS error of the voltage reference, the ADC error needs also needs to be calculated using the RSS method as seen in Equation 6. Equation 7 can then be used to sum both errors. It is important to make sure that only the applicable voltage reference error in relation to the measured signal is used.

$$\text{Total Unadjusted Error} = \text{Error}_{\text{ADC}}\big|_{\text{Total}} = \sqrt{(\text{Gain Error})^2 + (\text{Offset Error})^2 + (\text{INL Error})^2 + (\text{DNL Error})^2} \quad (6)$$

$$\text{Error}_{\text{VREF+ADC}}\big|_{\text{Total}} = \sqrt{\left(\text{Error}_{\text{VREF@AIN}}\big|_{\text{Total}}\right)^2 + \left(\text{Error}_{\text{ADC}}\big|_{\text{Total}}\right)^2} \quad (7)$$

11.2.2.4 Enable Feature in ADAS

In ADAS applications it is important to have a low quiescent current when the automotive application does not require the ADAS system to be in use. This creates a need for a low standby power so the battery life is preserved but there is also need for the system to still be readily available to start-up with minimal delays. In such situations the MCU and other systems will go into a standby mode to ensure that the power consumption is lowered to the absolute minimum. The REF3425-Q1 offers an enable pin that can be controlled by the MCU to activate shutdown mode with causes the REF3425-Q1 to go into stand by and consume 3 µA (maximum) and allow for a longer battery life.

12 Power Supply Recommendations

The REF34-Q1 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

13 Layout

13.1 Layout Guidelines

Figure 13-1 illustrates an example of a PCB layout for a data acquisition system using the REF34-Q1. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at V_{IN}, V_{REF} of the REF34-Q1.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

13.2 Layout Example

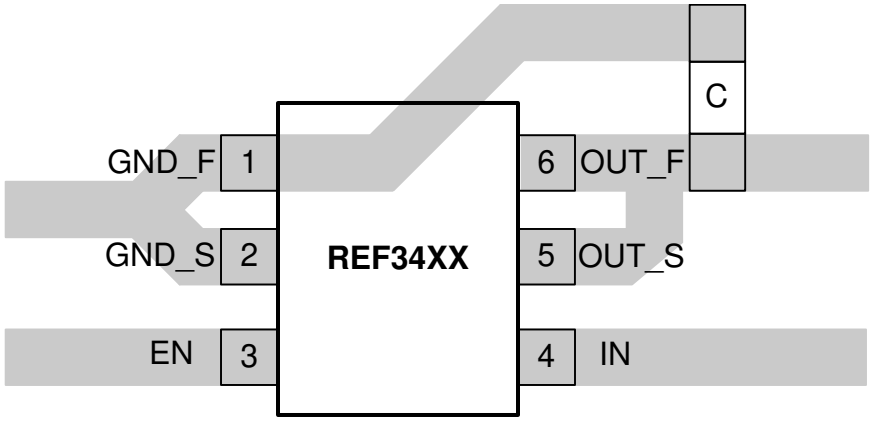


Figure 13-1. Layout Example (REF34xx-Q1 DBV Package)

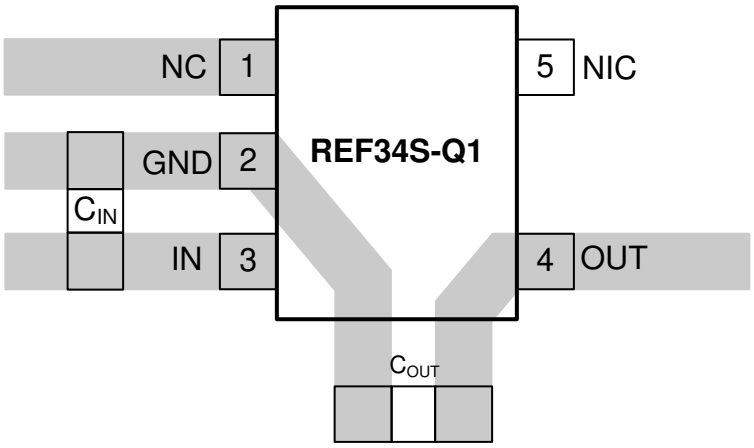


Figure 13-2. Layout Example (REF34xxS-Q1 DBV Package)

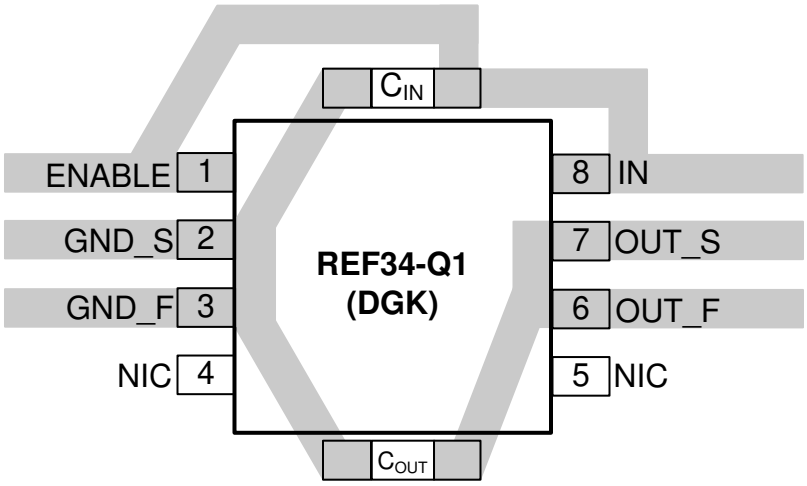


Figure 13-3. Layout Example (REF34xx-Q1 DGK Package)

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design*

14.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

14.4 Trademarks

Jacinto™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF3425QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OLC	Samples
REF3425QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2E93	Samples
REF3425SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D6C	Samples
REF3430QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OMC	Samples
REF3430QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FW3	Samples
REF3430SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D7C	Samples
REF3433QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1ONC	Samples
REF3433QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FV3	Samples
REF3433SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D8C	Samples
REF3440QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OOC	Samples
REF3440QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FQ3	Samples
REF3440SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D9C	Samples
REF3450QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OPC	Samples
REF3450QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FX3	Samples
REF3450SQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2DAC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

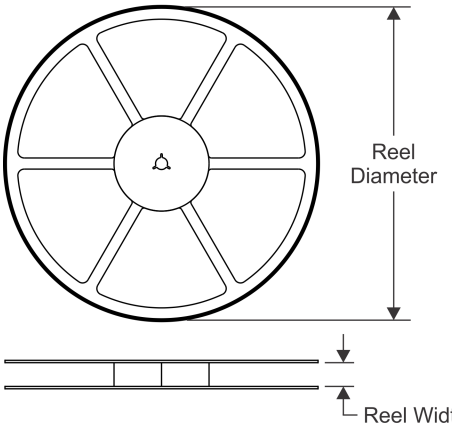
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

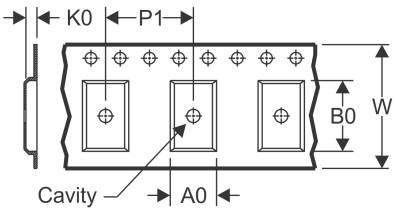
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

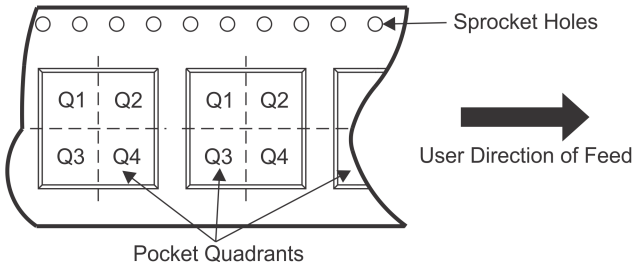


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

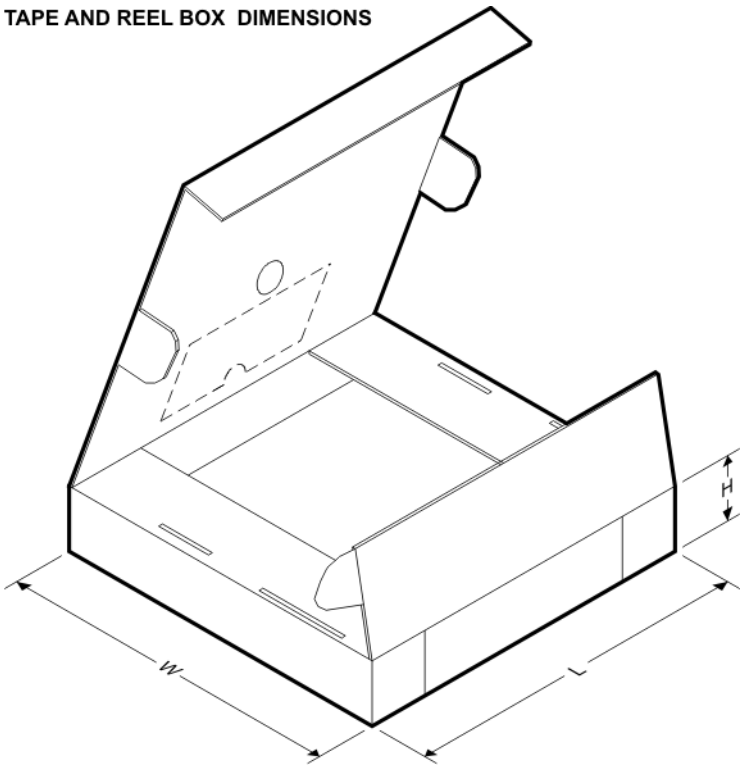
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF3425QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3425QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3425SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3430QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3430QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3430SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3433QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3433QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3433SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3440QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3440QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3440SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3450QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF3450QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF3450SQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

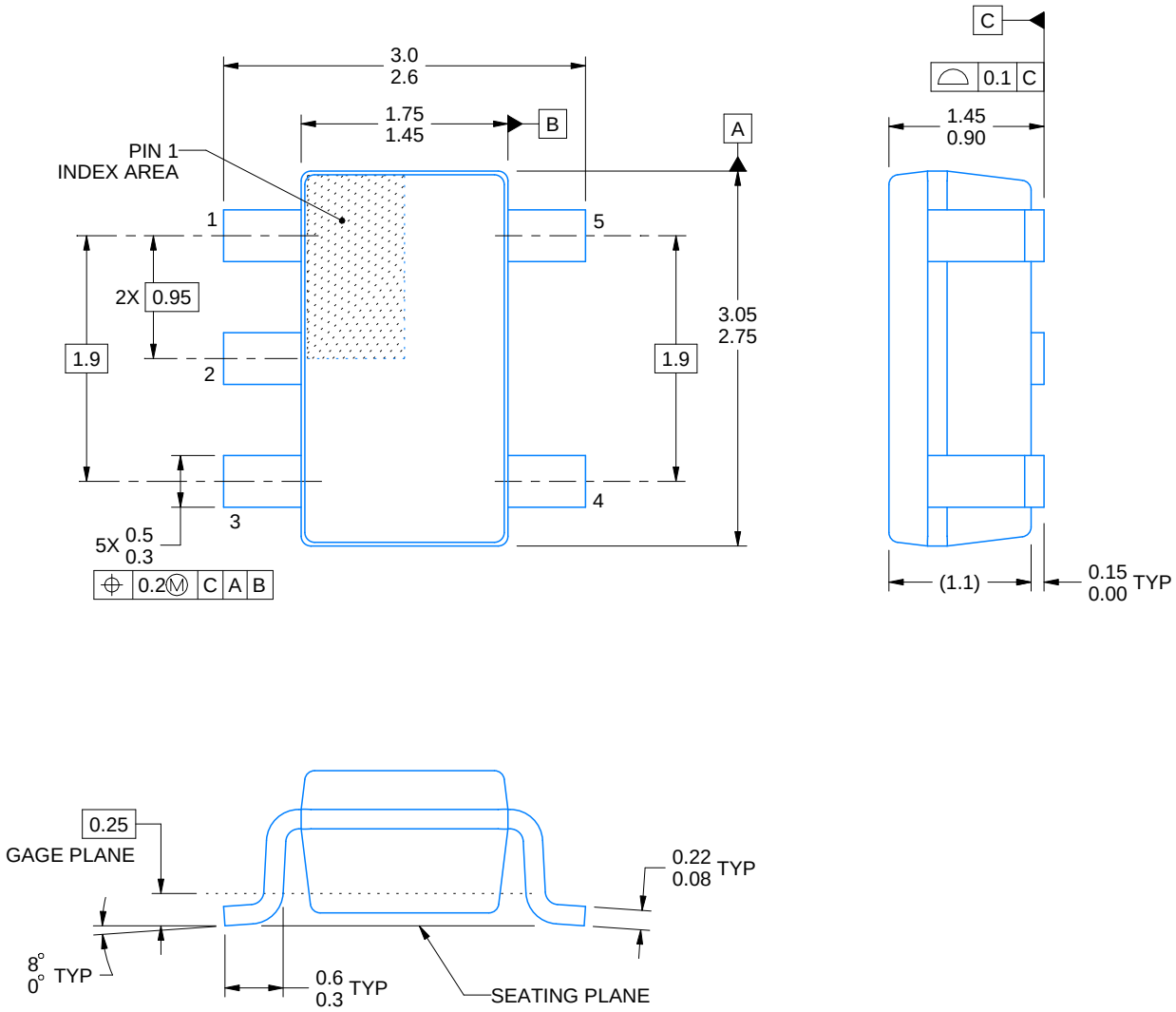
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF3425QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3425QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3425SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF3430QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3430QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3430SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF3433QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3433QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3433SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF3440QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3440QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3440SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF3450QDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF3450QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
REF3450SQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

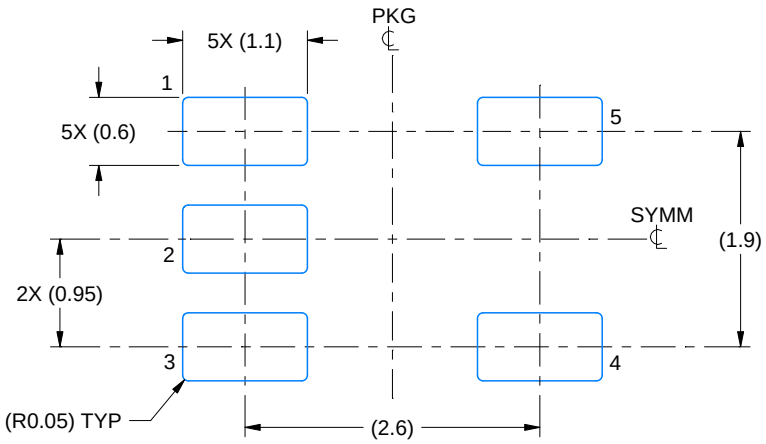
SMALL OUTLINE TRANSISTOR



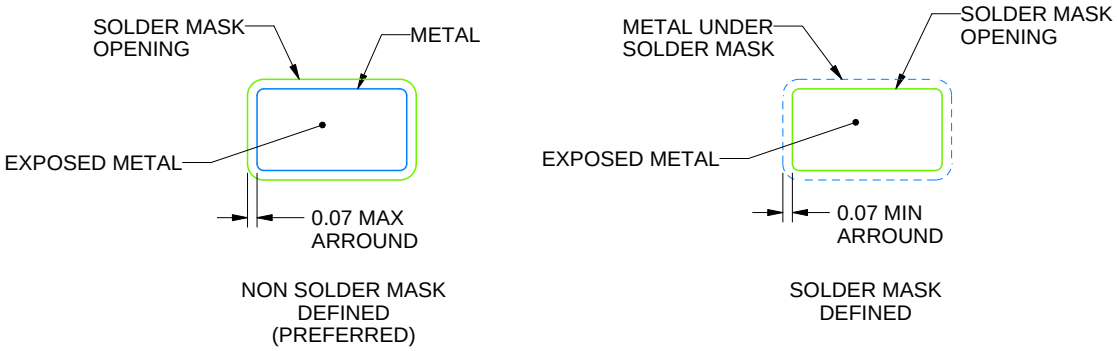
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

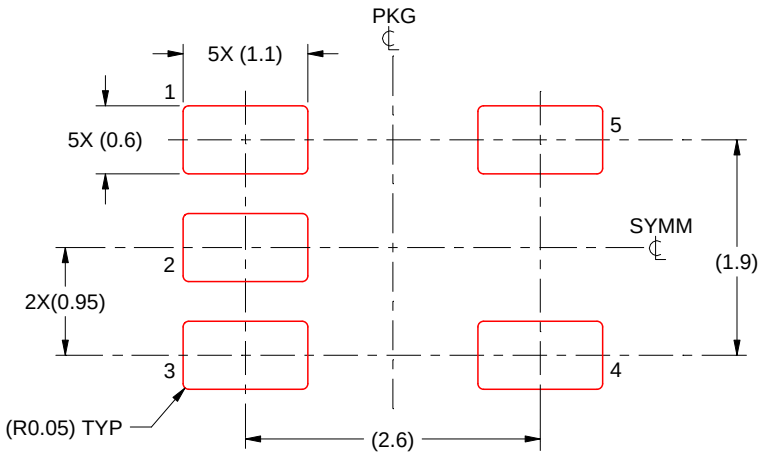


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



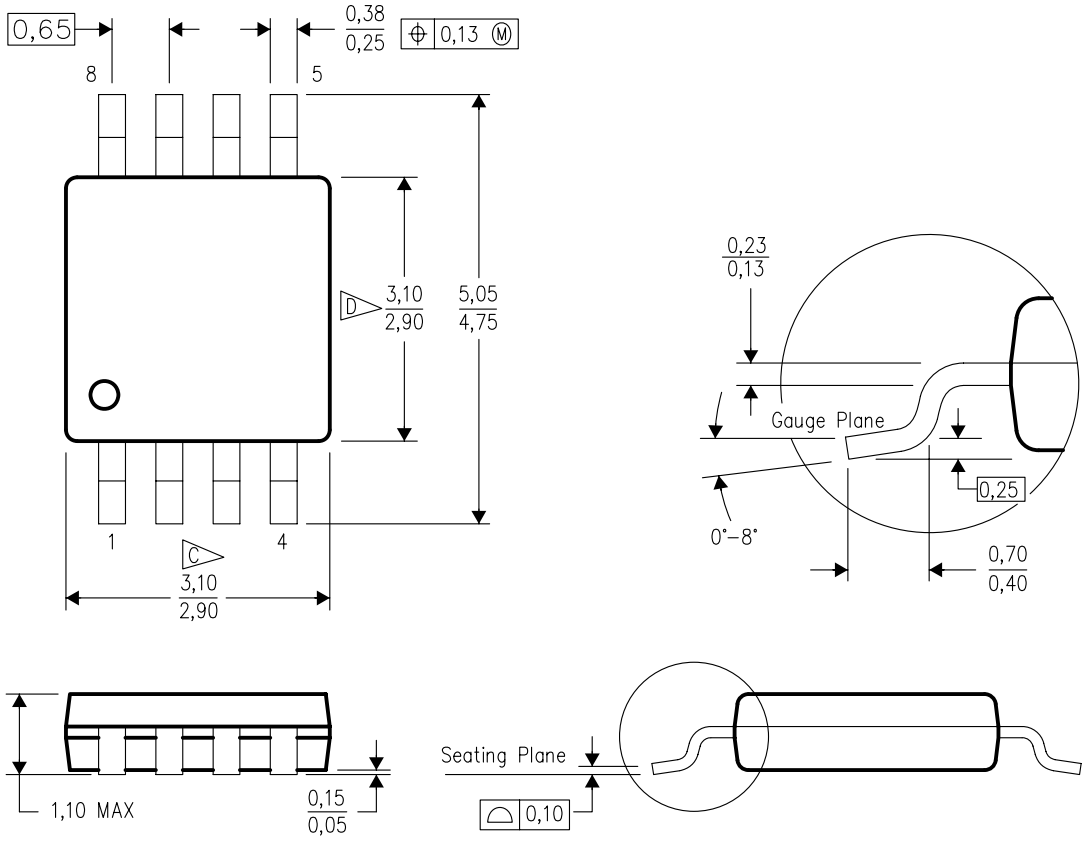
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

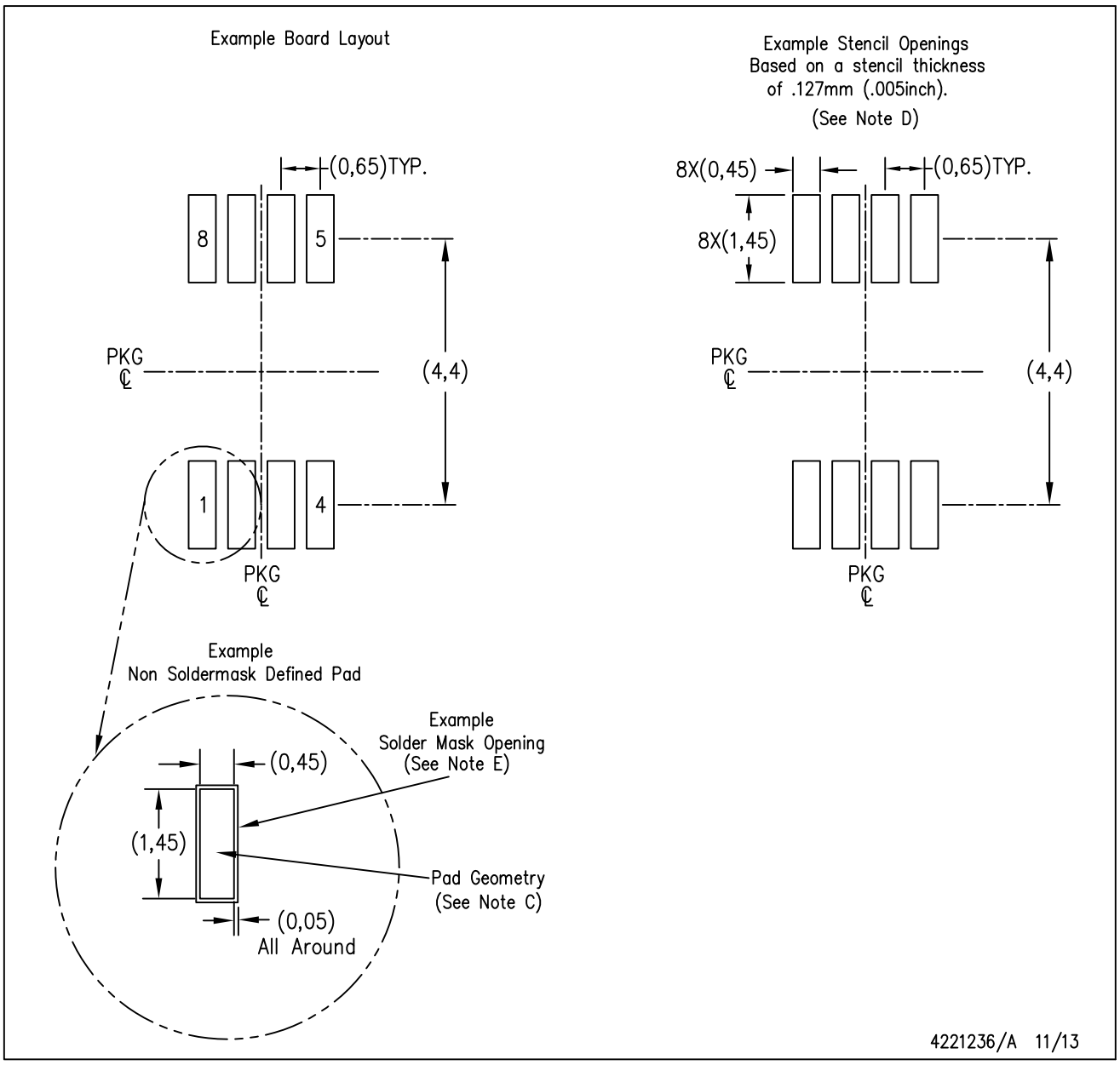
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



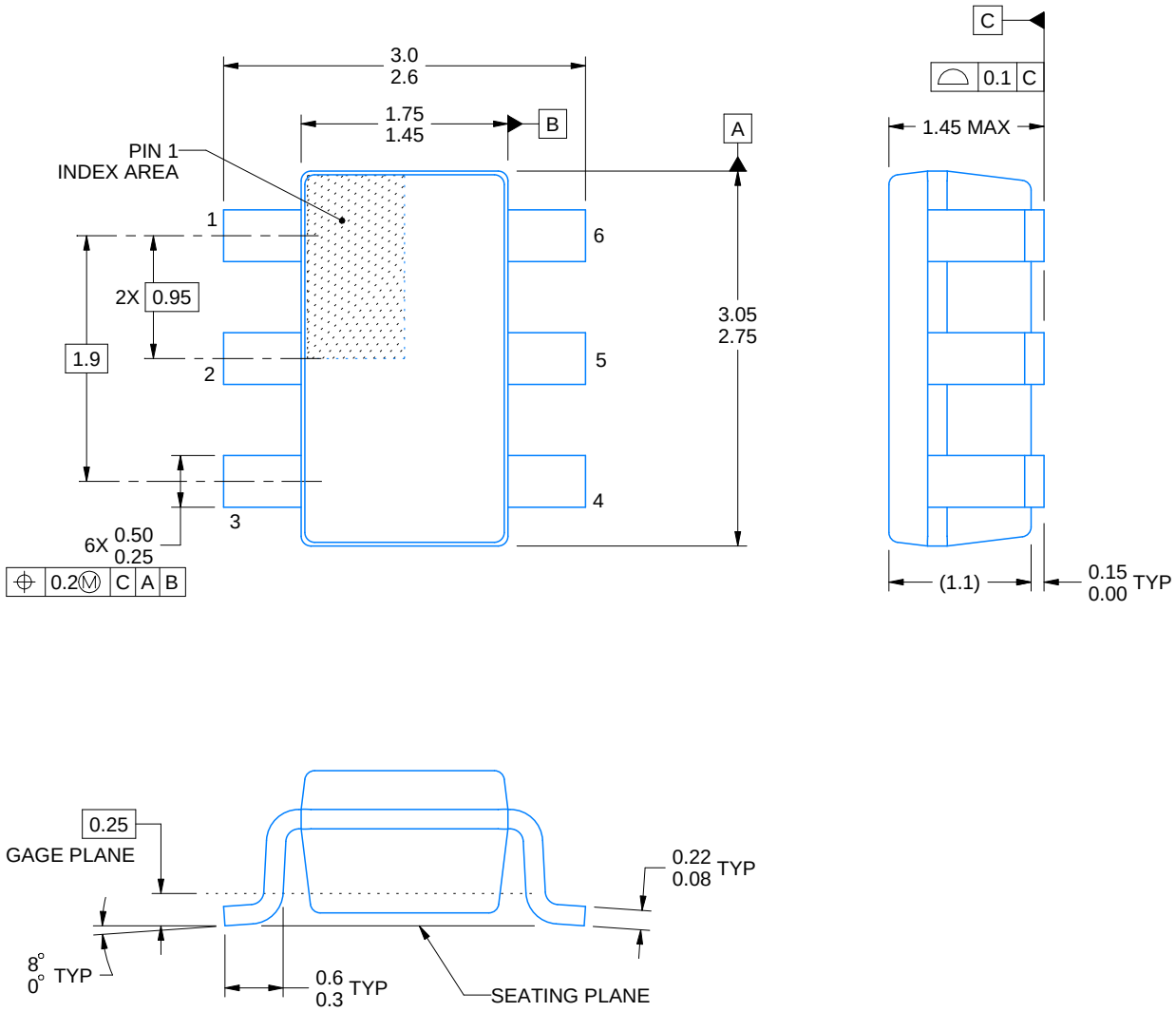
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

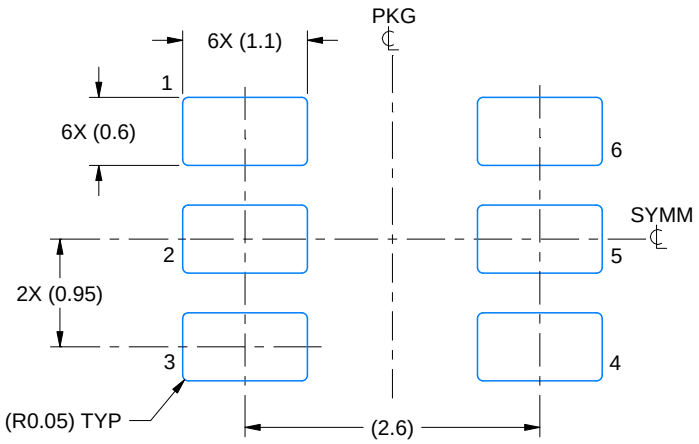
SMALL OUTLINE TRANSISTOR



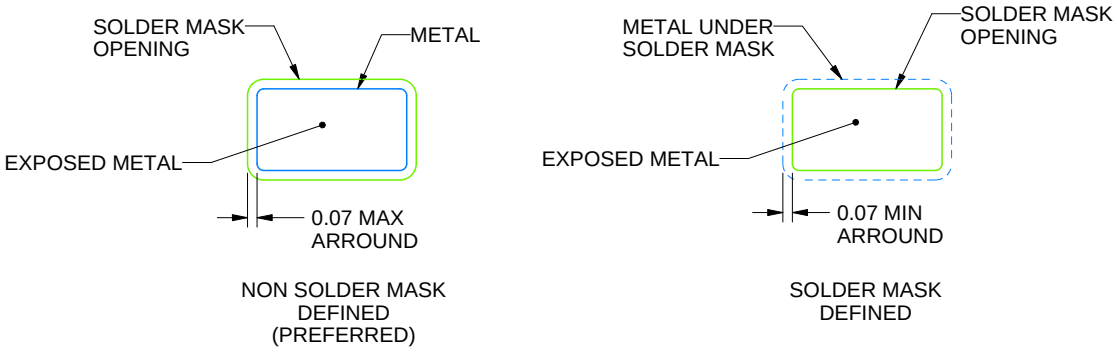
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

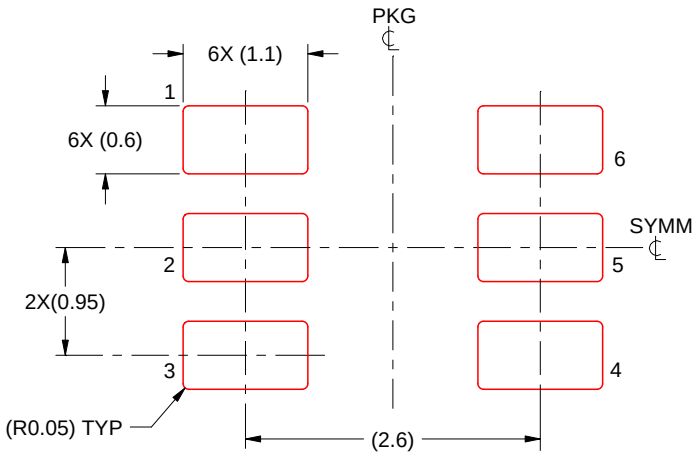


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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