PIC18F66K80

PIC18F66K80 Family
Silicon Errata and Data Sheet Clarification

The PIC18F66K80 family devices that you have received conform functionally to the current Device Data Sheet (DS39977**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F66K80 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 8, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device* and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F66K80 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A2	A3	A4
PIC18F66K80	60E0	2h	3h	4h
PIC18F65K80	6140			
PIC18F46K80	6100			
PIC18F45K80	6160			
PIC18F26K80	6120			
PIC18F25K80	6180			
PIC18LF66K80	61C0			
PIC18LF65K80	6220			
PIC18LF46K80	61E0			
PIC18LF45K80	6240			
PIC18LF26K80	6200			
PIC18LF25K80	6260			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC18F66K80 Flash Programming Specification"* (DS39972) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A3	A4
Analog-to-Digital Converter (A/D)	A/D Performance	1.	The 12-bit A/D performance is outside of data sheet's A/D Converter specifications.	X	X	X
EUSART	Synchronous Transmit	2.	When using the Synchronous Transmit mode, transmitted data may become corrupted if using the TXxIF bit to determine when to load the TXREGx register.	X		
ECCP	Auto-Shutdown	3.	The tri-state setting of the auto-shutdown feature in the enhanced PWM will not successfully drive the pin to tri-state.	X	X	X
ECAN	CAN Clock Source Selection	4.	CLKSEL bit in the CIOCON register is modifiable while the ECAN module is active.	X		
Ultra Low-Power Sleep	Sleep Entry	5.	Entering Ultra Low-Power Sleep mode by setting $\overline{\text{RETEN}}$ = 0 and SRETEN = 1, will cause the part to not be programmable through ICSP™.	X		
I_{PD} and I_{DD}	Maximum Limit	6.	Maximum current limits may be higher than specified in Table 31-2 of the data sheet.	X		
Reset (BOR)	Enable/Disable	7.	An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled, when the High/Low-Voltage Detection module (HLVD) is not enabled (HLVDCON<4> = 0).	X	X	X
ECAN	EWIN	8.	The enhanced window address feature, EWIN<4:0>, in the ECANCON register, will not move the BnCON $0 \leq n \leq 5$ registers into the access window of RAM.	X		
MCLRE	Master Clear Enable	9.	The Master Clear pin will not be readable when MCLRE is set to off for all 28-pin part variants (PIC18F2XK80).	X	X	X
Timer1/ Timer3	Gated Enable	10.	Timer1 and Timer3 gate control will not function up to the speed of FOSC when the TxCON is set to the system clock (TxCON<7:6> = 01).	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Analog-to-Digital Converter (A/D)

The 12-bit A/D performance is outside of the data sheet's A/D Converter specifications. When used as a 12-bit A/D, the possible issues are high offset error, up to a maximum of ±25 LSBs; high DNL error, up to a maximum of +6.0/-4.0 LSBs; and multiple missing codes, up to a maximum of twenty. Users should evaluate the 12-bit A/D performance in their application using the suggested work around below. See Table 3 for guidance specifications.

The 12-bit A/D issues will be fixed in future revisions of this part. Reduced bit resolution specifications can be derived by dividing, as appropriate. For instance, 10-bit guidance is obtained by dividing the parameters in Table 3 by four.

A/D Offset

The A/D may have high offset error, up to a maximum of ±25 LSBs; it can be used if the A/D is calibrated for the offset.

Work around

Calibrate for offset in Single-Ended mode by connecting A/D +ve input to ground and taking the A/D reading. This will be the offset of the device and can be used to compensate for the subsequent A/D readings on the actual inputs.

TABLE 3: A/D CONVERTER CHARACTERISTICS

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	—	—	12	bit	$\Delta V_{REF} \geq 5.0V$
A03	EIL	Integral Linearity Error	—	—	±10.0	LSb	$\Delta V_{REF} \geq 5.0V$
A04	EDL	Differential Linearity Error	—	—	+6.0/-4.0	LSb	$\Delta V_{REF} \geq 5.0V$
A06	EOFF	Offset Error	—	—	±25	LSb	$\Delta V_{REF} \geq 5.0V$
A07	EGN	Gain Error	—	—	±15	LSb	$\Delta V_{REF} \geq 5.0V$
A10	—	Monotonicity(1)	—				$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	ΔVREF	Reference Voltage Range ($V_{REFH} - V_{REFL}$)	3	—	$AV_{DD} - AV_{SS}$	V	
A21	VREFH	Reference Voltage High	AV_{SS} + 3.0V	—	AV_{DD} + 0.3V	V	
A22	VREFL	Reference Voltage Low	AV_{SS} – 0.3V	—	AV_{DD} – 3.0V	V	
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	

Note 1: The A/D conversion result never decreases with an increase in the input voltage.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: EUSART

In Synchronous Transmit mode, data may be corrupted if using the TXxIF bit to determine when to load the TXREGx register. One or more of the intended transmit messages may be incorrect.

Work around

A fixed delay added before loading the TXREGx may not be a reliable work around. When loading the TXREGx, check that the TRMT bit inside of the TXSTAx register is set instead of checking the TXxIF bit. The following code can be used:

```
while(!TXSTAxbits.TRMT);
// wait to load TXREGx until TRMT is set
```

Affected Silicon Revisions

A2	A3	A4					
X							

3. Module: ECCP

The tri-state setting of the auto-shutdown feature, in the enhanced PWM, will not successfully drive the pin to tri-state. The pin will remain an output and should not be driven externally. All tri-state settings will be affected.

Work around

Use one of the other two auto-shutdown states available, as outlined in the data sheet.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

4. Module: ECAN

The CLKSEL bit in the CIOCON register remains modifiable while the ECAN module is not in Configuration mode. Accidental state changes of this bit will result in immediate bit clock changes that will affect all nodes on the bus.

Work around

While the ECAN module is in Run mode, do not modify the state of the CLKSEL bit in the CIOCON register unless the CAN module is first changed into Configuration mode.

Affected Silicon Revisions

A2	A3	A4					
X							

5. Module: Ultra Low-Power Sleep

Entering Ultra Low-Power Sleep mode by setting RETEN = 0 and SRETEN = 1, will cause the part to not be programmable through ICSP. This issue occurs when the RETEN fuse bit in CONFIG1L<0> is cleared to '0', the SRETEN bit in the WDTCON register is set to '1' and a SLEEP instruction is executed within the first 350 µs of code execution. This happens after a Reset event, causing the part to enter Ultra Low-Power Sleep mode.

Work around

Use normal Sleep and Low-Power Sleep modes only, or on any Reset, ensure that at least 350 µs passes before executing a SLEEP instruction when ULP is enabled. To ensure the Ultra Low-Power Sleep mode is not enabled, the RETEN fuse bit in CONFIG1L<0> should be set to a '1', and the SRETEN bit in the WDTCON register should be cleared to a '0'. The following code can be used:

```
//This will ensure the RETEN fuse is set to 1
#pragma config RETEN = OFF

//This will ensure the SRETEN bit is 0
WDTCONbits.SRETEN = 0;
```

If the Ultra Low-Power Sleep mode is needed, then the user must ensure that the minimum time, before the first SLEEP instruction is executed, is greater than 350 µs.

Affected Silicon Revisions

A2	A3	A4					
X							

6. Module: IPD and IDD

The IPD and IDD limits do not match the data sheet. The IPD values, shown in **bold** in **Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/Extended)"** (below), reflect the updated silicon maximum limits.

All IDD maximum limits will equal 2.8 times the value listed in the data sheet.

Affected Silicon Revisions

A2	A3	A4					
X							

.

31.2 DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/Extended)

PIC18F66K80 (Industrial/Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Device	Typ	Max	Units	Conditions	
	Power-Down Current (IPD)(1)					
	PIC18LFXXK80	0.008	**7**	µA	-40°C	VDD = 1.8V(4) (Sleep mode) Regulator Disabled
		0.013	**7**	µA	+25°C	
		0.035	**9**	µA	+60°C	
		0.218	**10**	µA	+85°C	
		3	**12**	µA	±125ºC	
	PIC18LFXXK80	0.014	**8**	µA	-40°C	VDD = 3.3V(4) (Sleep mode) Regulator Disabled
		0.034	**8**	µA	+25°C	
		0.092	**9**	µA	+60°C	
		0.312	**10**	µA	+85°C	
		4	**16**	µA	±125ºC	
	PIC18FXXK80	0.2	**9**	µA	-40°C	VDD = 3.3V (Sleep mode) Regulator Enabled
		0.23	**9**	µA	+25°C	
		0.32	**10**	µA	+60°C	
		0.51	**11**	µA	+85°C	
		5	**18**	µA	±125ºC	
	PIC18FXXK80	0.22	**10**	µA	-40°C	VDD = 5V(5) (Sleep mode) Regulator Enabled
		0.24	**10**	µA	+25°C	
		0.34	**11**	µA	+60°C	
		0.54	**12**	µA	+85°C	
		5	**20**	µA	±125ºC	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS, and all features that add delta current disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
MCLR = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: For LF devices, RETEN (CONFIG1L<0>) = 1.

5: For F devices, SRETEN (WDTCON<4>) = 1 and RETEN (CONFIG1L<0>) = 0.

7. Module: Reset (BOR)

An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled, when the High/Low-Voltage Detection module (HLVD) is not enabled (HLVDCON<4> = 0). This issue affects BOR modes: BOREN<1:0> = 10 and BOREN<1:0> = 01. In both of these modes, if the BOR module is re-enabled while the device is active, unexpected Resets may be generated.

Work around

If BOR is required and power consumption is not an issue, use BOREN<1:0> = 11. For BOREN<1:0> = 10 mode, either switch to BOREN<1:0> = 11 mode or enable the HLVD (HLVDCON<4> = 1) prior to entering Sleep. If power consumption is an issue and low power is desired, do not use BOREN<1:0> = 10 mode. Instead, use BOREN<1:0> = 01 and follow the steps below when entering and exiting Sleep.

1. Disable BOR by clearing SBOREN (RCON<6> = 0).

```
WDTCONbits.SBOREN = 0;
```

2. Enter Sleep mode (if desired).

```
Sleep();
```

3. After exiting Sleep mode (if entered), enable the HLVD bit (HLVDCON<4> = 1).

```
HLVDCONbits.HLVDEN = 1;
```

4. Wait for the internal reference voltage (TIRVST) to stabilize (typically 25 μs).

```
while(!HLVDCONbits.IRVST);
```

5. Re-enable BOR by setting SBOREN (RCON<6> = 1).

```
WDTCONbits.SBOREN = 1;
```

6. Disable the HLVD by clearing HLVDEN (HLVDCON<4> = 0).

```
HLVDCONbits.HLVDEN = 0;
```

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

8. Module: ECAN

The enhanced window address feature, EWIN<4:0>, in the ECANCON register, will not move the BnCON 0≤n≤5 registers into the access window of RAM. The rest of the registers in B0 through B5 will be transferred into the access bank successfully. This feature is only available in Mode 1 and Mode 2; Mode 0 applications will not be affected.

Work around

1. Set the ECANCON register EWIN bits to the desired buffer.

```
ECANCONbits.EWIN = Buffer_Selection;
```

2. Decode the desired buffer to each individual Buffer Control register, BnCON 0≤n≤5.

```
switch( Buffer_Selection )
{
//EWIN code for Buffer B0
case 18:
      break;

//EWIN code for Buffer B5
case 23:
      break;
default:
      break;
}
```

3. Process information in the selected buffer control register. Note that the BnCON 0≤n≤5 Control registers can be set up for either transmit or receive operations.

```
case 18:
      //Save B0CON and clear flags
being processed
      temp = B0CON;
      //clear any flags
      break;
```

4. Continue processing the rest of the buffer in the windowed location.

Affected Silicon Revisions

A2	A3	A4					
X							

9. Module: MCLRE

The Master Clear pin will not be readable when MCLRE is set to off for all 28-pin part variants (PIC18F2XK80). When the MCLRE bit, CONFIG3H<7>, is cleared on 28-pin devices, the $\overline{MCLR}$ pin will be disabled but input data will not be available on RE3.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

10. Module: Timer1/Timer3

Timer1 and Timer3 gate control will not function up to the speed of FOSC when the TxCON is set to the system clock (TxCON<7:6> = 01). Results will always be at the resolution of FOSC/4, although the internal FOSC has been selected as the clock source.

Work around

Use the external clock input pin setting, TxCON<7:6> = 10 and TxCON<3> = 0.

Affected Silicon Revisions

A2	A3	A4					
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39977**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: RXFCON Registers

Table 6-1 on Page 116 of the Data Sheet should show the following register addresses:

E47h-RXFCON1

E46h-RXFCON0

2. Module: RXFCON Registers

Table 6-2 on Page 125 of the Data Sheet should show the following register addresses:

E47h-RXFCON1

E46h-RXFCON0

3. Module: Listen Only Mode

Page 441, **Section 27.3.4 “Listen Only Mode”** will be revised to:

Listen Only mode provides a means for the PIC18F66K80 family devices to receive all messages, including messages with errors. This mode can be used for bus monitor applications or for detecting the baud rate in ‘hot plugging’ situations. For Auto-Baud Detection, it is necessary that there are at least two other nodes which are communicating with each other. The baud rate can be detected empirically by testing different values until valid messages are received. The Listen Only mode is a silent mode, meaning no messages will be transmitted while in this state, including error flags or Acknowledge signals. **In Listen Only mode, both valid and invalid messages will be received regardless of RXMn bit settings. The filters and masks can still be used to allow only particular valid messages to be loaded into the Receive registers, or the filter masks can be set to all zeros to allow a message with any identifier to pass. All invalid messages will be received in this mode, regardless of filters and masks or RXMn Receive Buffer mode bits.** The error counters are reset and deactivated in this state. The Listen Only mode is activated by setting the mode request bits in the CANCON register.

4. Module: A/D Converter Characteristics

The values in Table 31-25 reflect the updated A/D Converter Characteristics. The new information is shown in **bold** text.

TABLE 31-25: A/D CONVERTER CHARACTERISTICS: PIC18F66K80 (INDUSTRIAL/EXTENDED)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	—	—	**12**	bit	**ΔVREF ≥ 5.0V**
A03	EIL	Integral Linearity Error	—	<±1	**±6.0**	LSB	**ΔVREF ≥ 5.0V**
A04	EDL	Differential Linearity Error	—	<±1	**+3.0/-1.0**	LSB	**ΔVREF ≥ 5.0V**
A06	EOFF	Offset Error	—	<±1	**±9.0**	LSB	**ΔVREF ≥ 5.0V**
A07	EGN	Gain Error	—	<±1	**±8.0**	LSB	**ΔVREF ≥ 5.0V**
A10	—	**Monotonicity(1)**		**—**		—	VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	VDD – VSS	V	For 12-bit resolution
A21	VREFH	Reference Voltage High	AVSS + 3.0V	—	AVDD + 0.3V	V	For 12-bit resolution
A22	VREFL	Reference Voltage Low	AVSS – 0.3V	—	AVDD – 3.0V	V	For 12-bit resolution
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	
A28	AVDD	Analog Supply Voltage	VDD – 0.3	—	VDD + 0.3	V	
A29	AVSS	Analog Supply Voltage	VSS – 0.3	—	VSS + 0.3	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ	
A50	IREF	VREF Input Current(2)	— —	— —	5 150	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

5. Module: HLVD

Note 1 under Register 26-1: HLVDCON, on page 387, should direct to Parameter D420:

Note 1: For the electrical specifications, see Parameter **D420** in Section 31.0 “Electrical Characteristics”.

6. Module: Power-up Timer Period

Table 31-11 on page 572 of the data sheet, **Parameter 33 TPWRT** will be revised to a typical value of **1.0 ms**.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2011)

Initial release of this document; issued for revision, A2. Includes silicon issues 1 (Analog-to-Digital Converter), 2 (EUSART), 3 (ECCP), 4 (ECAN), 5 (Ultra Low-Power Sleep) and 6 (I_{PD} and I_{DD}).

Rev B Document (4/2011)

Added silicon issues 7 (Reset – BOR) and 8 (ECAN). Added data sheet clarifications 1, 2 (RXFCON Registers) and 3 (Listen Only Mode).

Rev C Document (9/2011)

Added Table 3, 10-Bit A/D Converter Characteristics to silicon issue 1 (Analog-to-Digital Converter). Added silicon issues 9 (MCLRE) and 10 (Timer1/Timer3). Added data sheet clarifications 4 (A/D Converter Characteristics) and 5 (HLVD).

Rev D Document (12/2011)

Added silicon revision A4; includes issues 1 (Analog-to-Digital Converter – A/D), 3 (ECCP), 7 (Reset – BOR) issues 9 (MCLRE). Added data sheet clarification 6 (Power-up Timer Period).

Updated data sheet revision level to “D”. All previous clarifications carried into this revision.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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