TEXAS INSTRUMENTS
PGA855
SBOSAE0 – APRIL 2023

PGA855 Low-Noise, Wide-Bandwidth, Fully Differential Output Programmable-Gain Instrumentation Amplifier

1 Features

- Eight pin-programmable binary gains
  - G (V/V) = ⅛, ¼, ½, 1, 2, 4, 8, and 16
- Low gain error drift: 2 ppm/°C (max)
- Fully differential outputs
  - Independent output power-supply pins
  - Output common-mode control
- Faster signal processing:
  - Wide bandwidth: 10 MHz at all gains
  - High slew rate: 35 V/µs
  - Settling time:
    500 ns to 0.01%, 950 ns to 0.0015%
  - Input stage noise: 7.8 nV/√Hz at G = 16 V/V
  - Filter option to achieve better SNR
- Input overvoltage protection to ±40 V beyond supplies
- Input-stage supply range:
  - Single supply: 8 V to 36 V
  - Dual supply: ±4 V to ±18 V
- Output-stage supply range:
  - Single supply: 4.5 V to 36 V
  - Dual supply: ±2.25 V to ±18 V
- Specified temperature range: –40°C to +125°C
- Small package: 3-mm × 3-mm QFN

2 Applications

- Factory automation and control
- Analog input module
- Data acquisition (DAQ)
- Test and measurement
- Semiconductor test

3 Description

The PGA855 is a high-bandwidth programmable gain instrumentation amplifier with fully differential outputs. The PGA855 is equipped with eight binary gain settings, from an attenuating gain of 0.125 V/V to a maximum of 16 V/V, using three digital gain selection pins. The output common-mode voltage can be independently set using the VOCM pin.

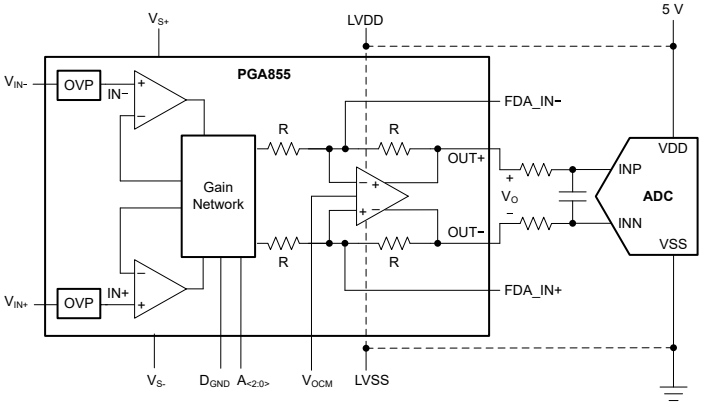
The PGA855 architecture is optimized to drive inputs of high-resolution, precision analog-to-digital converters (ADCs) with sampling rates up to 1 MSPS without the need for an additional ADC driver. The output-stage power supplies are decoupled from the input stage to protect the ADC or downstream device against overdrive damage.

The super-beta input transistors offer an impressively low input bias current, which in turn provides a very low input current noise density of 0.3 pA/√Hz, making the PGA855 a versatile choice for virtually any sensor type. The low-noise current-feedback front-end architecture offers excellent gain flatness even at high frequencies, making the PGA855 an excellent high-impedance sensor readout device. Integrated protection circuitry on the input pins handles overvoltages up to ±40 V beyond the power-supply voltages.

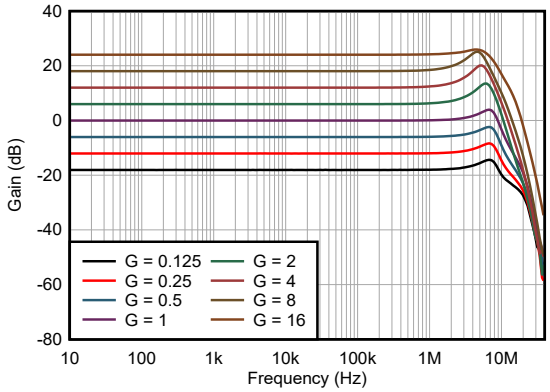
Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
PGA855	RGT (VQFN, 16)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



PGA855 Simplified Application



Gain vs Frequency

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2023	*	Initial draft.

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA849	Ultralow-noise (1-nV/√Hz), high-bandwidth instrumentation amplifier	G = 1 + 6 kΩ / RG	2, 3
INA851	Low-noise (3.2 nV/√Hz), high-speed (22 MHz), fully-differential instrumentation amp with overvoltage protection (±40 V)	G = 1 + 6 kΩ / RG	2, 3
PGA280	20-mV to ±10-V programmable gain instrumentation amplifier with 3-V or 5-V differential output; analog supply up to ±18 V	Digitally programmable with SPI	N/A
PGA281	Zero-drift, high-voltage programmable gain amplifier	Digitally pin-programmable	N/A

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6 Pin Configuration and Functions

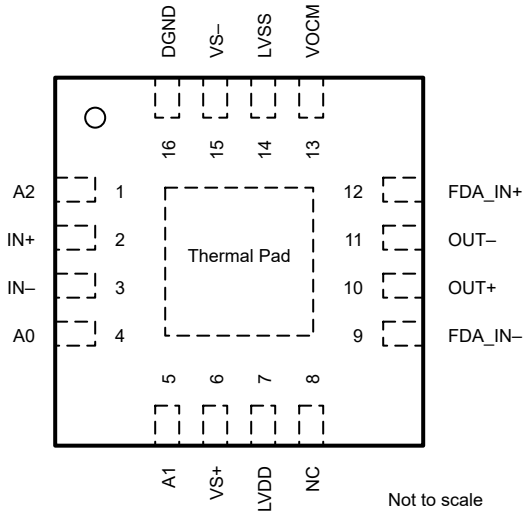

Figure 6-1. RGT Package, 16-Pin VQFN (Top View)

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	4	Input	Gain option pin 0
A1	5	Input	Gain option pin 1
A2	1	Input	Gain option pin 2
DGND	16	Power	Ground reference for digital logic and gain setting pins
FDA_IN–	9	Input	Connection to output driver summing node
FDA_IN+	12	Input	Connection to output driver summing node
IN–	3	Input	Negative (inverting) input
IN+	2	Input	Positive (noninverting) input
LVDD	7	Power	Output driver positive supply
LVSS	14	Power	Output driver negative supply
NC	8	—	Do not connect
OUT–	11	Output	Output (inverting)
OUT+	10	Output	Output (noninverting)
VOCM	13	Input	Level set for output common mode value
VS+	6	Power	Input stage positive supply
VS–	15	Power	Input stage negative supply
Thermal Pad	Thermal pad	—	The thermal pad must be soldered to the printed-circuit board (PCB). Connect thermal pad to a plane or large copper pour that is either floating or electrically connected to VS–, even for applications that have low power dissipation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage on V_{S+}, $V_{S–}$ pins; $V_S = (V_{S+}) – (V_{S–})$	0	40	V
V_{SOUT}	Supply voltage on LVDD, LVSS pins; $V_{SOUT} = V_{LVDD} – V_{LVSS}$	0	40	V
	Voltage on power pins LVDD, LVSS	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
V_{IN}	Voltage on signal-input pins IN+, IN–	$(V_{S–}) – 40$	$(V_{S+}) + 40$	V
	DGND, FDA_IN+, FDA_IN– pin voltage	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
	Voltage on gain-select pins A2, A1, A0	$V_{DGND} – 0.5$	$(V_{S+}) + 0.5$	V
V_O	Signal output pins maximum voltage on OUT+, OUT–	$V_{LVSS} – 0.5$	$V_{LVDD} + 0.5$	V
V_{OCM}	Output common-mode voltage	$V_{LVSS} – 0.5$	$V_{LVDD} + 0.5$	V
I_O	Signal-output pins current	–100	100	mA
I_{SC}	Output short-circuit current((2))	Continuous		
T_A	Operating temperature	–50	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_{SOUT} / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001((1))	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002((2))	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Input stage supply voltage	Single supply	8	36	V
		Dual supply	±4	±18	
V_{SOUT}	Output stage supply voltage	Single supply	4.5	36	V
		Dual supply	±2.25	±18	
T_A	Specified temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		PGA855 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

at T_A = 25 °C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} is at mid-supply, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Differential offset voltage (input referred)	G = 1 to 16			±70	±400	µV
		G < 1			±70/G	±400/G	
	Differential offset voltage drift (input referred)	G = 1 to 16, T_A = –40°C to +125°C			±0.3	±1.0	µV/°C
		G < 1, T_A = –40°C to +125°C			±0.3/G	±1.0/G	
PSRR	Power-supply rejection ratio	±4 V ≤ V_S ≤ ±18 V, RTI	G = 0.125	95	110		dB
			G = 0.25	98	114		dB
			G = 0.5	100	118		
			G = 1	120	134		
			G = 2	120	126		
			G = 4	120	132		
			G = 8	120	136		
			G = 16	120	140		
z_{id}	Differential impedance				1 || 1		GΩ || pF
z_{ic}	Common-mode impedance				1 || 7		GΩ || pF
V_{ICM}	Common-mode input voltage	V_S = ±4 V to ±18 V		($V_{S–}$) + 2.5		(V_{S+}) – 2.5	V
		V_S = ±4 V to ±18 V, T_A = –40°C to +125°C		($V_{S–}$) + 3		(V_{S+}) – 2.5	
CMRR	Common-mode rejection ratio	At dc to 60 Hz, V_{ICM} = ± 10 V, T_A = –40°C to +125°C, RTI	G = 0.125	64	82		dB
			G = 0.25	70	88		
			G = 0.5	76	94		
			G = 1	82	100		
			G = 2	88	106		
			G = 4	94	112		
			G = 8	100	118		
			G = 16	106	124		
BIAS CURRENT							
I_B	Input bias current				0.5		nA
		T_A = –40°C to +125°C			1		
	Input bias current drift	T_A = –40°C to +125°C				10	pA/°C
I_{OS}	Input offset current				0.5		nA
		T_A = –40°C to +125°C			1		
	Input offset current drift	T_A = –40°C to +125°C				10	pA/°C

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7.5 Electrical Characteristics (continued)

at T_A = 25 °C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} is at mid-supply, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE VOLTAGE							
e_{NI}	Input-referred voltage noise density	f = 1 kHz	G = 16		7.8		nV/√Hz
			G = 8		8.0		
			G = 4		8.6		
			G = 2		12.6		
			G = 1		21.6		
			G = 0.5		42		
			G = 0.25		84		
			G = 0.125		168		
	Input-referred voltage noise	f_B = 0.1 Hz to 10 Hz	G = 16		0.26		μV_{PP}
			G = 8		0.27		
			G = 4		0.29		
			G = 2		0.44		
			G = 1		0.8		
			G = 0.5		1.6		
			G = 0.25		3.2		
			G = 0.125		6.4		
i_N	Input current noise density	f = 1 kHz			0.3		pA/√Hz
	Input current noise	f_B = 0.1 Hz to 10 Hz			13		pA_{PP}
GAIN							
	Differential gain range			0.125		16	V/V
GE	Differential gain error	G = 1			±0.02	±0.03	%
		All other gains			±0.03	±0.1	
	Differential gain drift	G = 0.125 to 16, T_A = –40°C to +125°C				±2	ppm/°C
	Differential gain nonlinearity	G = 0.125 to 16, $V_{OUTDIFF}$ = 10 V			2	10	ppm
OUTPUT							
V_{OUT}	Output voltage	R_L = 10 kΩ	V_{SOUT} = ±4 V	V_{LVSS} + 0.3		V_{LVDD} – 0.3	V
			V_{SOUT} = ±18V	V_{LVSS} + 0.6		V_{LVDD} – 0.6	
C_L	Load capacitance	Stable operation for differential load			50		pF
I_{SC}	Short-circuit current	Continuous to V_{SOUT} / 2			±45		mA
			T_A = –40°C to +125°C	±20		±60	
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 0.125 to 16			10		MHz
SR	Slew rate	G = 0.125 to 16, $V_{OUTDIFF}$ > 5 V			35		V/µs
t_S	Settling time	G = 0.125 to 16 V_{INDIFF} = 10-V step or $V_{OUTDIFF}$ = 10-V step	To 0.01%		0.5		µs
			To 0.0015%		0.95		
	Gain switching time				2		µs
THD+N	Total harmonic distortion and Noise	Differential input, f = 10 kHz, V_O = 10 V_{PP}			–110		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}			–105		
HD2	Second-order harmonic distortion	Differential input, f = 10 kHz, V_O = 10 V_{PP}			–120		
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}			–110		
HD3	Third-order harmonic distortion	Differential input, f = 10 kHz, V_O = 10 V_{PP}			–120		
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}			–110		

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7.5 Electrical Characteristics (continued)

at T_A = 25 °C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} is at mid-supply, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL						
V_{OCM}	Common-mode input voltage	V_S = ±4 V	V_{LVSS} + 1.5		V_{LVDD} – 1.5	
		V_S = ±18 V	V_{LVSS} + 2		V_{LVDD} – 2	
	Small-signal bandwidth V_{OCM} pin	V_{OCM} = 100 mV_{PP}		30		MHz
	Large-signal bandwidth V_{OCM} pin	V_{OCM} = 0.6 V_{PP}		TBD		MHz
	DC output balance	V_{OCM} fixed at mid-supply (V_O = ±1 V)		70		dB
	Input impedance V_{VOCM} pin			250 || 1		kΩ || pF
	V_{OCM} offset from mid-supply	VOCM pin floating		±1	±3.5	mV
	V_{OCM} offset voltage	V_{OCM} = V_{ICM}, V_O = 0 V		±1	±3.5	mV
	V_{OCM} offset voltage drift	V_{OCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C		±20	±40	µV/°C
INPUT STAGE POWER SUPPLY						
I_{Q_input}	Input stage quiescent current V_{S+}, $V_{S–}$	V_{IN} = 0 V		3		mA
		T_A = –40°C to +125°C			4.5	
OUTPUT STAGE POWER SUPPLY						
I_{Q_output}	Output stage quiescent current LVDD, LVSS	V_{IN} = 0 V, V_{OCM} fixed at mid-supply		2.2		mA
		T_A = –40°C to 125°C			3	
DIGITAL LOGIC						
V_{IL}	Digital input logic low	A0, A1, A2 pins, referred to DGND	V_{DGND}		V_{DGND} + 0.8	V
V_{IH}	Digital input logic high	A0, A1, A2 pins, referred to DGND	V_{DGND} + 2		V_{S+}	V
	Digital input pin current	A0, A1, A2 pins		1.5	3	µA
V_{DGND}	DGND voltage		$V_{S–}$		(V_{S+}) – 4	V
	DGND reference current			4	10	µA

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7.6 Typical Characteristics

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

Table 7-1. Table of Graphs

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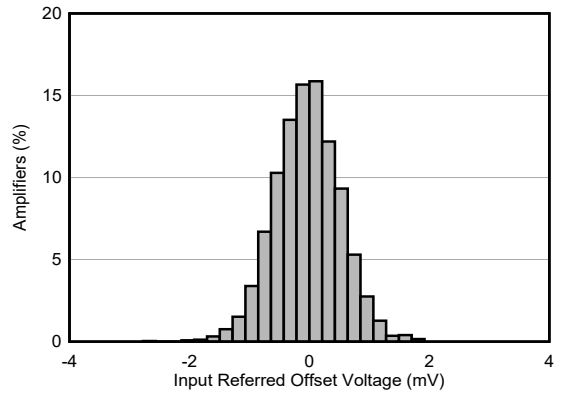
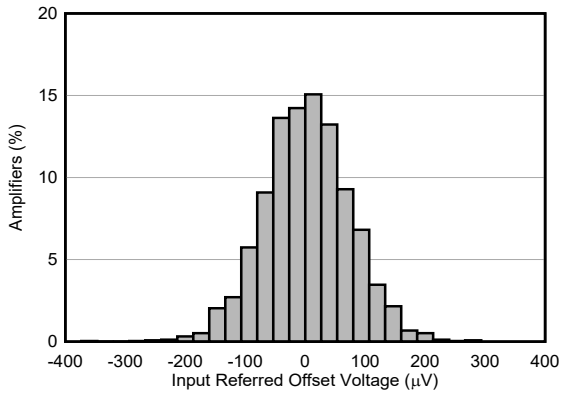
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



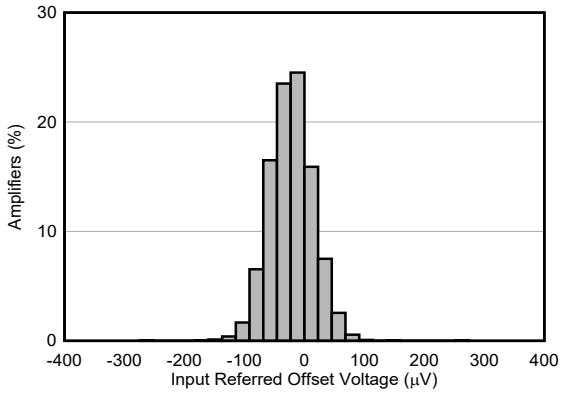
N = 2500 Mean = –36 µV Std. dev. = 540 µV
G = 0.125 V/V

Figure 7-1. Distribution of Offset Voltage (RTI)



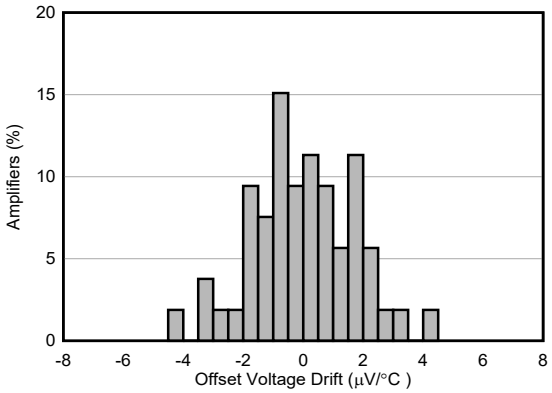
N = 2500 Mean = 2.83 µV Std. dev. = 71.58 µV
G = 1 V/V

Figure 7-2. Distribution of Offset Voltage (RTI)



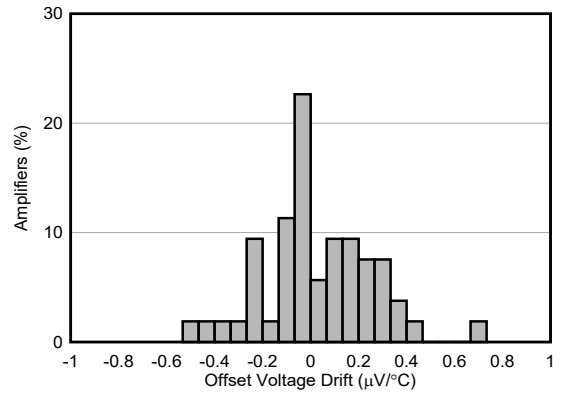
N = 2500 Mean = –21.25 µV Std. dev. = 36.79 µV
G = 16 V/V

Figure 7-3. Distribution of Offset Voltage (RTI)



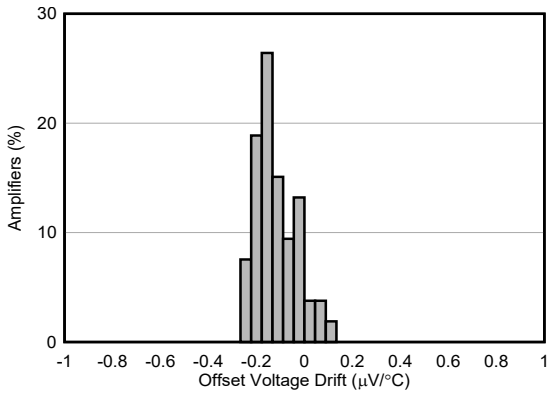
N = 53 Mean = –0.028 µV/°C Std. dev. = 1.69 µV/°C
G = 0.125 V/V

Figure 7-4. Distribution of Offset Voltage Drift (RTI)



N = 53 Mean = –0.024 µV/°C Std. dev. = 0.22 µV/°C
G = 1 V/V

Figure 7-5. Distribution of Offset Voltage Drift (RTI)



N = 53 Mean = –0.11 µV/°C Std. dev. = 0.08 µV/°C
G = 16 V/V

Figure 7-6. Distribution of Offset Voltage Drift (RTI)

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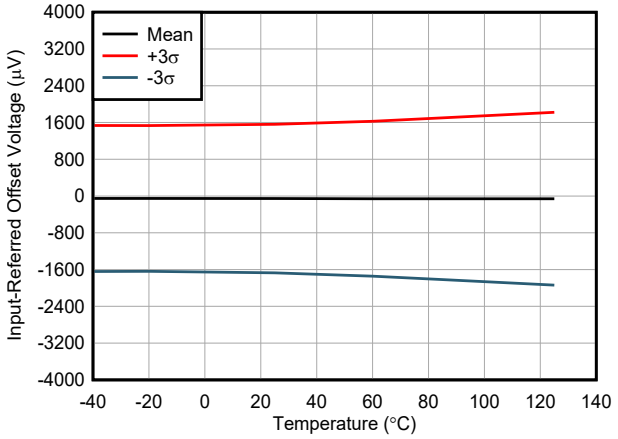
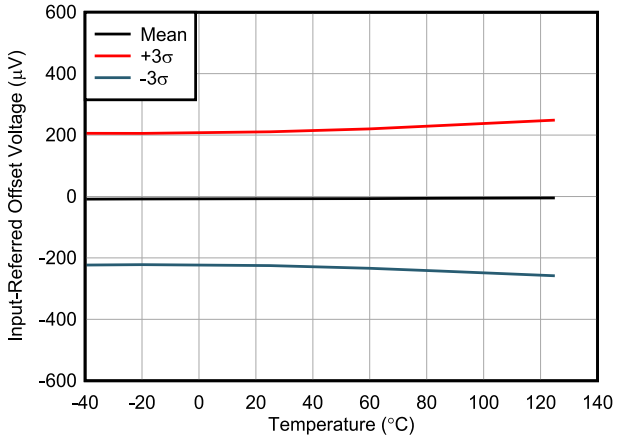
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



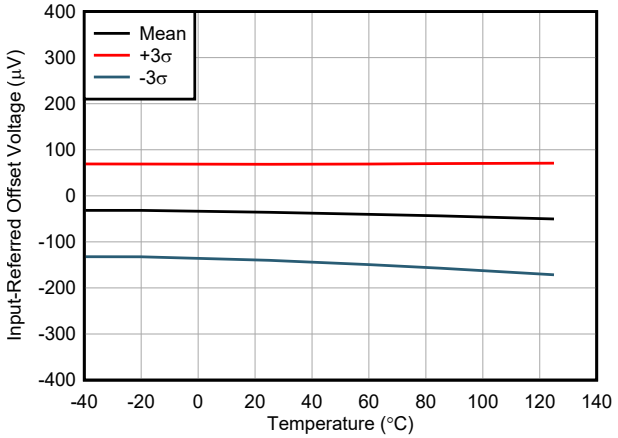
G = 0.125 V/V 53 units, 1 wafer lot

Figure 7-7. Offset Voltage (RTI) vs Temperature



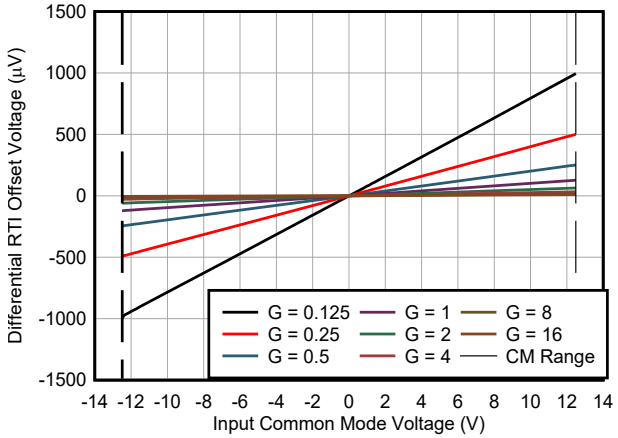
G = 1 V/V 53 units, 1 wafer lot

Figure 7-8. Offset Voltage (RTI) vs Temperature



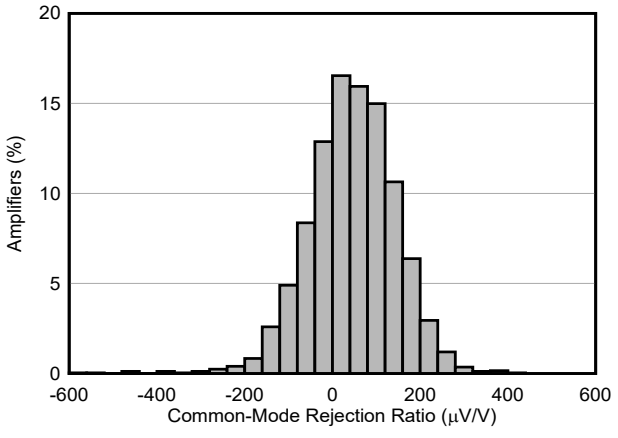
G = 16 V/V 53 units, 1 wafer lot

Figure 7-9. Offset Voltage (RTI) vs Temperature



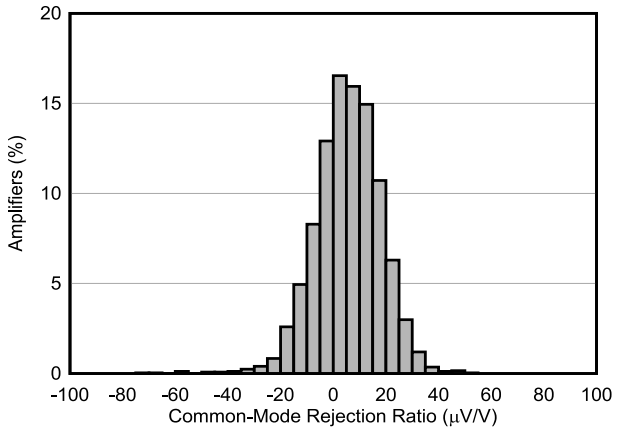
Typical unit shown

Figure 7-10. Offset Voltage (RTI) vs Input Common-Mode Voltage



N = 2500 Mean = 44.98 µV/V Std. dev. = 100 µV/V
G = 0.125 V/V

Figure 7-11. CMRR Distribution



N = 2500 Mean = 5.61 µV/V Std. dev. = 12.50 µV/V
G = 1 V/V

Figure 7-12. CMRR Distribution

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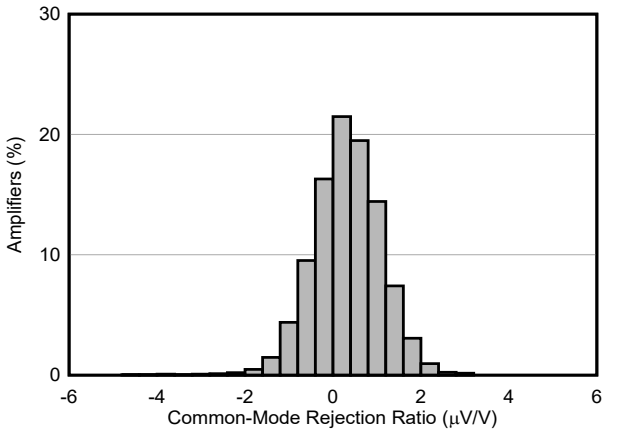
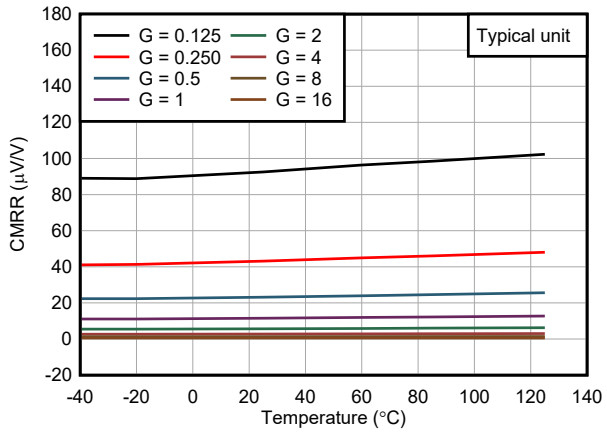
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



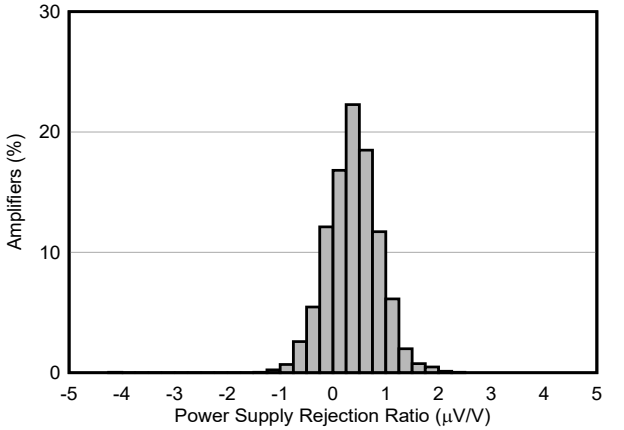
N = 2500 Mean = 0.31 µV/V Std. dev. = 0.78 µV/V
G = 16 V/V

Figure 7-13. CMRR Distribution



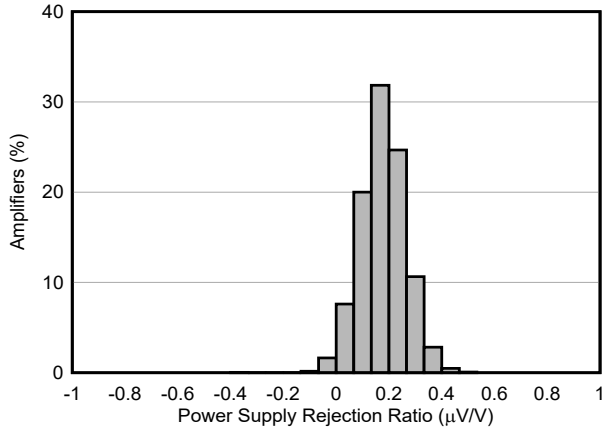
Typical unit shown

Figure 7-14. Typical CMRR vs Temperature



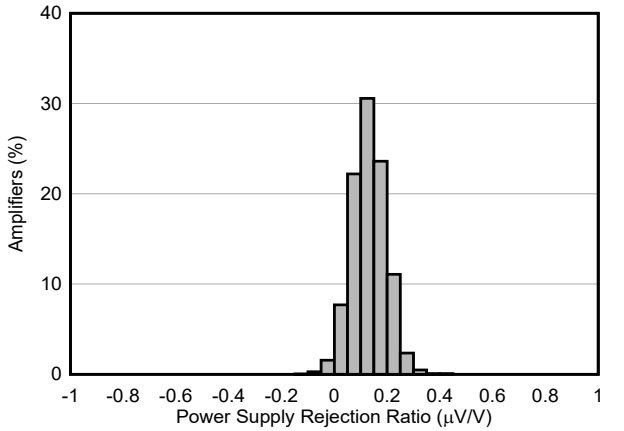
N = 2500 Mean = 0.38 µV/V Std. dev. = 0.48 µV/V
G = 0.125 V/V

Figure 7-15. PSRR Distribution



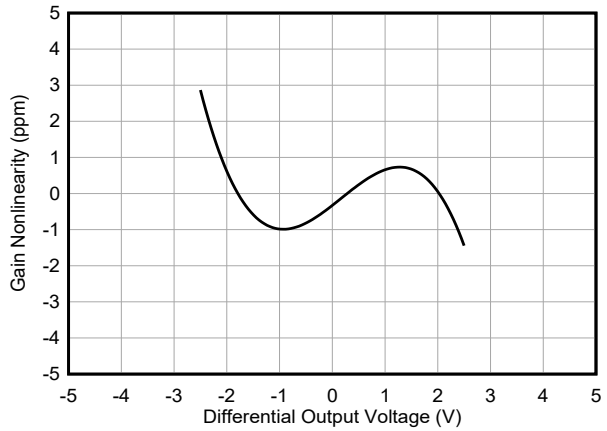
N = 2500 Mean = 0.17 µV/V Std. dev. = 0.08 µV/V
G = 1 V/V

Figure 7-16. PSRR Distribution



N = 2500 Mean = 0.13 µV/V Std. dev. = 0.06 µV/V
G = 16 V/V

Figure 7-17. PSRR Distribution



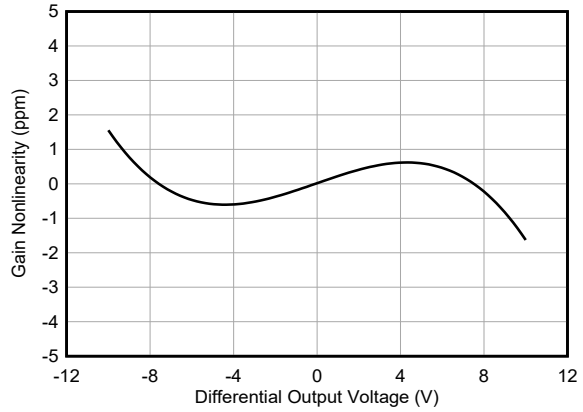
G = 0.125 V/V $V_{OUTDIFF}$ = 2.5 V

Figure 7-18. Gain Nonlinearity

ADVANCE INFORMATION

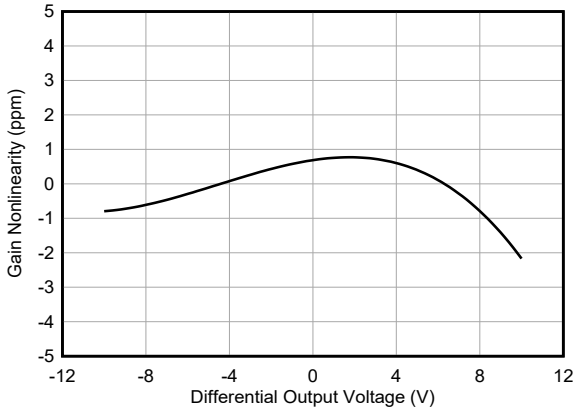
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



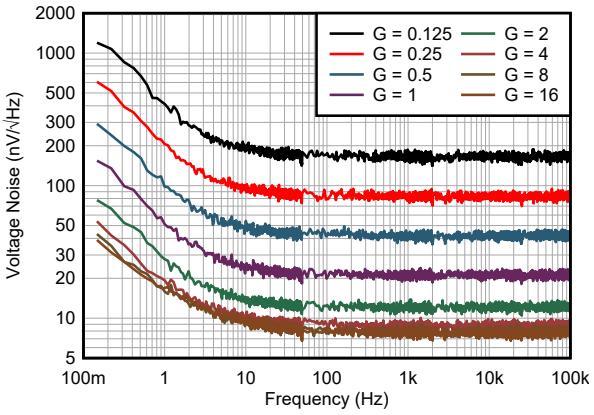
G = 1 V/V $V_{OUTDIFF}$ = 10 V

Figure 7-19. Gain Nonlinearity



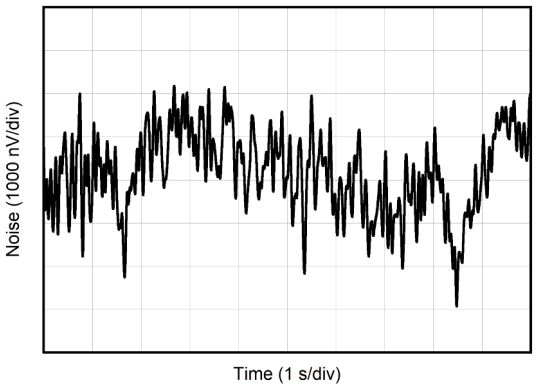
G = 16 V/V $V_{OUTDIFF}$ = 10 V

Figure 7-20. Gain Nonlinearity



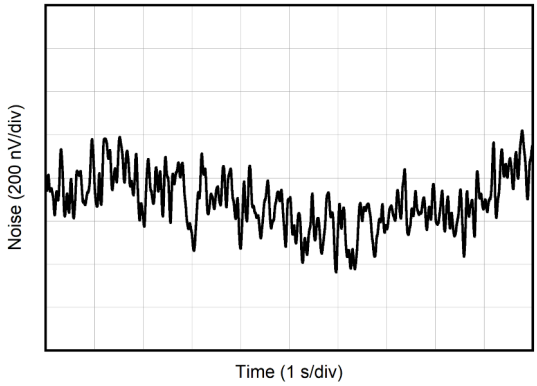
Typical unit shown

Figure 7-21. Voltage Noise Spectral Density (RTI) vs Frequency



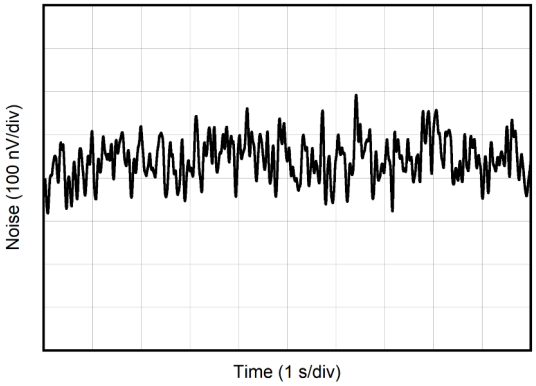
G = 0.125 V/V

Figure 7-22. 0.1-Hz to 10-Hz Voltage Noise (RTI)



G = 1 V/V

Figure 7-23. 0.1-Hz to 10-Hz Voltage Noise (RTI)



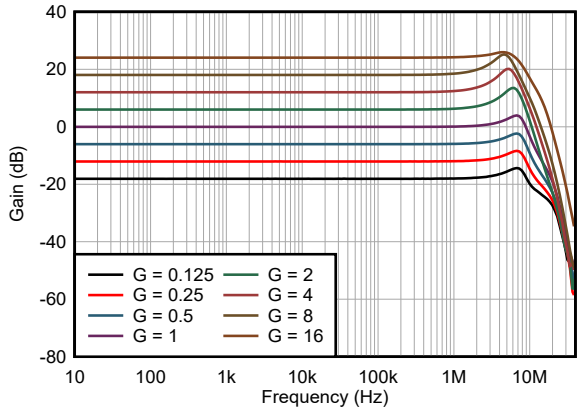
G = 16 V/V

Figure 7-24. 0.1-Hz to 10-Hz Voltage Noise (RTI)

ADVANCE INFORMATION

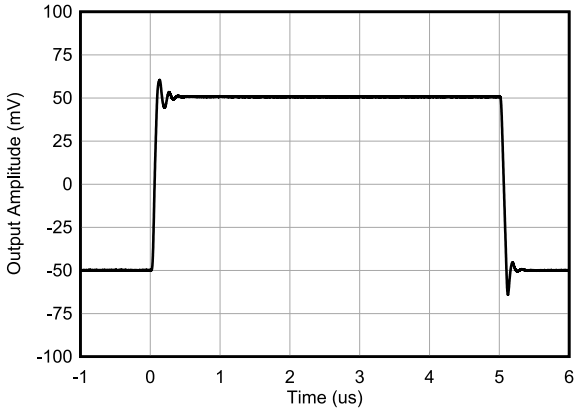
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



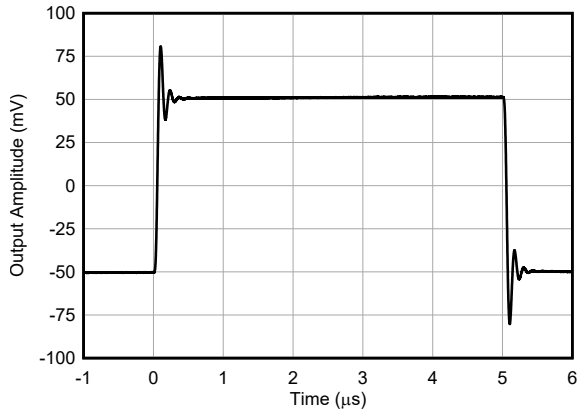
Differential load capacitance = 50 pF

Figure 7-25. Gain vs Frequency



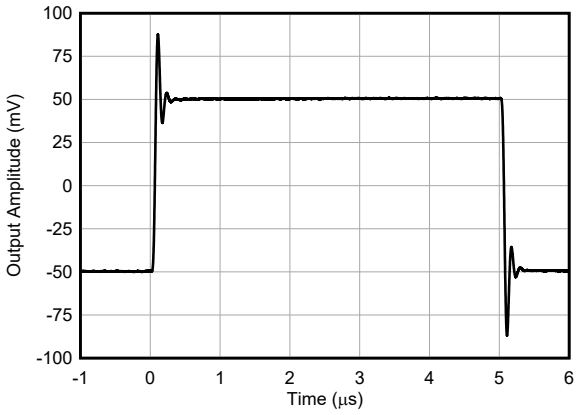
G = 0.125 V/V Differential load capacitance = 50 pF

Figure 7-26. Small-Signal Step Response



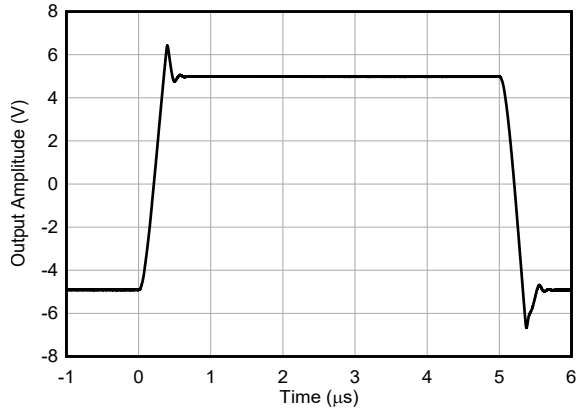
G = 1 V/V Differential load capacitance = 50 pF

Figure 7-27. Small-Signal Step Response



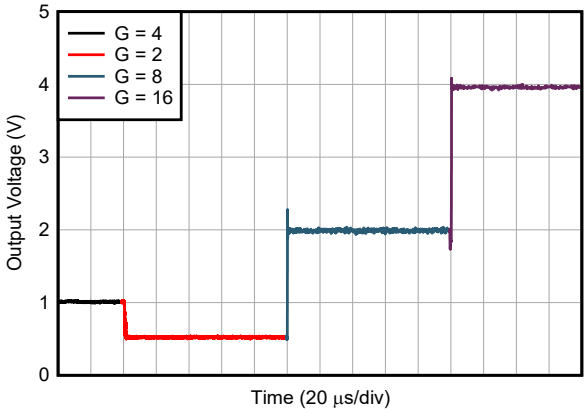
G = 16 V/V Differential load capacitance = 50 pF

Figure 7-28. Small-Signal Step Response



G = 1 V/V

Figure 7-29. Large-Signal Step Response



Input voltage = 250 mV_{PP}

Figure 7-30. Gain Switching Transient Response

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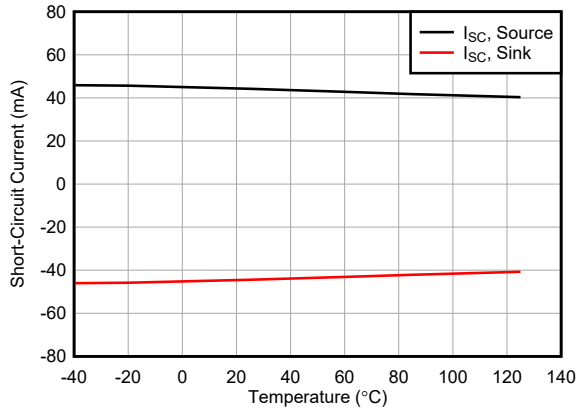
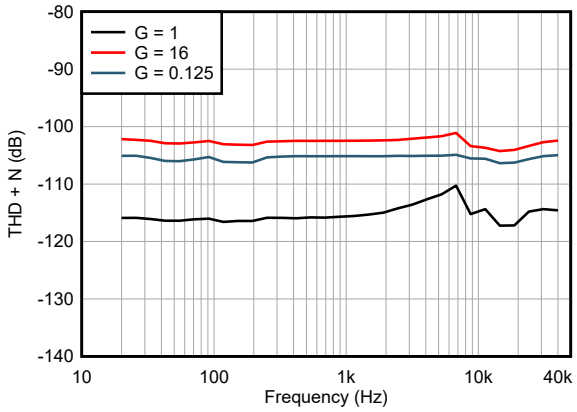
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



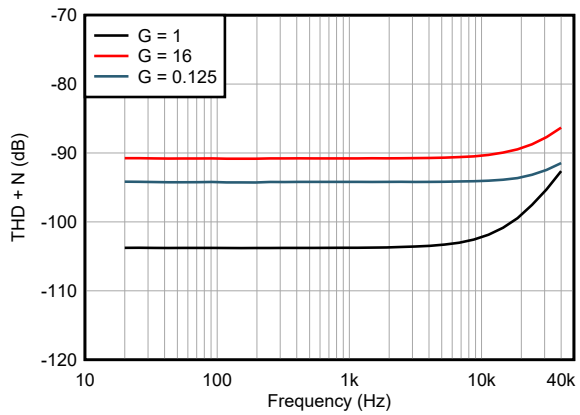
Short to V_{SOUT}/2

Figure 7-31. Output Short-Circuit Current vs Temperature



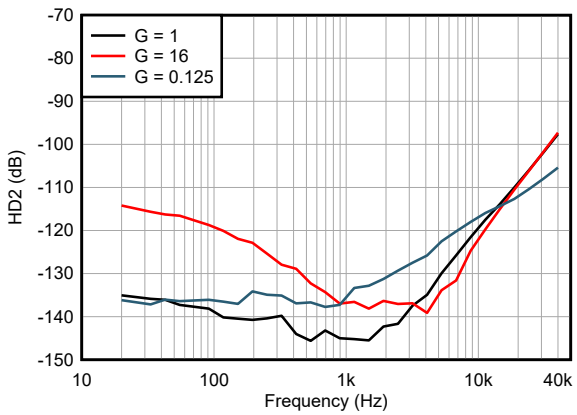
10-Hz to 22-kHz band-pass filter $V_{OUTDIFF}$ > 2.5 V_{PP}

Figure 7-32. Total Harmonic Distortion + Noise vs Frequency



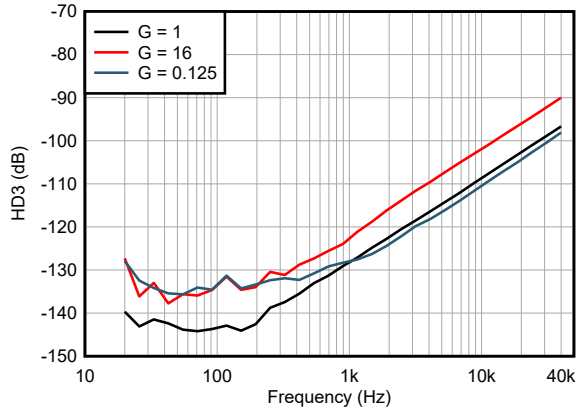
10-Hz to 500-kHz band-pass filter $V_{OUTDIFF}$ > 2.5 V_{PP}

Figure 7-33. Total Harmonic Distortion + Noise vs Frequency



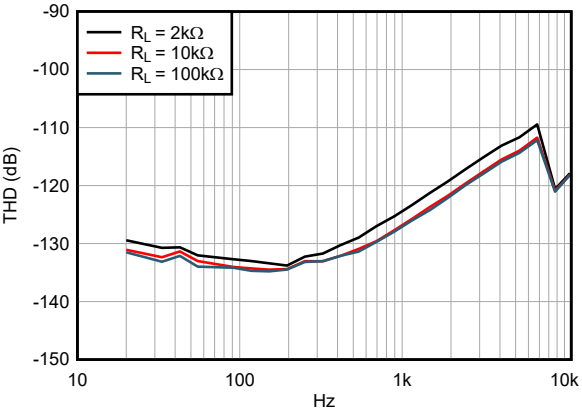
$V_{OUTDIFF}$ > 2.5 V_{PP}

Figure 7-34. 2nd Harmonic Distortion vs Frequency



$V_{OUTDIFF}$ > 2.5 V_{PP}

Figure 7-35. 3rd Harmonic Distortion vs Frequency



G = 1 V/V $V_{OUTDIFF}$ = 10 V_{PP}

Figure 7-36. Total Harmonic Distortion vs Frequency

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8 Detailed Description

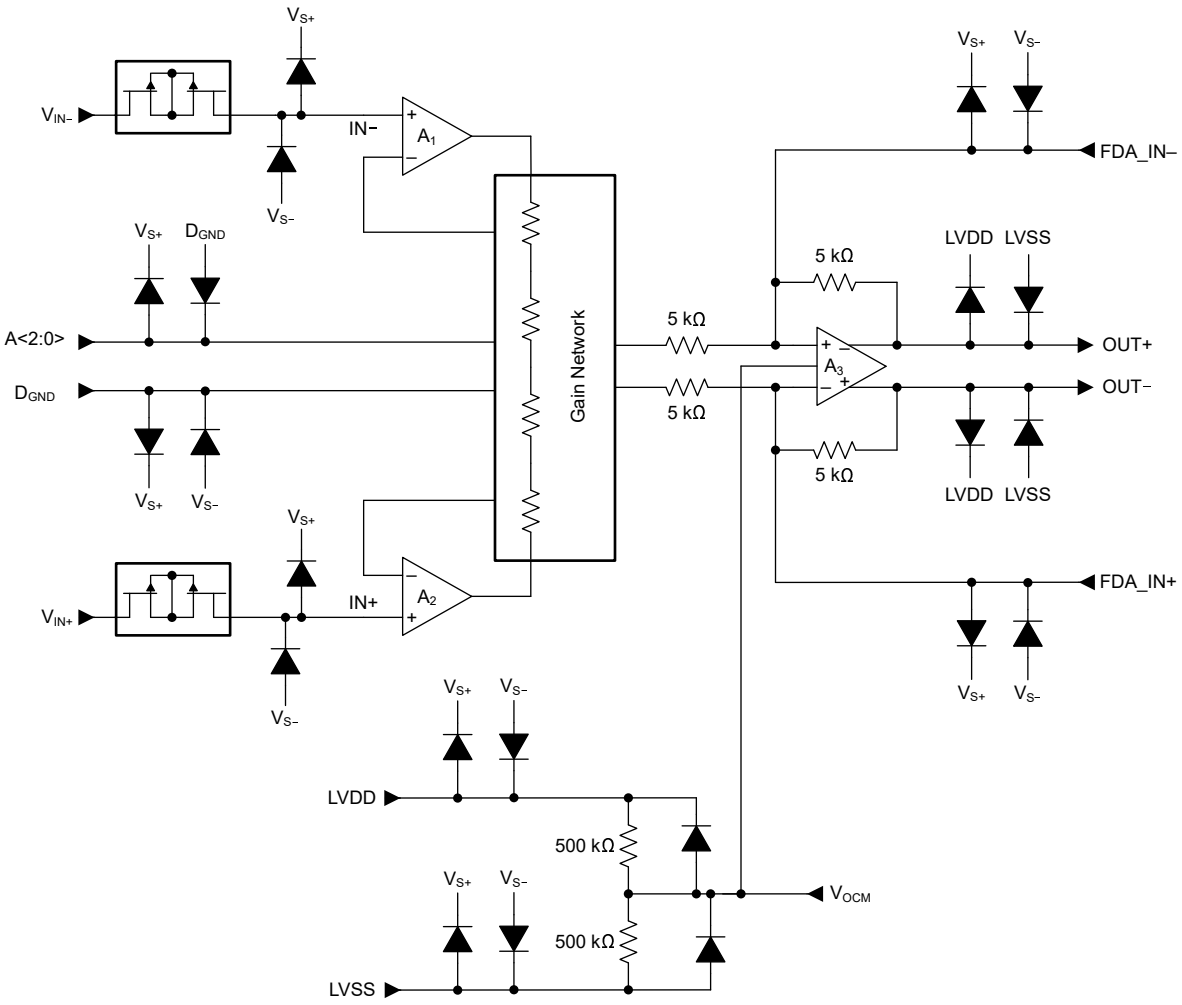
8.1 Overview

The PGA855 is a monolithic, high-voltage, precision programmable-gain instrumentation amplifier. The PGA855 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, fully differential amplifier output stage. Eight preprogrammed binary gains, ranging from 0.125 V/V to 16 V/V are selectable using gain-select pins A0, A1, and A2.

A functional block diagram for PGA855 is shown in the next section. The differential input voltage is fed into a pair of matched, high-impedance input-current-feedback amplifiers. An integrated precision-matched gain resistor network is used to amplify the differential input voltage. A fully differential output difference amplifier, A_3, rejects the input common-mode component and refers the output signal to the voltage level set by the VOCM pin.

The PGA855 output amplifier bandwidth is optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1 MSPS, without the need for an additional ADC driver. The output amplifier uses a separate power supply that is independent of the input-stage power supply. When driving an ADC, use a low-impedance connection from LVDD and LVSS to the ADC power supplies. This configuration protects the ADC inputs from damage due to inadvertent overvoltage conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Gain Control

The PGA855 uses three pins to set the amplifier gain. These gain select pins are set with respect to DGND. This configuration simplifies design when compared to programmable-gain amplifiers requiring an SPI or other digital interface options for gain changes. Figure 8-1 shows the gain-setting block diagram. Table 8-1 lists the gain options. Any gain select pin that is not driven by an external source is automatically biased at DGND using internal pulldown options.

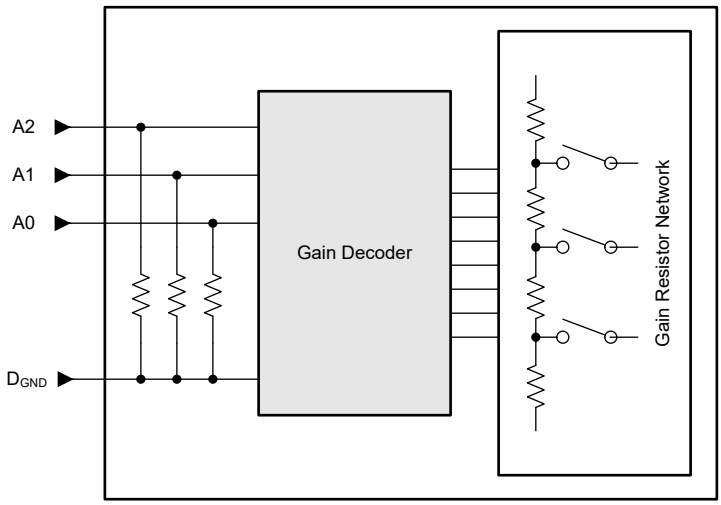


Figure 8-1. PGA855 Gain Setting Block Diagram

Table 8-1. Gain Options

A2:A0	GAIN
000	0.125
001	0.25
010	0.5
011	1
100	2
101	4
110	8
111	16

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8.3.2 Input Protection

The inputs of PGA855 are individually protected for voltages up to ±40 V beyond either supply. For example, an input common-mode voltage anywhere between –55 V and +55 V does not cause damage when powered from ±15-V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions, thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8 mA. Figure 8-2 shows the input protection functionality during an overvoltage condition.

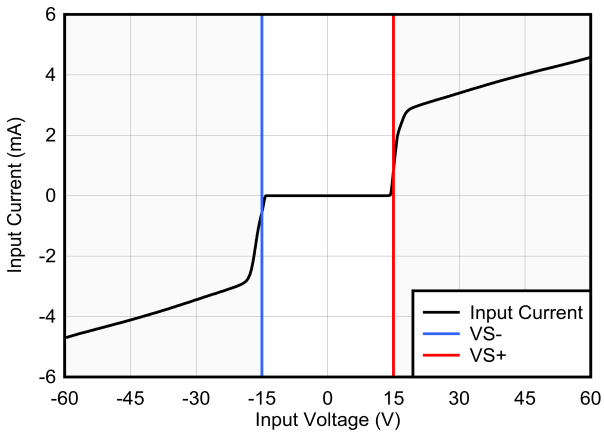

Figure 8-2. Input Current vs Input Overvoltage

Figure 8-3 shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. In applications where the power supplies are unable to sink current, place Zener diode clamps (ZD1 and ZD2) on the power supplies to provide a current pathway to ground.

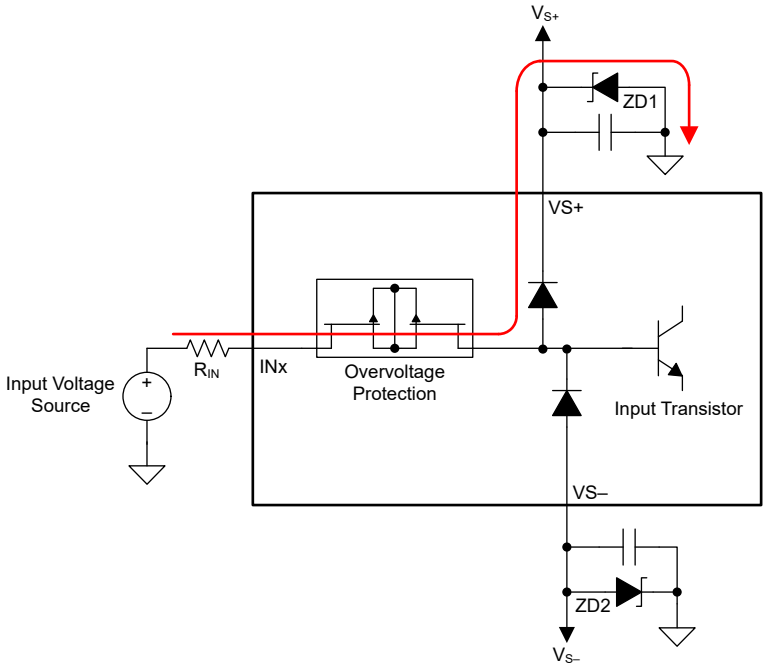

Figure 8-3. Input Current Path During an Overvoltage Condition

8.3.3 Output Common-Mode Pin

The output voltages of the PGA855 are balanced with respect to the voltage on the output common-mode pin, V_{OCM}. The starting point for most designs is to assign an output common-mode voltage for the PGA855. For ac-coupled signal paths, this voltage is often the default mid-supply voltage, so as to retain the most available output swing around the voltage centered at V_{OCM}. For dc-coupled signal paths, set this voltage between a maximum of V_{LVDD} – 1.5 V and minimum of V_{LVSS} + 1.5 V. For precision ADC applications, this voltage is typically the input common-mode voltage of the ADC.

The voltage at the V_{OCM} pin is internally buffered to bias the fully differential output amplifier, eliminating the need for an external V_{OCM} buffer. In the event that the V_{OCM} pin is left floating, the output common-mode voltage is biased at output mid-supply using an internal 500-kΩ / 500-kΩ resistor divider network connected between the output-stage power-supply pins.

8.3.4 Using the Fully Differential Output Amplifier to Shape Noise

Section 8.2 shows that the PGA855 output-stage fully-differential amplifier uses 5-kΩ feedback resistors between the OUT+ and OUT– outputs and the inverting and noninverting inputs, respectively. External direct access to the inverting and noninverting inputs of the fully differential amplifier is provided through the FDA_IN– and FDA_IN+ pins, respectively. This option allows circuit designers to add external feedback capacitors in parallel with the internal feedback resistors to implement noise-filtering or noise-shaping techniques. These pins can also be used to implement customized attenuating gains for the output stage. Consider the following important factors when designing parallel circuits with the internal feedback resistors:

- The accuracy of the internal resistor network is 0.01 % or better. This accuracy results in a common-mode rejection (CMRR) of 80 dB or better. Mismatched leakage currents on these pins can cause CMRR degradation.
- The internal resistors have ±15% absolute resistance variation and must be considered when implementing custom attenuating gains or noise filters.
- **CAUTION**
  Do not treat these pins as outputs, nor use the pins to source or sink current. Excessive currents through the feedback resistors can cause permanent damage to internal circuitry.

8.4 Device Functional Modes

The PGA855 has a single functional mode and operates when the input-stage power supply is greater than ±4 V (8 V) and the output-stage power supply is greater than ±2.25 V (4.5 V); see also Section 7.3.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The PGA855 is a monolithic, high-voltage, high bandwidth, precision programmable gain instrumentation amplifier with fully differential outputs. The PGA855 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, fully differential amplifier output stage. The PGA855 is equipped with 8 binary-gain settings, from 0.125 V/V to 16 V/V, using three digital gain-selection pins: A0, A1, and A2.

The PGA855 is designed to work with applications such as factory automation and control, analog input modules, data acquisition, test and measurement, and semiconductor test.

9.2 Typical Applications

9.2.1 ADS127L11, 24-Bit, Delta-Sigma ADC Driver Circuit

The application circuit in Figure 9-1 shows a schematic for a 24-bit wide-bandwidth, delta-sigma ADC. The ADS127L11 ADC offers two digital filters to optimize ac applications (wideband filter) or dc applications (sinc4 filter). Table 9-2 and Table 9-3 show measurement results in both filter settings. For a detailed design procedure to operate the ADS127L11 ADC, see the ADS127L11EVM-PDK evaluation module user's guide.

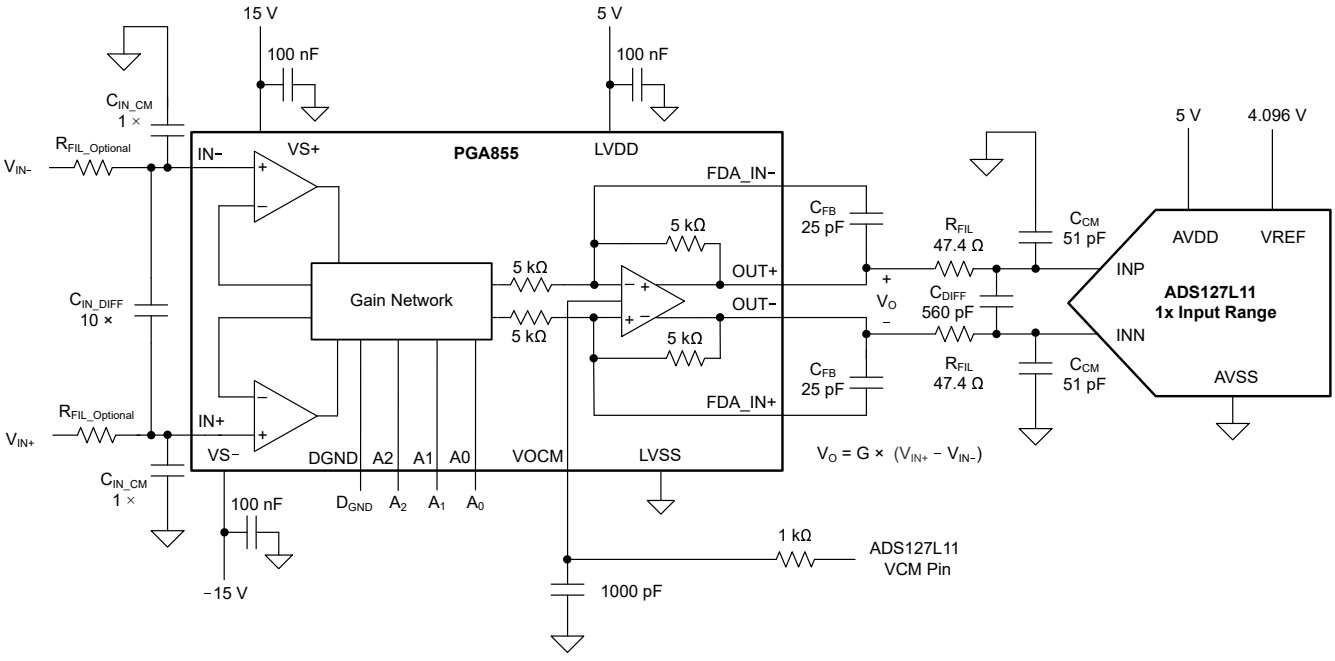

Figure 9-1. Driving the Delta-Sigma ADC ADS127L11

9.2.1.1 Design Requirements

The design requirements for the application driving the ADS127L11 ADC are listed in the following table.

Table 9-1. Design Parameters

PARAMETER	VALUE
Differential-to-differential conversion	V_{INDIFF} to $V_{OUTDIFF}$
Supply voltages	$V_{S\pm}$ = ±15 V, LVDD = 5 V, LVSS = GND, VREF = 4.096 V
Full-scale range of ADC	FSR = ± 4.096 V
Data rate of ADC	f_{DATA} = 187.5 kSPS
ADC filter configuration	(1) High-speed mode, Sinc4 filter, OSR = 64
	(2) High-speed mode, Wideband filter, OSR = 64
PGA gain	See Table 9-2 and Table 9-3
Signal frequency	Tested at f_{IN} = 1 kHz
RC kickback filter(1)	R_{FIL} = 47.4 Ω, C_{DIFF} = 560 pF, C_{CM} = 51 pF

(1) A trade-off must be considered between THD, frequency response and drift. The differential current drift into the ADC can interact with the filter resistors and result in higher drift errors. However, lower resistance degrades the phase margin of the PGA855. For low drift applications, keep R_{FIL} < 50 Ω.

9.2.1.2 Detailed Design Procedure

Table 9-2 and Table 9-3 show the typical signal-to-noise (SNR) and total harmonic distortion (THD) of the PGA855 driving the ADS127L11 delta-sigma ADC using a sinc4 or wideband filter. Figure 9-2 and Figure 9-3 show the respective FFT plots. For the SNR and THD measurements, a 1-kHz differential signal is applied. The signal amplitude is adjusted to produce a PGA855 output at –0.2 dBFS of the ADC full-scale range. For a list of the equivalent input voltage amplitude signals for the different PGA855 gain configurations, see Table 9-2 and Table 9-3.

The R-C-R differential low-pass filter at the input of the instrumentation amplifier helps reduce EMI/RFI high-frequency extrinsic noise. This filter can be customized per the bandwidth and application requirements. This design example (see Figure 9-1) suggests a filter with the capacitor ratio of C_{IN_DIFF} = 10 × C_{IN_CM}. Using the 10-to-1 ratio for differential capacitor C_{IN_DIFF} versus common-mode capacitors C_{IN_CM} offers good differential and common-mode noise rejection, and this arrangement tends to be less sensitive to the tolerance variation and mismatch of the filter capacitors.

The feedback capacitor, C_{FB}, is in parallel with the PGA855 output-stage 5-kΩ feedback resistors to implement additional noise filtering. The internal resistors have ±15 % absolute resistance variation, and this variation must be taken in to account when implementing noise filtering. In this example, C_{FB} is set to 25 pF, providing a typical $f_{–3dB}$ corner frequency of 1 MHz. The estimated minimum $f_{–3dB}$ corner frequency for this circuit is approximately 938 kHz when accounting for the feedback-resistor variation.

The filter at the ADS127L11 inputs works as a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that otherwise can degrade because of incomplete amplifier settling. The ADC input filter values are R_{FIL} = 47.4 Ω, C_{DIFF} = 560 pF, and C_{CM} = 51 pF.

High-grade COG (NPO) are used everywhere in the signal path (C_{IN_DIFF}, C_{IN_CM}, C_{FB}, C_{DIFF}, C_{CM}) for low distortion. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance accuracy. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

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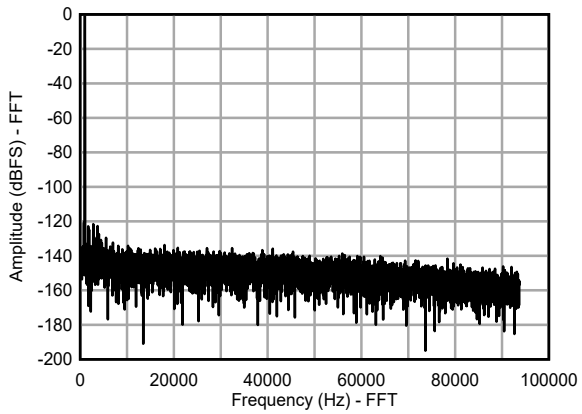
Table 9-2. PGA855 and ADS127L11 FFT Data Summary, OSR = 64, Sinc4 Filter

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	SNR (dB)	THD (dB)	ENOB (Bits)
0.125	—	—	—	—
0.25	16.011	109.0	–119.3	17.8
0.5	8.006	109.8	–121.2	17.9
1	4.003	109.6	–121.4	17.9
2	2.001	109.6	–121.4	17.9
4	1.001	107.4	–121.4	17.5
8	0.500	104.0	–121.4	17.0
16	0.250	99.1	–117.0	16.2

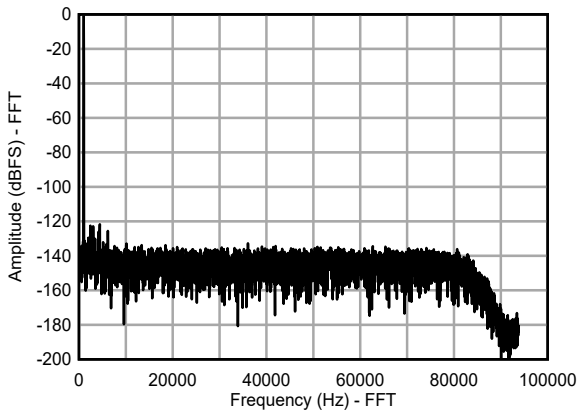
Table 9-3. PGA855 and ADS127L11 FFT Data Summary, OSR = 64, Wideband Filter

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	SNR (dB)	THD (dB)	ENOB (Bits)
0.125	—	—	—	—
0.25	16.011	107.5	–119.0	17.5
0.5	8.006	107.7	–121.2	17.6
1	4.003	107.6	–121.4	17.6
2	2.001	107.0	–121.4	17.5
4	1.001	105.4	–121.4	17.2
8	0.500	101.7	–121.4	16.6
16	0.250	96.7	–117.0	15.8



G = 1 V/V, f_{IN} = 1 kHz, SNR = 109.6 dB, THD = –121.4 dB

Figure 9-2. Performance FFT Plots With ADS127L11, OSR = 64, Sinc4 Filter



G = 1 V/V, f_{IN} = 1 kHz, SNR = 107.6 dB, THD = –121.4 dB

Figure 9-3. Performance FFT Plots With ADS127L11, OSR = 64, Wideband Filter

9.3 Power Supply Recommendations

The nominal performance of the PGA855 is specified with input-stage supply and output-stage supply voltages of ±15 V, and V_{ICM} and V_{OCM} at mid-supply. Within the specified limits, custom input and output common-mode voltages can be used without compromising performance; see also Section 7.3.

CAUTION

To prevent damage to internal circuitry, the output-stage power supplies are clamped to stay within the input-stage supply voltage levels; see Section 8.2.

9.4 Layout

9.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), make sure that both input paths are symmetrical and well-matched for source impedance and capacitance.
- Noise can propagate into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Leakage on the FDA_IN+ and FDA_IN– pins can cause in a dc offset error in the output voltages. Additionally, excessive parasitic capacitance at these pins can result in decreased phase margin and affect the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance.
- Follow best practices to minimize leakage and parasitic capacitance, which includes implementing *keep-out* areas in any ground planes that lie immediately below the input pins.
- Minimize the number of thermal junctions. If possible, route the signal path using a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the effects of the thermal energy source on the high and low sides of the differential signal path are evenly matched.
- Keep the traces as short as possible.

9.4.2 Layout Example

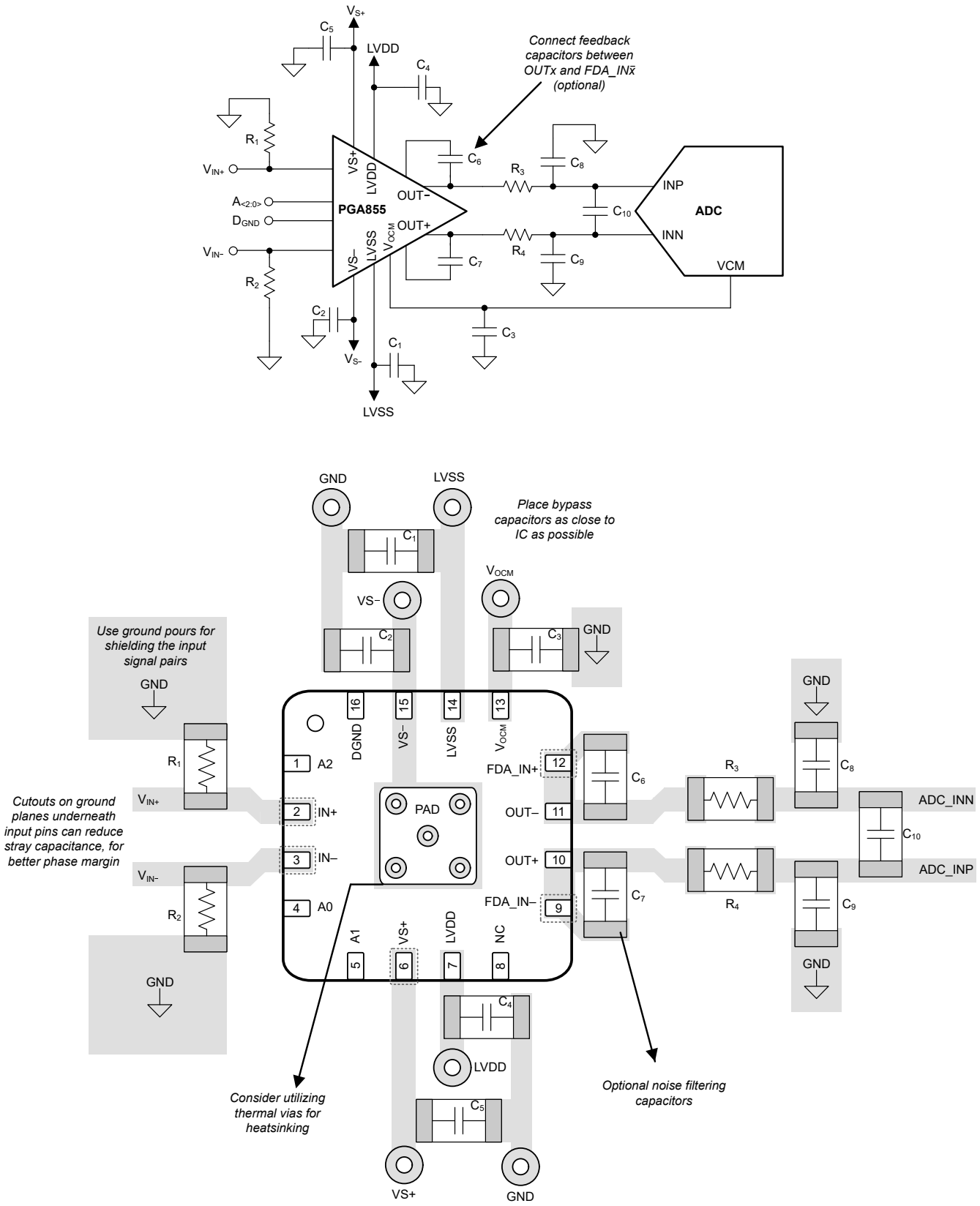


Figure 9-4. Example Schematic and Associated PCB Layout

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note
- Texas Instruments, *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XPGA855RGTR	ACTIVE	VQFN	RGT	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

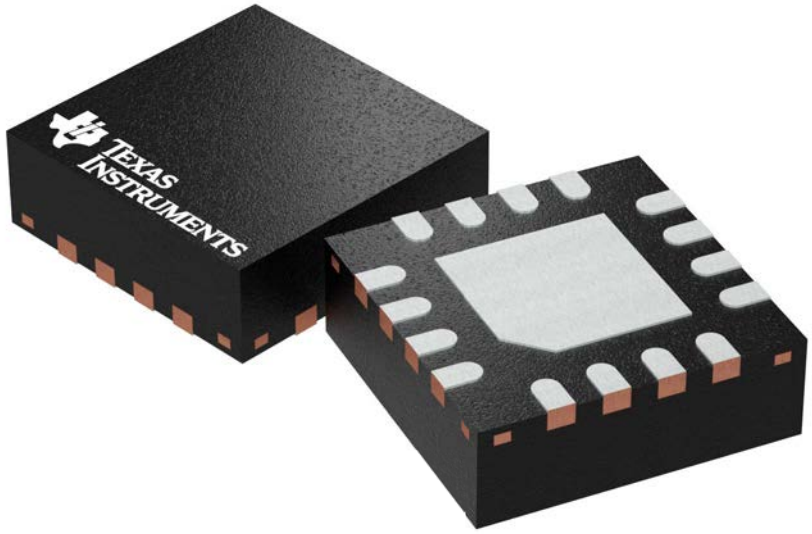
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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