



## PD54008L-E

RF power transistors  
The LdmoST Plastic family

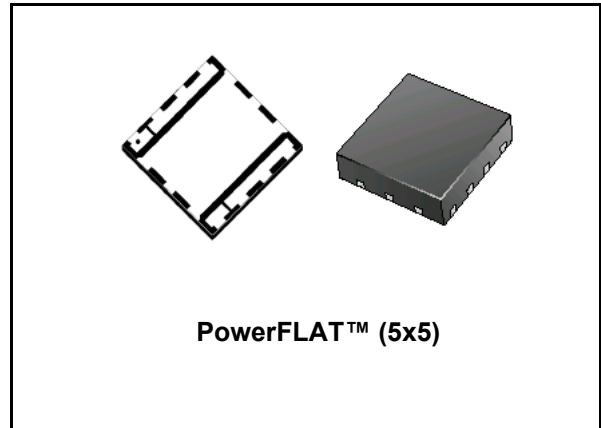
### Features

- Excellent thermal stability
- Common source configuration
- Broadband performances  $P_{OUT} = 8W$  with 15 dB gain @ 500MHz
- New leadless plastic package
- EDS protection
- Supplied in tape & reel of 3K units
- In compliance with the 2002/93/EC european directive

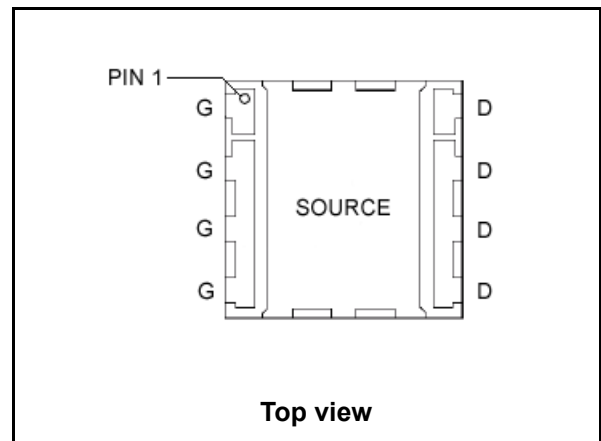
### Description

The PD54008L-E is a common source N-Channel, enhancement-mode lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 7 V in common source mode at frequencies of up to 1 GHz. PD54008L-E boasts the excellent gain, linearity and reliability of STH1LV latest LDMOS technology mounted in the innovative leadless SMD plastic package, PowerFLAT™.

PD54008L-E's superior linearity performance makes it an ideal solution for portable radio.



### Pin connection



### Order codes

Part Number	Marking	Package	Packaging
PD54008L-E	54008	PowerFLAT (5x5)	Tape & Reel

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# 1 Electrical data

## 1.1 Maximum ratings

**Table 1. Absolute maximum ratings** ( $T_{CASE} = 25^{\circ}C$ )

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain source voltage	25	V
$V_{GS}$	Gate-source voltage	-0.5 to +15	V
$I_D$	Drain current	5	A
$P_{DISS}$	Power dissipation ( $t_{CASE} = 70^{\circ}C$ )	26.7	W
$T_J$	Maximum operating junction temperature	150	$^{\circ}C$
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}C$

## 1.2 Thermal data

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction to case thermal resistance	3	$^{\circ}C/W$

## 1.3 Electrical characteristics

**Table 3. Static** ( $T_{CASE} = 25^{\circ}C$ )

Symbol	Test conditions			Min	Typ	Max	Unit
$I_{DSS}$	$V_{GS} = 0V$	$V_{DS} = 25V$				1	$\mu A$
$I_{GSS}$	$V_{GS} = 5V$	$V_{DS} = 0V$				1	$\mu A$
$V_{GS(Q)}$	$V_{DS} = 10V$	$I_D = 50mA$		2.0		5.0	V
$V_{DS(ON)}$	$V_{GS} = 10V$	$I_D = 0.5A$			0.09		V
$C_{ISS}$	$V_{GS} = 0V$	$V_{DS} = 7.5V$	$f = 1MHz$		80		pF
$C_{OSS}$	$V_{GS} = 0V$	$V_{DS} = 7.5V$	$f = 1MHz$		60		pF
$C_{RSS}$	$V_{GS} = 0V$	$V_{DS} = 7.5V$	$f = 1MHz$		6.6		pF

**Table 4. Dynamic**

Symbol	Test conditions			Min.	Typ.	Max.	Unit
$P_{1dB}$	$V_{DD} = 7.5 V$	$I_{DQ} = 200 mA$	$f = 500MHz$	8			W
$G_{PS}$	$V_{DD} = 7.5 V$	$I_{DQ} = 200 mA$	$P_{OUT} = 8 W$	$f = 500MHz$	15		dB
$\eta_D$	$V_{DD} = 7.5 V$	$I_{DQ} = 200 mA$	$P_{OUT} = 8 W$	$f = 500MHz$	50		%
Load Mismatch	$V_{DD} = 7.5 V$	$I_{DQ} = 200 mA$	$P_{OUT} = 8W$	$f = 500MHz$	20:1		VSW R

**Table 5. ESD protection characteristics**

Test conditions	Class
Human body model	2
Machine model	M3

**Table 6. Moisture sensitivity level**

Test methodology	Rating
J-STD-020B	MSL 3

## 2 Impedances

Figure 1. Impedance data schematic

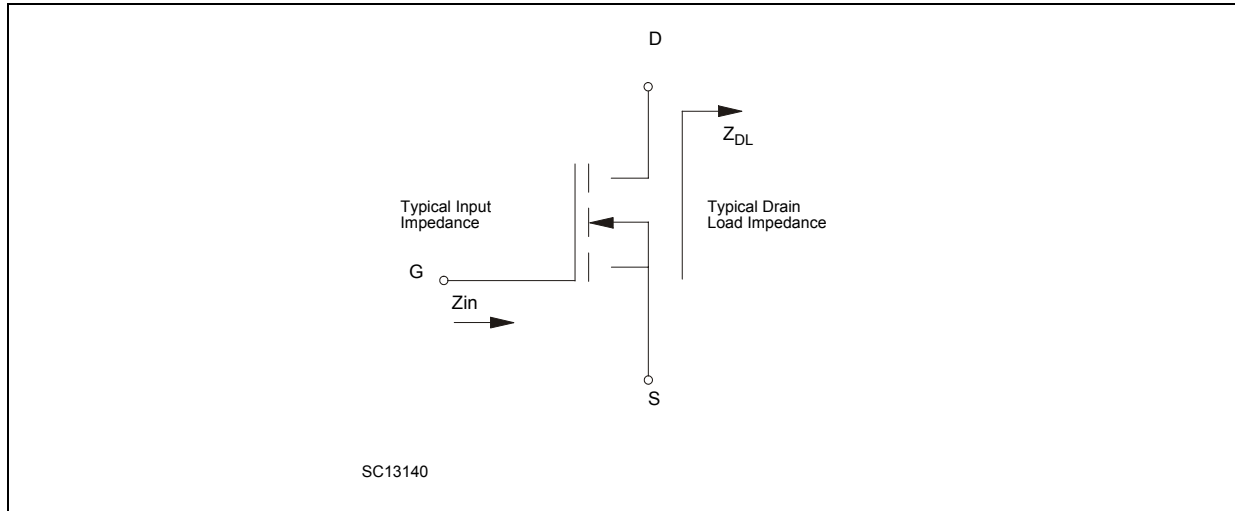


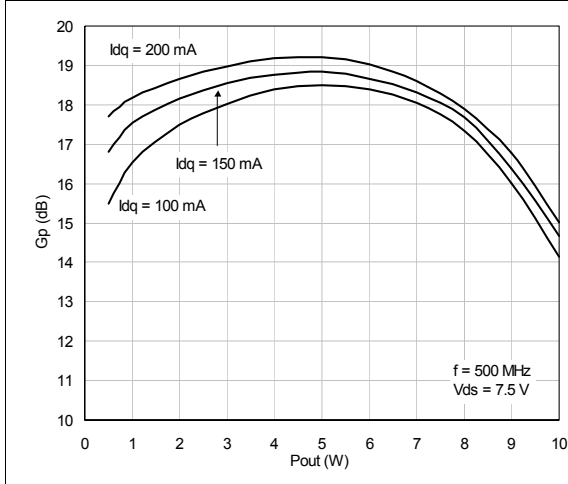
Table 7. Impedance data (1)

f	$Z_{IN} (\Omega)$	$Z_{DL} (\Omega)$
480MHz	$1.12 - j 2.02$	$2.01 + j 0.13$
500MHz	$1.3 - j 2.01$	$1.84 + j 0.7$
520MHz	$1.66 - j 2.55$	$1.66 + j 1.51$

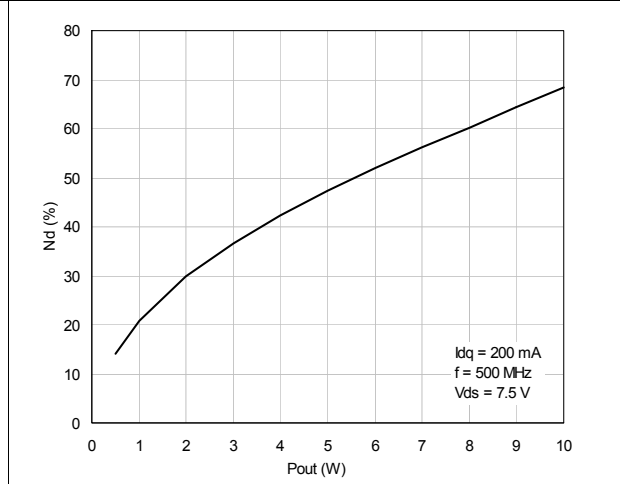
1. In Broadband amplifier

### 3 Typical performance

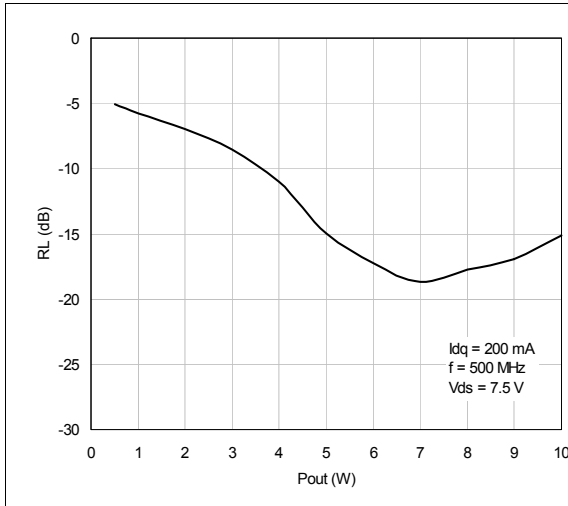
**Figure 2. Power gain vs output power**



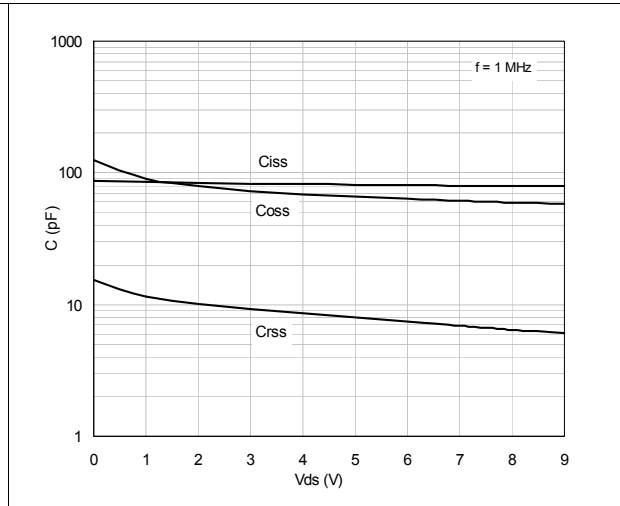
**Figure 3. Efficiency vs output power**



**Figure 4. Return loss vs output power**



**Figure 5. Capacitance vs supply voltage**



### 3.1 Typical performance (Broadband)

Figure 6. Power gain vs frequency

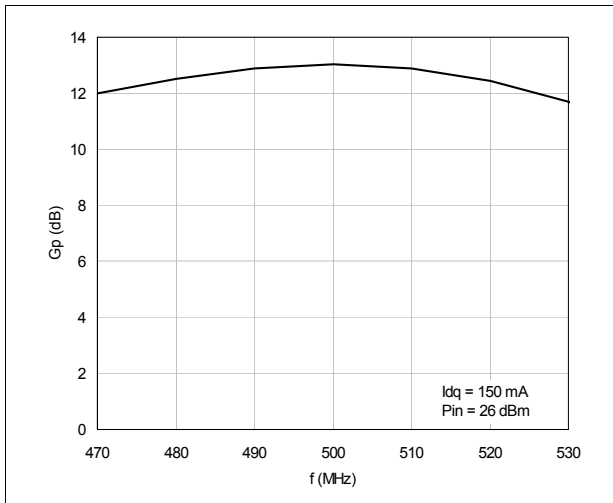


Figure 7. Efficiency vs frequency

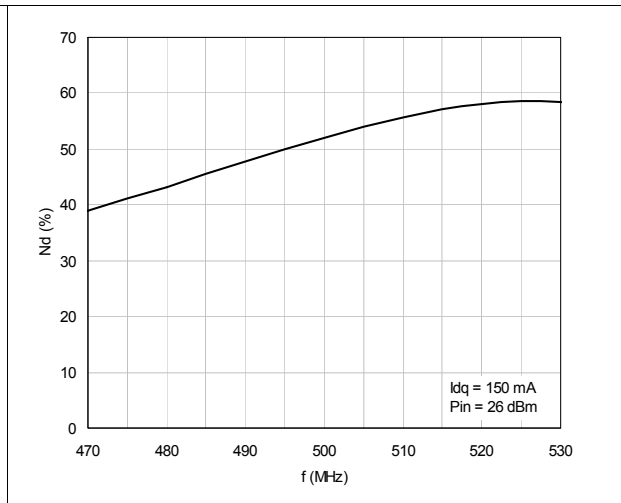
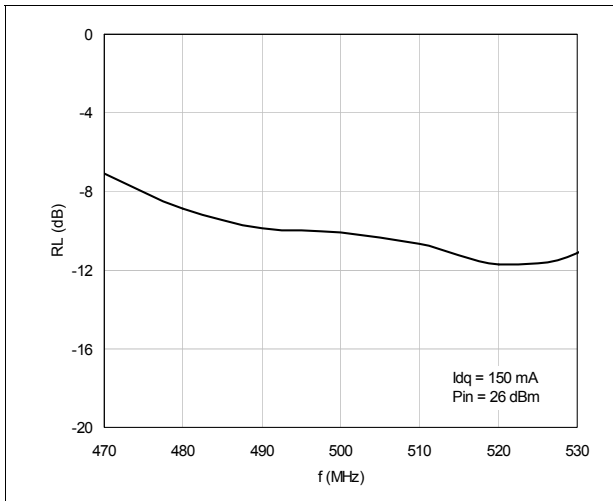


Figure 8. Return loss vs frequency



## 4 Test circuit schematic

Figure 9. Internal schematic

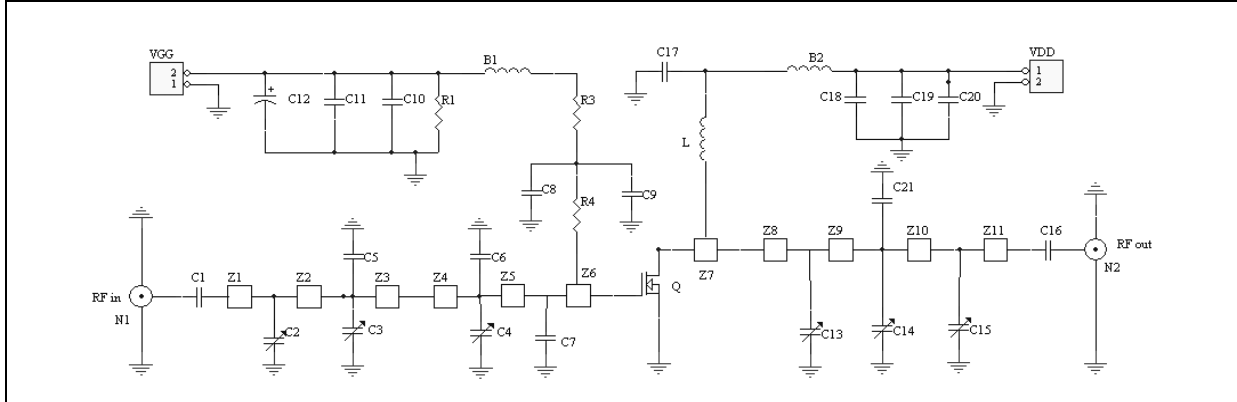


Table 8. Test circuit component part list

Component	Description
B1, B2	Ferrite bead
C1, C16	300 pF, 100 mil ATC
C2, C3, C4, C13,C14	1 -:- 20 pF Trimmer cap - JOHANSON
C15	0.8 -:- 10 pF Trimmer cap - JOHANSON
C5	36 pF, 100 mil ATC
C6	51 pF, 100 mil ATC
C7	62 pF, 100 mil ATC
C8, C17	150 pF, 100 mil CHIP CAP
C9	1 nF, 100 mil CHIP CAP
C10, C18	1000 pF, 100 mil CHIP CAP
C11, C19	0.1 nF, 100 mil CHIP CAP
C12, C20	10 $\mu$ F 50 V Electrolytic Capacitor
C21	15 pF, 100 mil ATC
L	43nH, Coilcraft
R1	33 K $\Omega$ , 1W CHIP Resistor
R3	1 K $\Omega$ , 1W CHIP Resistor
R4	15 $\Omega$ , 1W CHIP Resistor
Z1	0.49" X 0.080" MICROSTRIP
Z2	1.024" X 0.080" MICROSTRIP
Z3	0.079" X 0.080" MICROSTRIP
Z4	0.24" X 0.223" MICROSTRIP
Z5	0.079" X 0.223" MICROSTRIP



**Table 8. Test circuit component part list**

Z6	0.138" X 0.223" MICROSTRIP
Z7	0.259" X 0.223" MICROSTRIP
Z8	0.079" X 0.080" MICROSTRIP
Z9	0.413" X 0.080" MICROSTRIP
Z10	0.756" X 0.080" MICROSTRIP
Z11	0.61" X 0.080" MICROSTRIP
N1, N2	Type N Flange Mount
Board	ROGER, ULTRA LAM 2000 THK 0.030", $\epsilon_r = 2.55$ 2oz. ED cu SIDES

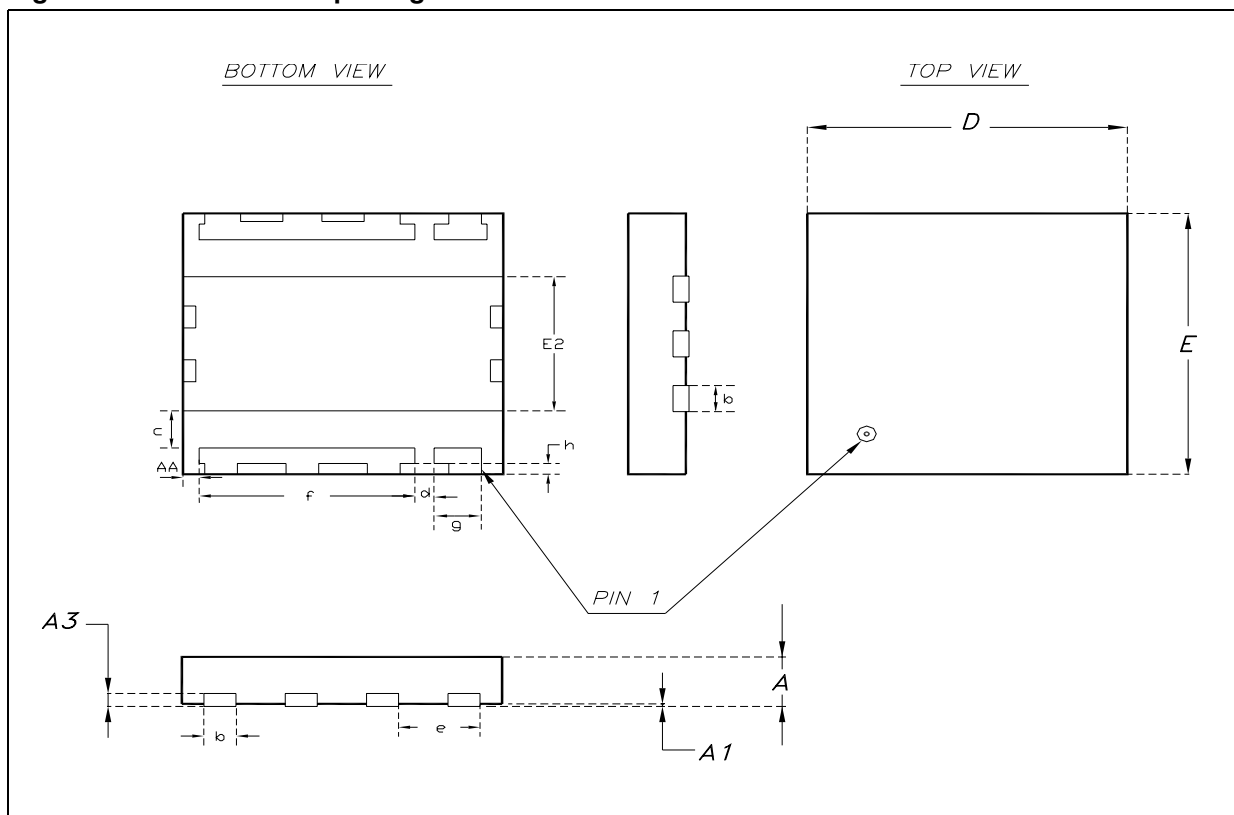
## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Table 9. PowerFLAT™ mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.24			0.009	
AA	0.15	0.25	0.35	0.006	0.01	0.014
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.64	0.71	0.79	0.025	0.028	0.031
D		5.00			0.197	
d		0.30			0.011	
E		5.00			0.197	
E2	2.49	2.57	2.64	0.098	0.101	0.104
e		1.27			0.050	
f		3.37			0.132	
g		0.74			0.03	
h		0.21			0.008	

Figure 10. PowerFLAT™ package dimensions



**Table 10. PowerFLAT™ tape & reel dimensions**

DIM.	mm.		
	Min.	Typ	Max.
Ao	5.15	5.25	5.35
Bo	5.15	5.25	5.35
Ko	1.0	1.1	1.2

**Figure 11. PowerFLAT™ tape & reel**

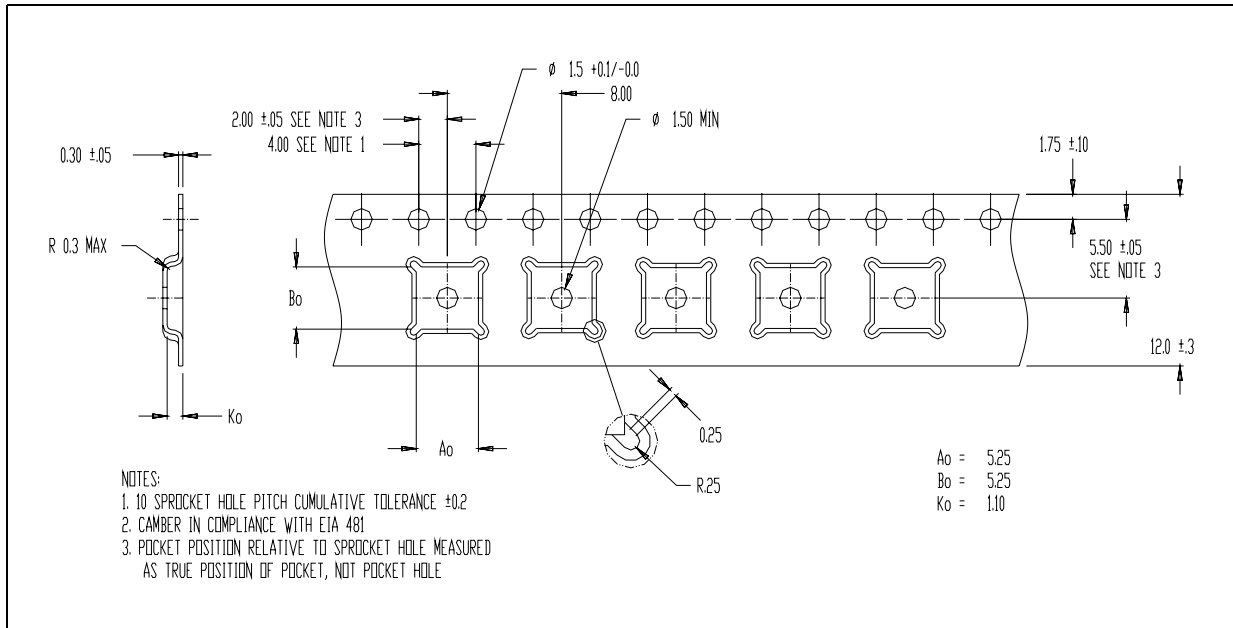
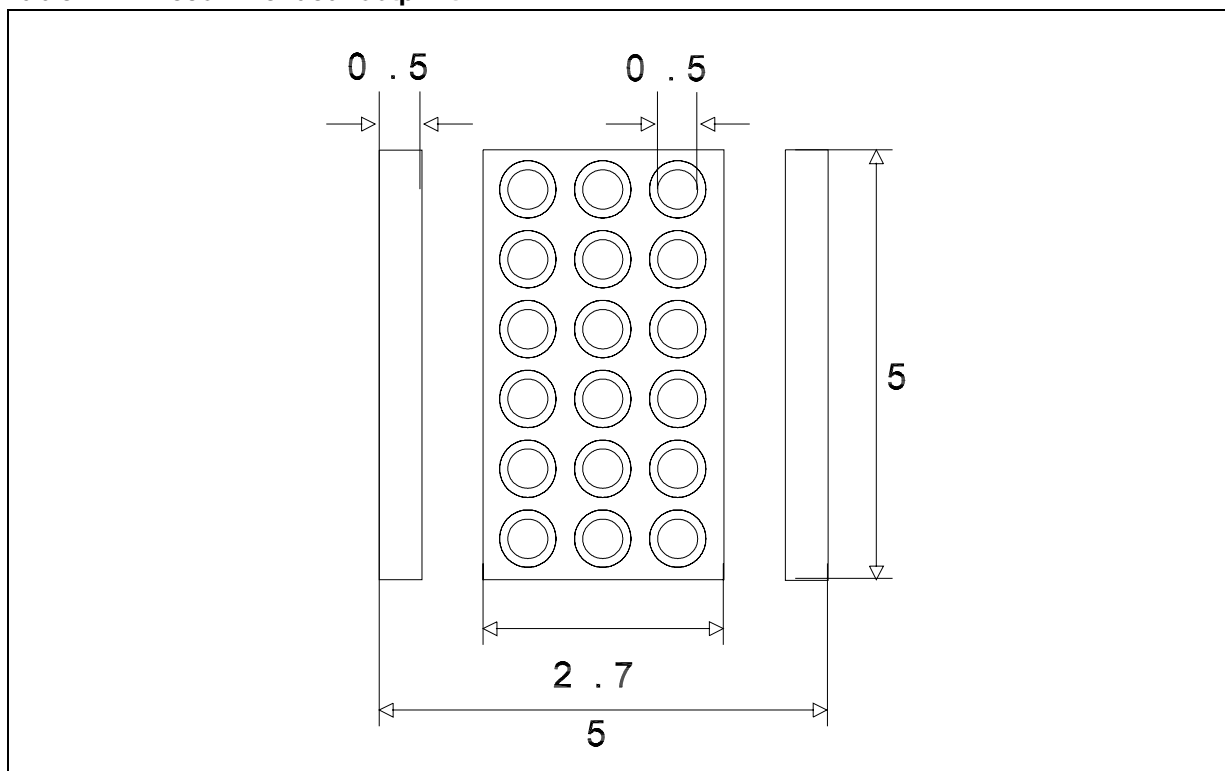


Table 11. Recommended footprint



## 6 Revision history

**Table 12. Revision history**

Date	Revision	Changes
19-Jan-2006	1	First Issue
23-Jan-2007	2	Document has been reformatted

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