TEXAS INSTRUMENTS

PCA9554

SCPS128C – JULY 2006 – REVISED JUNE 2014

PCA9554 Remote 8-Bit I²C AND SMBus I/O Expander With Interrupt Output and Configuration Registers

1 Features

- I²C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant I/Os
- 400-kHz Fast I²C Bus
- Three Hardware Address Pins Allow up to Eight Devices on the I²C/SMBus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- Power-Up With All Channels Configured as Inputs
- No Glitch On Power Up
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

This 8-bit I/O expander for the two-line bidirectional bus (I²C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL), serial data (SDA)].

The PCA9554 consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs with a weak pullup to V_{CC}. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the PCA9554 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I²C/SMBus state machine.
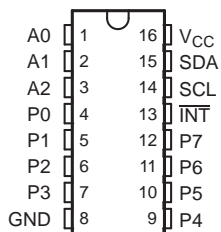
The PCA9554 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.
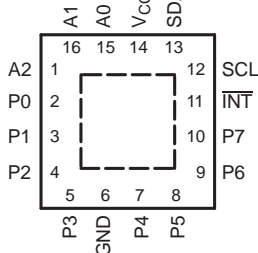
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9554	SSOP (16)	6.20 mm × 5.30 mm
	VQFN (16)	4.00 mm × 4.00 mm
	QFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

A0	1	16	V_{CC}
A1	2	15	SDA
A2	3	14	SCL
P0	4	13	$\overline{INT}$
P1	5	12	P7
P2	6	11	P6
P3	7	10	P5
GND	8	9	P4

RGV PACKAGE
(TOP VIEW)

Top pins: A1 (16), A0 (15), V_{CC} (14), SDA (13)
Left pins: A2 (1), P0 (2), P1 (3), P2 (4)
Right pins: SCL (12), $\overline{INT}$ (11), P7 (10), P6 (9)
Bottom pins: P3 (5), GND (6), P4 (7), P5 (8)

RGT PACKAGE
(TOP VIEW)

Top pins: A1 (16), A0 (15), V_{CC} (14), SDA (13)
Left pins: A2 (1), P0 (2), P1 (3), P2 (4)
Right pins: SCL (12), $\overline{INT}$ (11), P7 (10), P6 (9)
Bottom pins: P3 (5), GND (6), P4 (7), P5 (8)

Table of Contents

3   Revision History

Changes from Revision B (August 2008) to Revision C   **Page**

Product Folder Links: *PCA9554*

4 Description (Continued)

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Thus, the PCA9554 can remain a simple slave device.

The device's outputs (latched) have high-current drive capability for directly driving LEDs and low current consumption.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I²C address and allow up to eight devices to share the same I²C bus or SMBus.

The PCA9554 is pin-to-pin and I²C address compatible with the PCF8574. However, software changes are required, due to the enhancements in the PCA9554 over the PCF8574.
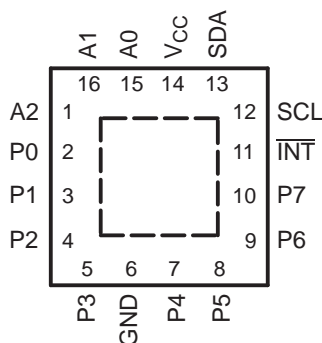
The PCA9554 and PCA9554A are identical except for their fixed I²C address. This allows for up to 16 of these devices (eight of each) on the same I²C/SMBus.
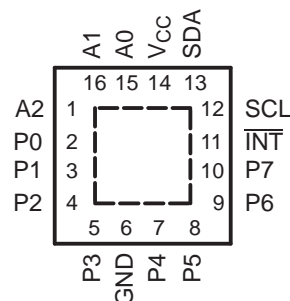
5 Pin Configuration and Functions

DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)
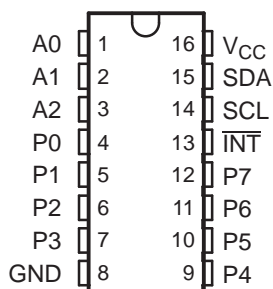
RGV PACKAGE (TOP VIEW)

RGT PACKAGE (TOP VIEW)

Pin Functions

PIN			DESCRIPTION
NAME	QSOP (DBQ) SOIC (DW), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGT) AND QFN (RGV)	
A0	1	15	Address input. Connect directly to V_{CC} or ground.
A1	2	16	Address input. Connect directly to V_{CC} or ground.
A2	3	1	Address input. Connect directly to V_{CC} or ground.
P0	4	2	P-port input/output. Push-pull design structure.
P1	5	3	P-port input/output. Push-pull design structure.
P2	6	4	P-port input/output. Push-pull design structure.
P3	7	5	P-port input/output. Push-pull design structure.
GND	8	6	Ground
P4	9	7	P-port input/output. Push-pull design structure.
P5	10	8	P-port input/output. Push-pull design structure.
P6	11	9	P-port input/output. Push-pull design structure.
P7	12	10	P-port input/output. Push-pull design structure.
$\overline{INT}$	13	11	Interrupt output. Connect to V_{CC} through a pullup resistor.
SCL	14	12	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	15	13	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	16	14	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6	V
V_I	Input voltage range[2]		−0.5	6	V
V_O	Output voltage range[2]		−0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		−50	mA
I_{CC}	Continuous current through GND			−250	mA
	Continuous current through V_{CC}			160	mA
θ_{JA}	Package thermal impedance[3]	DB package		82	°C/W
		DBQ package		90	
		DGV package		120	
		DW package		57	
		N package		67	
		PW package		108	
		RGT package		TBD	
		RGV package		TBD	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		A2–A0, P7–P0	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	−0.5	$0.3 \times V_{CC}$	V
		A2–A0, P7–P0	−0.5	0.8	
I_{OH}	High-level output current	P7–P0		−10	mA
I_{OL}	Low-level output current	P7–P0		25	mA
T_A	Operating free-air temperature		−40	85	°C

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.3 V to 5.5 V	−1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, $I_O = 0$	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage [2]	$I_{OH} = -8$ mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	3.1			
			4.75 V	4.1			
		$I_{OH} = -10$ mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	3			
			4.75 V	4			
I_{OL}	SDA	$V_{OL} = 0.4$ V	2.3 V to 5.5 V	3	8		mA
	P port [3]	$V_{OL} = 0.5$ V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	35		
		$V_{OL} = 0.7$ V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	45		
	$\overline{INT}$	$V_{OL} = 0.4$ V	2.3 V to 5.5 V	3	10		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
	A2–A0					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	µA
I_{IL}	P port	$V_I = $ GND	2.3 V to 5.5 V			−100	µA
I_{CC}	Operating mode	$V_I = V_{CC}$, $I_O = 0$, I/O = inputs, $f_{scl} = 400$ kHz, No load	5.5 V		104	175	µA
			3.6 V		50	90	
			2.7 V		20	65	
		$V_I = V_{CC}$, $I_O = 0$, I/O = inputs, $f_{scl} = 100$ kHz, No load	5.5 V		60	150	
			3.6 V		15	40	
			2.7 V		8	20	
	Standby mode	$V_I = $ GND, $I_O = 0$, I/O = inputs, $f_{scl} = 0$ kHz, No load	5.5 V		450	700	
			3.6 V		300	600	
			2.7 V		225	500	
		$V_I = V_{CC}$, $I_O = 0$, I/O = inputs, $f_{scl} = 0$ kHz, No load	5.5 V		0.25	1	
			3.6 V		0.2	0.9	
			2.7 V		0.1	0.8	
ΔI_{CC}	Additional current in standby mode	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
		Every LED I/O at $V_I = 4.3$ V, $f_{scl} = 0$ kHz	5.5 V			1	
C_i	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	5	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5.5	6.5	pF
	P port				8	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and $T_A = 25°C$.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P0 to P7) must be limited to a maximum current of 200 mA.

6.5 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 14)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
t_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0		0		ns
t_{icr}	I²C input rise time			1000	$20 + 0.1C_b$ [(1)]	300	ns
t_{icf}	I²C input fall time			300	$20 + 0.1C_b$ [(1)]	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ [(1)]	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	300		50		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	0.1	0.9	µs
C_b	I²C bus capacitive load			400		400	ns

(1) C_b = Total capacitive load of one bus in pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 15 and Figure 16)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	µs
t_{pv}	Output data valid	SCL	P7–P0		200		200	ns
t_{ps}	Input data setup time	P port	SCL	100		100		ns
t_{ph}	Input data hold time	P port	SCL	1		1		µs

Product Folder Links: *PCA9554*
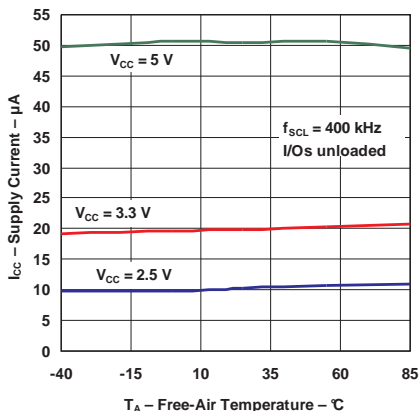
6.7 Typical Characteristics

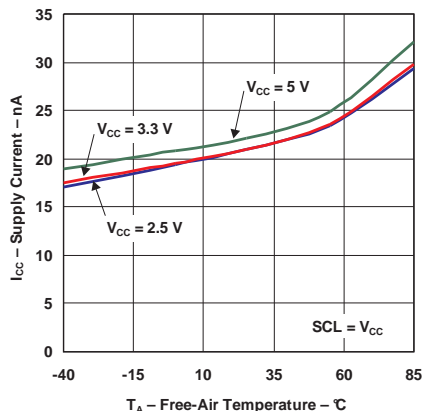Figure 1. Supply Current vs Temperature

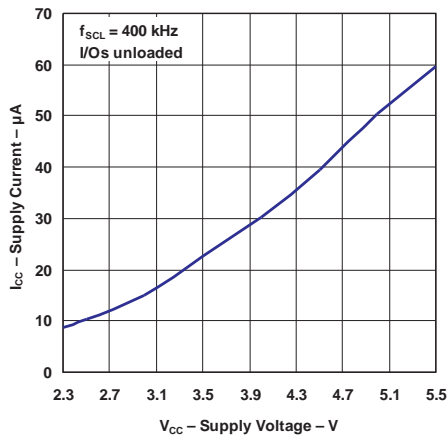Figure 2. Quiescent Supply Current vs Temperature

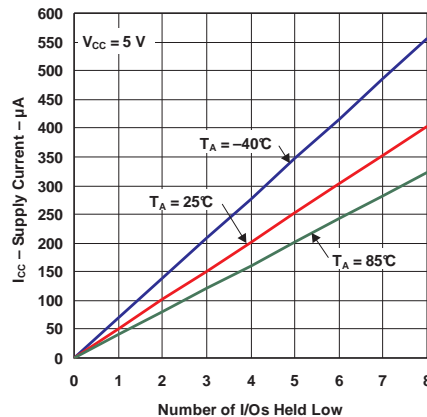Figure 3. Supply Current vs Supply Voltage
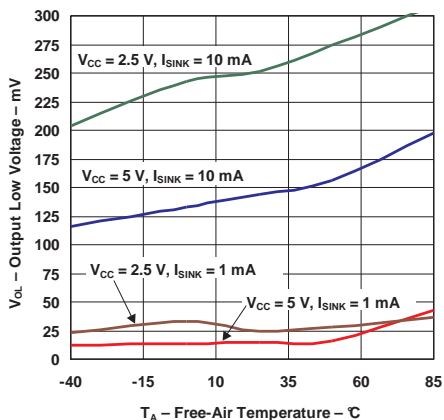

Figure 4. Supply Current vs Number Of I/Os Held Low
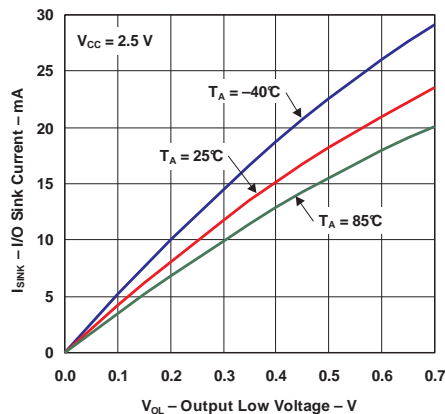

Figure 5. I/O Output Low Voltage vs Temperature
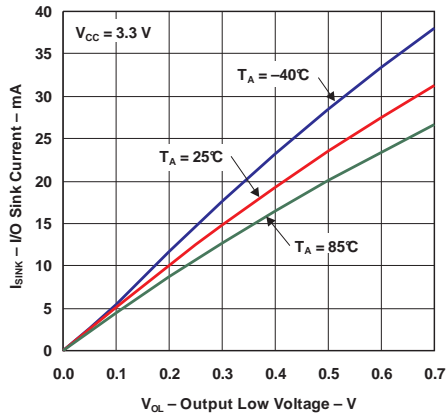

Figure 6. I/O Sink Current vs Output Low Voltage

Product Folder Links: *PCA9554*

Typical Characteristics (continued)

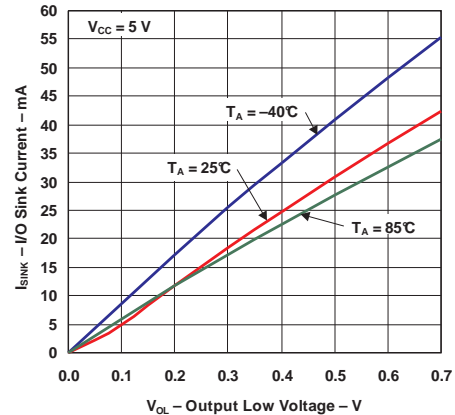Figure 7. I/O Sink Current vs Output Low Voltage

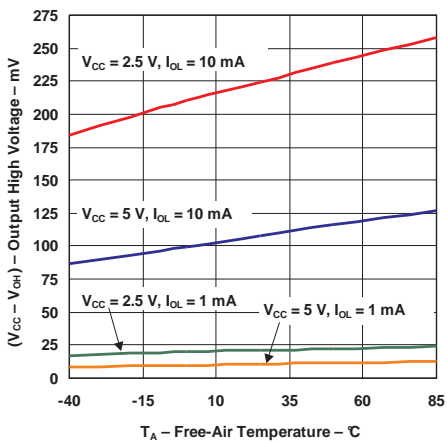Figure 8. I/O Sink Current vs Output Low Voltage

Figure 9. I/O Output High Voltage vs Temperature
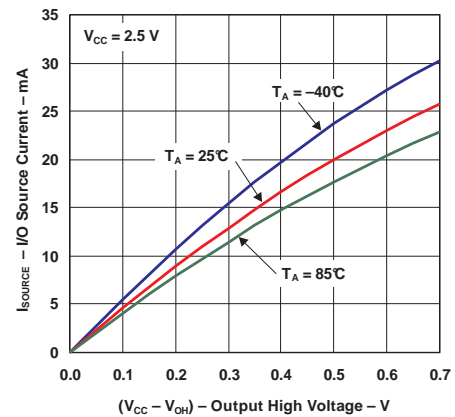

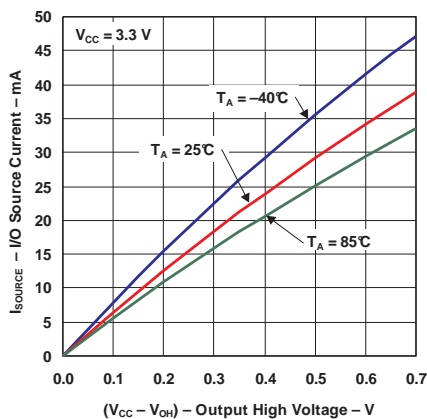Figure 10. I/O Source Current vs Output High Voltage

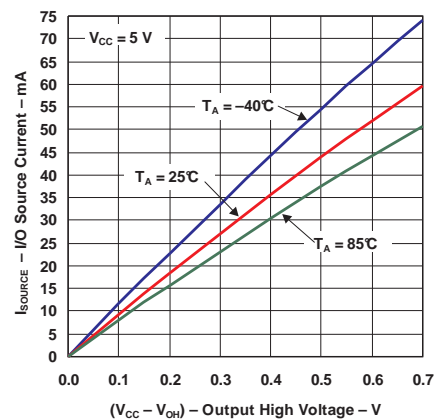Figure 11. I/O Source Current vs Output High Voltage

Figure 12. I/O Source Current vs Output High Voltage

Product Folder Links: *PCA9554*
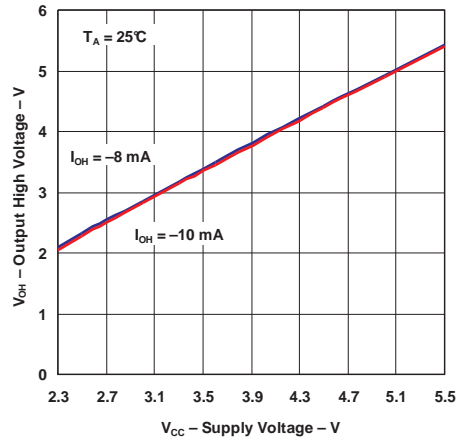
Typical Characteristics (continued)

Figure 13. Output High Voltage vs Supply Voltage

7 Parameter Measurement Information
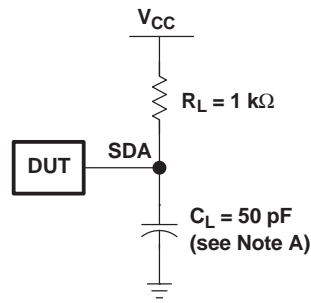
SDA LOAD CONFIGURATION
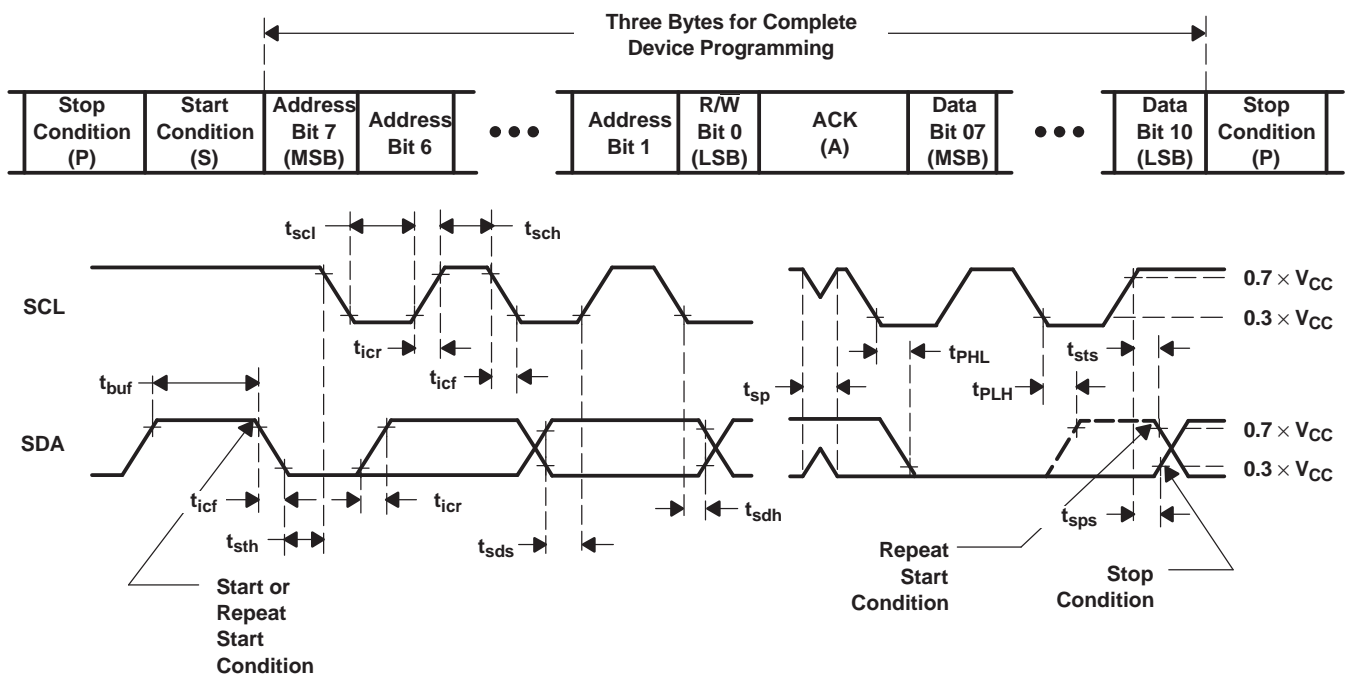
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^{2}C address
2, 3	P-port data

A. C$_L$ includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z$_O$ = 50 Ω, t$_r$/t$_f$ ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 14. I^{2}C Interface Load Circuit And Voltage Waveforms

Product Folder Links: *PCA9554*

Parameter Measurement Information (continued)

INTERRUPT LOAD CONFIGURATION

View A–A

View B–B

A. C_L includes probe and jig capacitance.

B.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C.   All parameters and waveforms are not applicable to all devices.

Figure 15. Interrupt Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)
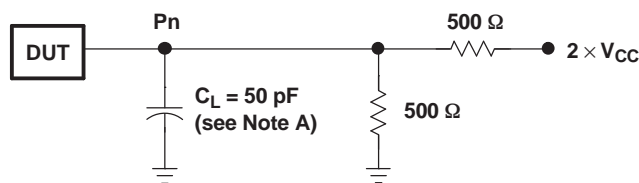
P-PORT LOAD CONFIGURATION
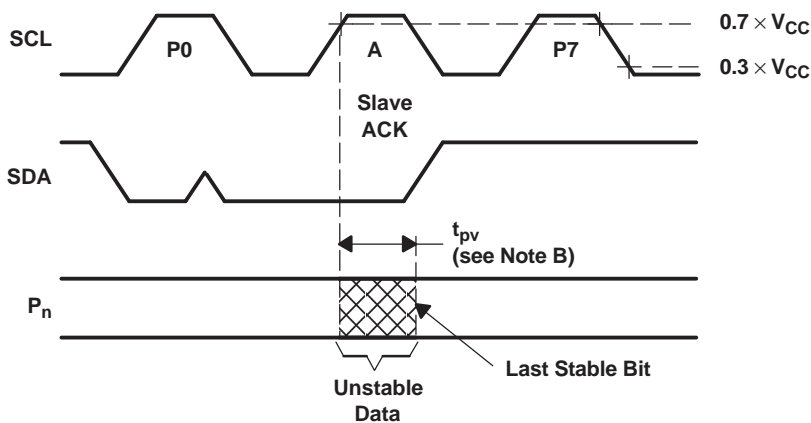
WRITE MODE (R/$\overline{W}$ = 0)
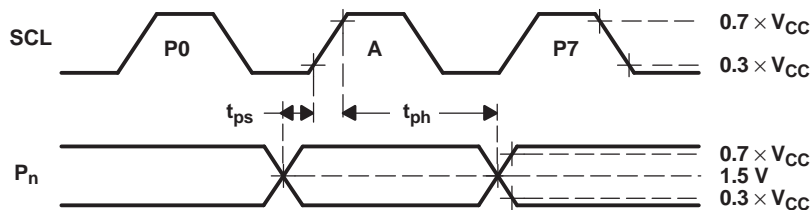
READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O pin output.

C.   All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D.   The outputs are measured one at a time, with one transition per measurement.

E.   All parameters and waveforms are not applicable to all devices.

Figure 16. P-Port Load Circuit And Voltage Waveforms

Product Folder Links: *PCA9554*

8 Detailed Description

8.1 Functional Block Diagram
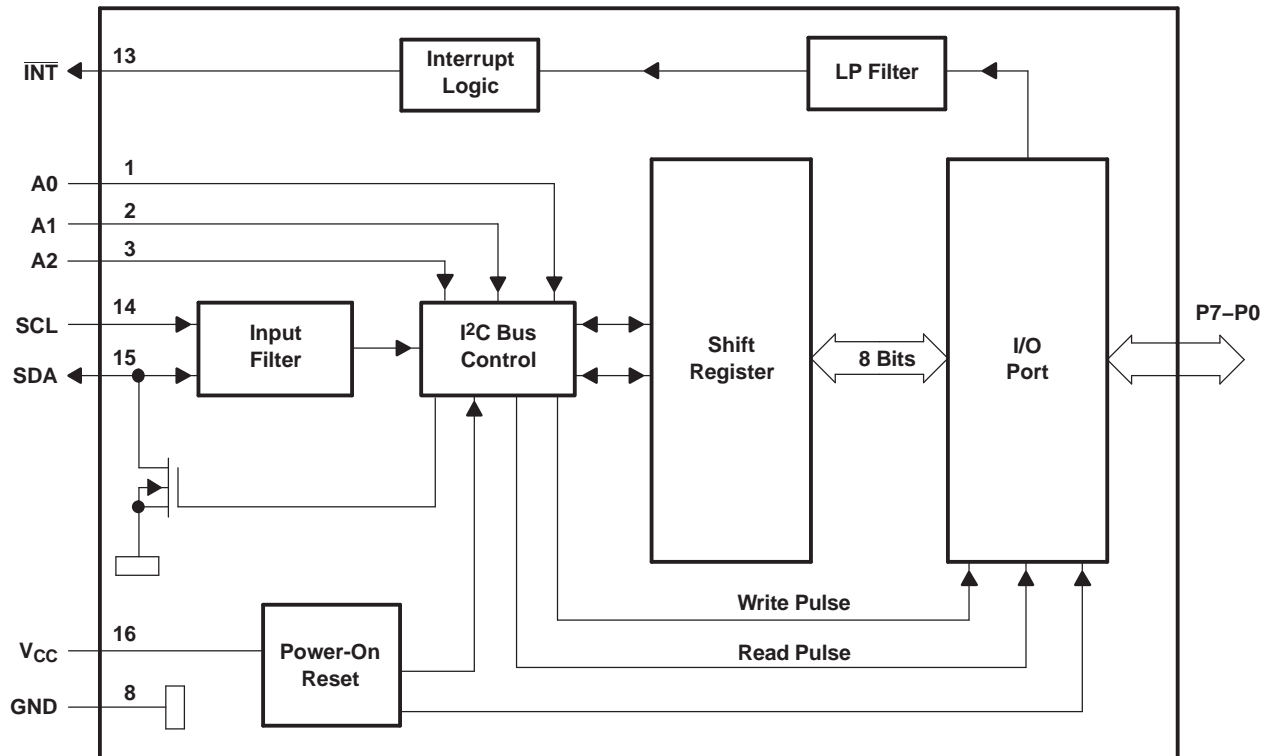
A.   Pin numbers shown are for the DB, DBQ, DGV, DW, N, or PW package.

B.   All I/Os are set to inputs at reset.

Figure 17. Logic Diagram

Functional Block Diagram (continued)
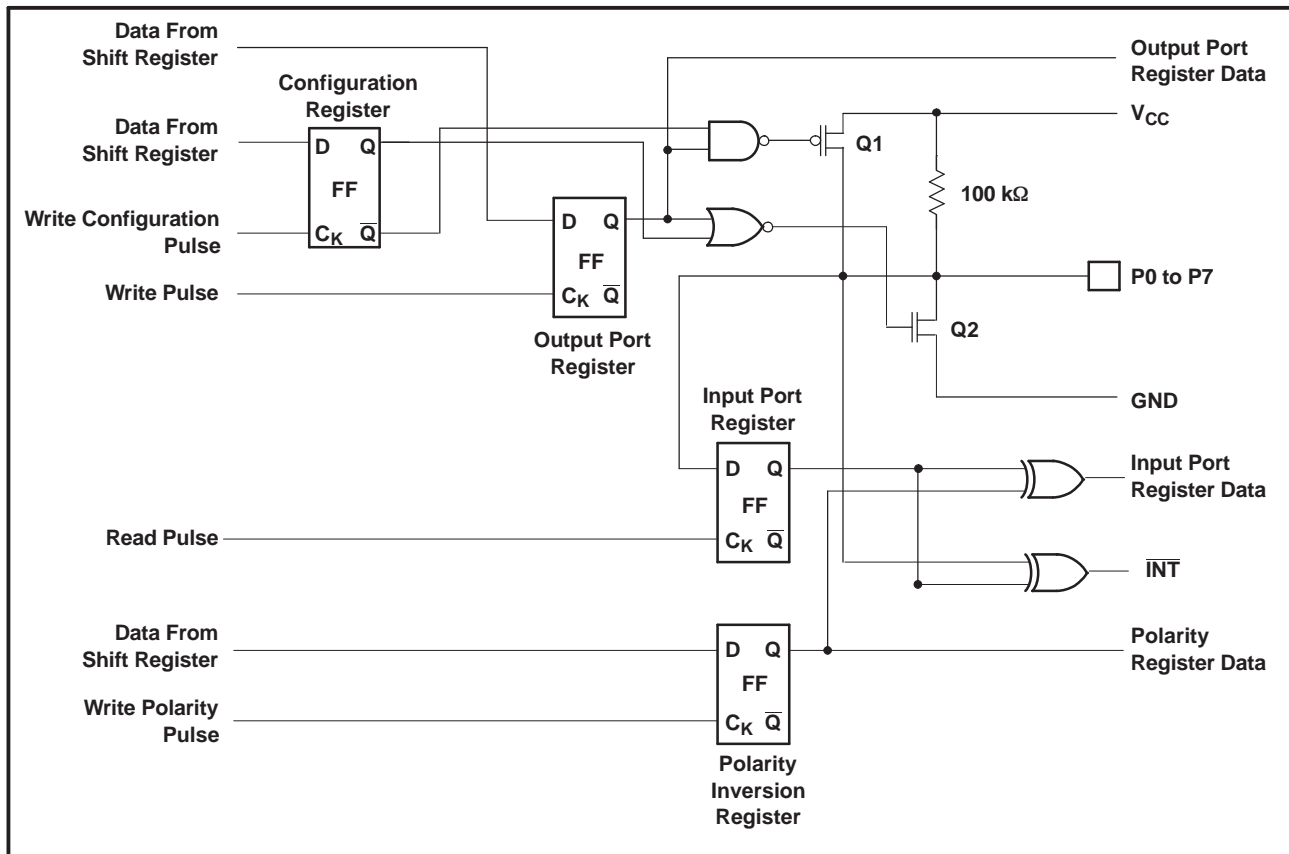
A.   At power-on reset, all registers return to default values.

Figure 18. Simplified Schematic Of P0 To P7

8.2   Device Functional Modes

8.2.1   Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9554 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9554 registers and I^{2}C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Refer to the *Power-On Reset Errata* section.

8.2.2   I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in Figure 18) are off, which creates a high-impedance input with a weak pullup (100 kΩ typ) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

Product Folder Links: *PCA9554*

Device Functional Modes (continued)

8.2.3 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{INT}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

8.2.3.1 Interrupt Errata

Description

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I²C command byte (register pointer) written to the device was 00h.

> **NOTE**
> This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I²C bus acknowledges an address byte with the R/W bit set high

System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9554 device or before reading from another slave device.

> **NOTE**
> Software change will be compatible with other versions (competition and TI redesigns) of this device.

8.3 Programming

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 19). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

Programming (continued)

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 20).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 19).

Any number of data bytes can be transferred from the transmitter to the receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 21). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.
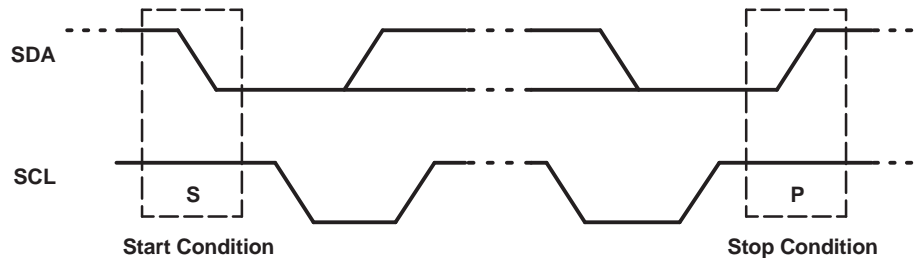
Figure 19. Definition Of Start And Stop Conditions
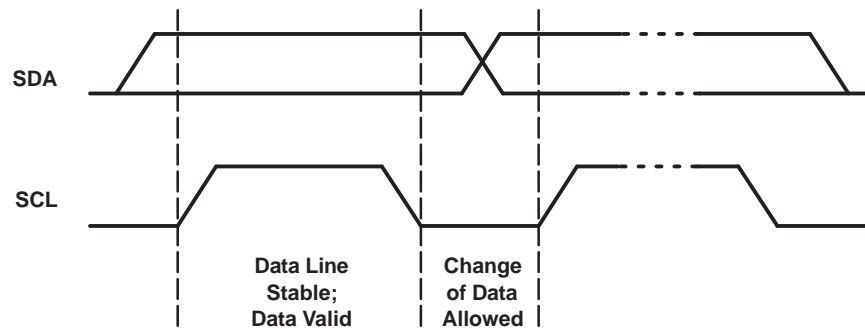
Figure 20. Bit Transfer

Product Folder Links: *PCA9554*

Programming (continued)
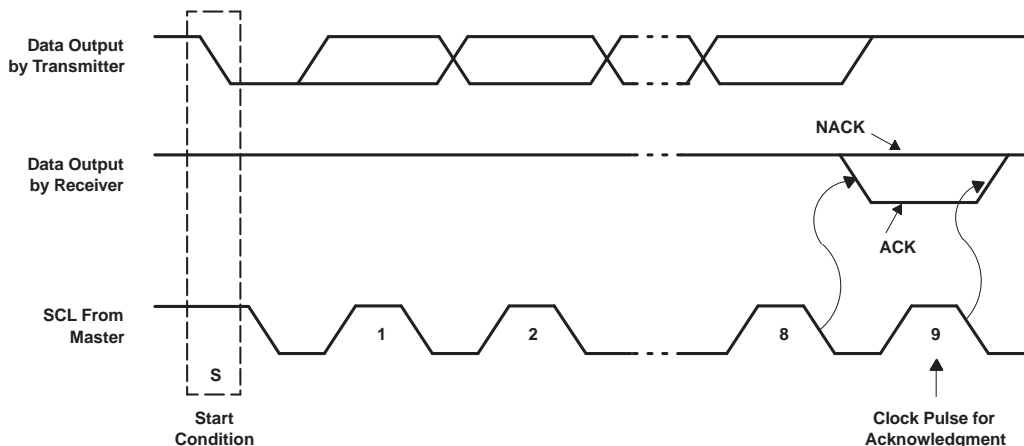
Figure 21. Acknowledgment On The I²C Bus

8.3.2 Register Map

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.3.2.1 Device Address

Figure 22 shows the address byte for the PCA9554.
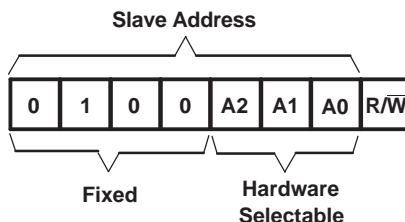
Figure 22. PCA9554 Address

Table 2. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9554. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by readsuntil a new command byte has been sent.

0	0	0	0	0	0	B1	B0
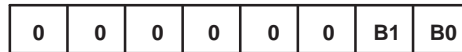
Figure 23. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port Register	Read byte	XXXX XXXX
0	1	0x01	Output Port Register	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion Register	Read/write byte	0000 0000
1	1	0x03	Configuration Register	Read/write byte	1111 1111

8.3.2.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I²C device that the Input Port register will be accessed next.

Table 4. Register 0 (Input Port Register) Table

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Register 1 (Output Port Register) Table

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Table 6. Register 2 (Polarity Inversion Register) Table

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Register 3 (Configuration Register) Table

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

8.3.2.4 Bus Transactions

Data is exchanged between the master and PCA9554 through write and read commands.

8.3.2.4.1 Writes

Data is transmitted to the PCA9554 by sending the device address and setting the least-significant bit to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.
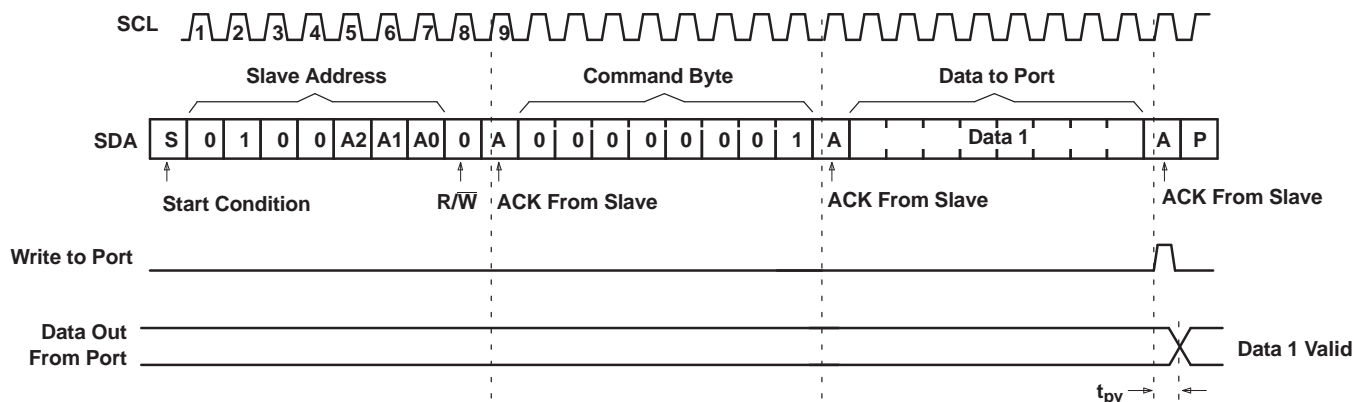
Figure 24. Write To Output Port Register
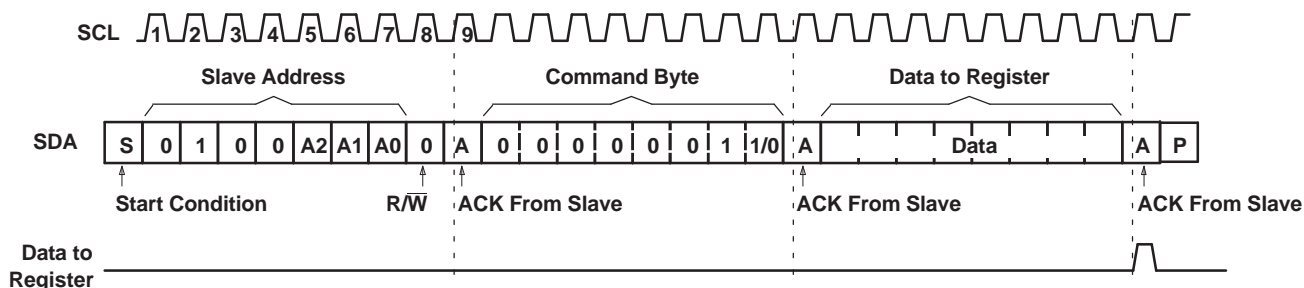
Figure 25. Write To Configuration Or Polarity Inversion Registers

8.3.2.4.2 Reads

The bus master first must send the PCA9554 address with the least-significant bit set to a logic 0 (see Figure 22 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9554 (see Figure 26 and Figure 27). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data
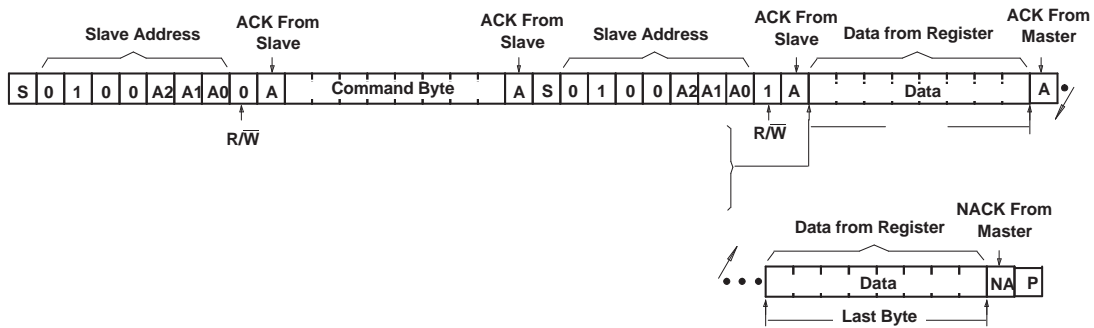
Figure 26. Read From Register
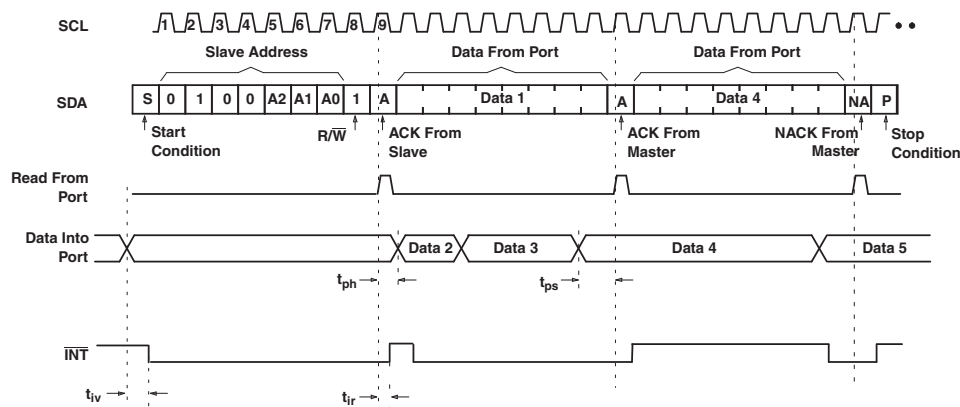
A. This figure assumes the command byte has previously been programmed with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition.

C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port. See Figure 26 for these details.

Figure 27. Read From Input Port Register

Product Folder Links: *PCA9554*

9 Application And Implementation

9.1 Typical Application

Figure 28 shows an application in which the PCA9554 can be used.
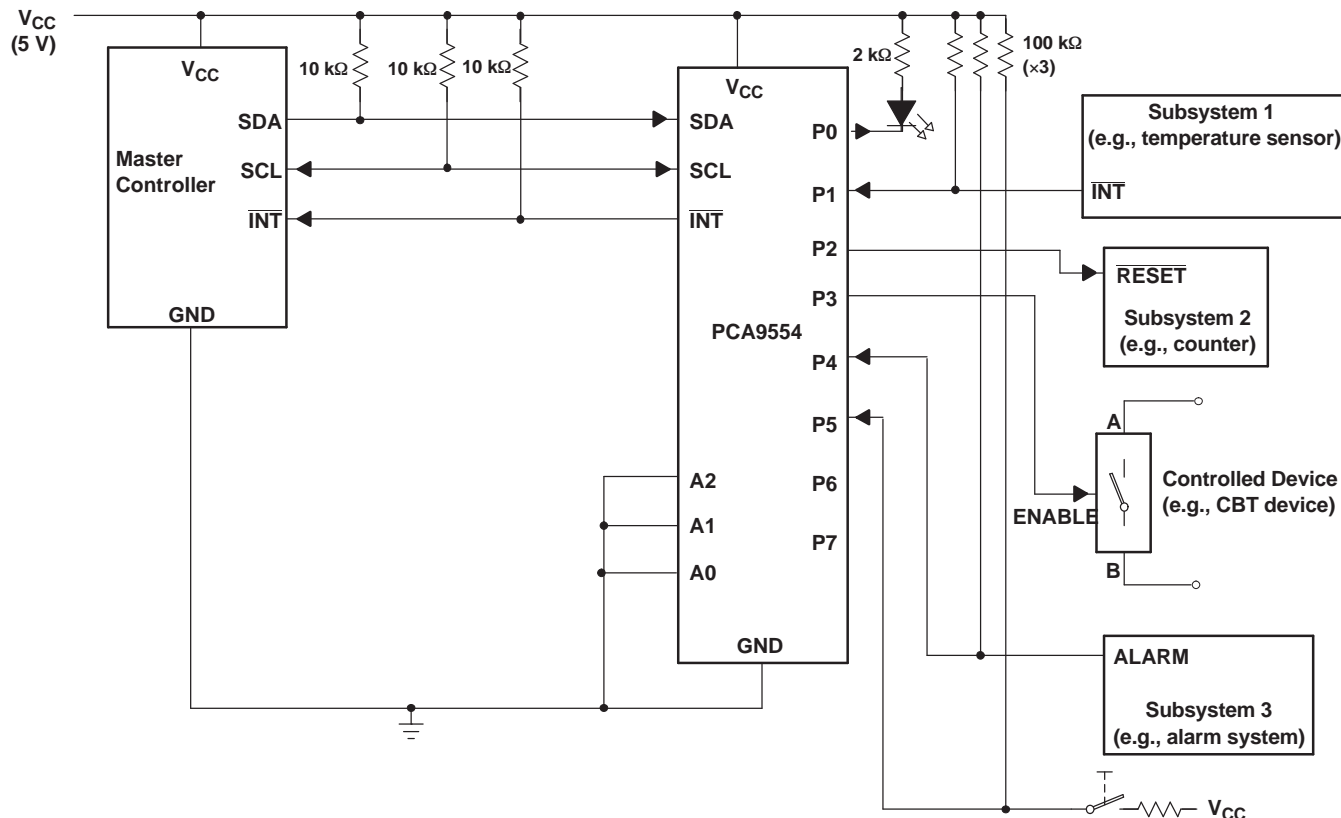
A.   Device address is configured as 0100000 for this example.

B.   P0, P2, and P3 are configured as outputs.

C.   P1, P4, and P5 are configured as inputs.

D.   P6 and P7 are not used and and have internal 100-kΩ pullup resistors to protect them from floating.

Figure 28. Typical Application

Typical Application (continued)
9.1.1 Design Requirements

9.1.1.1 Minimizing I_{CC} When I/Os Control Leds

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in Figure 28. The LED acts as a diode, so when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. ΔI_{CC} in *Electrical Characteristics* shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}.

For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. Figure 29 shows a high-value resistor in parallel with the LED. Figure 30 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.
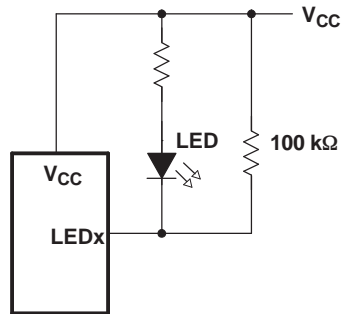
Figure 29. High-Value Resistor In Parallel With Led
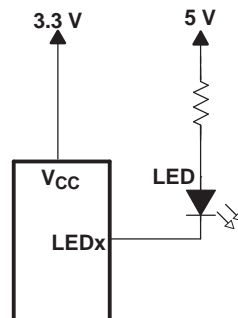
Figure 30. Device Supplied By A Lower Voltage

Product Folder Links: *PCA9554*

10 Power Supply Recommendations

10.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.
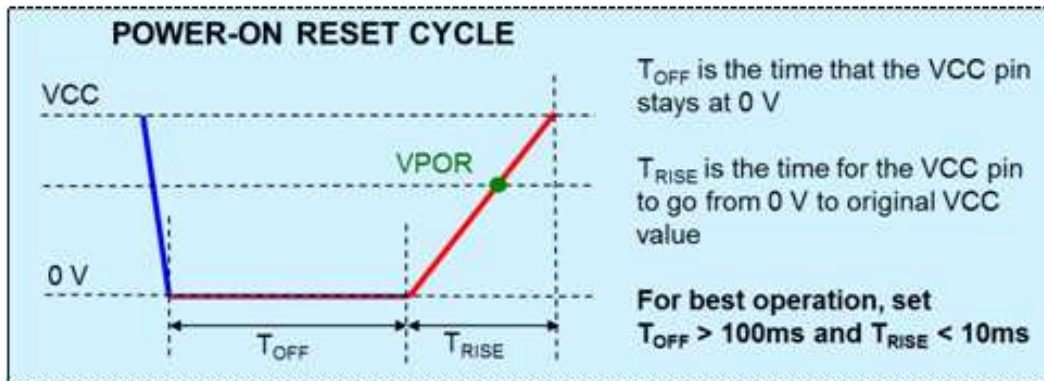
System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9554DB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554	Samples
PCA9554DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554	Samples
PCA9554DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554	Samples
PCA9554DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9554	Samples
PCA9554DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9554	Samples
PCA9554PW	NRND	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554	
PCA9554PWG4	NRND	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554	
PCA9554PWR	NRND	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554	
PCA9554PWRG4	NRND	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9554DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
PCA9554DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9554DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9554PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9554DBR	SSOP	DB	16	2000	367.0	367.0	38.0
PCA9554DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
PCA9554DWR	SOIC	DW	16	2000	367.0	367.0	38.0
PCA9554PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

4,50
4,30

6,60
6,20

5,10
4,90

1,20 MAX

0,15
0,05

Seating Plane

0,10

0,65

0,30
0,19

0,10 (M)

4040064−4/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0,15 each side.
          D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE
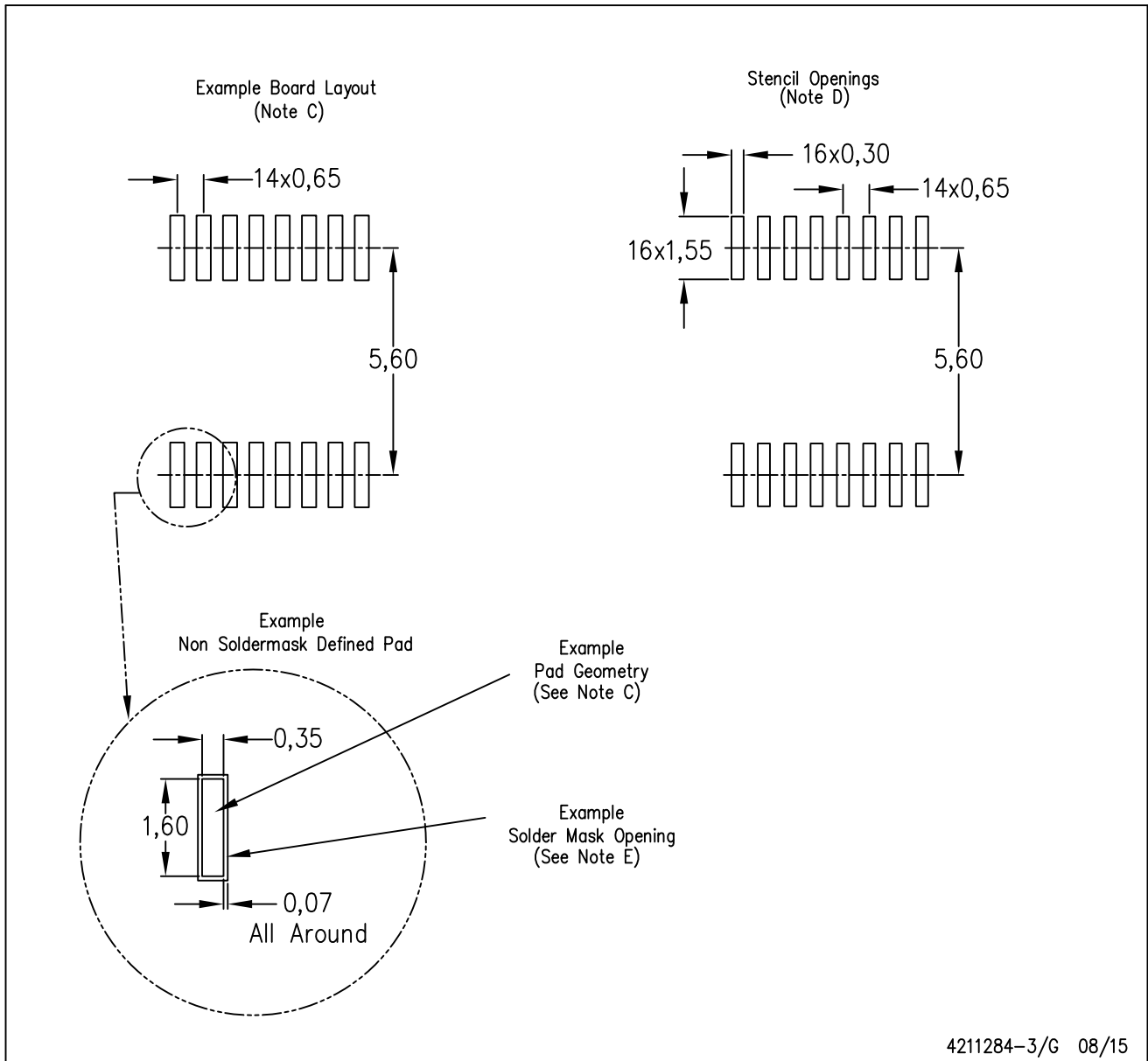
Example Board Layout
(Note C)

├─ 14x0,65

5,60

Stencil Openings
(Note D)

├─ 16x0,30

├─ 14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

├─0,35

1,60

Example
Solder Mask Opening
(See Note E)

├─ 0,07
All Around

4211284−3/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01
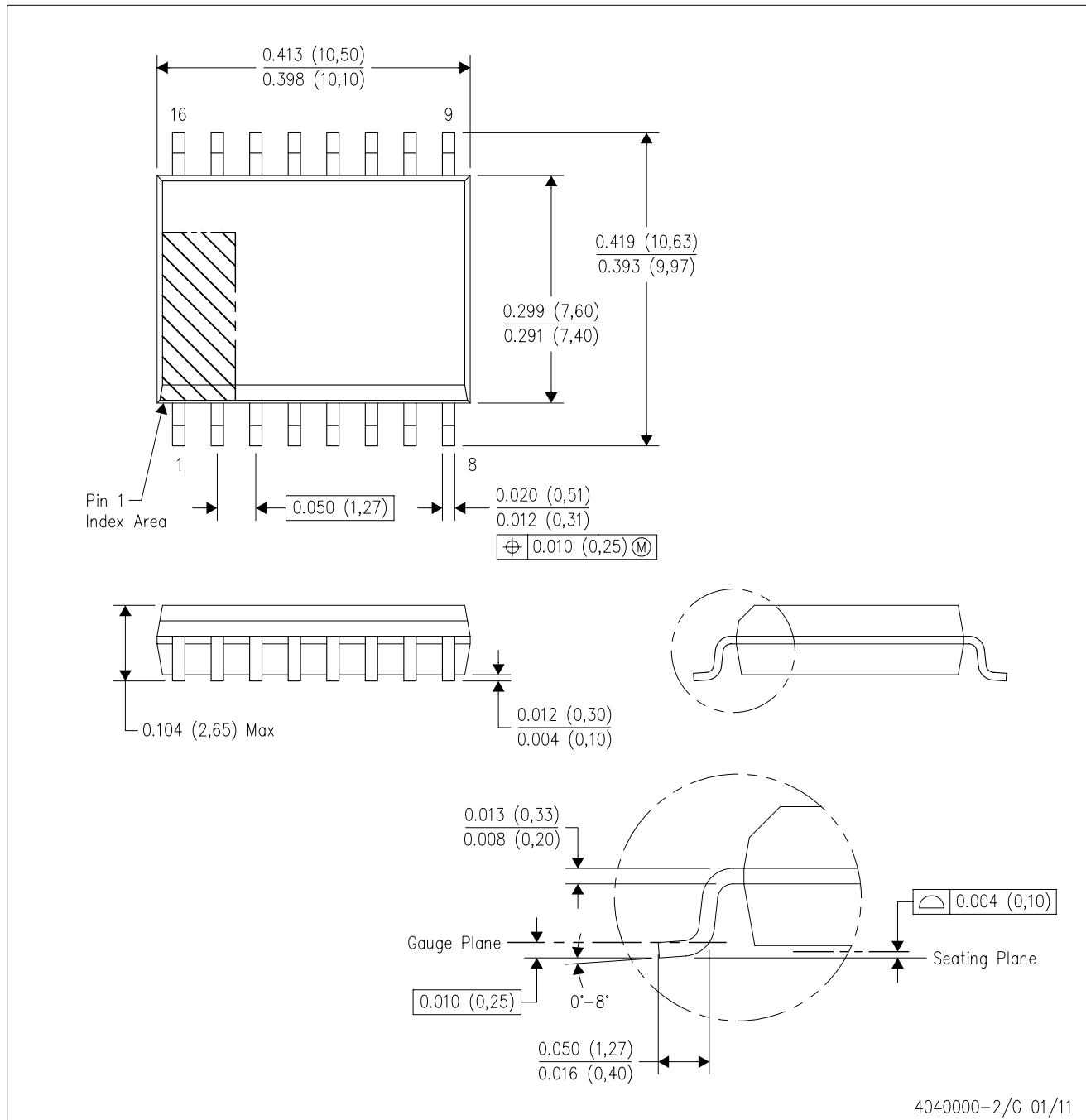
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

DW (R–PDSO–G16)   PLASTIC SMALL OUTLINE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040000–2/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
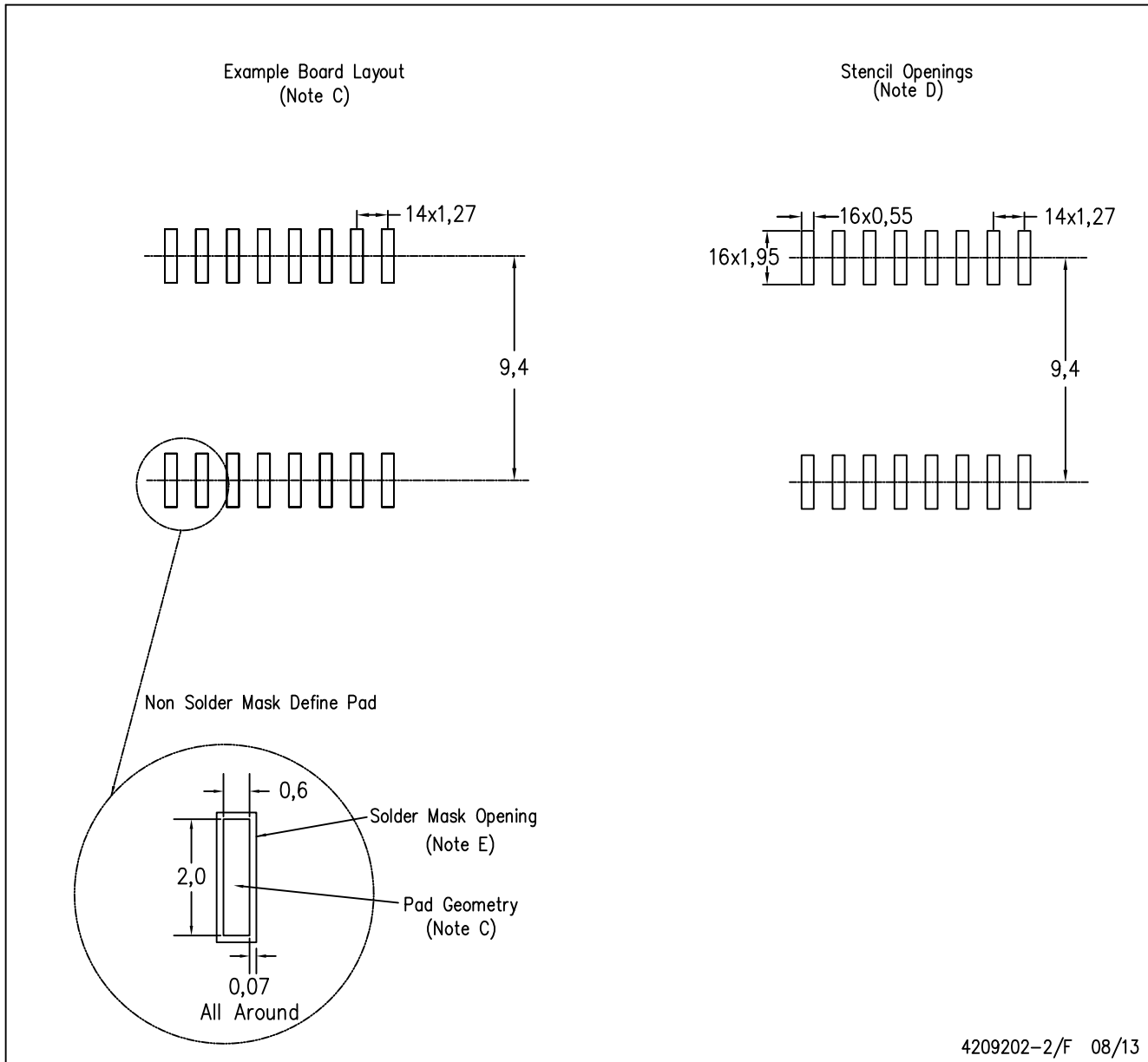   D.   Falls within JEDEC MS–013 variation AA.

DW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

9,4

16x0,55   14x1,27

16x1,95

9,4

Non Solder Mask Define Pad

0,6

2,0

Solder Mask Opening
(Note E)

Pad Geometry
(Note C)

0,07
All Around

4209202−2/F   08/13

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Refer to IPC7351 for alternate board design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		