DATA SHEET

PCA9511

Hot swappable I^{2}C-bus and SMBus bus buffer

Product data sheet
2006 Aug 23
Replaces data sheet PCA9510; PCA9511 of 2006 Aug 15

Philips Semiconductors

PHILIPS

Hot swappable I²C-bus and SMBus bus buffer PCA9511

DESCRIPTION

The PCA9511 is a are hot swappable I²C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a STOP command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9511 provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The PCA9511 rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements to prevent interference when there are multiple devices in the same system. The PCA9511 incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

During insertion, the PCA9511 SDA and SCL lines are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

The dynamic offset design of the PCA9510/11/12/13/14 I/O drivers allow them to be connected to another PCA9510/11/12/13/14 device in series or in parallel and to the A side of the PCA9517. The PCA9510/11/12/13/14 can **not** connect to the static offset I/Os used on the PCA9515/15A/16/16A/17 B side and PCA9518.

APPLICATION

- cPCI, VME, AdvancedTCA cards and other multi-point backplane cards that are required to be inserted or removed from an operating system.

FEATURES

- Bidirectional buffer for SDA and SCL lines increases fanout and prevents SDA and SCL corruption during live board insertion and removal from multi-point backplane systems
- Compatible with I²C-bus Standard-mode, I²C-bus Fast-mode, and SMBus standards
- ΔV/Δt rise time accelerators on all SDA and SCL lines
- Rise time accelerator threshold of 0.6 V
- Active HIGH ENABLE input
- Active HIGH READY open-drain output
- High-impedance SDA and SCL pins for V_{CC} = 0 V
- 1 V precharge on all SDA and SCL lines
- Supports clock stretching and multiple master arbitration/synchronization
- Operating power supply voltage range: 2.7 V to 5.5 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-pin plastic SO	–40 °C to +85 °C	PCA9511D	PCA9511	SOT96-1
8-pin plastic TSSOP (MSOP)	–40 °C to +85 °C	PCA9511DP	9511	SOT505-1

Standard packing quantities and other packaging data is available at www.standardproducts.philips.com/packaging.

PIN CONFIGURATION

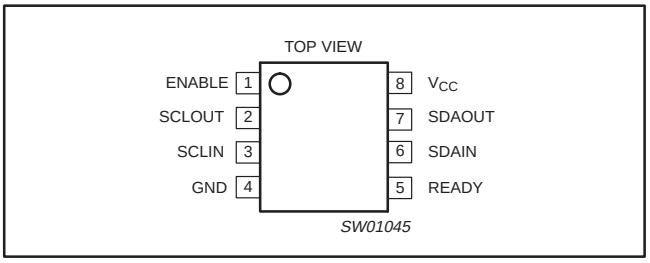


Figure 1. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	ENABLE	Chip enable pin. Grounding this pin puts the part in a low current (<1 μA) mode. It also disables the rise time accelerators, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.
2	SCLOUT	Serial clock output to and from the SCL bus on the card.
3	SCLIN	Serial clock input to and from the SCL bus on the backplane.
4	GND	Ground. Connect this pin to a ground plane for best results.
5	READY	This is an open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and turns off when the two sides are connected.
6	SDAIN	Serial data input to and from the SDA bus on the backplane.
7	SDAOUT	Serial data output to and from the SDA bus on the card.
8	V_{CC}	Power supply.

FEATURE SELECTION CHART

FEATURES	PCA9510	PCA9511	PCA9512	PCA9513	PCA9514
Idle detect	Yes	Yes	Yes	Yes	Yes
High impedance SDA, SCL pins for V_{CC} = 0 V	Yes	Yes	Yes	Yes	Yes
Rise time accelerator circuitry on all SDA and SCL lines	—	Yes	Yes	Yes	Yes
Rise time accelerator circuitry hardware disable pin for lightly loaded systems	—	—	Yes	—	—
Rise time accelerator threshold 0.8 V vs 0.6 V improves noise margin	—	—	—	Yes	Yes
Ready open-drain output	Yes	Yes	—	Yes	Yes
Two V_{CC} pins to support 5 V to 3.3 V level translation with improved noise margins	—	—	Yes	—	—
1 V precharge on all SDA and SCL lines	IN only	Yes	Yes	—	—
92 μA current source on SCLIN and SDAIN for PICMG applications	—	—	—	Yes	—

TYPICAL APPLICATION

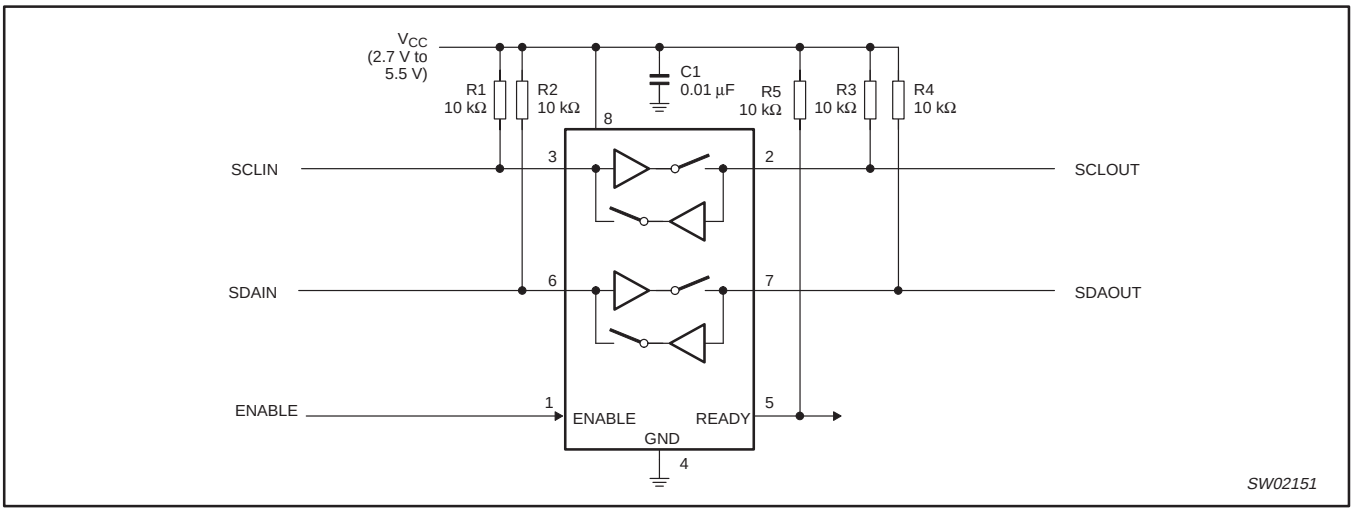


Figure 2. Typical application

BLOCK DIAGRAM

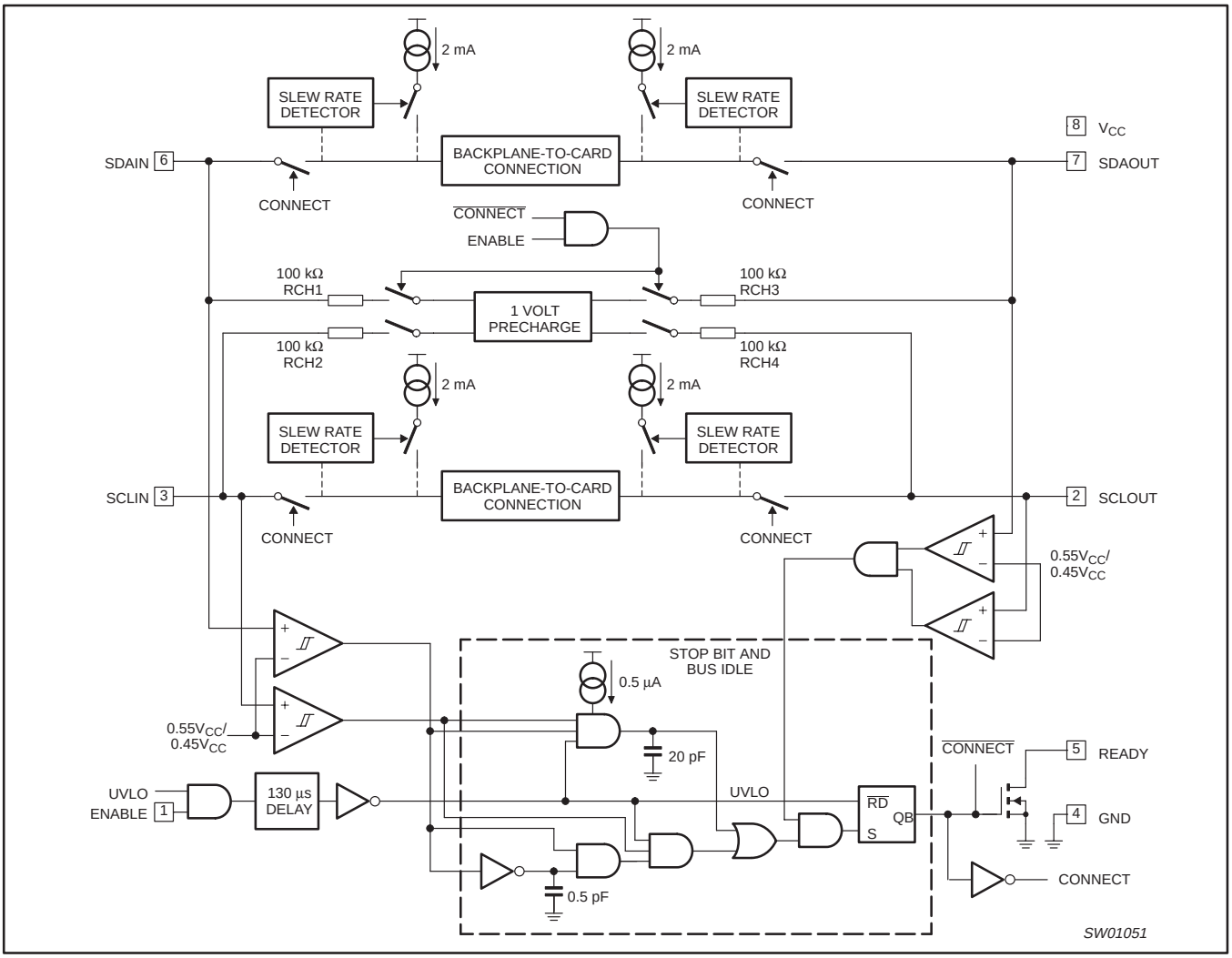


Figure 3. Block diagram

OPERATION

Start-up

An under voltage/initialization circuit holds the parts in a disconnected state which presents high-impedance to all SDA and SCL pins during power-up. A LOW on the ENABLE pin also forces the parts into the low current disconnected state when the I_{CC} is essentially zero. As the power supply is brought up and the ENABLE is HIGH or the part is powered and the ENABLE is taken from LOW to HIGH, it enters an initialization state where the internal references are stabilized and the precharge circuit for PCA9511 is enabled. At the end of the initialization state the “Stop Bit And Bus Idle” detect circuit is enabled. With the ENABLE pin HIGH long enough to complete the initialization state and remaining HIGH when all the SDA and SCI pins have been HIGH for the bus idle time, or when all pins are HIGH and a STOP condition is seen on the SDAIN and SCLIN pins, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT. The 1 V precharge circuitry is activated during the initialization and is deactivated when the connection is made. The precharge circuitry pulls up the SDA and SCL pins to 1 V through individual 100 kΩ nominal resistors. This precharges the pins to 1 V to minimize the worst-case disturbances that result from inserting a card into the backplane where the backplane and the card are at opposite logic levels.

Connect circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical with each acting as a bidirectional buffer that isolates the input capacitance from the output bus capacitance while communicating the logic levels. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. The same is also true for the SCL pins. Noise between $0.7V_{CC}$ and V_{CC} is generally ignored because a falling edge is only recognized when it falls below $0.7V_{CC}$ with a slew rate of at least 1.25 V/µs. When a falling edge is seen on one pin the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below $0.7V_{CC}$. The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull down rate will continue. If the first falling pin has a slow slew rate then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage the they will both continue down at the slew rate of the first.

Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value for instance, 10 mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise and rise above the nominal offset voltage until the internal driver catches up and pulls it back down to the offset voltage. This bounce is worst for low capacitances and low resistances, and may become excessive. When the last external driver stops driving a LOW, that pin will bounce up and settle out out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/µs, when the pin voltage exceeds 0.6 V, the rise time accelerators circuits are turned on and the pull down driver is turned off.

Maximum number of devices in series

Each buffer adds about 0.065 V dynamic level offset at 25 °C with the offset larger at higher temperatures. Maximum offset (V_{OS}) is 0.150 V. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is the I²C-bus specification of 3 mA will produce V_{OL} < 0.4 V, although if lightly loaded the V_{OL} may be ~0.1 V. Assuming V_{OL} = 0.1 V and V_{OS} = 0.1 V, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the V_{OL} moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two.

The PCA9510 (rise time accelerator is permanently disabled) and the PCA9512 (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns on the accelerator turns the pull-down off. If the V_{IL} is above ~0.6 V and a rising edge is detected, the pull-down will turn off and will not turn back on until a falling edge is detected; so if the noise is small enough it may be possible to use more than two PCA9510 or PCA9512 parts in series, but is not recommended.

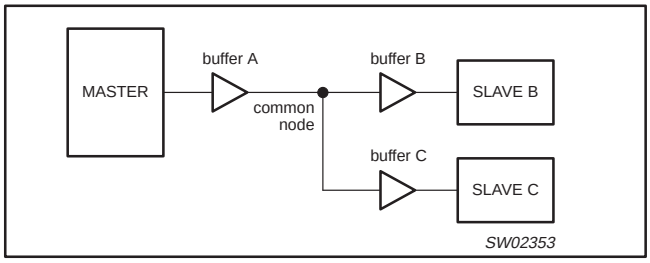


Figure 4.

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of Buffer A and Buffer B in series as shown in Figure 4. Consider if the V_{OL} at the input of Buffer A is 0.3 V and the V_{OL} of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe V_{IL} at the input of Buffer A of 0.3 V and its output, the common node, is ~0.4 V. The output of Buffer B and Buffer C would be ~0.5 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of Buffer C is ~0.5 V. When the Master pull-down turns off, the input of Buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before Buffer B’s output turns on, if the pull-up is strong the node will bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V the accelerators on both Buffer A and Buffer C will fire contending with the output of Buffer B. The node on the input of Buffer A will go HIGH as will the input node of Buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to ~0.5 V because the Buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to ~0.6 V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.6 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on Buffer A and Buffer C would see a false clock rather than a stretched clock, which would cause a system error.

Propagation delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below $0.7V_{CC}$, and the output turn on has a non-zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature. V_{CC} and process, as well as the load current and the load capacitance.

Rise time accelerators

During positive bus transitions a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V is exceeded. The rising edge rate should be at least 1.25 V/µs to guarantee turn on of the accelerators.

READY digital output

This pin provides a digital flag which is LOW when either ENABLE is LOW or the start-up sequence described earlier in this section has not been completed. READY goes HIGH when ENABLE is HIGH and start-up is complete. The pin is driven by an open-drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 kΩ to V_{CC} to provide the pull-up.

ENABLE low current disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise-time accelerators, drives READY LOW, disables the bus precharge circuitry, and puts the part in a low current state. When the pin voltage is driven all the way to V_{CC}, the part waits for data transactions on both the backplane and card sides to be complete before reconnecting the two sides.

Resistor pull-up value selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula:

$$R \leq 800 \cdot 10^3 \times \frac{V_{CC(MIN)} - 0.6}{C}$$

where R is the pull-up resistor value in Ω, $V_{CC(MIN)}$ is the minimum V_{CC} voltage in volts and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose $R \leq 16$ kΩ for $V_{CC} = 5.5$ V maximum, $R \leq 24$ kΩ for $V_{CC} = 3.6$ V maximum. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage. See the curves in Figures 5 and 6 for guidance in resistor pull-up selection.

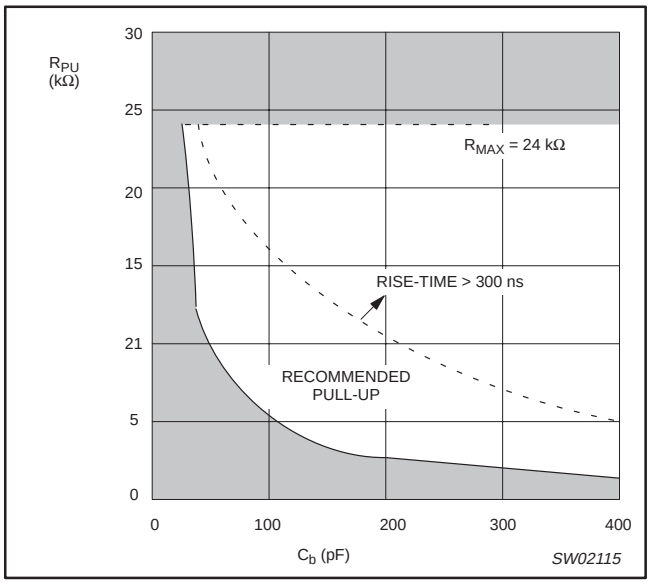


Figure 5. Bus requirements for 3.3 V systems

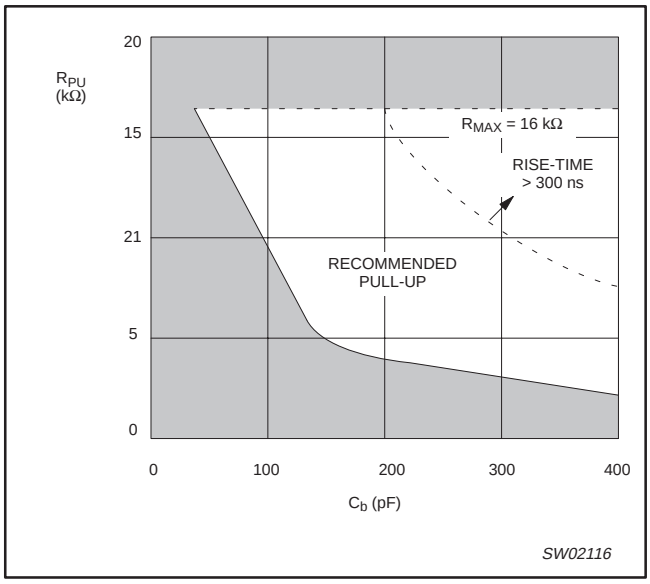


Figure 6. Bus requirements for 5 V systems

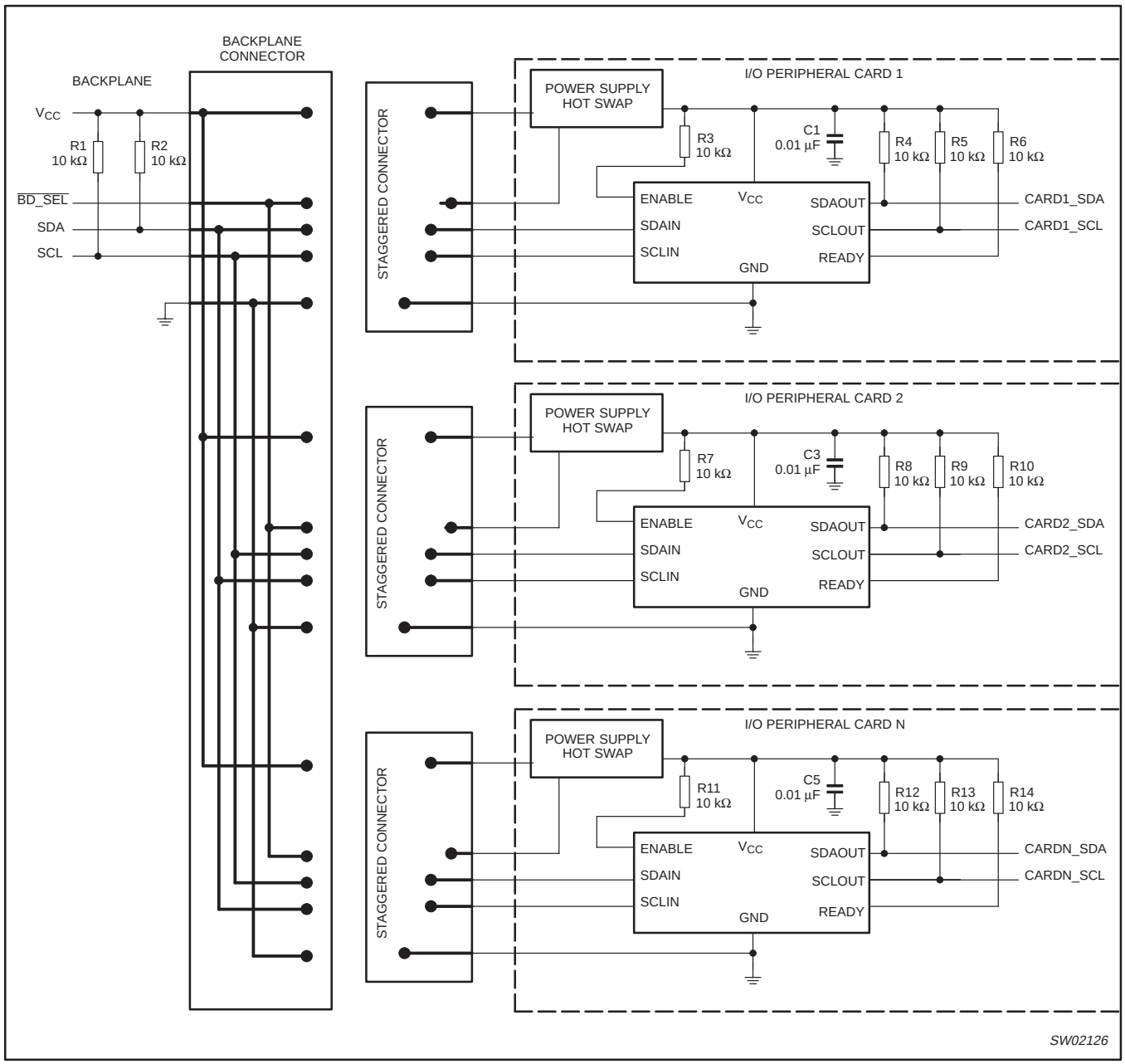
Minimum SDA and SCL capacitance requirements

The device connection circuitry requires a minimum capacitance loading on the SDA and SCL pins in order to function properly. The value of this capacitance is a function of V_{CC} and the bus pull-up resistance. Estimate the bus capacitance on both the backplane and the card data and clock buses, and refer to Figures 5 and 6 to choose appropriate pull-up resistor values. Note from the figures that 5 V systems should have at least 47 pF capacitance on their buses and 3.3 V systems should have at least 22 pF capacitance for proper operation. Although the device has been designed to be marginally stable with smaller capacitance loads, for applications with less capacitance, provisions need to be made to add a capacitor to ground to ensure these minimum capacitance conditions if oscillations are noticed during initial signal integrity verification.

Hot Swapping and Capacitance Buffering Application

Figures 7 through 9 illustrate the usage of the PCA9510 and PCA9511 in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9510 and PCA9511 drive the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

See Application Note *AN10160, Hot Swap Bus Buffer* for more information on applications and technical assistance.



NOTE: The PCA9510 and PCA9511 can be used in any combination depending on the number of rise time accelerators that are needed by the system. Normally only one PCA9511 would be required per bus.

Figure 7. Hot swapping multiple I/O cards into a backplane using the PCA9510 and PCA9511 in a CompactPCI, VME, and AdvancedTCA system

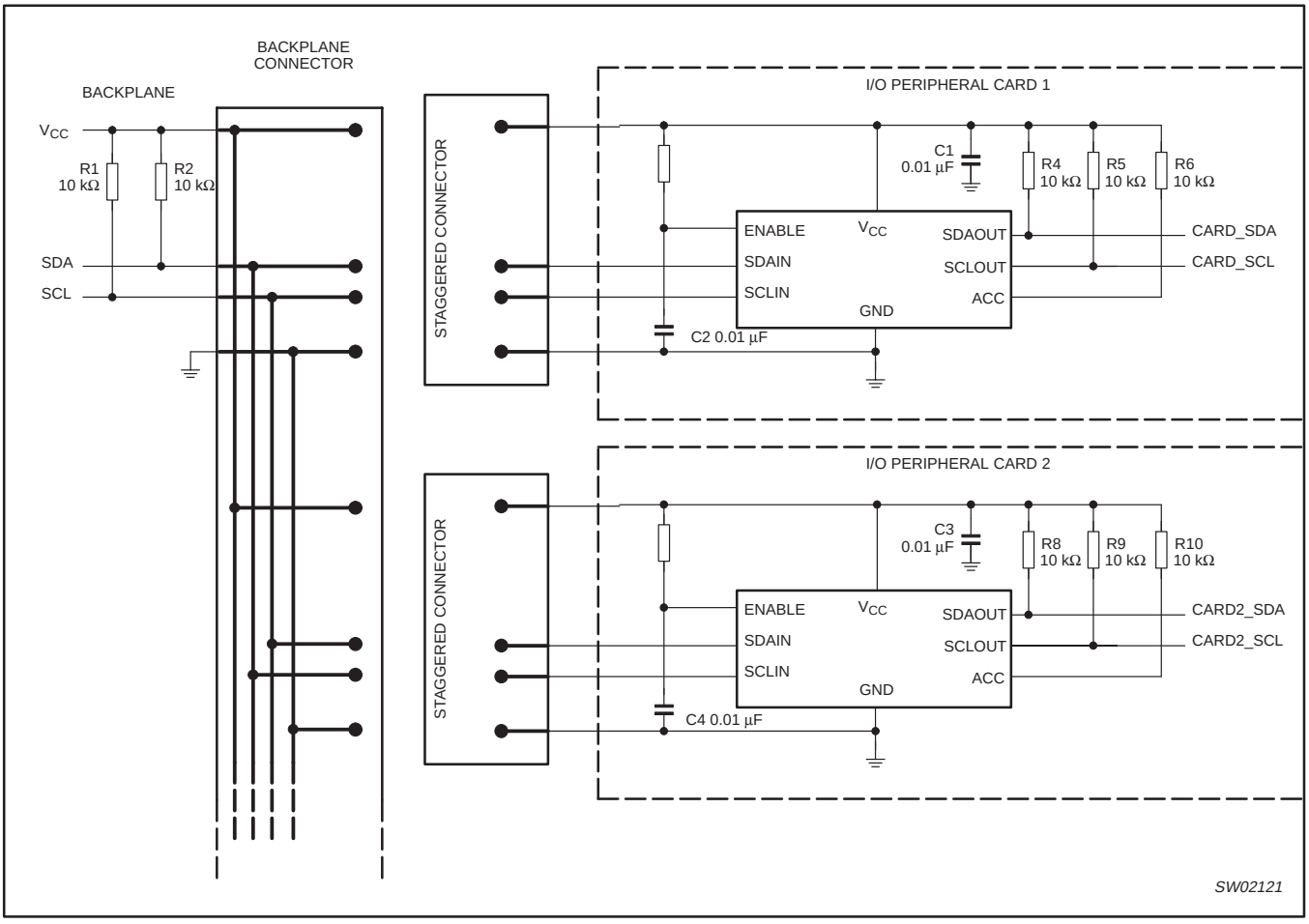


Figure 8. Hot swapping multiple I/O cards into a backplane using the PCA9510 and PCA9511 in a PCI system

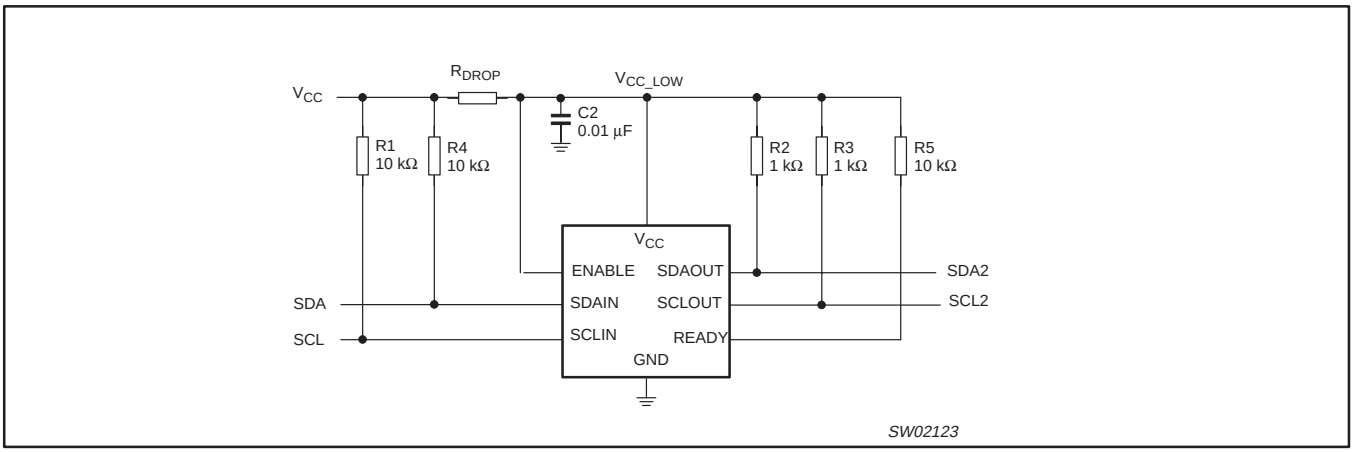


Figure 9. System with disparate V_{CC} voltages

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC}	Supply voltage range V_{CC}	–0.5	+7	V
V_n	SDAIN, SCLIN, SDAOUT, SCLOUT, READY, ENABLE	–0.5	+7	V
I_I	Maximum current for inputs	–	±20	mA
I_{IO}	Maximum current for I/O pins	–	±50	mA
T_{opr}	Operating temperature range	–40	+85	°C
T_{stg}	Storage temperature range	–65	+125	°C
T_{sld}	Lead soldering temperature (10 sec max)	–	+300	°C
$T_{j(max)}$	Maximum junction temperature	–	+125	°C

NOTE:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V; T_{amb} = –40 to +85 °C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power supply						
V_{CC}	Supply voltage	Note 1	2.7	—	5.5	V
I_{CC}	Supply current	V_{CC} = 5.5 V; V_{SDAIN} = V_{SCLIN} = 0 V; Note 1.	—	2.8	6	mA
$I_{CC(sd)}$	Supply current in shut-down mode	V_{ENABLE} = 0 V, all other pins at V_{CC} or GND	—	200	—	µA
Start-up circuitry						
V_{PRE}	Precharge voltage	SDA, SCL floating; Note 1	0.8	1.0	1.2	V
V_{EN}	Enable threshold voltage		—	$0.5V_{CC}$	$0.7V_{CC}$	V
V_{DIS}	Disable threshold voltage		$0.3V_{CC}$	$0.5V_{CC}$	—	V
I_{EN}	Enable input current	Enable from 0 V to V_{CC}	—	±0.1	±1	µA
t_{EN}	Enable delay or initialization time		—	130	—	µs
t_{IDLE}	Bus idle time	Note 1	50	120	250	µs
t_{DIS}	Disable time, ENABLE to READY		—	15	—	ns
t_{STOP}	SDAIN to READY delay after STOP	Note 7	—	1.3	—	µs
t_{READY}	SCLOUT/SDAOUT to READY	Note 7	—	1.2	—	µs
I_{OFF}	READY off-state leakage current	V_{EN} = V_{CC}	—	±0.3	—	µA
C_i	ENABLE capacitance	V_I = V_{CC} or GND, Note 4	—	2	—	pF
C_O	READY capacitance	V_I = V_{CC} or GND, Note 4	—	2	—	pF
$V_{OL(READY)}$	LOW-level output voltage on READY pin	$I_{pull-up}$ = 3 mA; V_{EN} = V_{CC}; Note 1.	—	—	0.4	V
Rise time accelerators						
$I_{PULLUPAC}$	Transient boosted pull-up current	Positive transition on SDA, SCL, V_{CC} = 2.7 V; Slew rate = 1.25 V/µs Note 2.	1	2	—	mA
Input–output connection						
V_{OS}	Input–output offset voltage	10 kΩ to V_{CC} on SDA, SCL; V_{CC} = 3.3 V; Note 1; Note 3.	0	65	150	mV
f_{SCL_SDA}	operating frequency		0	—	400	kHz
t_{PLH}	SCL to SCL and SDA to SDA	10 kΩ to V_{CC}, C_L = 100 pF each side	—	25	—	ns
t_{PHL}	SCL to SCL and SDA to SDA	10 kΩ to V_{CC}, C_L = 100 pF each side	—	380	—	ns
C_{IN}	Digital input capacitance	Note 4	—	—	10	pF
V_{OL}	LOW-level output voltage	Input = 0 V, SDA, SCL pins, I_{SINK} = 3 mA; V_{CC} = 2.7 V; Note 1	0	—	0.4	V
I_{LI}	Input leakage current	SDA, SCL pins = V_{CC} = 5.5 V	—	—	±5	µA

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
System characteristics						
f_{I2C}	I²C operating frequency		0	—	400	kHz
t_{BUF}	Bus free time between STOP and START condition	Note 4	1.3	—	—	µs
$t_{HD,STA}$	Hold time after (repeated) START condition	Note 4	0.6	—	—	µs
$t_{SU,STA}$	Repeated START condition setup time	Note 4	0.6	—	—	µs
$t_{SU,STO}$	STOP condition setup time	Note 4	0.6	—	—	µs
$t_{HD,DAT}$	Data hold time	Note 4	300	—	—	ns
$t_{SU,DAT}$	Data setup time	Note 4	100	—	—	ns
t_{LOW}	Clock LOW period	Note 4	1.3	—	—	µs
t_{HIGH}	Clock HIGH period	Note 4	0.6	—	—	µs
t_t	Clock, data fall time	Notes 4 and 5	20 +0.1C_b	—	300	ns
t_r	Clock, data rise time	Notes 4 and 5	20 +0.1C_b	—	300	ns

NOTES:
1. This specification applies over the full operating temperature range.
2. $I_{PULLUPAC}$ varies with temperature and V_{CC} voltage, as shown in the Typical Performance Characteristics section.
3. The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in the Typical Performance Characteristics section.
4. Guaranteed by design, not production tested.
5. C_B = total capacitance of one bus line in pF.
6. SDA_IN/SCL_IN = 0.1 V, SDA_OUT/SCL_OUT through resistor to V_{CC}.
7. Delays that can occur after ENABLE and/or idle times have passed.

TYPICAL PERFORMANCE CHARACTERISTICS

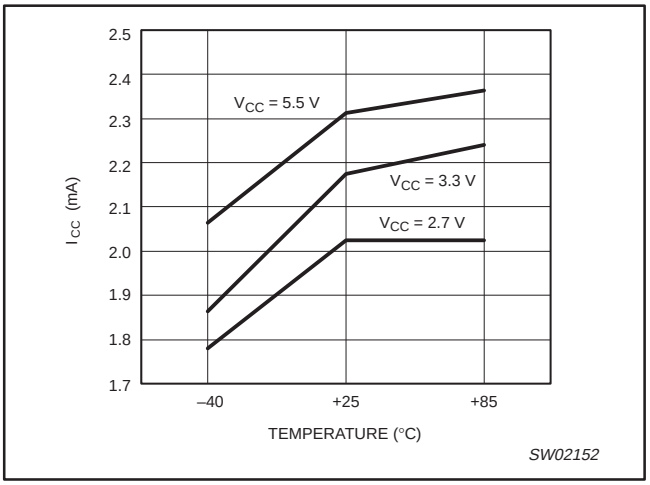


Figure 10. I_{CC} versus Temperature

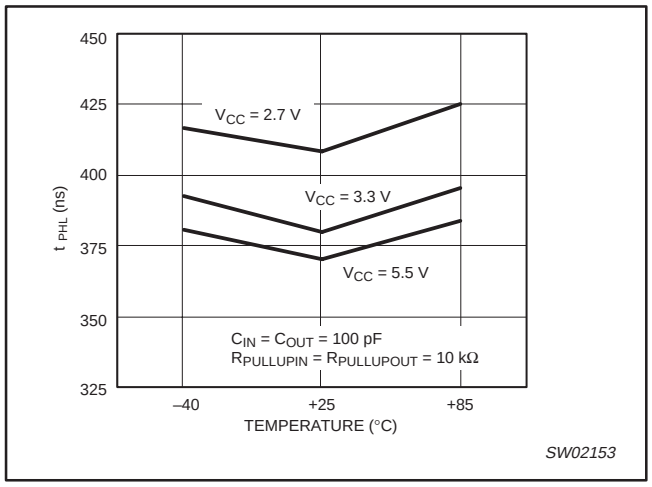


Figure 12. Input–output t_{PHL} versus Temperature

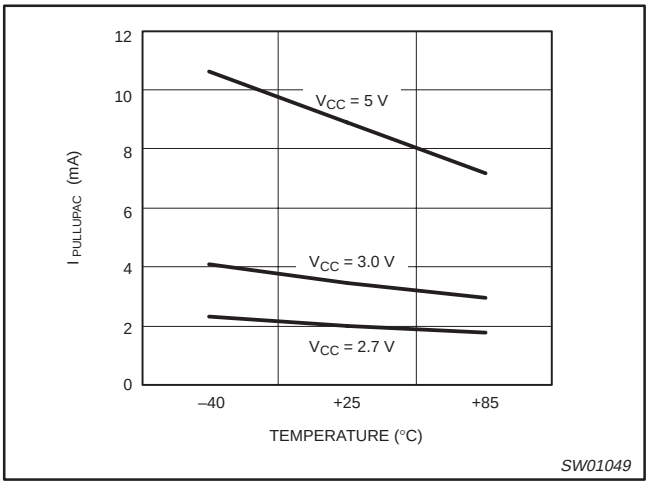


Figure 11. $I_{PULLUPAC}$ versus Temperature

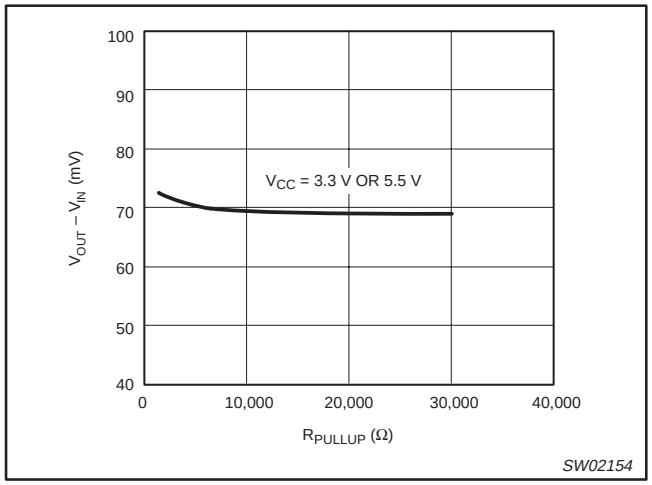


Figure 13. Connection circuitry V_{OUT} – V_{IN}

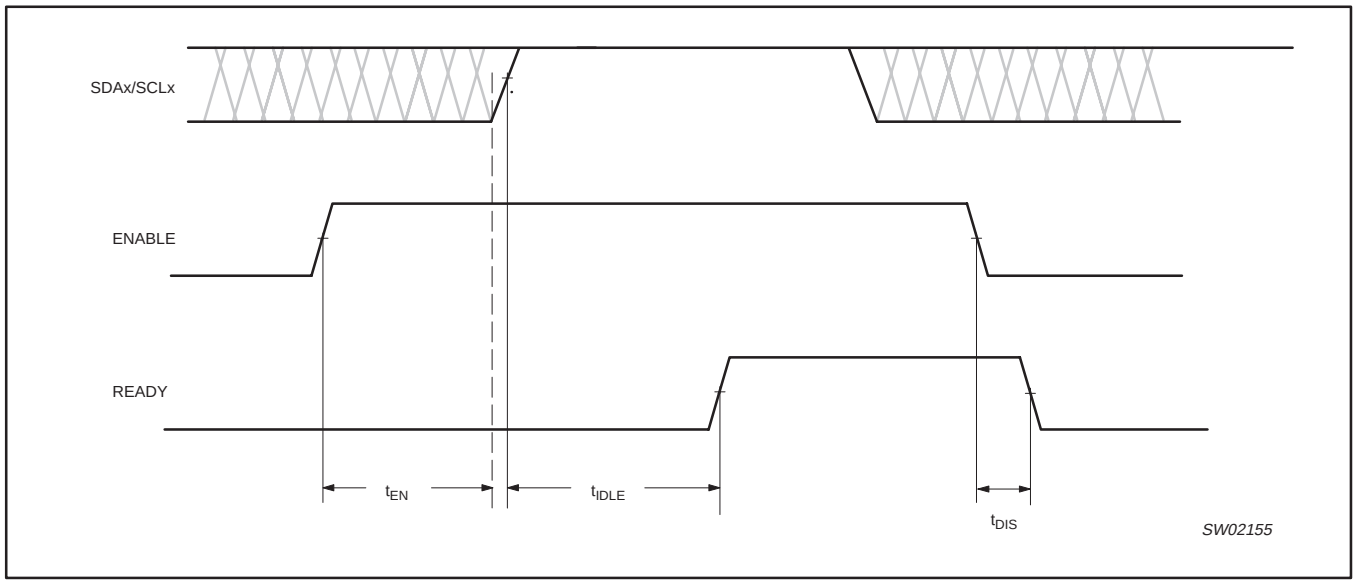


Figure 14. Timing for t_{ENABLE}, t_{IDLE}, and $t_{DISABLE}$

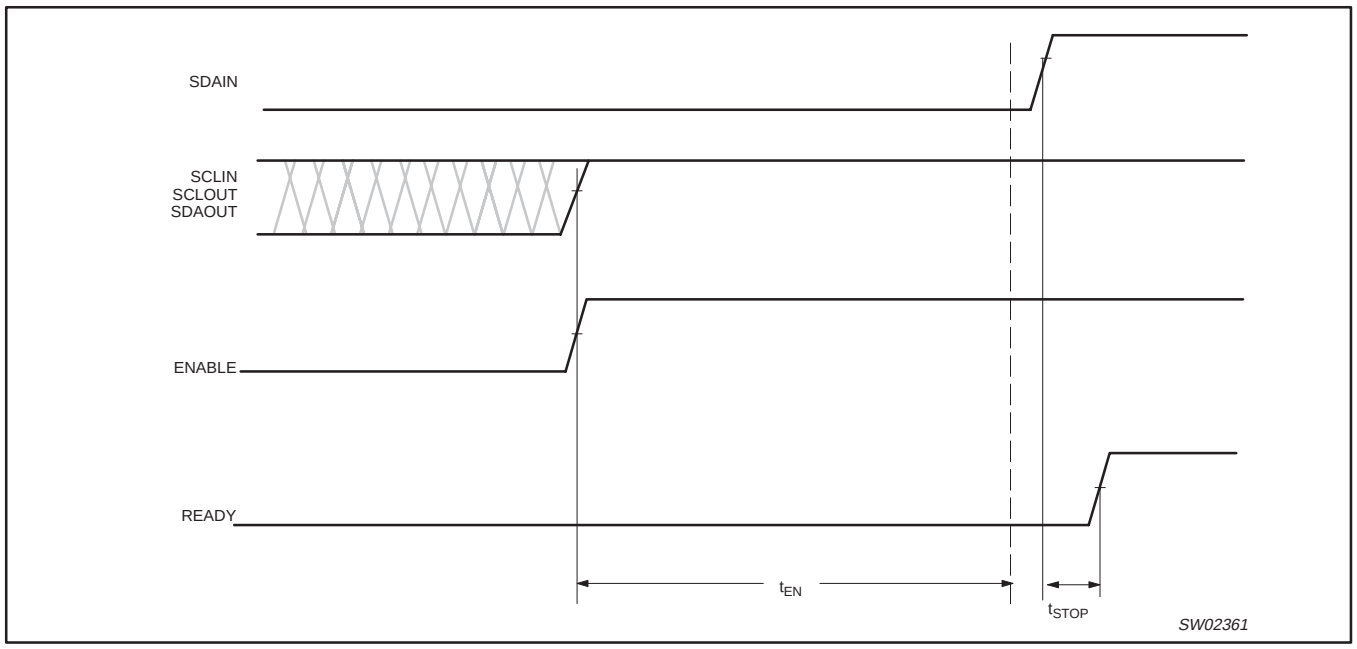


Figure 15. t_{STOP} that can occur after t_{ENABLE}

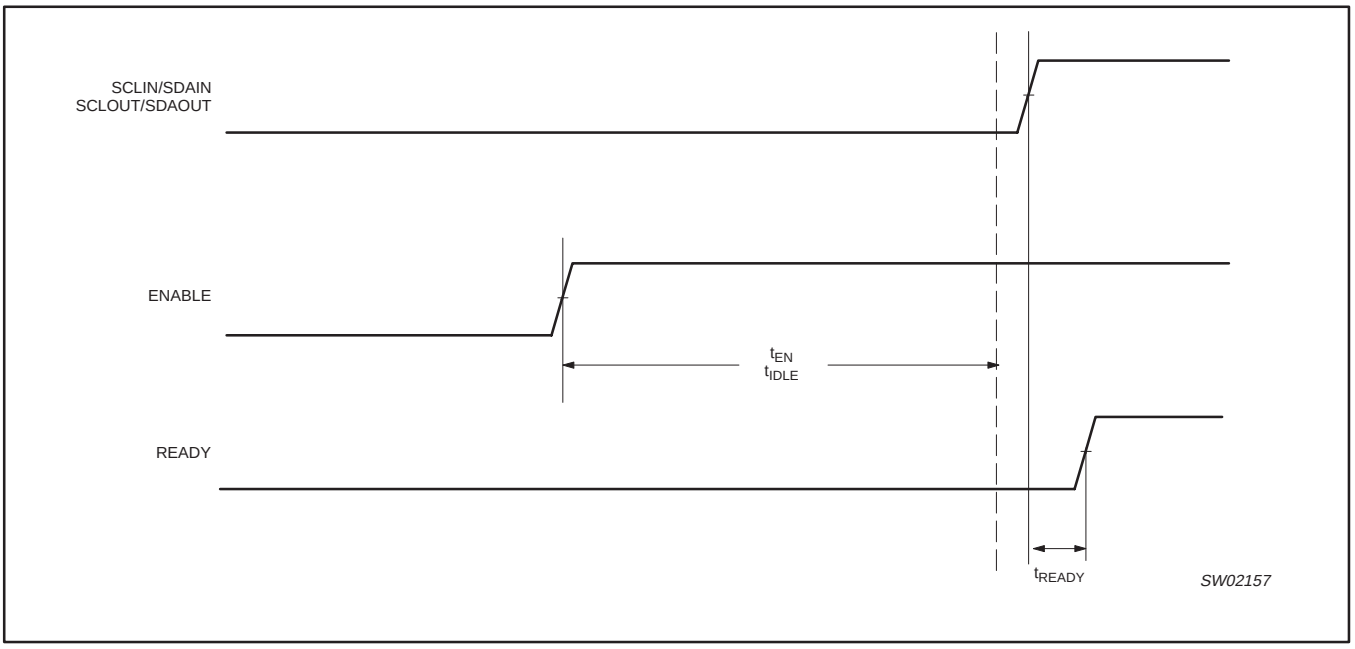
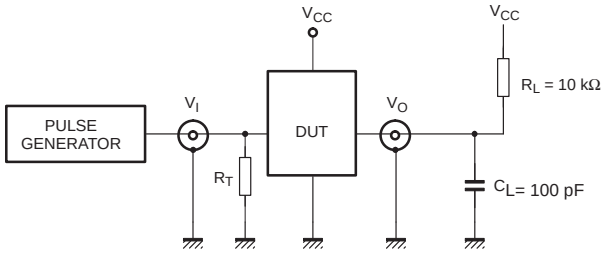


Figure 16. t_{READY} delay that can occur after t_{ENABLE} and t_{IDLE}



DEFINITIONS

R_L = Load resistor.

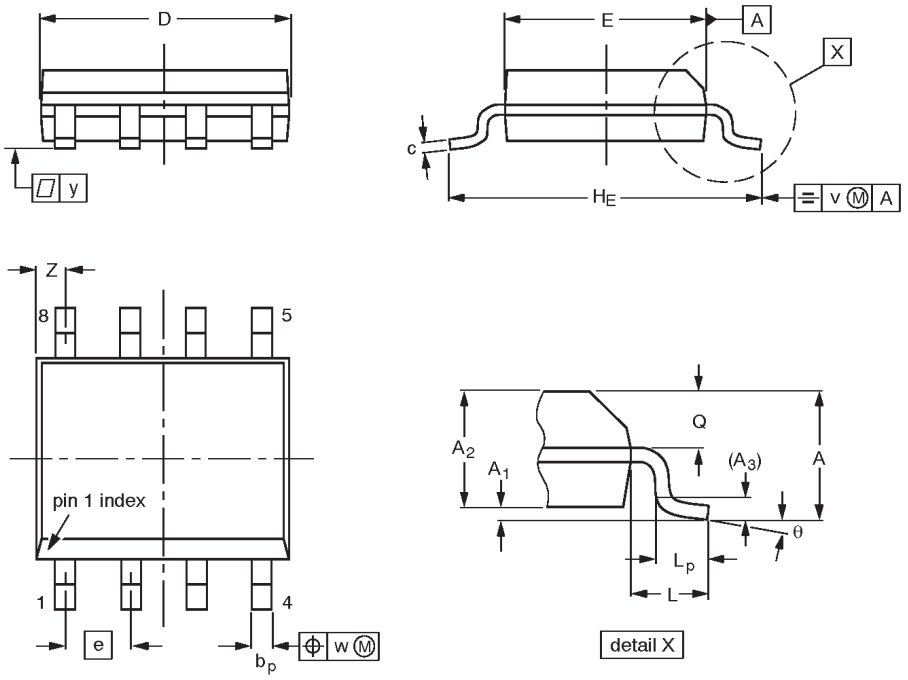
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

SW02345

Figure 17. Test circuitry for switching times

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

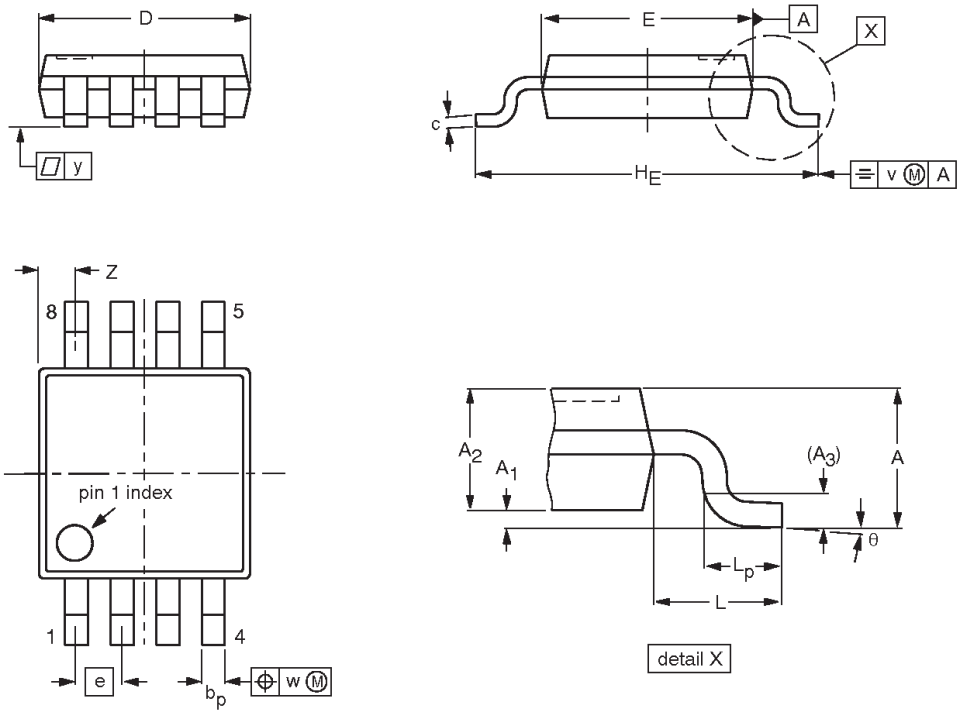
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

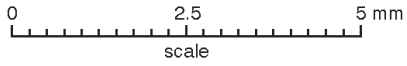
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
PCA9511_4	20060823	Product data sheet. Replaces data sheet PCA9510_PCA9511_3 of 2006 Aug 15. Modifications: ● Removed part type PCA9510 and its specific features from this data sheet. ● Features section on page 2: removed bullet item “5.5 V tolerant I/Os”
PCA9510_PCA9511_3	20060815	Product data sheet (9397 750 14494). Supersedes data of 2004 Oct 05 (9397 750 13998).
PCA9510_PCA9511_2	20041005	Product data sheet (9397 750 13998). Supersedes data of 2003 Dec 18 (9397 750 12561).
PCA9510_PCA9511_1	20031218	Product data (9397 750 12561). ECN 853-2442 01-A14987 dated 15 December 2003.

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this data sheet was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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