PCA85133

Universal LCD driver for low multiplex rates

Rev. 1 — 23 October 2009 Product data sheet

1. General description

The PCA85133 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 80 segments and can easily be cascaded for larger LCD applications. The PCA85133 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

AEC-Q100 compliant for automotive applications.

2. Features

- Single-chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, ½, or ⅓
- Selectable frame frequency: 82 Hz or 110 Hz
- Internal LCD bias generation with voltage-follower buffers
- 80 segment drives:
  - Up to 40 7-segment alphanumeric characters
  - Up to 21 14-segment alphanumeric characters
  - Any graphics of up to 320 elements
- 80 × 4 bit RAM for display data storage
- Auto-incremental display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide LCD supply range for low-threshold LCDs, for guest-host LCDs, and high-threshold (automobile) twisted nematic LCDs: from 2.5 V to 8.0 V
- Low power consumption
- 400 kHz I^2C-bus interface
- Compatible with 4-bit, 8-bit, or 16-bit microprocessors or microcontrollers
- May be cascaded for large LCD applications (up to 5120 segments possible)
- No external components needed
- Compatible with Chip-On-Glass (COG) technology

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 17.

- Manufactured using silicon gate CMOS process

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Name	Description	Delivery form[1]	Version
PCA85133U/2DA/Q1	PCA85133	bare die; 110 bumps; 4.16 × 1.07 × 0.40 mm	chip with hard bumps in tray	PCA85133
PCA85133U/2DB/Q1	PCA85133	bare die; 110 bumps; 4.16 × 1.07 × 0.40 mm	chip with soft bumps in tray	PCA85133

[1] Bump hardness see Table 20.

4. Marking

Table 2. Marking codes

Type number	Marking code
PCA85133U/2DA/Q1	PC85133-1
PCA85133U/2DB/Q1	PC85133-1

5. Block diagram

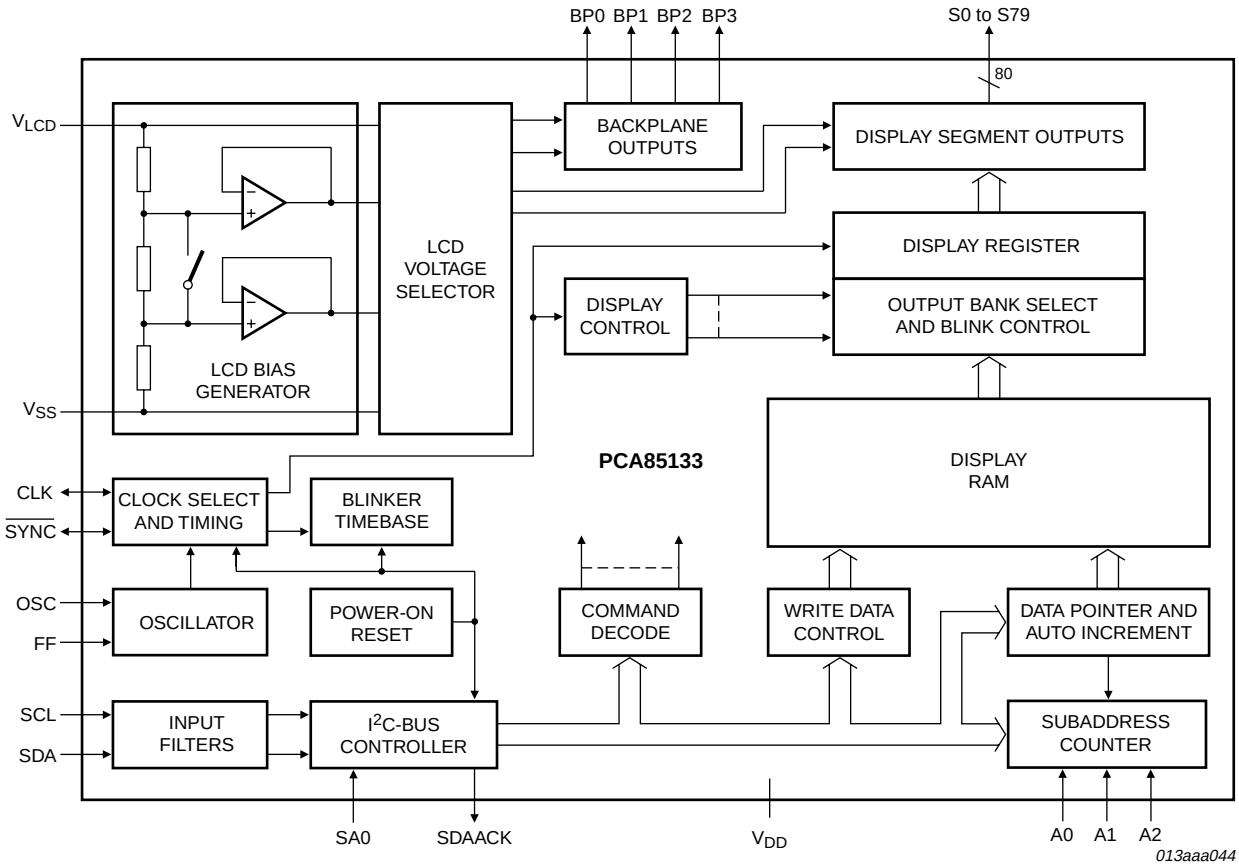
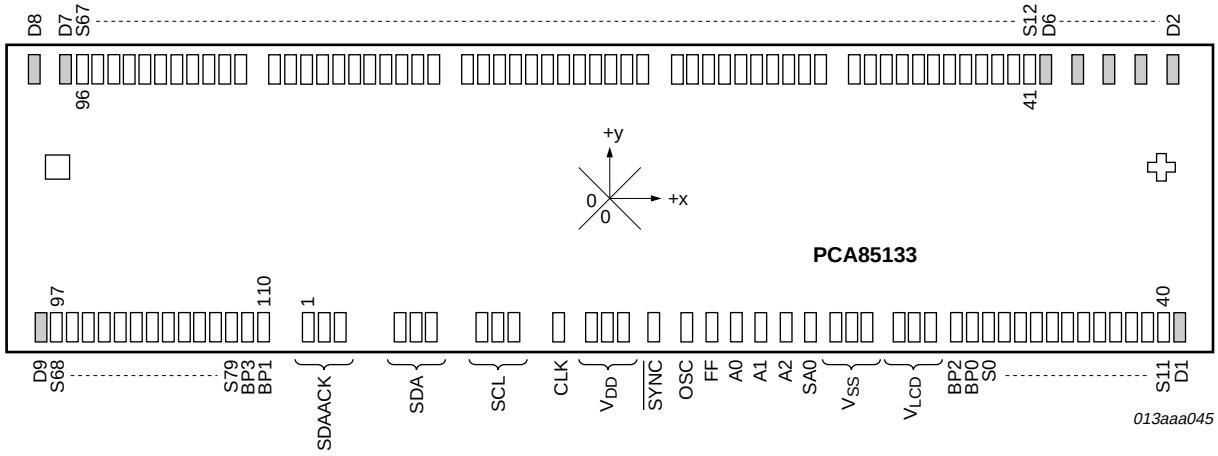


Fig 1. Block diagram of PCA85133

6. Pinning information

6.1 Pinning



Viewed from active side. For mechanical details, see Figure 23.

Fig 2. Pin configuration of PCA85133

6.2 Pin description

Table 3. Pin description overview

Symbol	Pin	Description
SDAACK	1 to 3	I^2C-bus acknowledge output
SDA	4 to 6	I^2C-bus serial data input
SCL	7 to 9	I^2C-bus serial clock input
CLK	10	clock input and output
V_{DD}	11 to 13	supply voltage
$\overline{SYNC}$	14	cascade synchronization input and output
OSC	15	oscillator select
FF	16	frame frequency select
A0, A1 and A2	17 to 19	subaddress input
SA0	20	I^2C-bus slave address input
V_{SS}[1]	21 to 23	ground supply voltage
V_{LCD}	24 to 26	LCD supply voltage
BP2, BP0, BP3 and BP1	27, 28, 109 and 110	LCD backplane output
S0 to S79	29 to 108	LCD segment output
D1 to D9	-	dummy pins

[1] The substrate (rear side of the die) is wired to V_{SS} but should not be electrically contacted.

7. Functional description

The PCA85133 is a versatile peripheral device, designed to interface between any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 80 segments.

The display configurations possible with the PCA85133 depend on the required number of active backplane outputs. A selection of display configurations is shown in Table 4.

All of the display configurations can be implemented in a typical system as shown in Figure 3.

Table 4. Possible display configurations

Number of		7-segment alphanumeric		14-segment alphanumeric		Dot matrix
Backplanes	Elements	Digits	Indicator symbols	Characters	Indicator symbols	
4	320	40	40	20	40	320 (4 × 80)
3	240	30	30	16	16	240 (3 × 80)
2	160	20	20	10	20	160 (2 × 80)
1	80	10	10	5	10	80 (1 × 80)

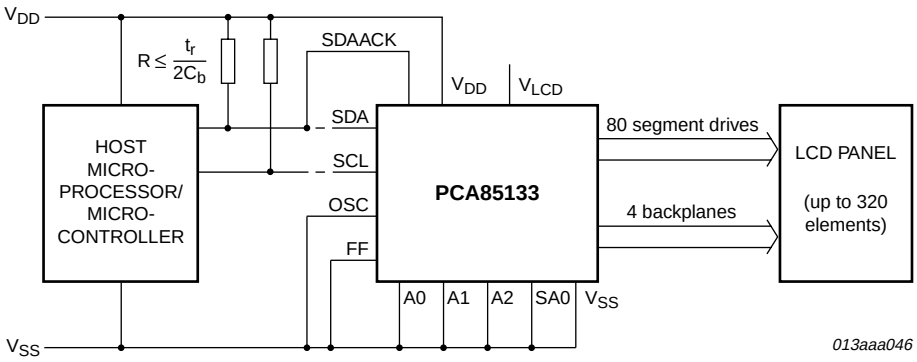


Fig 3. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I^2C-bus communication channel with the PCA85133.

The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel selected for the application.

7.1 Power-on reset

At power-on the PCA85133 resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors between V_{LCD} and V_{SS}. The center resistor is bypassed by switch if the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration is selected.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command (see Table 10) from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 5.

Table 5. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2+2a+n}{n\times(1+a)^2}} \quad (1)$$

where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 3 for 1:3 multiplex

n = 4 for 1:4 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2-2a+n}{n\times(1+a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2+(n-1)}{(a-1)^2+(n-1)}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6}\times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4\times\sqrt{3})}{3}\right] = 2.309V_{off(RMS)}$

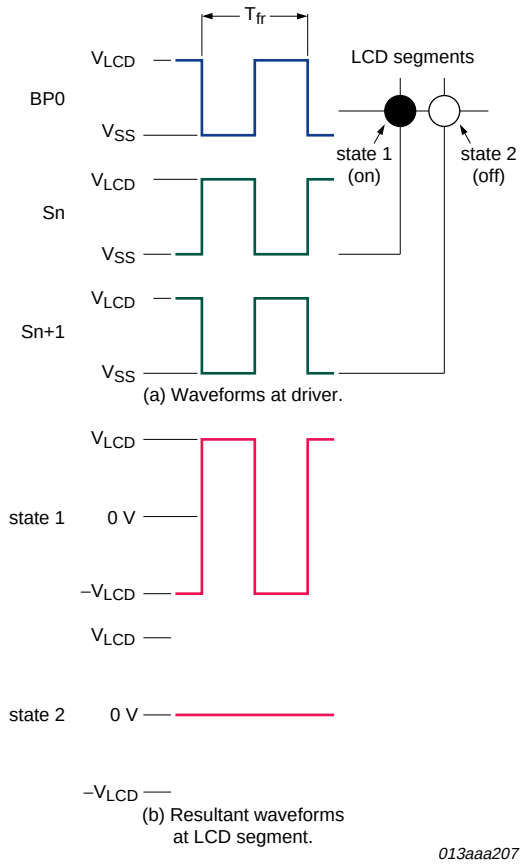
These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 4.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

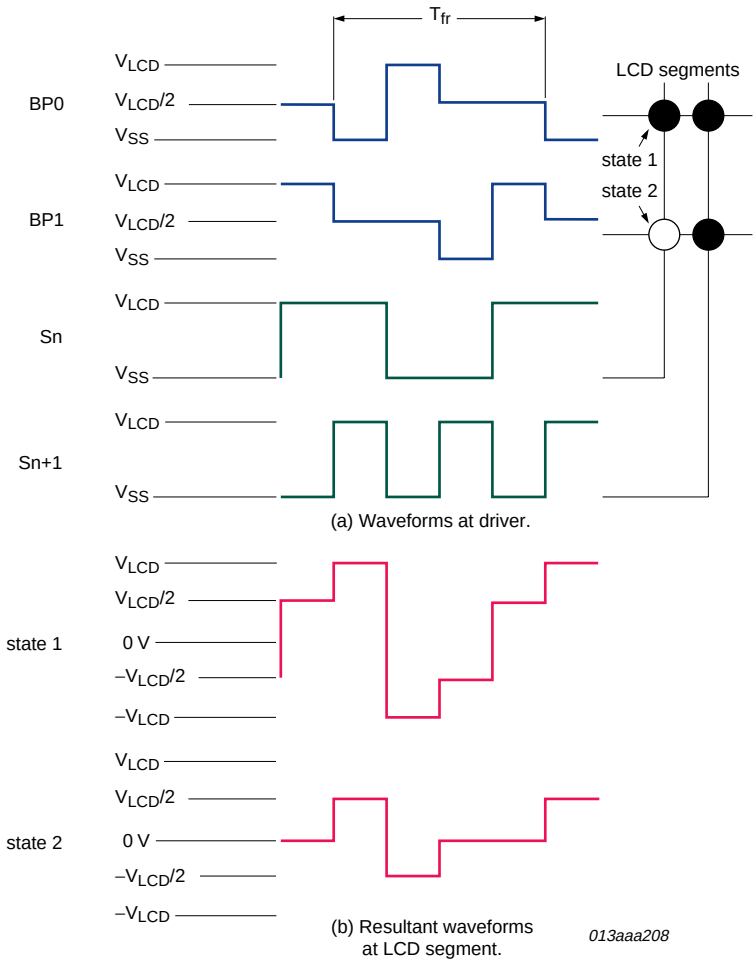
$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 4. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA85133 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 5 and Figure 6.



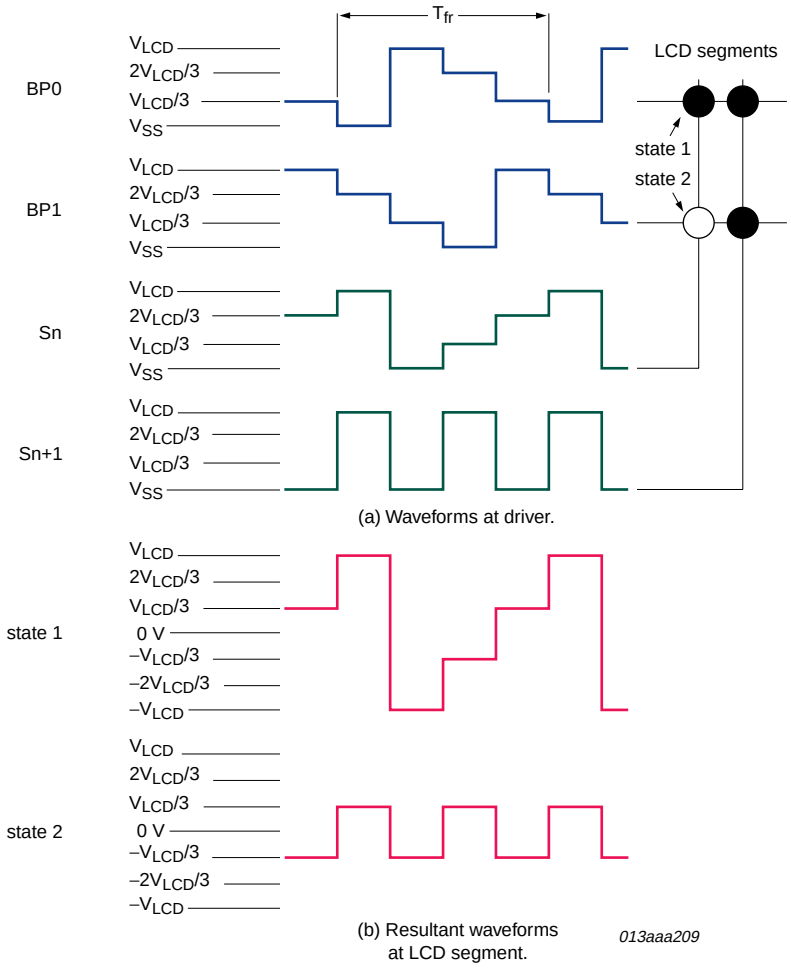
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 5. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

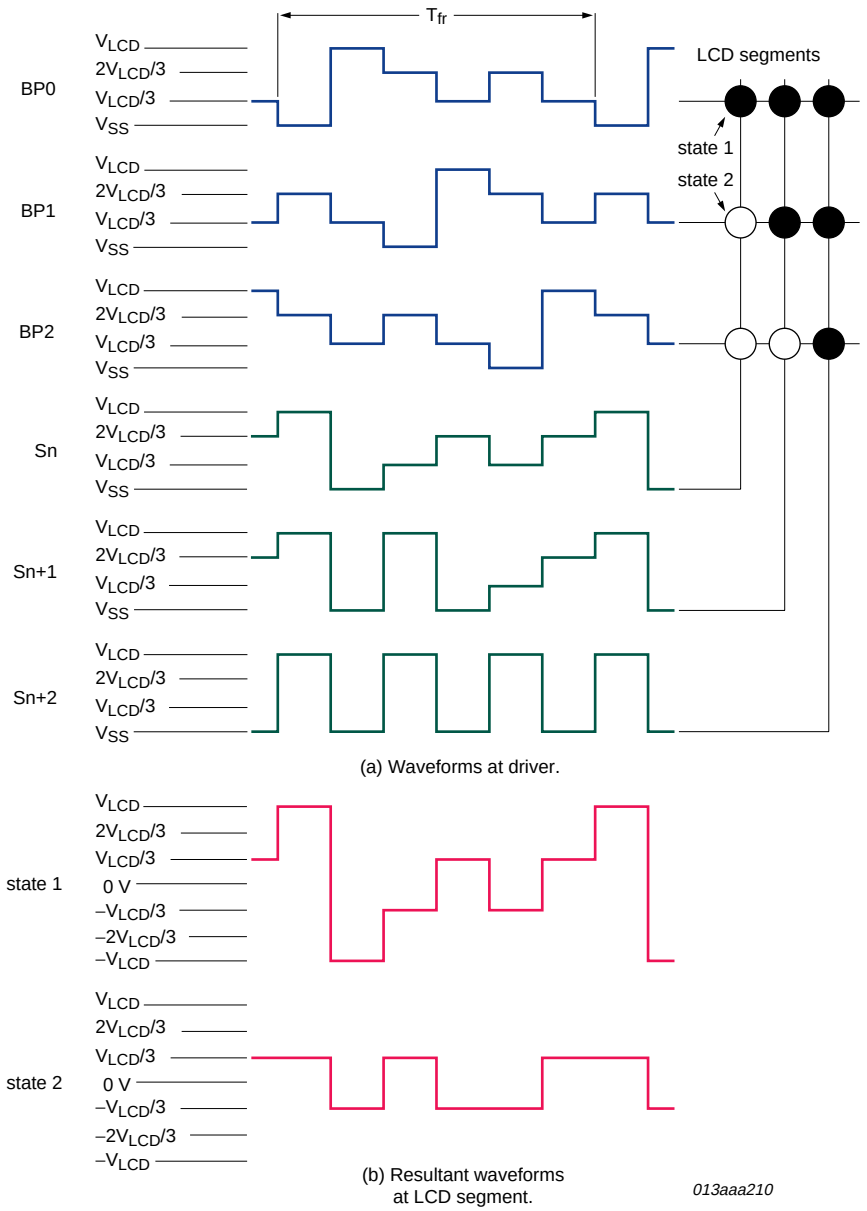
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 6. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 7.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

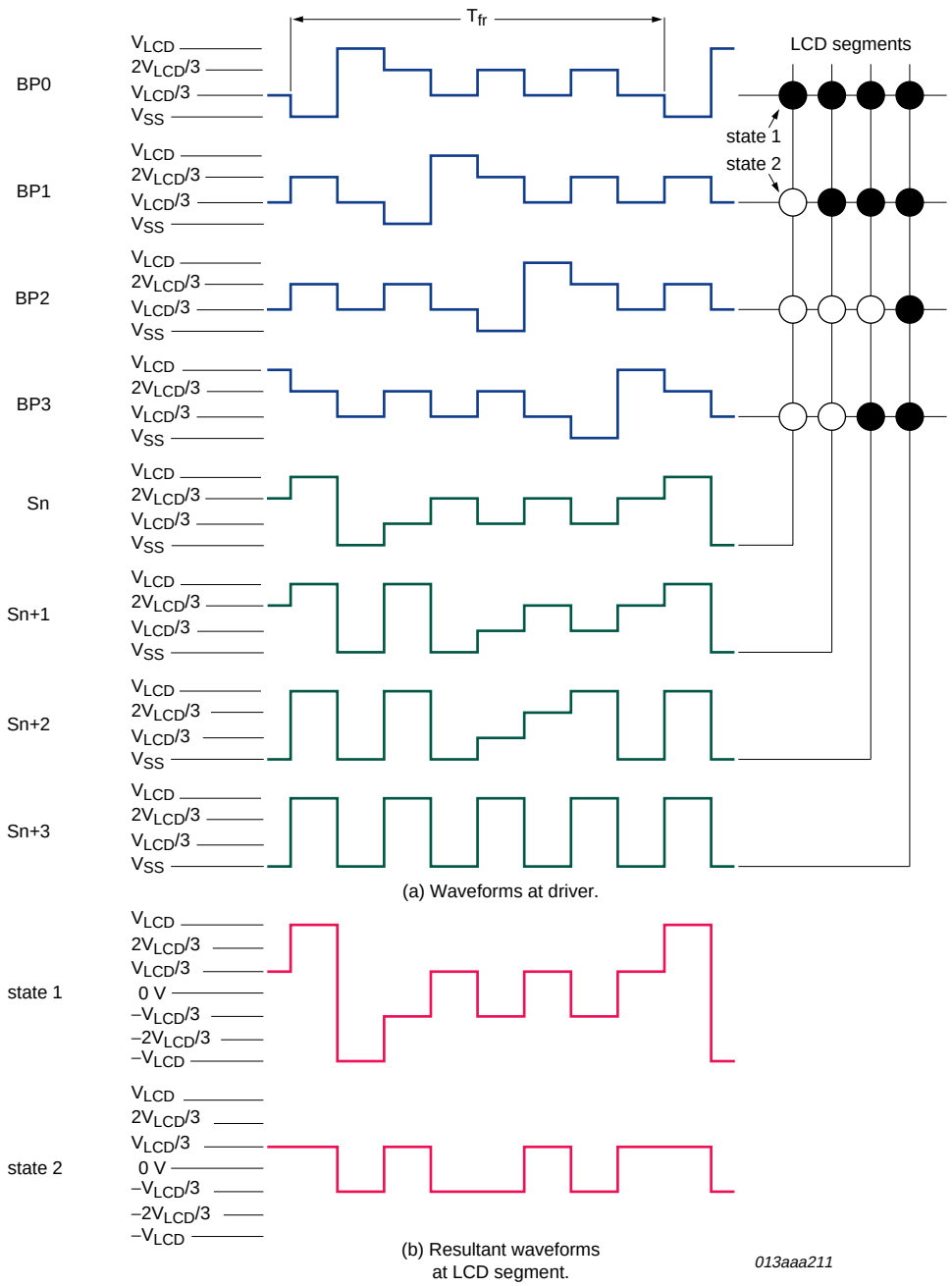
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 7. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 8.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.5 Oscillator

The internal logic and the LCD drive signals of the PCA85133 are timed by a frequency f_{clk} which either is derived from the built-in oscillator frequency f_{osc}:

$$f_{clk} = \frac{f_{osc}}{64} \quad (4)$$

or equals an external clock frequency $f_{clk(ext)}$:

$$f_{clk} = f_{clk(ext)} \quad (5)$$

7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to V_{SS}. In this case the output from pin CLK provides the clock signal for any cascaded PCA85133 in the system. After power-on, pin SDA must be HIGH to guarantee that the clock starts.

7.5.2 External clock

Connecting pin OSC to V_{DD} enables an external clock source. Pin CLK then becomes the external clock input.

Remark: A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing and frame frequency

The clock frequency f_{clk} determines the LCD frame frequency f_{fr} and is calculated as follows:

$$f_{fr} = \frac{f_{clk}}{24} \quad (6)$$

The internal clock frequency f_{clk} can be selected using pin FF. As a result 2 frame frequencies are available: 82 Hz or 110 Hz (typical), see Table 6.

Table 6. LCD frame frequencies

Pin FF tied to	Typical clock frequency (Hz)	LCD frame frequency (Hz)
V_{DD}	1970	82
V_{SS}	2640	110

The timing of the PCA85133 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between all the PCA85133 in the system.

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs and one column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 80 segment outputs (S0 to S79) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 80 segment outputs are required the unused segment outputs must be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated in accordance with the selected LCD drive mode.

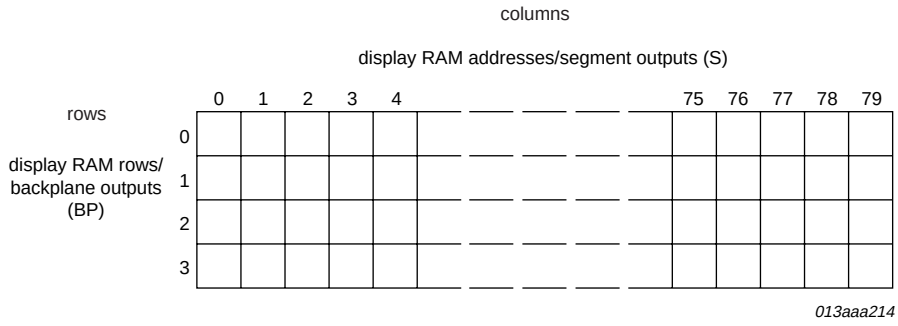
- In the 1:4 multiplex drive mode BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1; therefore, these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, BP1 and BP3 respectively carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: The same signal is carried by all four backplane outputs; and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

The display RAM is a static 80 × 4 bit RAM which stores LCD data. A logic 1 in the RAM bit map indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs and between the individual bits of a RAM word and the backplane outputs. The display RAM bit map Figure 9 shows rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and columns 0 to 79 which correspond with the segment outputs S0 to S79. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



The display RAM bitmap shows the direct relationship between the display RAM addresses and the segment outputs and between the bits in a RAM word and the backplane outputs.

Fig 9. Display RAM bitmap

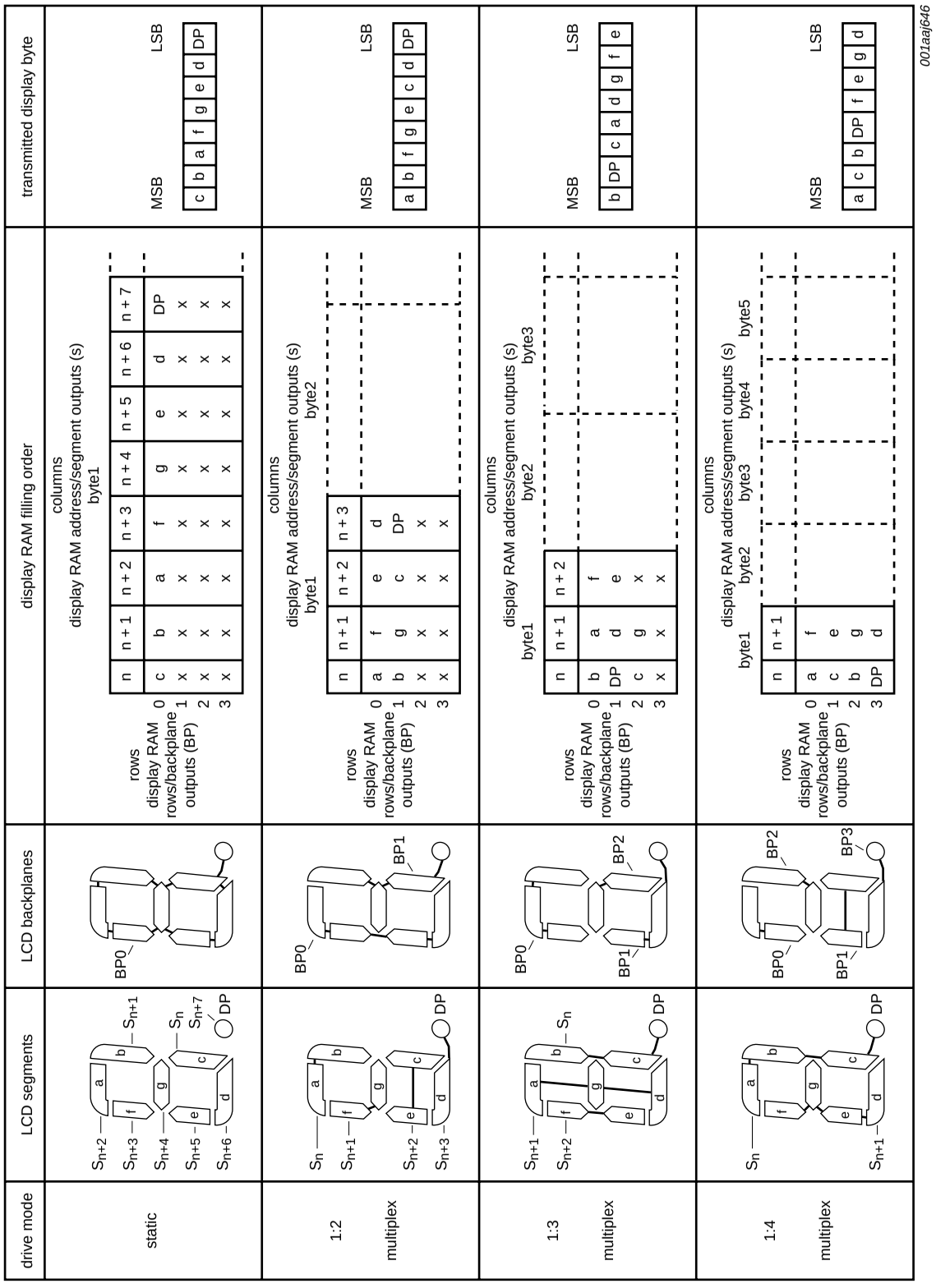


Fig 10. Relationships between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

When display data is transmitted to the PCA85133, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 10; the RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 10:

- In static drive mode the eight transmitted data bits are placed into row 0 of eight successive 4-bit RAM words.
- In 1:2 multiplex mode the eight transmitted data bits are placed in pairs into row 0 and 1 of four successive 4-bit RAM words.
- In 1:3 multiplex mode the eight bits are placed in triples into row 0, 1 and 2 of three successive 4-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In the 1:4 multiplex mode the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 of two successive 4-bit RAM words.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using a data pointer.

This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command.

Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 10.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I^2C-bus data access is terminated early then the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

7.12 Subaddress counter

The storage of display data is conditioned by the content of the subaddress counter. Storage is allowed only when the content of the subaddress counter match with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 12). If the content of the subaddress counter and the hardware subaddress do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCA85133 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 27th display data byte transmitted in 1:3 multiplex mode).

The hardware subaddress must not be changed whilst the device is being accessed on the I^2C-bus interface.

7.13 Output bank selector

The output bank selector selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, row 2, and then row 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCA85133 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command. The input bank selector functions independently to the output bank selector.

7.15 Blinking

The display blink capabilities of the PCA85133 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 14). The blink frequencies are fractions of the clock frequency. The ratios between the clock and blink frequencies depend on the blink mode selected (see Table 7).

Table 7. Blink frequencies

Blink mode	Operating mode ratio	Blink frequency with respect to f_{clk} (typical)		Unit
		f_{clk} = 1.970 kHz	f_{clk} = 2.640 kHz	
off	-	blinking off	blinking off	Hz
1	$\frac{f_{clk}}{768}$	2.5	3.5	Hz
2	$\frac{f_{clk}}{1536}$	1.3	1.7	Hz
3	$\frac{f_{clk}}{3072}$	0.6	0.9	Hz

An additional feature is for an arbitrary selection of LCD segments to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can blink by selectively changing the display RAM data at fixed time intervals.

If the entire display can blink at a frequency other then the typical blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 10).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

By connecting pin SDAACK to pin SDA on the PCA85133, the SDA line becomes fully I²C-bus compatible. In COG applications where the track resistance from the SDAACK pin to the system SDA line can be significant, possibly a voltage divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. As a consequence it may be possible that the acknowledge generated by the PCA85133 can't be interpreted as logic 0 by the master. In COG applications where the acknowledge cycle is required, it is therefore necessary to minimize the track resistance from the SDAACK pin to the system SDA line to guarantee a valid LOW level.

By separating the acknowledge output from the serial data line (having the SDAACK open circuit) design efforts to generate a valid acknowledge level can be avoided. However, in that case the I²C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

The following definition assumes SDA and SDAACK are connected and refers to the pair as SDA.

2. For further information, please consider the NXP application note: Ref. 1 "AN10170".

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 11).

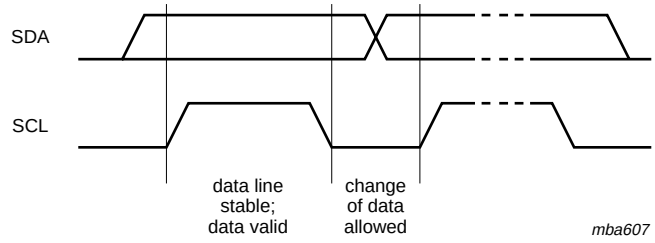


Fig 11. Bit transfer

7.16.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 12.

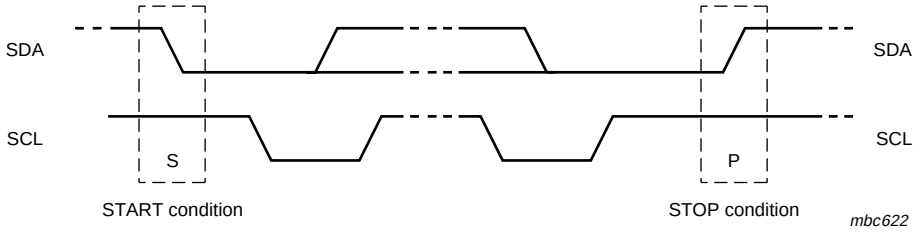


Fig 12. Definition of START and STOP conditions

7.16.2 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 13.

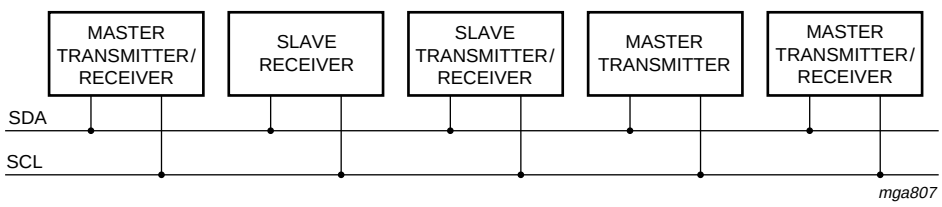


Fig 13. System configuration

7.16.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is shown in Figure 14.

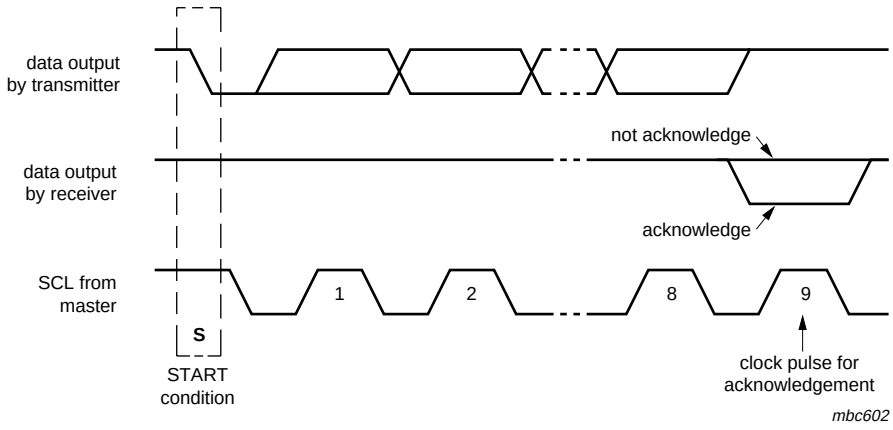


Fig 14. Acknowledgement on the I^2C-bus

7.16.4 I^2C-bus controller

The PCA85133 acts as an I^2C-bus slave receiver. It does not initiate I^2C-bus transfers or transmit data to an I^2C-bus master receiver. The only data output from the PCA85133 are the acknowledge signals from the selected devices. Device selection depends on the I^2C-bus slave address, on the transferred command data, and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I^2C-bus slave address have the same hardware subaddress.

7.16.5 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.6 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCA85133. The least significant bit of the slave address is bit R/$\overline{W}$. The PCA85133 is a write-only device. It will not respond to a read access, so this bit should always be logic 0. The second bit of the slave address is defined by the level tied at input SA0. Two types of PCA85133 can be distinguished on the same I²C-bus which allows:

- Up to 16 PCA85133 on the same I²C-bus for very large LCD applications
- The use of two types of LCD multiplex drive modes on the same I²C-bus

The I²C-bus protocol is shown in Figure 15. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the available PCA85133 slave addresses. All PCA85133 with the same SA0 level acknowledge in parallel to the slave address. All PCA85133 with the alternative SA0 level ignore the whole I²C-bus transfer.

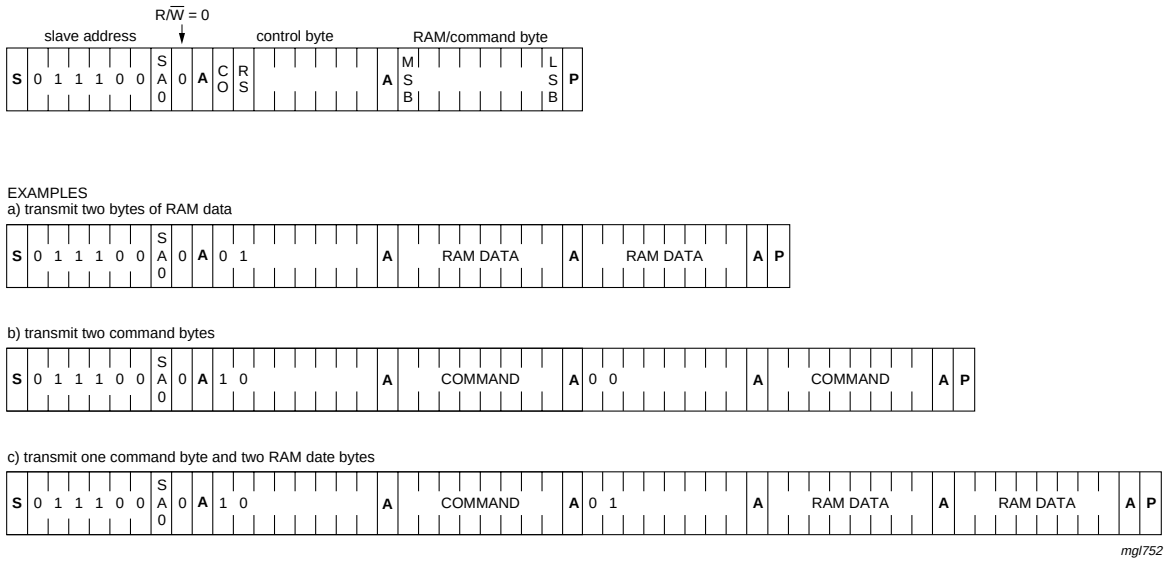


Fig 15. I²C-bus protocol

After acknowledgement, the control byte is sent, defining if the next byte is a RAM or command information. The control byte also defines if the next byte is a control byte or further RAM or command data (see Figure 16 and Table 8). In this way it is possible to configure the device and then fill the display RAM with little overhead.

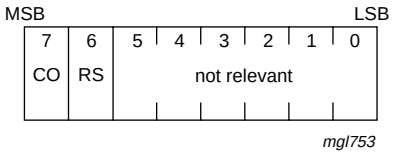


Fig 16. Control byte format

Table 8. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		**register selection**
		0	command register
		1	data register
5 to 0	-		not relevant

The command bytes and control bytes are also acknowledged by all addressed PCA85133 connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated.

The acknowledgement after each byte is made only by the (A0, A1, and A2) addressed PCA85133. After the last display byte, the I^2C-bus master issues a STOP condition (P). Alternatively a START may be asserted to RESTART an I^2C-bus access.

7.17 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The commands available to the PCA85133 are defined in Table 9.

Table 9. Definition of commands

Command	Operation code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	1	1	0	0	E	B	M1	M0	Table 10
load-data-pointer	0	P6	P5	P4	P3	P2	P1	P0	Table 11
device-select	1	1	1	0	0	A2	A1	A0	Table 12
bank-select	1	1	1	1	1	0	I	O	Table 13
blink-select	1	1	1	1	0	A	BF1	BF0	Table 14

Table 10. Mode-set command bit description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status**[1]
		0	disabled (blank)
		1	enabled
2	B		**LCD bias configuration**
		0	⅓ bias
		1	½ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; 1 backplane
		10	1:2 multiplex; 2 backplanes
		11	1:3 multiplex; 3 backplanes
		00	1:4 multiplex; 4 backplanes

[1] The possibility to disable the display allows implementation of blinking under external control.

Table 11. Load-data-pointer command bit description

See Section 7.11.

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	0000000 to 1001111	7-bit binary value of 0 to 79, transferred to the data pointer to define one of 80 display RAM addresses

Table 12. Device-select command bit description

See Section 7.12.

Bit	Symbol	Value	Description
7 to 3	-	11100	fixed value
2 to 0	A[2:0]	000 to 111	3-bit binary value of 0 to 7, transferred to the subaddress counter to define one of 8 hardware subaddresses

Table 13. Bank-select command bit description[1]

See Section 7.10, Section 7.11, Section 7.12, Section 7.13 and Section 7.14.

Bit	Symbol	Value	Description	
			Static	1:2 multiplex
7 to 2	-	111110	fixed value	
1	I		**input bank selection**: storage of arriving display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		**output bank selection**: retrieval of LCD display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank-select command has no effect in 1:3 or 1:4 multiplex drive modes.

Table 14. Blink-select command bit description

See Section 7.15.

Bit	Symbol	Value	Description
7 to 3	-	11110	fixed value
2	A		**blink mode selection**[1]
		0	normal blinking
		1	blinking by alternating display RAM banks
1 to 0	BF[1:0]		**blink frequency selection**[2]
		00	off
		01	1
		10	2
		11	3

[1] Normal blinking can only be selected in multiplex drive mode 1:3 or 1:4.

[2] For the blink frequencies, see Table 7.

7.18 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers and coordinates their effects. The display controller also loads the display data into the display RAM as required by the storage order.

8. Internal circuitry

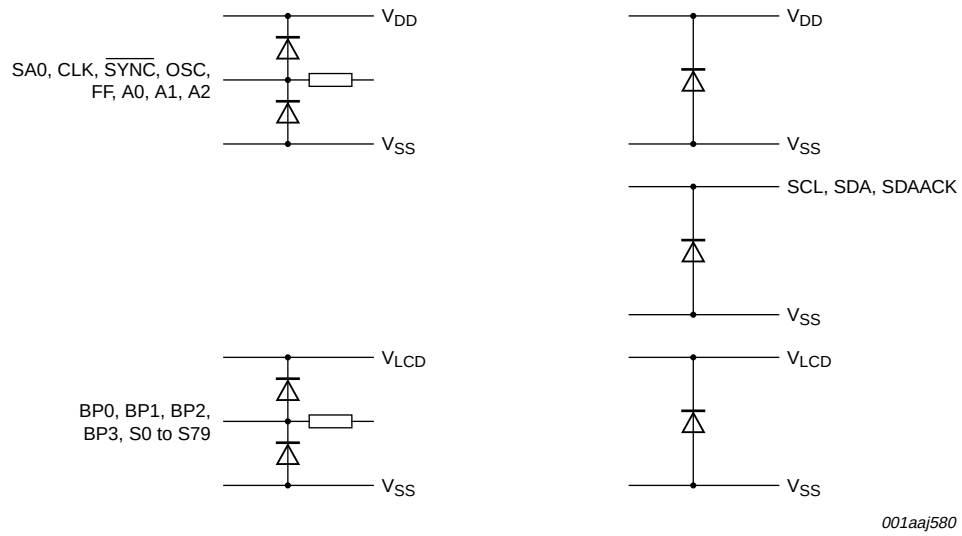


Fig 17. Device protection diagram

9. Limiting values

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
V_{LCD}	LCD supply voltage			–0.5	+9.0	V
$V_{i(n)}$	voltage on any input	V_{DD} related inputs		–0.5	+6.5	V
$V_{o(n)}$	voltage on any output	V_{LCD} related outputs		–0.5	+9.0	V
I_I	input current			–10	+10	mA
I_O	output current			–10	+10	mA
I_{DD}	supply current			–50	+50	mA
I_{SS}	ground supply current			–50	+50	mA
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	Human Body Model	[2]	-	±4500	V
		Machine Model	[3]	-	±250	V
I_{lu}	latch-up current		[4]	-	200	mA
T_{stg}	storage temperature		[5]	–65	+150	°C

[1] Stresses above these values listed may cause permanent damage to the device.

[2] Pass level; Human Body Model (HBM) according to Ref. 5 “JESD22-A114”.

[3] Pass level; Machine Model (MM), according to Ref. 6 “JESD22-A115”.

[4] Pass level; latch-up testing, according to Ref. 7 “JESD78” at maximum ambient temperature ($T_{amb(max)}$ = +95 °C).

[5] According to the NXP store and transport requirements (see Ref. 9 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

10. Static characteristics

Table 16. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 8.0 V; T_{amb} = −40 °C to +95 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	$V_{LCD} \leq 6.5$ V		1.8	-	5.5	V
		$V_{LCD} > 6.5$ V		2.5	-	5.5	V
V_{LCD}	LCD supply voltage	$V_{DD} \geq 2.5$ V		2.5	-	8.0	V
		$V_{DD} < 2.5$ V		2.5	-	6.5	V
V_{POR}	power-on reset voltage			1.0	1.3	1.6	V
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 1536 Hz	[1]	-	16	60	µA
I_{DD}	supply current	$f_{clk(ext)}$ = 1536 Hz	[1]	-	2	20	µA
Logic							
V_I	input voltage			V_{SS} − 0.5	-	V_{DD} + 0.5	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0, FF		$0.7V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2, SA0, FF		V_{SS}	-	$0.3V_{DD}$	V
V_{OH}	HIGH-level output voltage			$0.8V_{DD}$	-	-	V
V_{OL}	LOW-level output voltage			-	-	$0.2V_{DD}$	V
I_{OH}	HIGH-level output current	on pin CLK; V_{OH} = 4.6 V; V_{DD} = 5 V		+1	-	-	mA
I_{OL}	LOW-level output current	on pin CLK, $\overline{SYNC}$; V_{OL} = 0.4 V; V_{DD} = 5 V		-	-	−1	mA
I_L	leakage current	on pins OSC, CLK, SCL, SDA, A0 to A2, SA0, FF; $V_I = V_{DD}$ or V_{SS}		−1	-	+1	µA
C_I	input capacitance		[2]	-	-	7	pF
I²C-bus							
Input on pins SDA and SCL							
V_I	input voltage			V_{SS} − 0.5	-	5.5	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
V_{IL}	LOW-level input voltage			V_{SS}	-	$0.3V_{DD}$	V
C_I	input capacitance		[2]	-	-	7	pF
$I_{OL(SDA)}$	LOW-level output current on pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V		+3	-	-	mA
LCD outputs							
ΔV_O	output voltage variation	on pin BPx; C_{bpl} = 35 nF		−100	-	+100	mV
		on pin Sx; C_{sgm} = 5 nF		−100	-	+100	mV
R_O	output resistance	V_{LCD} = 5 V					
		on pin BPx	[3]	-	1.5	10	kΩ
		on pin Sx	[3]	-	6.0	13.5	kΩ

[1] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I²C-bus inactive.

[2] Not tested, design specification only.

[3] Outputs measured individually and sequentially.

11. Dynamic characteristics

Table 17. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 8.0 V; T_{amb} = −40 °C to +95 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
Internal: output pin CLK							
f_{clk}	clock frequency	pin FF = V_{DD}	[1][2]	1440	1970	2640	Hz
		pin FF = V_{SS}	[1][2]	1920	2640	3600	Hz
f_{fr}	frame frequency	pin FF = V_{DD}		60	82	110	Hz
		pin FF = V_{SS}		80	110	150	Hz
External: input pin CLK							
$f_{clk(ext)}$	external clock frequency		[2]	800	-	5000	Hz
$t_{clk(H)}$	HIGH-level clock time			90	-	-	µs
$t_{clk(L)}$	LOW-level clock time			90	-	-	µs
Synchronization: input pin $\overline{SYNC}$							
$t_{PD(SYNC\_N)}$	$\overline{SYNC}$ propagation delay			-	30	-	ns
t_{SYNC_NL}	$\overline{SYNC}$ LOW time			1	-	-	µs
Outputs: pins BP0 to BP3 and S0 to S79							
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V		-	-	30	µs
I^2C-bus: timing [3][4]							
Pin SCL							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals			-	-	0.3	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{w(spike)}$	spike pulse width	on bus		-	-	50	ns

[1] Typical output duty cycle of 50 %.

[2] The corresponding frame frequency is $f_{fr} = \frac{f_{clk}}{24}$.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[4] For I^2C-bus timings see Figure 19.

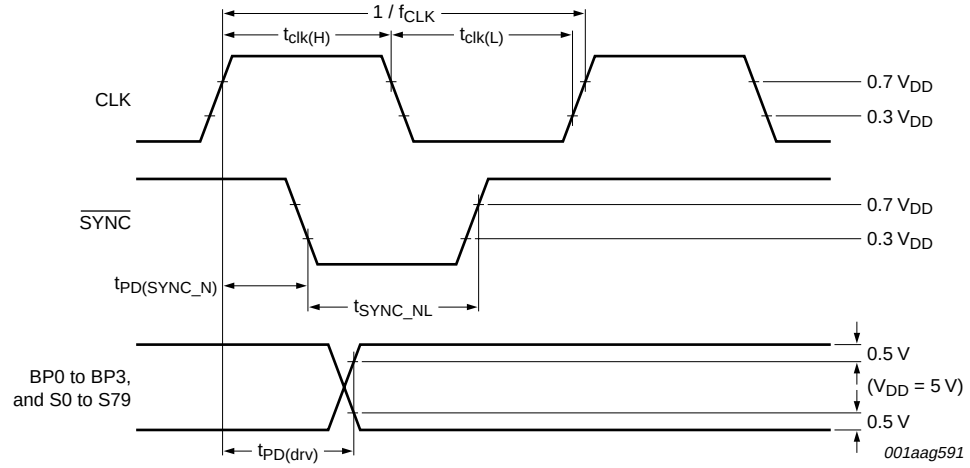


Fig 18. Driver timing waveforms

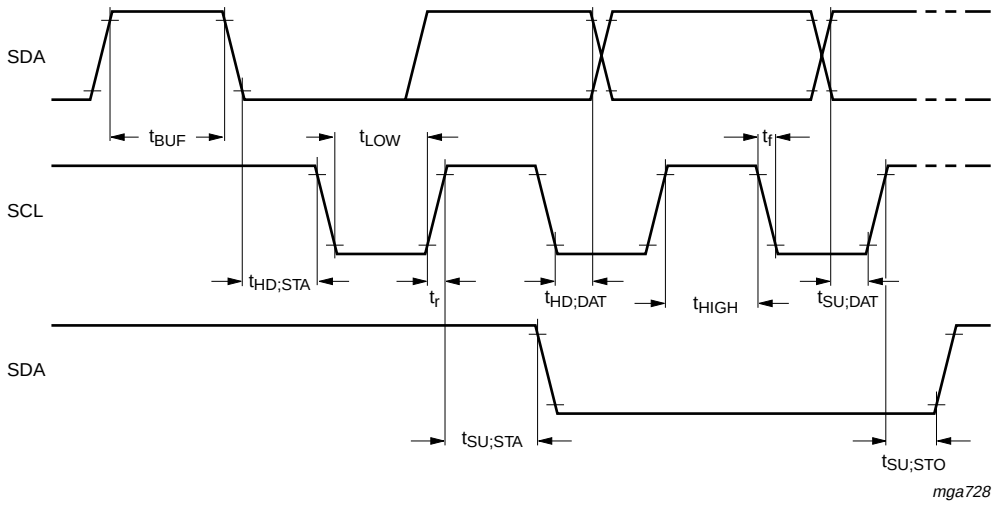


Fig 19. I²C-bus timing waveforms

12. Application information

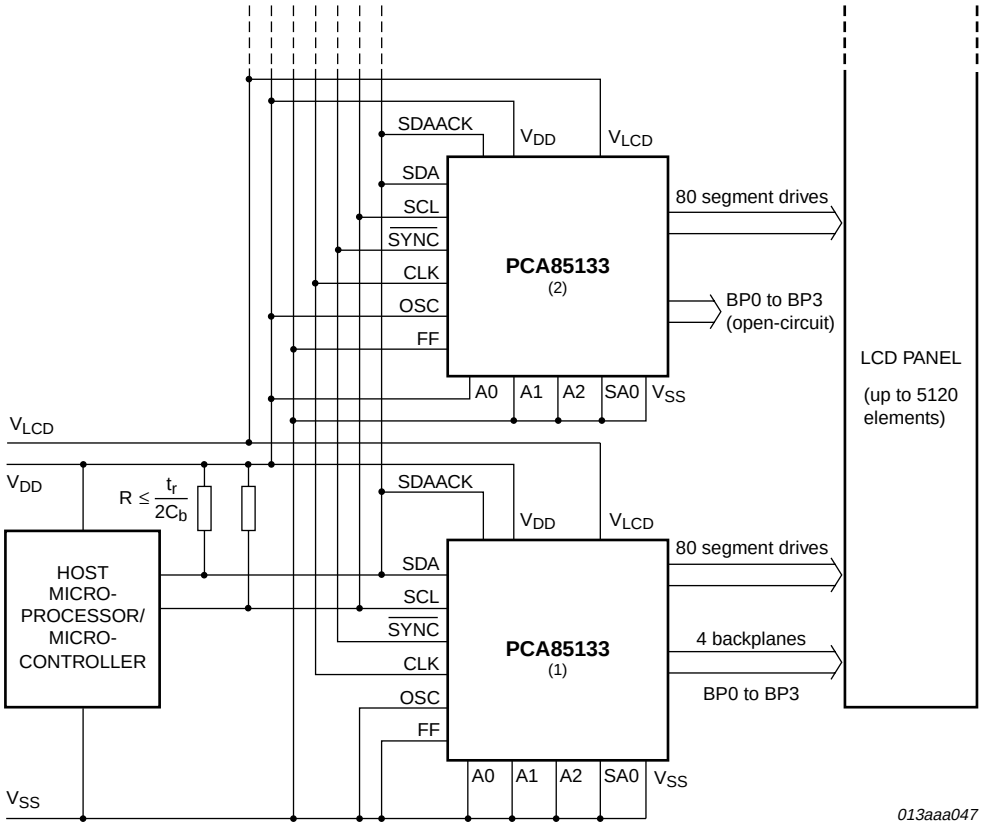
12.1 Cascaded operation

In large display configurations up to 16 PCA85133 can be recognized on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1, and A2) and the programmable I^2C-bus slave address (SA0).

Table 18. Addressing cascaded PCA85133

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

When cascaded PCA85133 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCA85133 of the cascade contribute additional segment outputs, but their backplane outputs are left open-circuit (see Figure 20).



(1) Is master (OSC connected to V_{SS}).

(2) Is slave (OSC connected to V_{DD}).

Fig 20. Cascaded PCA85133 configuration

For display sizes that are not multiple of 320 elements, a mixed cascaded system can be considered containing only devices like PCA85133 and PCA85132. Depending on the application, one must take care of the software command and pin connection compatibility.

Only one master but multiple slaves are allowed in a cascade. No external clock should be used; the slaves get the clock from the master.

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCA85133. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by the definition of a multiplex drive mode when PCA85133 with different SA0 levels are cascaded).

$\overline{\text{SYNC}}$ is organized as an input/output pin; The output selection is realized as an open-drain driver with an internal pull-up resistor. A PCA85133 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCA85133 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCA85133 are shown in Figure 21.

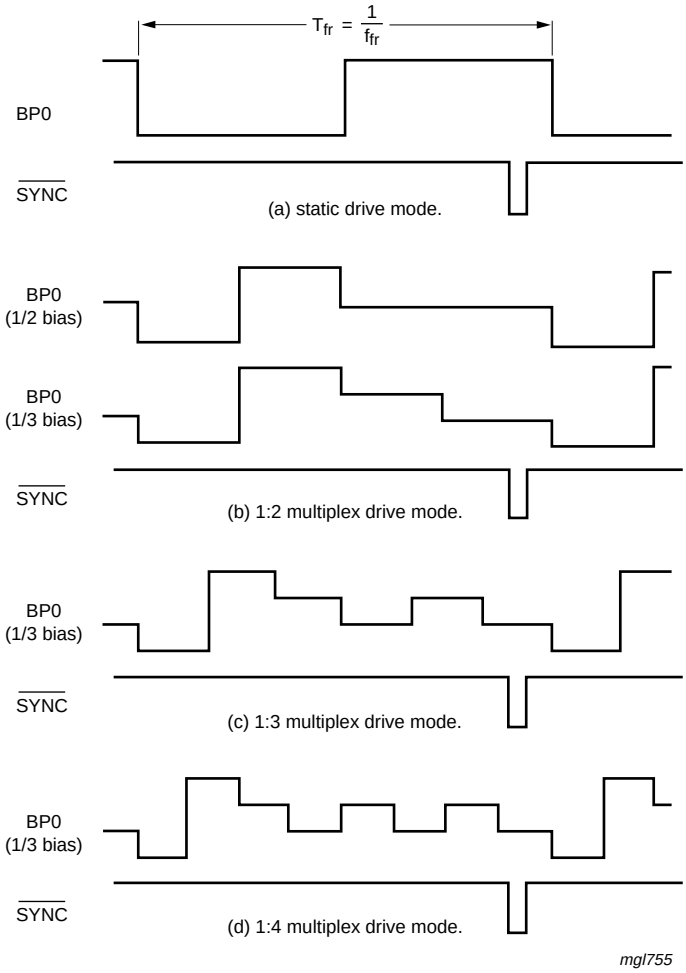


Fig 21. Synchronization of the cascade for the various PCA85133 drive modes

The contact resistance between the $\overline{SYNC}$ pins of cascaded devices must be controlled. If the resistance is too high, then the device will not be able to synchronize properly. This is particularly applicable to COG applications. Table 19 shows the limiting values for contact resistance.

Table 19. $\overline{SYNC}$ contact resistance

Number of devices	Maximum contact resistance
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
11 to 16	700 Ω

13. Bare die description

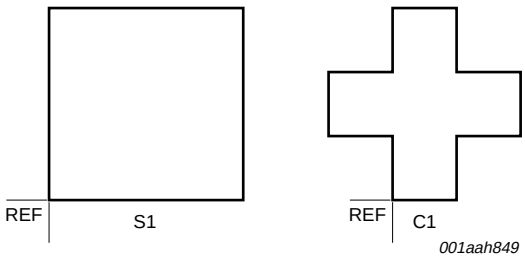
13.1 General description

Table 20. Gold bump hardness

Type number	Min	Max	Unit[1]
PCA85133U/2DA/Q1	60	120	HV
PCA85133U/2DB/Q1	35	80	HV

[1] Pressure of diamond head: 10 g to 50 g.

13.2 Alignment marks



The approximate positions of the alignment marks are shown in Figure 23.

Fig 22. Alignment marks of PCA85133

Table 21. Alignment mark locations

All x/y coordinates represent the position of the REF point (see Figure 22) with respect to the center (x/y = 0) of the chip; see Figure 23.

Symbol	Size (μm)	X (μm)	Y (μm)
S1	81 × 81	−1916.1	45
C1	81 × 81	1855.8	45

13.3 Bump locations

Table 22. Bump locations

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 23.

Symbol	Bump	X (μm)	Y (μm)		Description
SDAACK	1	−1022.67	−436.5	[1]	I²C-bus acknowledge output
SDAACK	2	−968.67	−436.5		
SDAACK	3	−914.67	−436.5		
SDA	4	−712.17	−436.5	[1]	I²C-bus serial data input
SDA	5	−658.17	−436.5		
SDA	6	−604.17	−436.5		
SCL	7	−433.17	−436.5		I²C-bus serial clock input
SCL	8	−379.17	−436.5		
SCL	9	−325.17	−436.5		
CLK	10	−173.52	−436.5		clock input/output
V_{DD}	11	−61.47	−436.5		supply voltage
V_{DD}	12	−7.47	−436.5		
V_{DD}	13	46.53	−436.5		
$\overline{SYNC}$	14	149.58	−436.5		cascade synchronization input/output
OSC	15	262.08	−436.5		oscillator select
FF	16	345.78	−436.5		frame frequency select
A0	17	429.48	−436.5		subaddress input
A1	18	513.18	−436.5		
A2	19	596.88	−436.5		
SA0	20	680.58	−436.5		I²C-bus slave address input; bit 0
V_{SS}	21	765.63	−436.5		ground supply voltage
V_{SS}	22	819.63	−436.5		
V_{SS}	23	873.63	−436.5		
V_{LCD}	24	979.83	−436.5		LCD supply voltage
V_{LCD}	25	1033.83	−436.5		
V_{LCD}	26	1087.83	−436.5		
BP2	27	1176.03	−436.5		LCD backplane output
BP0	28	1230.03	−436.5		
S0	29	1284.03	−436.5		LCD segment output
S1	30	1338.03	−436.5		
S2	31	1392.03	−436.5		
S3	32	1446.03	−436.5		
S4	33	1500.03	−436.5		
S5	34	1554.03	−436.5		
S6	35	1608.03	−436.5		
S7	36	1662.03	−436.5		
S8	37	1716.03	−436.5		
S9	38	1770.03	−436.5		

Table 22. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 23.

Symbol	Bump	X (μm)	Y (μm)	Description
S10	39	1824.03	–436.5	LCD segment output
S11	40	1878.03	–436.5	
S12	41	1423.53	436.5	
S13	42	1369.53	436.5	
S14	43	1315.53	436.5	
S15	44	1261.53	436.5	
S16	45	1207.53	436.5	
S17	46	1153.53	436.5	
S18	47	1099.53	436.5	
S19	48	1045.53	436.5	
S20	49	991.53	436.5	
S21	50	937.53	436.5	
S22	51	883.53	436.5	
S23	52	829.53	436.5	
S24	53	714.06	436.5	
S25	54	660.06	436.5	
S26	55	606.06	436.5	
S27	56	552.06	436.5	
S28	57	498.06	436.5	
S29	58	444.06	436.5	
S30	59	390.06	436.5	
S31	60	336.06	436.5	
S32	61	282.06	436.5	
S33	62	228.06	436.5	
S34	63	112.59	436.5	
S35	64	58.59	436.5	
S36	65	4.59	436.5	
S37	66	–49.41	436.5	
S38	67	–103.41	436.5	
S39	68	–157.41	436.5	
S40	69	–211.41	436.5	
S41	70	–265.41	436.5	
S42	71	–319.41	436.5	
S43	72	–373.41	436.5	
S44	73	–427.41	436.5	
S45	74	–481.41	436.5	
S46	75	–596.88	436.5	
S47	76	–650.88	436.5	
S48	77	–704.88	436.5	

Table 22. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 23.

Symbol	Bump	X (μm)	Y (μm)		Description
S49	78	–758.88	436.5		LCD segment output
S50	79	–812.88	436.5		
S51	80	–866.88	436.5		
S52	81	–920.88	436.5		
S53	82	–974.88	436.5		
S54	83	–1028.88	436.5		
S55	84	–1082.88	436.5		
S56	85	–1136.88	436.5		
S57	86	–1252.35	436.5		
S58	87	–1306.35	436.5		
S59	88	–1360.35	436.5		
S60	89	–1414.35	436.5		
S61	90	–1468.35	436.5		
S62	91	–1522.35	436.5		
S63	92	–1576.35	436.5		
S64	93	–1630.35	436.5		
S65	94	–1684.35	436.5		
S66	95	–1738.35	436.5		
S67	96	–1792.35	436.5		
S68	97	–1876.05	–436.5		
S69	98	–1822.05	–436.5		
S70	99	–1768.05	–436.5		
S71	100	–1714.05	–436.5		
S72	101	–1660.05	–436.5		
S73	102	–1606.05	–436.5		
S74	103	–1552.05	–436.5		
S75	104	–1498.05	–436.5		
S76	105	–1444.05	–436.5		
S77	106	–1390.05	–436.5		
S78	107	–1336.05	–436.5		
S79	108	–1282.05	–436.5		
BP3	109	–1228.05	–436.5		LCD backplane output
BP1	110	–1174.05	–436.5		
D1	-	1932.03	–436.5	[2]	dummy pad
D2	-	1909.53	436.5		
D3	-	1801.53	436.5		
D4	-	1693.53	436.5		
D5	-	1585.53	436.5		
D6	-	1477.53	436.5		

Table 22. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 23.

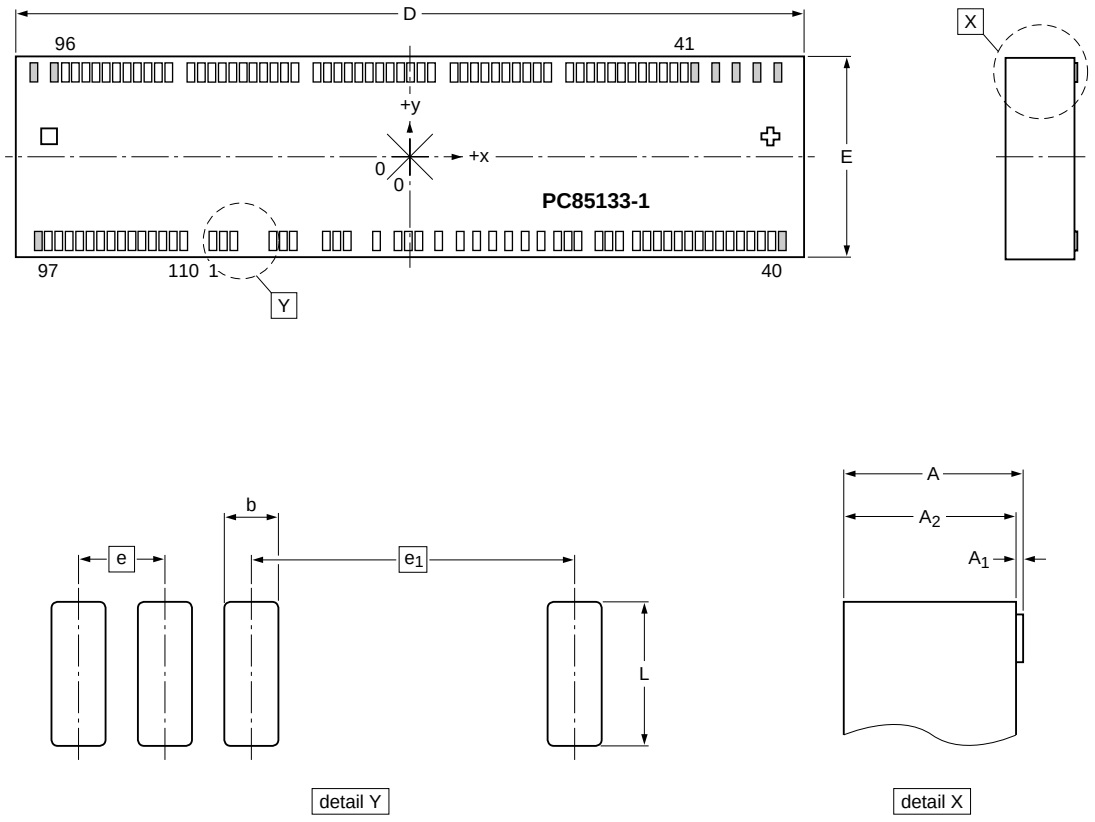
Symbol	Bump	X (μm)	Y (μm)	Description
D7	-	–1846.35	436.5	dummy pad
D8	-	–1953	436.5	
D9	-	–1930.05	–436.5	

[1] For most applications SDA and SDAACK are shorted together; see Section 7.16.

[2] The dummy pads are connected to V_{SS} but are not tested.

14. Bare die outline

Bare die; 110 bumps; 4.16 x 1.07 x 0.40 mm **PCA85133**



Dimensions

Unit		A(1)	A1(1)	A2(1)	b(1)	D	E	e(1)	e1(1)	L(1)
mm	max	0.40	0.018	0.388	0.0338	4.156	1.069	0.054	0.2026	0.090
	nom		0.015	0.385						
	min		0.012	0.382						

Note
1. Dimension not drawn to scale.

pca85133_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA85133	- - -	- - -	- - -			~~09-08-18~~ 09-09-24

Fig 23. Bare die outline of PCA85133

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

16. Packing information

16.1 Tray information for PCA85133

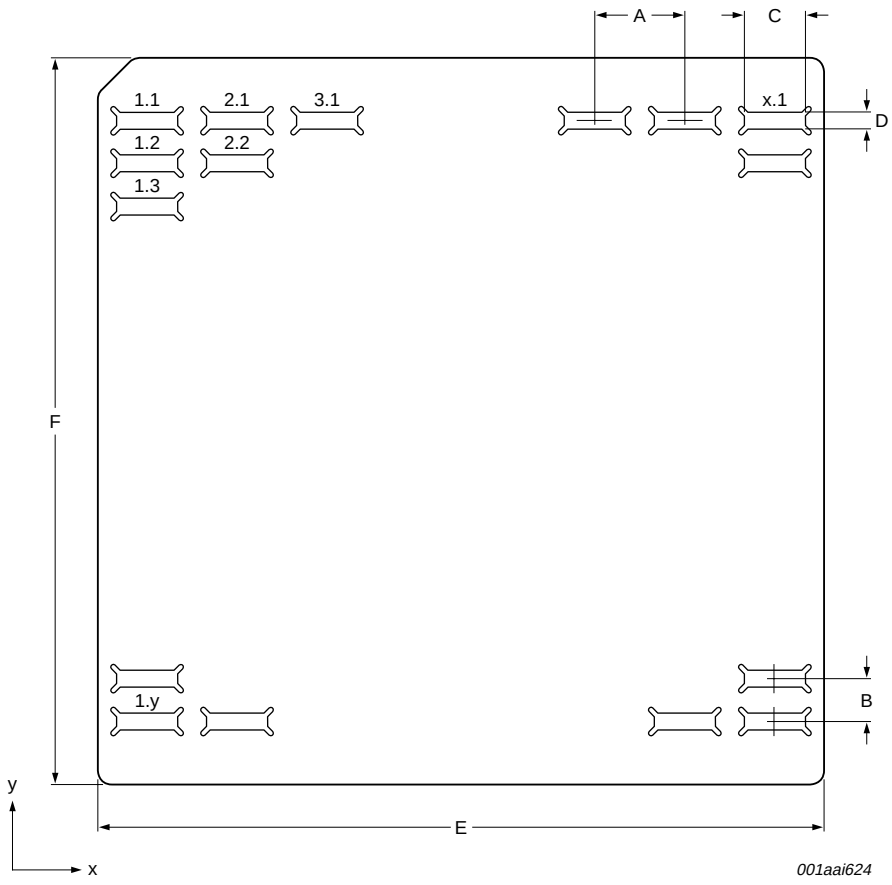


Fig 24. Tray details for PCA85133

Table 23. Tray dimensions of PCA85133 tray

See Figure 24.

Symbol	Description	Value
A	pocket pitch in x direction	6.3 mm
B	pocket pitch in y direction	3 mm
C	pocket width in x direction	4.26 mm
D	pocket width in y direction	1.17 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
N	number of pockets, x direction	7
M	number of pockets, y direction	15

The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray (see Figure 25). Refer to the bump location diagram (see Figure 23) for the orientation and position of the type name on the die surface.

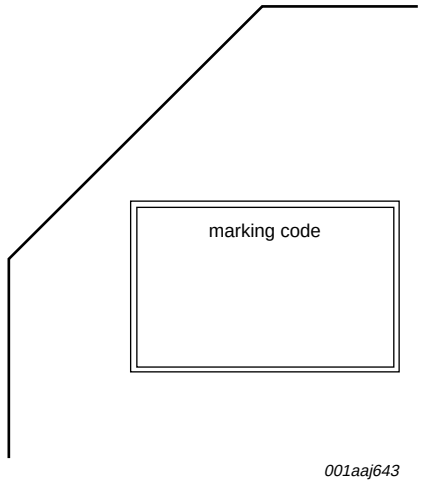


Fig 25. Tray alignment for PCA85133 tray

17. Abbreviations

Table 24. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
COG	Chip-On-Glass
DC	Direct Current
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
MM	Machine Model
RAM	Random Access Memory
RC	Resistance-Capacitance
RMS	Root Mean Square

18. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10706 —** Handling bare die

[3] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[7] **JESD78 —** IC Latch-Up Test

[8] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[9] **NX3-00092 —** NXP store and transport requirements

[10] **UM10204 —** I^2C-bus specification and user manual

19. Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA85133_1	20091023	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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22. Contents

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