PAC1720

Dual High-Side Current Sense Monitor with Power Calculation

PRODUCT FEATURES

Datasheet

General Description

The PAC1720 is a dual high-side bi-directional current sensing monitor with precision voltage measurement capabilities. Each sensor measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. The PAC1720 also measures the SENSE+ pin voltage and calculates average power over the integration period. The PAC1720 can be programmed to assert the $\overline{\text{ALERT}}$ pin when high and low limits are exceeded for Current Sense and Bus Voltage.

Available in a RoHS compliant 3 X 3mm 10-pin DFN package.

The PAC1720 device is good for measuring dynamic power. The long integration time allows for extending system polling cycles without losing any power consumption information. In addition the alert ensures that transient events are captured between the polling cycles.

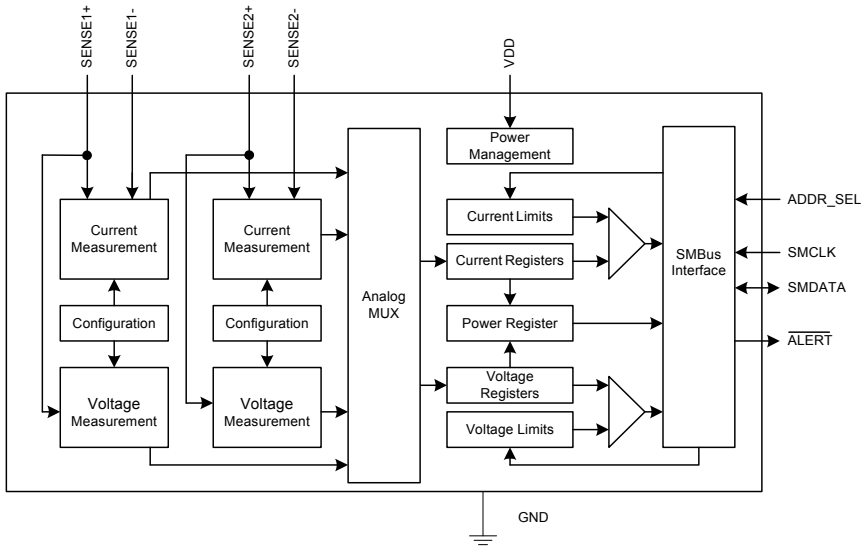
Applications

- Notebook and Desktop Computers
- Industrial
- Power Management Systems
- Embedded Applications

Features

- Dual high-side current sensor
  - Current measurement is integrated over 2.5ms to 2.6sec with up to 11-bit resolution
  - 1% current measurement accuracy in positive range
  - Measures V_{SOURCE} voltages
- Calculates proportional power
- V_{SOURCE} voltage range 0V to 40V
  - Bi-directional current sensing
- Auto-zero input offset voltage
- Digital averaging
  - Adjustable sampling time and resolution
- 5µA typical Standby current
- Programmable sense voltage range
  - ±10mV, ±20mV, ±40mV, and ±80mV
- Power supply range 3.0V to 5.5V
- Wide temperature operating range: -40°C to +85°C
- $\overline{\text{ALERT}}$ output for voltage and current out of limit transients between sampling interval
- SMBus 2.0 communications interface
  - Address selectable by resistor decode
- Sample time configurable from 2.5ms-320ms
  - With averaging effective sampling times up to 2.6sec
- 3x3 mm DFN-10 package

Block Diagram



Ordering Information:

ORDERING NUMBER	PACKAGE	FEATURES
PAC1720-1-AIA-TR	10-pin 3 X 3 DFN (Lead Free RoHS compliant)	SMBus 2.0 communications interface, ALERT pin, dual sensor

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

Table of Contents

List of Figures

List of Tables

Chapter 1 Pin Description

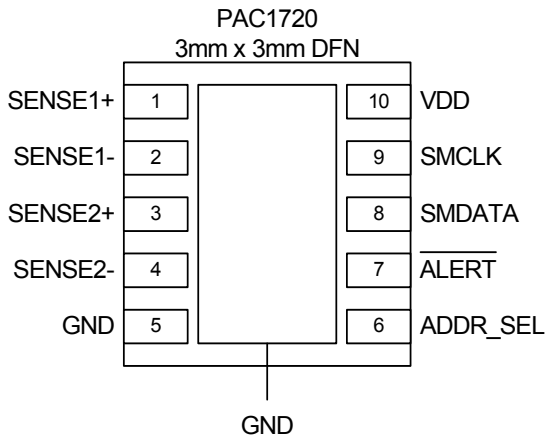


Figure 1.1 PAC1720 Pin Diagram

Table 1.1 Pin Description for PAC1720

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
1	SENSE1+	Positive current sense measurement point	AI (40V)
2	SENSE1-	Negative current sense measurement point	AI (40V)
3	SENSE2+	Positive current sense measurement point	AI (40V)
4	SENSE2-	Negative current sense measurement point	AI (40V)
5	GND	Ground	Power
6	ADDR_SEL	Selects SMBus address	AI (5V)
7	$\overline{\text{ALERT}}$	Active low output - requires pull - up resistor	OD (5V)
8	SMDATA	SMBus data input/output - requires pull-up resistor	DIOD (5V)
9	SMCLK	SMBus clock input - requires external pull-up resistor	DI (5V)
10	VDD	Positive power supply voltage	Power (5V)

The pin types are described in Table 1.2. All pins labeled with (5V) are 5V tolerant. All pins labeled with (40V) are 40V tolerant.

Table 1.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
AI	Analog Input - this pin is used as an input for analog signals.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DI	Digital Input - this pin is used for digital inputs. This pin is 5V tolerant.
DIOD	Open Drain Digital Input / Output - this pin is bi-directional. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 2 Electrical Characteristics

Table 2.1 Absolute Maximum Ratings

Supply voltage, GND to VDD	-0.3 to 6.0	V
Analog input voltage, GND to SENSE pins	-0.3 to 42.0	V
Differential input voltage, SENSE- to SENSE+	-42.0 to 42.0	V
Voltage on 5V tolerant pins with respect to GND	GND-0.3 to VDD+0.3	V
Input current to any pin except VDD or GND	±10	mA
Output short circuit (to GND or VDD)	Continuous	
Package Power Dissipation 10-pin DFN (up to T_A = 85°C)	0.5	W
Junction to Ambient (θ_{JA}) (DFN-10 package)	78	°C/W
Operating Ambient Temperature Range	-40 to 85	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating - SMCLK, SMDATA, and $\overline{\text{ALERT}}$ pins - HBM	8000	V
ESD Rating - All other pins - HBM	2000	V

Note 2.1 Stresses at or above those values listed could cause permanent damage to the device. This is a stress rating only, and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. Prolonged stresses above the stated operating levels and below the Absolute Maximum Ratings may degrade device performance and lead to permanent damage.

Note 2.2 All voltages are relative to ground.

Note 2.3 The Package Power Dissipation specification assumes a thermal via design with the thermal landing be soldered to the PCB ground plane with four 0.3048mm (12 mil) vias (where applicable).

Note 2.4 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias.

2.1 Electrical Specifications

Table 2.2 Electrical Specifications

MAX values are at T_A = -40°C to 85, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V TYP values are at T_A = 25°C, V_{DD} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ - SENSE-) = 0V CURRENT SENSE FULL SCALE RANGE = 80mV unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS / NOTES**
DC Power						
Voltage on SENSE+	V_{SOURCE}	0		40	V	
V_{DD} Range	V_{DD}	3.0		5.5	V	
VDD Pin Supply Current	I_{DD}		0.525	1.3	mA	Both measurement channels enabled. Continuous Conversions (see Table 5.4)
			13	50	µA	Both measurement channels enabled. 1 Conversion / second (see Table 5.4) VSRC_SAMP_TIME = 2.5ms CS_SAMP_TIME = 2.5ms No SMBus communications
VDD Pin Supply Current	I_{DD}		360	900	µA	One measurement channel enabled. Continuous Conversions (see Table 5.4)
			10	35	µA	One measurement channel enabled. 1 Conversion / second (see Table 5.4) VSRC_SAMP_TIME = 2.5ms CS_SAMP_TIME = 2.5ms No SMBus communications
V_{DD} Rise Rate	V_{DD_RISE}	0.03			V/ms	0 to 3V in 100ms
V_{DD} Standby Current	I_{DD_STBY}		5.5	15	µA	Standby state
SENSEX+ Pin Bias Current	I_{SENSE+}		100	150	µA	-80mV < V_{SENSE} < 80mV Active state
SENSEX- Pin Bias Current	I_{SENSE-}		0.1	1	µA	-80mV < V_{SENSE} < 80mV Active state
SENSEX+ Pin Leakage Current	I_{SENSE+_LEAK}		0.01	1	µA	V_{SENSE} = 0V Standby state
SENSEX- Pin Leakage Current	I_{SENSE-_LEAK}		0.01	1	µA	V_{SENSE} = 0V Standby state
Current Sense						
SENSE+ / SENSE- Pins Common Mode Voltage Range	V_{CM}	0		40	V	Common mode voltage on SENSE pins, referenced to ground
V_{SENSE} Differential Input Voltage Range	V_{DIFF}	-80		+80	mV	Voltage between SENSE+ and SENSE- pins

Table 2.2 Electrical Specifications (continued)

MAX values are at T_A = -40°C to 85, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V TYP values are at T_A = 25°C, V_{DD} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ - SENSE-) = 0V CURRENT SENSE FULL SCALE RANGE = 80mV unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS / NOTES**
Current Sense Power Supply Rejection Ratio	PSRR_CS		10		µV/V	3.0V < VDD < 5.5V
Full Scale Range (±) (see Section 5.9)	FSR	-10		10	mV	1 LSB = 4.885µV 11-bit data resolution
		-20		20	mV	1 LSB = 9.77µV 11-bit data resolution
		-40		40	mV	1 LSB = 19.54µV 11-bit data resolution
		-80		80	mV	1 LSB = 39.08µV 11-bit data resolution
Common Mode Rejection	V_{SENSE_CMRR}	80	100		dB	Common Mode Rejection, 0V < V_{SOURCE} < 40V
Current Sense Offset Error Voltage						
Offset Error Voltage (referred to input)	V_{os}		±15		µV	FSR = ±10mV
			±15		µV	FSR = ±20mV
			±20		µV	FSR = ±40mV
			±40		µV	FSR = ±80mV
Current Sense Total Measurement Error						
Total Error (positive range) (see Section 4.3)	$V_{SENSE\_TOT\_ERR}$		±0.5	±1	% FSR	FSR = 0 to +10mV
			±0.3	±0.6	% FSR	FSR = 0 to +20mV
			±0.2	±0.4	% FSR	FSR = 0 to +40mV
			±0.2	±0.4	% FSR	FSR = 0 to +80mV
Total Error (negative range) (see Section 4.3)	$V_{SENSE\_TOT\_ERR}$	-1	-1.3	-1.6	% FSR	FSR = -10mV to 0
		-1	-1.3	-1.6	% FSR	FSR = -20mV to 0
		-1	-1.3	-1.6	% FSR	FSR = -40mV to 0
		-1.6	-2	-2.4	% FSR	FSR = -80mV to 0
V_{SOURCE} Voltage Measurement						
Power Supply Rejection Ratio	PSRR		10		mV/V	3.0V < V_{DD} < 5.5V
V_{SOURCE} Error (±)	V_{SOURCE_ERR}		0.15	0.3	% FSV	
Power Ratio						
Total Power Ratio Measurement Error (±) (positive range)	P_{RATIO_ERR}			1	% FSR	FSR = 0 to +10mV, 0 to +20mV, 0 to +40mV, or 0 to +80mV

Table 2.2 Electrical Specifications (continued)

MAX values are at T_A = -40°C to 85, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V TYP values are at T_A = 25°C, V_{DD} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ - SENSE-) = 0V CURRENT SENSE FULL SCALE RANGE = 80mV unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS / NOTES**
Total Power Ratio Measurement Error (±) (negative range)	P_{RATIO_ERR}			2	% FSR	FSR = -10mV to 0, -20mV to 0, -40mV to 0, or -80mV to 0
First Power Ratio Ready	t_{CONV_P}			220	ms	Time after power up before P_{RATIO} updated
Digital I/O Pins (SMCLK, SMDATA, $\overline{\text{ALERT}}$)						
Pull-up Voltage Range	V_{PULLUP}	3.0		5.5	V	Pull-up voltage for SMBus and $\overline{\text{ALERT}}$ pins
Time to First Communications	t_{COMM}			25	ms	
Input High Voltage	V_{IH}	2.0			V	SMCLK, SMDATA OD pins pulled up to V_{PULLUP}
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	OD pin pulled to V_{PULLUP} 3mA current sink
Leakage Current (±)	I_{LEAK}			5	µA	powered or unpowered TA < 85°C

2.2 SMBus Electrical Specifications

Table 2.3 SMBus Electrical Specifications

MAX values are at T_A = -40°C to 85, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V TYP values are at T_A = 25°C, V_{DD} = 3.3V, V_{PULLUP} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ - SENSE-) = 0V CURRENT SENSE FULL SCALE RANGE = 80mV unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Input Capacitance	C_{IN}		4	10	pF	
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			100	ns	
Bus Free Time Stop to Start	t_{BUF}	1.3			µs	
Start Setup Time	$t_{SU:STA}$	0.6			µs	
Start Hold Time	$t_{HD:STA}$	0.6			µs	
Stop Setup Time	$t_{SU:STO}$	0.6			µs	
Data Hold Time	$t_{HD:DAT}$	0			µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3			µs	When receiving from the master

Table 2.3 SMBus Electrical Specifications (continued)

MAX values are at T_A = -40°C to 85, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V TYP values are at T_A = 25°C, V_{DD} = 3.3V, V_{PULLUP} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ - SENSE-) = 0V CURRENT SENSE FULL SCALE RANGE = 80mV unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Data Setup Time	$t_{SU:DAT}$	0.6			µs	
Clock Low Period	t_{LOW}	1.3			µs	
Clock High Period	t_{HIGH}	0.6			µs	
Clock / Data Fall Time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock / Data Rise Time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	Total per bus line

Chapter 3 Communications

3.1 System Management SMBus Interface Protocol

The PAC1720 communicates with a host controller through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the PAC1720 will not stretch the clock signal.

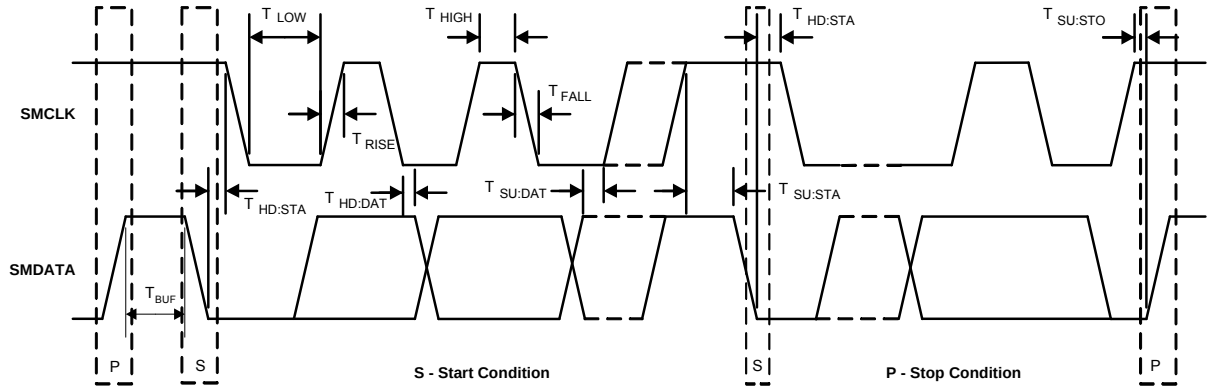


Figure 3.1 SMBus Timing Diagram

3.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

3.1.2 SMBus Address and RD / $\overline{\text{WR}}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by a 1-bit RD / $\overline{\text{WR}}$ indicator. If this RD / $\overline{\text{WR}}$ bit is a logic ‘0’, the SMBus host is writing data to the client device. If this RD / $\overline{\text{WR}}$ bit is a logic ‘1’, the SMBus host is reading data from the client device.

The PAC1720 SMBus address is determined by a single resistor connected between ground and the ADDR_SEL pin as shown in Table 3.1.

Table 3.1 ADDR_SEL Resistor Setting

RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)	1600	0101_000(r/w)
100	1001_101(r/w)	2000	0101_001(r/w)
180	1001_110(r/w)	2700	0101_010(r/w)
300	1001_111(r/w)	3600	0101_011(r/w)
430	1001_000(r/w)	5600	0101_100(r/w)
560	1001_001(r/w)	9100	0101_101(r/w)
750	1001_010(r/w)	20000	0101_110(r/w)
1270	1001_011(r/w)	Open	0011_000(r/w)

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

3.1.3 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the $\overline{\text{ALERT}}$ pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the 8th data bit has been sent.

3.1.4 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the PAC1720 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.1.5 SMBus Timeout

The PAC1720 includes an SMBus timeout feature. Following a 30ms period of inactivity on the SMBus, the device will timeout and reset the SMBus interface.

The timeout functionality defaults to disabled and can be enabled by writing to the TIMEOUT bit (see Section 5.2, "Configuration Register").

3.1.6 SMBus and I^2C Compliance

The major differences between SMBus and I^2C devices are highlighted here. For more information, refer to the SMBus 2.0 and I^2C specifications.

1. PAC1720 supports I^2C fast mode at 400kHz. This covers the SMBus max time of 100kHz.
2. Minimum frequency for SMBus communications is 10kHz.
3. The SMBus client protocol will reset if the clock is held at a logic ‘0’ for longer than 30ms. This timeout functionality is disabled by default in the PAC1720 and can be enabled by writing to the TIMEOUT bit. I^2C does not have a timeout.

4. The SMBus client protocol will reset if both the clock and data lines are held at a logic '1' for longer than 200us (idle condition). This function is disabled by default in the PAC1720 and can be enabled by setting the TIMEOUT bit. I^2C does not have an idle condition.
5. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).
6. I^2C devices support Block Read and Block Write differently. I^2C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read / write is transmitted. The PAC1720 supports I^2C formatting only.

3.2 SMBus Protocols

The PAC1720 is SMBus 2.0 compatible and supports Write Byte, Read Byte, Send Byte, and Receive Byte as valid protocols. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the protocols listed below use the convention in Table 3.2.

Table 3.2 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

3.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers, as shown in Table 3.3:

Table 3.3 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 -> 1

3.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers, as shown in Table 3.4.

Table 3.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1	YYYY_YYY	1	0	XXh	1	0 -> 1

3.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in Table 3.5.

APPLICATION NOTE: The Send Byte protocol is not functional in the Standby state.

Table 3.5 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1

3.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte).

APPLICATION NOTE: The Receive Byte protocol is not functional in the Standby state.

Table 3.6 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_YYY	1	0	XXh	1	0 -> 1

3.2.5 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address, as shown in Table 3.7.

Table 3.7 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100	1	0	YYYY_YYY	1	0 -> 1

The PAC1720 will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

3.3 I^2C Protocols

The PAC1720 supports I^2C Block Read and Block Write.

The protocols listed below use the convention in Table 3.2.

3.3.1 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers, as shown in Table 3.8.

Table 3.8 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**		**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0		XXh	0	0 -> 1

3.3.2 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers, as shown in Table 3.9.

Table 3.9 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh
ACK	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**		**REGISTER DATA**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0		XXh	1	0 -> 1

Chapter 4 General Description

The PAC1720 is a bi-directional dual high-side current sensing device with precision voltage measurement capabilities. It measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. The PAC1720 also measures the SENSE1+ and SENSE2+ pin voltages ($V_{SOURCEX}$) and calculates average power over the integration period.

The PAC1720 measures the differential voltage across an external sense resistor, digitizes it with a variable resolution (6-bit to 11-bit plus sign) Sigma-Delta ADC, and transmits via the SMBus or I^2C protocol. The current range allows for large variations in measured current with high accuracy and low voltage drop across the resistor.

The PAC1720 has programmable high and low limits for current sense and bus voltage with a maskable $\overline{\text{ALERT}}$ signal to the host when an out-of-limit measurement occurs.

A system diagram is shown in Figure 4.1.

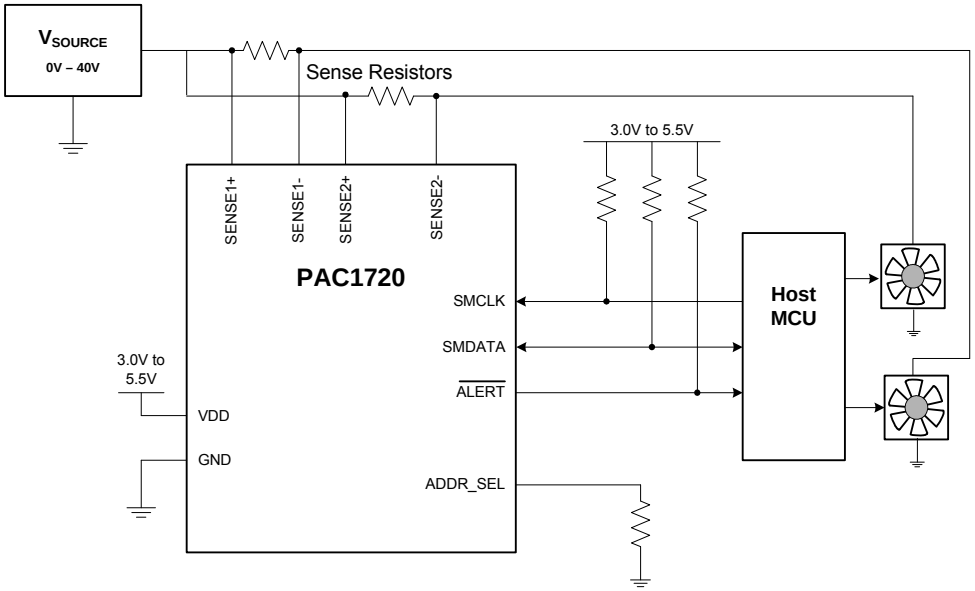


Figure 4.1 PAC1720 System Diagram

4.1 Power States

The PAC1720 has three states of operation:

- Active - The PAC1720 initiates conversion cycles for the programmed conversion rate.
- Standby - This is the lowest power state. There are no conversion cycles. The majority of circuitry is powered down to reduce supply current to a minimum. The SMBus is active and the part will return requested data. To enter the Standby state, disable all four measurements (see Section 5.2, "Configuration Register").
- One-Shot - While the device is in Standby, the host can initiate a conversion cycle on demand (see Section 5.4, "One-Shot Register"). After the conversion cycle is complete, the device will return to the Standby state.

4.2 Conversion Cycle

The conversion cycle is the period of time in which the measurements are taken and the data is updated. In the Active state, individual measurements can be disabled. In the Standby state, all measurements are updated.

During the conversion cycle, both channels begin taking measurements at the same time. The V_{SENSE} sample is taken first for its programmed sample time. Then the V_{SOURCE} sample is taken for its programmed sample time. Digital averaging may be applied to average the last 2 to 8 samples. Sample time and digital averaging have separate controls for V_{SENSE} and V_{SOURCE} as well as for each channel (see Section 5.8, "VSOURCE Sampling Configuration Register" and Section 5.9, "VSENSE Sampling Configuration Registers").

At the end of the conversion cycle, the enabled measurements are updated. The Power Ratio, High Limit Status (which includes a CONV_DONE status bit), and Low Limit Status registers are always updated. The $\overline{ALERT}$ pin will be asserted, by default, if any out-of-limit conditions exist (see Section 4.6, "ALERT Output").

4.2.1 Conversion Rate

For power management in the Active state, a conversion rate can be programmed. Conversion rate specifies how often measurement data should be updated. Updates once per second is the lowest setting (see Section 5.3, "Conversion Rate Register").

If the actual sampling time for both measurements (V_{SOURCE} and V_{SENSE}) is greater than 1 / conversion rate for either channel, the PAC1720 will override the programmed conversion rate and operate in continuous mode.

4.3 Current Measurement

The PAC1720 includes two high-side current sensing circuits. These circuits measure the voltage, V_{SENSE}, induced across fixed external current sense resistors, R_{SENSE}, and store the voltage as a signed 11-bit (by default) number in the Sense Voltage Registers.

The PAC1720 current sensing operates in one of four bipolar full scale ranges (FSR): ±10mV, ±20mV, ±40mV, or ±80mV (see Section 5.9). The default FSR is ±80mV.

Full Scale Current (FSC) can be calculated from:

$$FSC = \frac{FSR}{R_{SENSE}} \quad [1]$$

where:
FSC is the full scale current
FSR is ±10mV, ±20mV, ±40mV, or ±80mV (see Section 5.9)
R_{SENSE} is the external sense resistor value

Actual current through R_{SENSE} can then be calculated using:

$$I_{BUS} = FSC \times \frac{V_{SENSE}}{Denominator} \quad [2]$$

where:
I_{BUS} is the actual bus current
FSC is the full scale current value (from Equation [1])
V_{SENSE} is the value read from the Sense Voltage Registers (in decimal), ignoring the four lowest bits which are always zero (see Section 5.10)
Denominator is determined by the sample time, as shown in Table 5.14, "Current Sensing Sampling Time Settings"

As an example, suppose the system is drawing 1.65A through a 10mΩ resistor, the FSR is set for ±20mV, and sample time is 80ms. Using Equation [1], the FSC is 2A. The measured V_{SENSE} is 1.65A * 10mΩ = 16.5mV. This value of V_{SENSE} is represented in the Sense Voltage Registers as 69_8h (0110_1001_1000b or 1688d) ignoring the 4 lower bits of the low byte as these are always 0. This value, when applied to Equation [2], results in an I_{BUS} current of 1.649A.

For a negative voltage the Sense Voltage Registers are read as 96_0h (again ignoring the lower 4 bits of the low byte as these are always 0). To calculate current, the binary value is first converted from two's complement by inverting the bits and adding one:

96_80h = 1001_0110_1000b. Inverting equals 0110_1001_0111b (69_7h) and adding one gives 0110_1001_1000b (69_8h).

This results in the same calculated value as in the positive voltage case.

4.4 Voltage Measurement

The pin voltage is measured on the supply side of SENSE1+ and SENSE2+ and stored as an unsigned 11-bit number in the VSOURCE Voltage Registers as V_{SOURCE} (see Section 5.11).

Full Scale Voltage (FSV) is given by the maximum value of the VSENSE Voltage Registers:

$$FSV = 40 - \frac{40}{Denominator} \quad [3]$$

where:
FSV is the full scale voltage
Denominator is determined by the sample time, as shown in Table 5.10, "Voltage Source Sampling Time Settings".

Actual voltage at SENSE+ can be calculated using:

$$V_{SOURCE\_PIN} = FSV \times \frac{V_{SOURCE}}{Denominator} \quad [4]$$

where:
V_{SOURCE} is the actual voltage on the SENSEX+ pin
FSV is the full scale voltage (from Equation [3])
V_{SOURCE} is the value read from the VSOURCE Voltage Registers (in decimal), ignoring the lowest five bits which are always zero. (see Section 5.11, "VSOURCE Voltage Registers")
Denominator is determined by the sample time, as shown in Table 5.10, "Voltage Source Sampling Time Settings".

As an example using 10-bit resolution, suppose that the actual pin voltage is 24V. The VSOURCE Voltage Registers will report a value of 99_80h (1001_1001_10XX_XXXXb) in 10-bit resolution (default). When reading the data, the lower 5 bits are always ignored. Because the default operation is to measure the VSOURCE voltage with 10-bit resolution, the 6th bit is likewise ignored. Therefore, decoding the upper 10-bits results in a decimal value of 614. This value, when applied in Equation [4], results in V_{SOURCE_PIN} equal to 23.98V.

As an example using 11-bit resolution, suppose that the actual pin voltage is 10.65V. The VSOURCE Voltage Registers will report a value of 44_10h (0100_0100_001X_XXXXb). Because the lower 5-bits are ignored, the decimal result is 545d. This value, when applied in Equation [4], results in V_{SOURCE_PIN} equal to 10.64V.

The V_{SOURCE} voltage may also be determined by scaling each bit set by the indicated bit weighting as described in Section 5.11.

4.5 Power Calculation

The PAC1720 may be used to determine the average power provided at the source side of SENSE1+ and SENSE2+ using the value, P_{RATIO}, contained in the Power Ratio Registers (see Section 5.12). The value represents the percentage of maximum calculable power.

P_{RATIO} is mathematically generated by multiplying the absolute values of V_{SENSE} and V_{SOURCE} (see Section 4.3 and Section 4.4) and is stored as a 16-bit number. P_{RATIO} is updated whenever either V_{SENSE} or V_{SOURCE} is updated.

Full Scale Power can be calculated from:

$$FSP = FSC \times FSV \quad \textbf{[5]}$$

where:
FSP is the full scale power
FSC is the full scale current (from Equation [1])
FSV is the full scale voltage (from Equation [3])

Actual power drawn from the source can be calculated using:

$$P_{BUS} = FSP \times \frac{P_{RATIO}}{65,535} \quad \textbf{[6]}$$

where:
P_{BUS} is the actual power provided by the source measured at SENSE+
FSP is the full scale power (from Equation [5])
P_{RATIO} is the value read from the Power Ratio Registers (in decimal) (see Section 5.12)

As an example, suppose that the actual pin voltage is 10.65V, the current through a 10mΩ resistor is 1.65A, the FSR is set for ±20mV, and the sample times are the defaults. The FSC value is 2A per Equation [1]. The FSV value is 39.96V per Equation [3]. Using Equation [5], the FSP value is 79.92W. Applying P = V * I, the expected power is 17.57W which is 21.98% of the FSP value.

Reading the Power Ratio Registers will report P_{RATIO} as 38_47h (0011_1000_0100_0111b or 14,407d). Using Equation [6], this value results in a calculated bus power of 17.57W which is ~21.98% of the FSP value.

4.6 $\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ pin is an open drain output and requires a pull-up resistor to V_{PULLUP}.

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more SMBus Alert outputs can be hard-wired together.

The $\overline{\text{ALERT}}$ pin will be asserted (by default) if the measured V_{SOURCE} voltage or V_{SENSE} voltage are out of limit ($\geq$ high limit or < low limit). The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate status bits are cleared.

The $\overline{\text{ALERT}}$ pin can be masked for all out-of-limit measurements by setting the MASK_ALL bit (see Section 5.2, "Configuration Register") or for an individual out-of-limit measurement (see Section 5.5, "Mask Register"). Once the $\overline{\text{ALERT}}$ pin has been masked, it will be de-asserted if no unmasked out-of-limit conditions exist. Any interrupt conditions that occur while the $\overline{\text{ALERT}}$ pin is masked will update the status registers normally.

The $\overline{\text{ALERT}}$ pin can be asserted for 5us when all measurements are finished (if enabled by setting CONV_DONE_EN - see Section 5.2, "Configuration Register").

Chapter 5 Register Descriptions

The registers shown in Table 5.1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 5.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R/W	Configuration	Controls the general operation of the device	00h	Page 26
01h	R/W	Conversion Rate	Controls the conversion rate for updating measurement data in the Active state	03h	Page 27
02h	W	One-Shot	In Standby, a write to this register initiates a conversion cycle, updating all measurements	00h	Page 27
03h	R/W	Channel Mask Register	Controls the masking of out-of-limit measurements	00h	Page 28
04h	R-C	High Limit Status	Status bits for the high limits	00h	Page 29
05h	R-C	Low Limit Status	Status bits for the low limits	00h	Page 29
0Ah	R/W	VSOURCE Sampling Configuration	Controls V_{SOURCE} voltage sampling settings	88h	Page 30
0Bh	R/W	CH1 VSENSE Sampling Configuration	Controls V_{SENSE} sampling settings for channel 1	53h	Page 31
0Ch	R/W	CH2 VSENSE Sampling Configuration	Controls V_{SENSE} sampling settings for channel 2	53h	Page 31
0Dh	R	CH1 Sense Voltage High Byte	Stores the voltage measured across channel 1 R_{SENSE}	00h	Page 32
0Eh	R	CH1 Sense Voltage Low Byte		00h	Page 32
0Fh	R	CH2 Sense Voltage High Byte	Stores the voltage measured across channel 2 R_{SENSE}	00h	Page 32
10h	R	CH2 Sense Voltage Low Byte		00h	Page 32
11	R	CH1 VSOURCE Voltage High Byte	Stores voltage measured at channel 1 V_{SOURCE}	00h	Page 34
12	R	CH1 VSOURCE Voltage Low Byte		00h	Page 34
13h	R	CH2 VSOURCE Voltage High Byte	Stores voltage measured at channel 2 V_{SOURCE}	00h	Page 34
14h	R	CH2 VSOURCE Voltage Low Byte		00h	Page 34

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
15h	R	CH1 Power Ratio High Byte	Stores the power ratio value for channel 1	00h	Page 35
16h	R	CH1 Power Ratio Low Byte		00h	Page 35
17h	R	CH2 Power Ratio High Byte	Stores the power ratio value for channel 2	00h	Page 35
18h	R	CH2 Power Ratio Low Byte		00h	Page 35
19h	R/W	CH1 Sense Voltage High Limit	Stores the high limit for channel 1 V_{SENSE}	7Fh	Page 35
1Ah	R/W	CH2 Sense Voltage High Limit	Stores the high limit for channel 2 V_{SENSE}	7Fh	Page 35
1Bh	R/W	CH1 Sense Voltage Low Limit	Stores the low or negative limit for channel 1 V_{SENSE} voltage	80h	Page 35
1Ch	R/W	CH2 Sense Voltage Low Limit	Stores the low or negative limit for channel 2 V_{SENSE} voltage	80h	Page 35
1Dh	R/W	CH1 VSOURCE Voltage High Limit	Stores the high limit for the channel 1 V_{SOURCE}voltage	FFh	Page 36
1Eh	R/W	CH2 VSOURCE Voltage High Limit	Stores the high limit for the channel 2 V_{SOURCE} voltage	FFh	Page 36
1Fh	R/W	CH1 VSOURCE Voltage Low Limit	Stores the low limit for the channel 1 V_{SOURCE} voltage	00h	Page 36
20h	R/W	CH2 VSOURCE Voltage Low Limit	Stores the low limit for the channel 2 V_{SOURCE} voltage	00h	Page 36
FDh	R	Product ID	Stores a fixed value that identifies each product	57h	Page 36
FEh	R	SMSC ID	Stores a fixed value that represents SMSC	5Dh	Page 36
FFh	R	Revision	Stores a fixed value that represents the revision number	81h	Page 37

5.1 Data Read Interlock

When any measurement high byte register is read (V_{SOURCE} or V_{SENSE}), the corresponding low byte is copied into an internal ‘shadow’ register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

5.2 Configuration Register

Table 5.2 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R/W	Configuration	-	CONV_ DONE_ EN	MASK_ ALL	CH2_ IMEAS_ DIS	CH2_ VMEAS_ DIS	TIME OUT	CH1_ IMEAS_ DIS	CH1_ VMEAS_ DIS	00h

The Configuration Register controls the basic operation of the device.

Bit 6 - CONV_DONE_EN - Enables the $\overline{\text{ALERT}}$ pin to be asserted when the conversion cycle is finished.

- '0' (default) - The $\overline{\text{ALERT}}$ pin will not be asserted when the conversion cycle is finished.
- '1' - The $\overline{\text{ALERT}}$ pin will be asserted for 5us when the conversion cycle is finished.

Bit 5 - MASK_ALL - Masks the $\overline{\text{ALERT}}$ pin from asserting due to out-of-limit conditions.

- '0' (default) - The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}$ pin will be asserted.
- '1' - The $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition. The Status Registers will be updated normally.

Bit 4 - CH2_ IMEAS_DIS - Disables V_{SENSE} measurement for channel 2.

APPLICATION NOTE: CH2_IMEAS_DIS should only be changed from '1' (disabled) to '0' (enabled) when the PAC1720 is in the Standby state. To do this, disable all measurements in the Configuration Register 00h, wait for the conversion cycle to complete by monitoring the XMEAS_DIS bits until they stay set to '1', and then enable the desired measurements with one register write.

- '0' (default) - The device is measuring sense voltage for current sense channel 2.
- '1' - The device is not measuring the sense voltage for current sense channel 2. It will update CH2 Sense Voltage Registers when a One-Shot command is given.

Bit 3 - CH2_VMEAS_DIS - Disables V_{SOURCE} measurement for channel 2.

- '0' (default) - The device is measuring V_{SOURCE} voltage for current sense channel 2.
- '1' - The device is not measuring the V_{SOURCE} voltage. It will update the CH2 VSOURCE Voltage Registers when a One-Shot command is given.

Bit 2 - TIMEOUT - Determines whether the timeout / idle function is enabled.

- '0' (default) - The timeout / idle feature is disabled.
- '1' - The timeout / idle feature is enabled. If the SMCLK line is held low for more than 30ms or both the clock and data lines are held at a logic '1' for longer than 200us, the device will reset the communications protocol.

Bit 1 - CH1_IMEAS_DIS - Disables the V_{SENSE} measurement for current sense channel 1.

APPLICATION NOTE: CH1_IMEAS_DIS should only be changed from '1' (disabled) to '0' (enabled) when the PAC1720 is in the Standby state. To do this, disable all measurements in the Configuration Register 00h, wait for the conversion cycle to complete by monitoring the XMEAS_DIS bits until they stay set to '1', and then enable the desired measurements with one register write.

- '0' (default) - The device is measuring sense voltage for current sense channel 1.
- '1' - The device is not measuring the sense voltage. It will update CH1 Sense Voltage Registers when a One-Shot command is given.

Bit 0 - CH1_VMEAS_DIS - Disables V_{SOURCE} measurement for current sense channel 1.

- '0' (default) - The device is measuring V_{SOURCE} voltage for current sense channel 1.
- '1' - The device is not measuring the V_{SOURCE} voltage. It will update CH1 VSOURCE Voltage Registers when a One-Shot command is given.

5.3 Conversion Rate Register

Table 5.3 Conversion Rate Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
01h	R/W	Conversion Rate	-	-	-	-	-	-	CONV_ RATE		03h

The Conversion Rate Register controls how often V_{SENSE}, V_{SOURCE}, P_{RATIO}, and the status bits are updated in the Active state (see Section 4.2.1, "Conversion Rate").

Bits 1 - 0 - CONV_RATE - Determines the conversion rate as shown in Table 5.4.

APPLICATION NOTE: The conversion rate should only be updated when the PAC1720 is in the Standby state. To do this, disable the measurements in the Configuration Register 00h, wait for the conversion cycle to complete by monitoring the XMEAS_DIS bits in 00h until they stay set to '1', change the conversion rate, and then enable the desired measurements.

Table 5.4 Conversion Rate for Measurement

CONV_RATE[2:0]		CONVERSION RATE
1	0	
0	0	1 per sec
0	1	2 per sec
1	0	4 per sec
1	1	Continuous (default)

5.4 One-Shot Register

Table 5.5 One-Shot Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	W	One-Shot	Writing to this register initiates a single conversion cycle. Data is not stored in this register, so it always reads 00h.								00h

When the device is in the Standby state, writing to the One-Shot Register will initiate a conversion cycle and update all measurements (see Section 4.2, "Conversion Cycle").

APPLICATION NOTE: Do not write to the One-Shot Register when the PAC1720 is in the Active state (i.e., when any measurements are enabled in the Configuration Register 00h).

5.5 Mask Register

Table 5.6 Channel Mask Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h	R/W	Channel Mask	-	-	-	-	CH2_ VSENSE_ MASK	CH2_ VSRC_ MASK	CH1_ VSENSE_ MASK	CH1_ VSRC_ MASK	00h

The Channel Mask Register controls individual out-of-limit measurement masking. When a measurement is masked, the $\overline{\text{ALERT}}$ pin will not be asserted when the masked measurement is out of limit.

APPLICATION NOTE: If the MASK_ALL bit in the Configuration Register 00h is set to mask the $\overline{\text{ALERT}}$ pin, this register will have no effect.

Bit - 3 - CH2_VSENSE_MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the channel 2 V_{SENSE} value meets or exceeds the high limit or drops below the low limit.

- '0' (default) - The channel 2 V_{SENSE} voltage measurement can cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
- '1' - The channel 2 V_{SENSE} voltage measurement cannot cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

Bit - 2 - CH2_VSRC_MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the channel 2 V_{SOURCE} value meets or exceeds the high limit or drops below the low limit.

- '0' (default) - The channel 2 V_{SOURCE} voltage measurement can cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
- '1' - The channel 2 V_{SOURCE} voltage measurement cannot cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

Bit - 1 - CH1_VSENSE_MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the channel 1 V_{SENSE} value meets or exceeds the high limit or drops below the low limit.

- '0' (default) - The channel 1 V_{SENSE} voltage measurement can cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
- '1' - The channel 1 V_{SENSE} voltage measurement cannot cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

Bit - 0 - CH1_VSRC_MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the channel 1 V_{SOURCE} value meets or exceeds the high limit or drops below the low limit.

- '0' (default) - The channel 1 V_{SOURCE} voltage measurement can cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
- '1' - The channel 1 V_{SOURCE} voltage measurement cannot cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

5.6 High Limit Status Register

Table 5.7 High Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h	R-C	High Limit Status	CONV_ DONE	-	-	-	CH2_ VSENSE_ HIGH	CH2_ VSRC _ HIGH	CH1_ VSENSE_ HIGH	CH1_ VSRC_ HIGH	00h

The High Limit Status Register contains the status bits that are set when a voltage measurement high limit is met or exceeded. Once set, the status bits will remain set until read. Reading from the High Limit Status Register will clear all bits if the error condition has been removed.

Bit - 7 - CONV_DONE - Indicates that the conversion cycle (see Section 4.2, "Conversion Cycle") is complete. This bit is cleared when read.

Bit - 3 - CH2_VSENSE_HIGH - This bit is set when the channel 2 V_{SENSE} value meets or exceeds its programmed high limit.

Bit - 2 - CH2_VSRC_HIGH - This bit is set when the channel 2 V_{SOURCE} value meets or exceeds its programmed high limit.

Bit - 1 - CH1_VSENSE_HIGH - This bit is set when the channel 1 V_{SENSE} value meets or exceeds its programmed high limit.

Bit - 0 - CH1_VSRC_HIGH - This bit is set when the channel 1 V_{SOURCE} value meets or exceeds its programmed high limit.

5.7 Low Limit Status Register

Table 5.8 Low Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
05h	R-C	Low Limit Status	-	-	-	-	CH2_ VSENSE_ LOW	CH2_ VSRC_ LOW	CH1_ VSENSE_ LOW	CH1_ VSRC_ LOW	00h

The Low Limit Status Register contains the status bits that are set when a voltage measurement drops below the low limit. Once set, the status bits will remain set until read. Reading from the Low Limit Status Register will clear all bits if the error condition has been removed.

Bit 3 - CH2_VSENSE_LOW - This bit is set when the channel 2 V_{SENSE} value drops below its programmed low limit.

Bit 2 - CH2_VSRC_LOW - This bit is set when the channel 2 V_{SOURCE} value drops below its programmed low limit.

Bit 1 - CH1_VSENSE_LOW - This bit is set when the channel 1 V_{SENSE} value drops below its programmed low limit.

Bit 0 - CH1_VSRC_LOW - This bit is set when the channel 1 V_{SOURCE} value drops below its programmed low limit.

5.8 VSOURCE Sampling Configuration Register

Table 5.9 Voltage Sampling Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Ah	R/W	VSOURCE Sampling Config	CH2_ VSRC_SAMP_ TIME[1:0]		CH2_ VSRC_AVG[1:0]		CH1_ VSRC_SAMP_ TIME[1:0]		CH1_ VSRC_AVG[1:0]		88h

The Voltage Sampling Configuration Register controls sampling settings for the V_{SOURCE} measurement.

Bits 7 - 6 - CH2_VSRC_SAMP_TIME[1:0] - Determines the channel 2 V_{SOURCE} measurement sample time, as shown in Table 5.10. This will affect the resolution of the data presented in the VSOURCE Voltage Registers.

Bits 5 - 4 - CH2_VSRC_AVG[1:0] - Controls the digital averaging that is applied to the channel 2 V_{SOURCE} measurement, as shown in Table 5.11. This determines the number of consecutive samples that are averaged.

Bits 3 - 2 - CH1_VSRC_SAMP_TIME[1:0] - Determines the channel 1 V_{SOURCE} measurement sample time, as shown in Table 5.10. This will affect the resolution of the data presented in the VSOURCE Voltage Registers.

Bits 1 - 0 - CH1_VSRC_AVG[1:0] - Controls the digital averaging that is applied to the channel 1 V_{SOURCE} measurement, as shown in Table 5.11. This determines the number of consecutive samples that are averaged.

Table 5.10 Voltage Source Sampling Time Settings

VSRC_SAMP_TIME		VSOURCE SAMPLE TIME	Equation [3] DENOMINATOR (SEE Note 5.1)	Equation [4] DENOMINATOR (SEE Note 5.1)
0	0	2.5ms (data = 8 bits)	256	255
0	1	5ms (data = 9 bits)	512	511
1	0	10ms (data = 10 bits) (Default)	1024	1023
1	1	20ms (data = 11 bits)	2048	2047

Note 5.1 The Equation [3] denominator is equal to the Equation [4] denominator + 1.

Table 5.11 Voltage Source Averaging Settings

VSRC_AVG		SAMPLES TO AVERAGE
0	0	Disabled (default)
0	1	2
1	0	4
1	1	8

5.9 VSENSE Sampling Configuration Registers

Table 5.12 VSENSE Sampling Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Bh	R/W	CH1 VSENSE Sampling Config	-	CH1_ CS_SAMP_TIME[2:0]			CH1_ CS_SAMP_ AVG[1:0]		CH1_ CS_RNG		53h
0Ch	R/W	CH2 VSENSE Sampling Config	-	CH2_ CS_SAMP_TIME[2:0]			CH2_ CS_SAMP_ AVG[1:0]		CH2_ CS_RNG		53h

The VSENSE Sampling Configuration Registers control sampling settings for the V_{SENSE} measurement.

5.9.1 CH1 VSENSE Sampling Configuration - 0Bh

Bits 6 - 4 - CH1_CS_SAMP_TIME[2:0] - Determine the channel 1 V_{SENSE} measurement sample time, as shown in Table 5.14. This will affect the resolution of the data in the CH1 Sense Voltage Registers.

Bits 3 - 2 - CH1_CS_SAMP_AVG[1:0] - Controls the digital averaging that is applied to the channel 1 V_{SENSE} measurement, as shown in Table 5.13. This determines the number of consecutive samples that are averaged.

Bits 1 - 0 - CH1_CS_RNG - Determines the Current Sense full scale range as shown in Table 5.15.

5.9.2 CH2 VSENSE Sampling Configuration - 0Ch

Bits 6 - 4 - CH2_CS_SAMP_TIME[2:0] - Determines the channel 2 V_{SENSE} voltage measurement sample time, as shown in Table 5.14. This will affect the resolution of the data in the CH2 Sense Voltage Registers.

Bits 3 - 2 - CH2_CS_SAMP_AVG[1:0] - Controls the digital averaging that is applied to the channel 2 V_{SENSE} measurement, as shown in Table 5.13. This determines the number of consecutive samples that are averaged.

Bits 1 - 0 - CH2_CS_RN - Determines the current sense FSR, as shown in Table 5.15.

Table 5.13 Current Sensing Averaging Settings

CS_SAMP_AVG[1:0]		SAMPLES TO AVERAGE
0	0	Disabled (default)
0	1	2
1	0	4
1	1	8

Table 5.14 Current Sensing Sampling Time Settings

CS_SAMP_TIME[2:0]			CURRENT SENSOR SAMPLE TIME	Equation [2] DENOMINATOR
0	0	0	2.5ms (Data = sign + 6 bits)	63
0	0	1	5ms (Data = sign + 7 bits)	127
0	1	0	10ms (Data = sign + 8 bits)	255
0	1	1	20ms (Data = sign + 9 bits)	511
1	0	0	40ms (Data = sign + 10 bits)	1023
1	0	1	80ms (Data = sign + 11 bits) (default)	2047
1	1	0	160ms (Data = sign + 11 bits) (see Note 5.2)	2047
1	1	1	320ms (Data = sign + 11 bits) (see Note 5.3)	2047

Note 5.2 160ms sampling time has built-in 2X analog oversampling using ADC at 12-bit resolution.

Note 5.3 320ms sampling time has built-in 4X analog oversampling using ADC at 13-bit resolution.

Table 5.15 Current Sensing Range Settings

CS_RNG[1:0]		FULL SCALE RANGE
0	0	-10mV to 10mV
0	1	-20mV to 20mV
1	0	-40mV to 40mV
1	1	-80mV to 80mV (default)

5.10 Sense Voltage Registers

Table 5.16 Sense Voltage Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Dh	R	CH1 Sense Voltage High Byte	Sign	1024	512	256	128	64	32	16	00h
0Eh	R	CH1 Sense Voltage Low Byte	8	4	2	1					00h
0Fh	R	CH2 Sense Voltage High Byte	Sign	1024	512	256	128	64	32	16	00h
10h	R	CH2 Sense Voltage Low Byte	8	4	2	1					00h

The Sense Voltage Registers store the measured V_{SENSE} value (see Section 4.3, "Current Measurement"). Note that the bit weighting values are for representation of the voltage relative to full scale. There is no internal scaling of data and all normal binary bit weightings still apply.

The Sense Voltage Registers data format is standard 2's complement format with the positive full scale value (7F_Fh) and negative full scale value (80_0h) equal to the programmed FSR (see Section 5.9).

The Sign bit indicates the direction of current flow. If the Sign bit is '0', current is flowing through R_{SENSE} from the SENSE+ pin to the SENSE- pin. If the Sign bit is '1', the current is flowing through R_{SENSE} from the SENSE- pin to the SENSE+ pin.

Data resolution is dependent upon sampling time as shown in Table 5.18. The data format (assuming 11-bit resolution) is shown in Table 5.17**.** This data will scale directly with the sampling time.

Table 5.17 V_{SENSE} Data Format

V_{SENSE}	BINARY	HEX (AS READ BY REGISTERS)
- Full Scale	1000_0000_0000	80_0h
-2 LSB	1111_1111_1110	FF_Eh
-1 LSB	1111_1111_1111	FF_Fh
0	0000_0000_0000	00_0h
+1 LSB	0000_0000_0001	00_1h
+2 LSB	0000_0000_0010	00_2h
+Full Scale - 1 LSB	0111_1111_1111	7F_Fh

Table 5.18 V_{SENSE} Data Resolution

SAMPLING TIME	RESOLUTION (±)			
	±10mV	±20mV	±40mV	±80mV
2.5ms	156.3µV	312.5µV	625.0µV	1.250mV
5ms	78.13µV	156.3µV	312.5µV	625.0µV
10ms	39.06µV	78.13µV	156.3µV	312.5µV
20ms	19.53µV	39.06µV	78.13µV	156.3µV
40ms	9.76µV	19.53µV	39.06µV	78.13µV
≥ 80ms	4.88µV	9.76µV	19.53µV	39.06µV

5.11 VSOURCE Voltage Registers

Table 5.19 VSOURCE Voltage Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
11h	R	CH1 VSOURCE Voltage High Byte	20	10	5	2.5	1.25	0.625	0.3125	0.1563	00h
12h	R	CH1 VSOURCE Voltage Low Byte	0.0781	0.0390	0.0195	-	-	-	-	-	00h
13h	R	CH2 VSOURCE Voltage High Byte	20	10	5	2.5	1.25	0.6250	0.3125	0.1563	00h
14h	R	CH2 VSOURCE Voltage Low Byte	0.0781	0.0390	0.0195						00h

The VSOURCE Voltage Registers store the measured V_{SOURCE} value (see Section 4.4, "Voltage Measurement").

The measured voltage is determined by summing the bit weights of each bit set. For example, if V_{SOURCE} was 7.4V, the VSOURCE Voltage Registers would read 0010_1111 for the high byte and 0100_0000b for the low byte corresponding to 5V + 1.25V + 0.625V + 0.3125V + 0.1563V + 0.0390V = 7.3828V.

The bit weightings are assigned for human interpretation. They should be disregarded when translating the information via a computing system as shown in Section 4.4, "Voltage Measurement".

The VSOURCE Voltage Registers cannot support negative values, so all values less than 0V will be recorded as 0V.

5.12 Power Ratio Registers

Table 5.20 Power Ratio Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
15h	R	CH1 Power Ratio High Byte	32768	16384	8192	4096	2048	1024	512	256	00h
16h	R	CH1 Power Ratio Low Byte	128	64	32	16	8	4	2	1	00h
17h	R	CH2 Power Ratio High Byte	32768	16384	8192	4096	2048	1024	512	256	00h
18h	R	CH2 Power Ratio Low Byte	128	64	32	16	8	4	2	1	00h

The Power Ratio Registers store a power factor value, P_{RATIO}, that is used to determine the final average power delivered to the system (see Section 4.5, "Power Calculation"). P_{RATIO} is the result of the multiplication of the V_{SENSE} reading and the V_{SOURCE} reading values shifted to a 16-bit number. It represents the ratio of delivered power with respect to maximum power.

5.13 V_{SENSE} Limit Registers

Table 5.21 V_{SENSE} Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
19h	R/W	CH1 Sense Voltage High Limit	Sign	1024	512	256	128	64	32	16	7Fh
1Ah	R/W	CH2 Sense Voltage High Limit	Sign	1024	512	256	128	64	32	16	7Fh
1Bh	R/W	CH1 Sense Voltage Low Limit	Sign	1024	512	256	128	64	32	16	80h
1Ch	R/W	CH2 Sense Voltage Low Limit	Sign	1024	512	256	128	64	32	16	80h

The V_{SENSE} Limit Registers store a high and low limit for V_{SENSE}. V_{SENSE} is compared against both limits after each conversion cycle.

The data format for the limit is a raw binary form that is relative to the maximum V_{SENSE} that has been programmed.

If the measured sense voltage meets or exceeds the high limit or drops below the low limit, the $\overline{\text{ALERT}}$ pin is asserted (by default - see Section 4.6, "ALERT Output") and the VSENSE_HIGH or VSENSE_LOW status bits are set in the High Limit Status or Low Limit Status registers (see Section 5.6 and Section 5.7).

APPLICATION NOTE: V_{SENSE} is always checked to meet or exceed the high limit or to be less than the low limit, including when V_{SENSE} is negative.

5.14 VSOURCE Voltage Limit Registers

Table 5.22 VSOURCE Voltage Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Dh	R/W	CH1 VSOURCE High Limit	20	10	5	2.5	1.25	0.625	0.3125	0.1563	FFh
1Eh	R/W	CH2 VSOURCE Voltage High Limit	20	10	5	2.5	1.25	0.625	0.3125	0.1563	FFh
1Fh	R/W	CH1 VSOURCE Voltage Low Limit	20	10	5	2.5	1.25	0.625	0.3125	0.1563	00h
20h	R/W	CH2 VSOURCE Voltage Low Limit	20	10	5	2.5	1.25	0.625	0.3125	0.1563	00h

The VSOURCE Voltage Limit Registers store the high and low limits for V_{SOURCE}. V_{SOURCE} is compared against both limits after each conversion cycle.

If V_{SOURCE} meets or exceeds the corresponding high limit or drops below the low limit, the $\overline{ALERT}$ pin is asserted (by default - see Section 4.6, "ALERT Output") and the VSRC_HIGH or VSRC_LOW status bits are set in the High Limit Status or Low Limit Status registers (see Section 5.6 and Section 5.7).

5.15 Product ID Register

Table 5.23 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID	0	1	0	1	0	1	1	1	57h

The Product ID Register holds a unique value that identifies the device.

5.16 SMSC ID Register

Table 5.24 Manufacturer ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	SMSC ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID Register contains an 8-bit word that identifies SMSC as the manufacturer of the PAC1720.

5.17 Revision Register

Table 5.25 Revision Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	1	0	0	0	0	0	0	1	81h

The Revision Register contains an 8-bit word that identifies the die revision.

Chapter 6 Package Description

6.1 PAC1720 Package Drawing (10-Pin DFN)

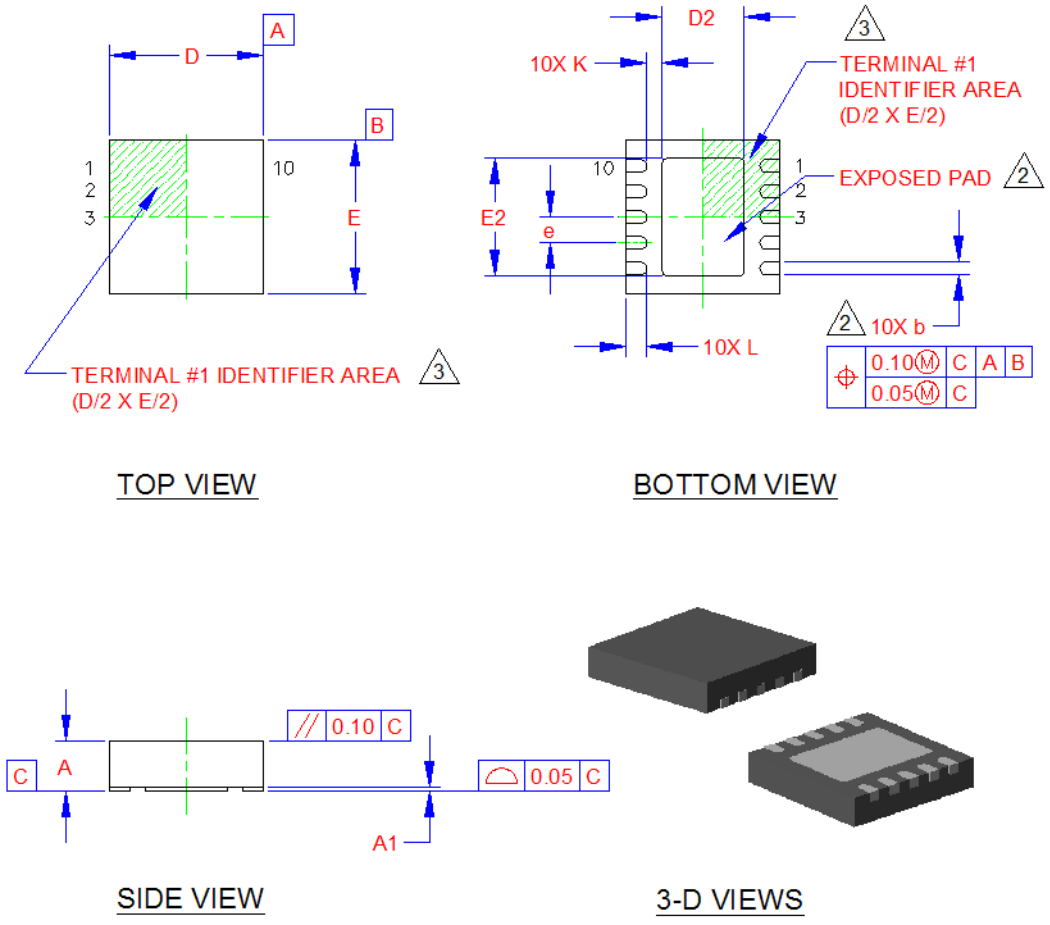
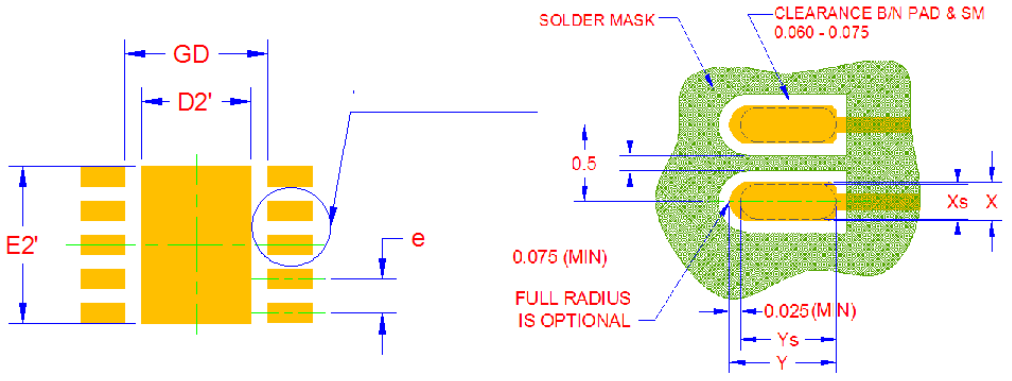


Figure 6.1 10-Pin DFN Package Drawings

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
D/E	2.90	3.00	3.10	-	X/Y BODY SIZE
D2	1.50	1.60	1.70	2	X EXPOSED PAD SIZE
E2	2.20	2.30	2.40	2	Y EXPOSED PAD SIZE
L	0.35	0.40	0.45	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.25	0.30	-	-	TERMINAL TO PAD DISTANCE
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD, AS WELL AS THE TERMINALS. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 6.2 10-Pin DFN Package Dimensions



PCB LAND PATTERN

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD	2.10	-	2.20
D2'	-	1.60	1.60
E2'	-	2.30	-
Pad: X	-	0.28	0.28
Pad: Y	-	0.69	0.69
e		0.50	

Figure 6.3 10-Pin DFN Recommended PCB Land Pattern

6.2 PAC1720 Package Markings

The PAC1720 is marked as shown in Figure 6.4.

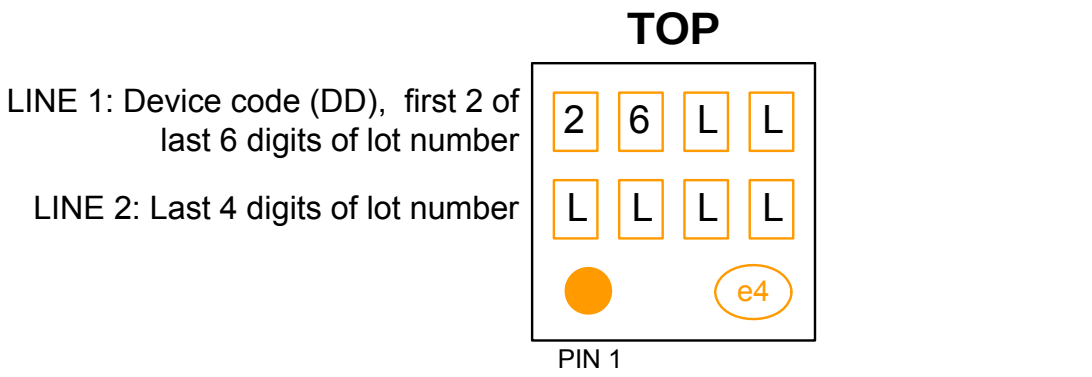


Figure 6.4 PAC1720 Package Marking

Chapter 7 Application Usage

7.1 Electrical Overstress

A common question during system board level design is about the capability of an integrated circuit (IC) to withstand electrical overstress. This question tends to focus on the device inputs, but may involve the supply voltage pins and even the output pins. Each of these different pin functions has electrical stress limits mainly determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific internal IC circuit connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events before and during product assembly, as well as during normal operation.

For the previously described reasons, it is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 7.1 illustrates the ESD circuits contained in the PAC1720 series (indicated by the shaded box). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins to absorption devices internal to the IC. This protection circuitry is intended to remain inactive during normal circuit operation.

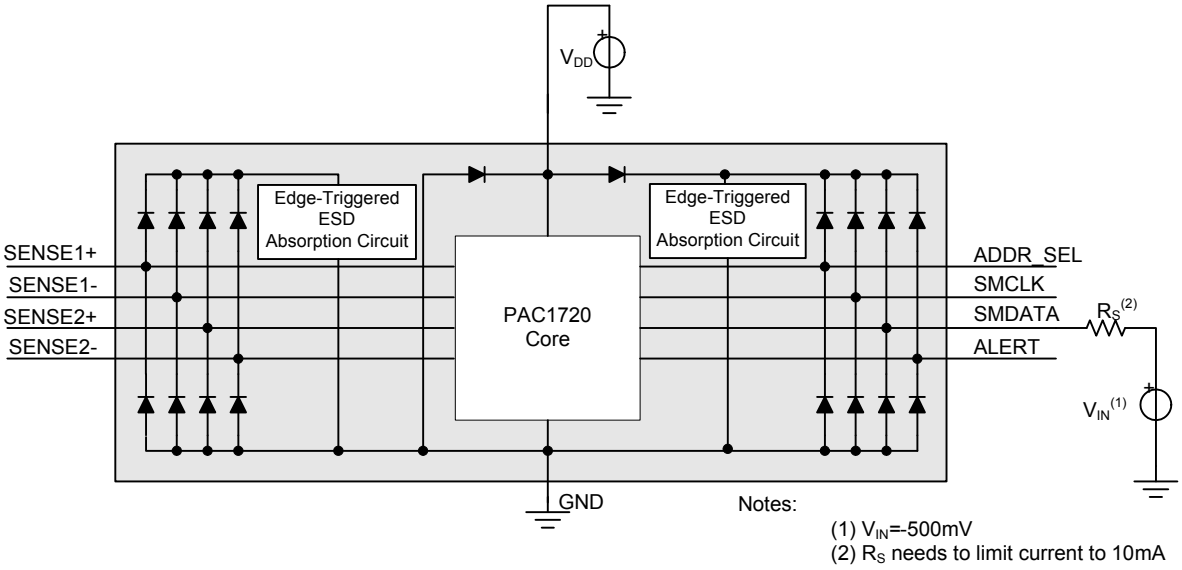


Figure 7.1 Equivalent Internal ESD Circuitry

An ESD event produces a short duration, high-voltage, high-current pulse which discharges through the semiconductor device. The ESD protection circuits are designed to provide a current path around the internal IC core while limiting the voltage to prevent the IC from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the IC device pins, current flows through one or more of the steering diodes. Depending on the path the current takes, the absorption device may activate. Fast changing voltage on the pin generally acts as a trigger, and the absorption device will quickly clamp the voltage across the supply rails to a safe level.

When the PAC1720 connects into a circuit such as the one Figure 7.1 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage

range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on and conduct current.

Figure 7.1 depicts a specific example where the input voltage, V_{IN}, is below ground by more than 500mV. The bottom steering diode will conduct and direct current to GND. Excessively high current levels can flow with increasingly lower V_{IN}. The current limiting resistor R_S is recommended, by datasheet specification, to keep the input current lower or equal to 10mA.

7.2 PAC1720 Internal Filtering

The application circuit shown in Figure 4.1, "PAC1720 System Diagram" does not need any additional filters on the SENSE+ and SENSE- input pins. The PAC1720 has internal circuitry to handle noise, so external filters are not necessary, and in fact, will introduce errors. This section describes noise and the PAC1720's methods for handling noise internally.

Due to high efficiency, low weight, and low volume, switch mode power supplies (SMPS) are used in most equipment today. Accurate measurement of current and voltage can be challenging due to the inherent noise of the SMPS. This noise is well known and defined. Sometimes external noise can be present which is much more difficult to predict.

The PAC1720 offers several options for dealing with the noise. The signal will first pass through the ESD structure which will protect the internal circuit from possible electrical overstress. Next it passes a built-in analog filter before the internal, high-performance analog-to-digital converter (ADC). This ADC is based on the delta-sigma ($\Delta\Sigma$) structure. This type of converter has very good inherent noise rejection due to oversampling and digital filtering of the sampled signal. Transients that occur at or very close to the sampling rate harmonics will be rejected due to the internal analog filter. In addition, advanced rolling averaging (8x) of the signal with variable sampling time (82ms to 2.6s) will remove any remaining noise.

Overload conditions of the SMPS can be another consideration for the system-level designer. One scenario might be a short to ground on the load side of the shunt. This type of event can result in increased voltage across the shunt resistor (as long as the power supply or energy storage capacitors support it). It is very unlikely that the short circuit current will be 100 times higher than the maximum nominal current. Also, in this case, the PAC1720 maximum differential voltage of 42V will prevent damage to the part. It must be remembered that removing a short to ground can result in inductive kickbacks that could exceed the absolute maximum voltage of all components connected to this line. Inductive kickback voltages are best dealt with by zener-type transient-absorbing devices (commonly called transzorbs) combined with sufficient energy storage capacitance.

In the case of the equipment malfunctioning and a hard physical short, this is most likely to cause excessive dV/dt present on the inputs of the PAC1720. Some applications that do not have large energy storage electrolytic capacitors on one or both sides of the shunt can be subject to this overstress. The PAC1720 ESD structure is designed to activate on the fast rising edge (an ESD event has a rising edge of less than 10ns). In the normal application, some capacitance is always present. To trigger the internal ESD structure of the PAC1720 when 1µF capacitor is present, a step current of approximately 1.2kA needs to be applied, as shown in Equation [7].

$$i = C \times \frac{\partial v}{\partial t} = 1\mu F \times \frac{12V}{10ns} = 1200A \qquad [7]$$

7.3 Do Not Apply a Filter Across the Current Shunt

Adding filter on the SENSE+ and SENSE- input pins will induce offset and cause accuracy error. This section explains the error that is introduced when unnecessary filters are added. As described in the section above, the PAC1720 has the internal circuitry to provide filtering without the need for external filters.

Figure 7.2 shows an example of unnecessary filter resistors R_{FILT} on the input pins.

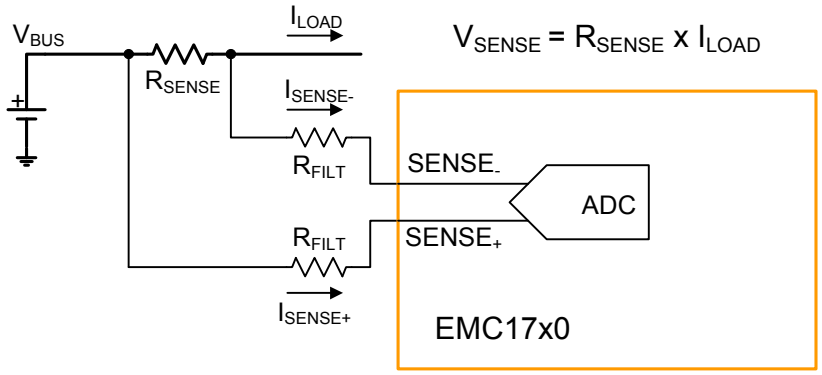


Figure 7.2 PAC1720 with Unnecessary Filters on the Input Pins

In the normal operation without the added filters, the voltage to measure is shown in Equation [8].

$$SENSE_+ - SENSE_- = V_{SENSE} = R_{SENSE} \times I_{LOAD} \quad \textbf{[8]}$$

To properly account for the offset error, TBDµV is added to this measurement, as shown in Equation [9].

$$V_{SENSE\_OFF\_MAX} = TBD\ LSB@80\text{mV} = TBD \times 39.08\mu V = TBD\mu V \quad \textbf{[9]}$$

The input bias current of the input circuit in combination with added filter resistor R_{FILT} (in this example 10Ω) will interfere with the measurement and add error, as shown in Equation [10] and Equation [11].

$$V_{R+} = R_{FILT} \times I_{SENSE+} = 10\Omega \times 150\mu A = 1500\mu V \quad \textbf{[10]}$$

$$V_{R-} = R_{FILT} \times I_{SENSE-} = 10\Omega \times 5\mu A = 50\mu V \quad \textbf{[11]}$$

Assuming the input bias current on both pins has the same direction, total added error is shown in Equation [12] and Equation [13].

$$V_{ERROR} = V_{R+} - V_{R-} = 1500\mu V - 50\mu V = 1450\mu V \quad \textbf{[12]}$$

$$V_{ERROR} = \frac{1450\mu V}{39.08\mu V} = 37 LSB@80\text{mV} \quad \textbf{[13]}$$

Adding resistors on the SENSE+ and SENSE- input pins will induce error which is several times greater than the inherent maximum offset error. For that reason, we do not recommend putting any additional filter on these input pins.

7.4 Initial Device Configuration

After power-up, configure the PAC1720 as follows:

1. Disable all channels by setting Configuration Register 00h to 1Bh (see Section 5.2, "Configuration Register").
2. Wait up to 220ms; read back Configuration Register 00h to ensure it's set to 1Bh.
3. Set conversion rate in Conversion Rate Register 01h (see Section 5.3, "Conversion Rate Register").
4. Enable desired channel enables in Configuration Register 00h.

Chapter 8 Typical Operating Curves

Figure 8.1 IDD Vs VDD

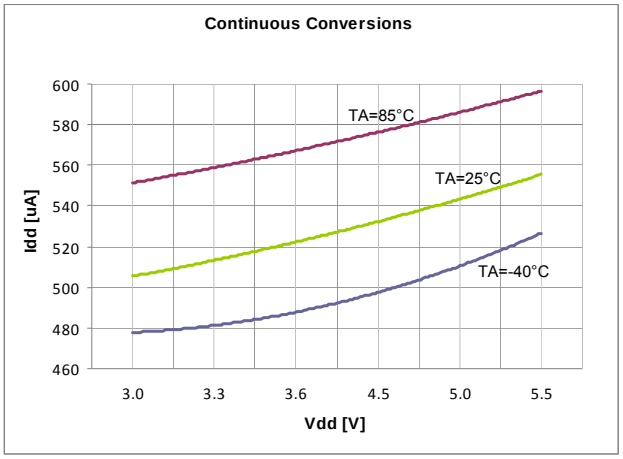


Figure 8.2 IDD Vs VDD

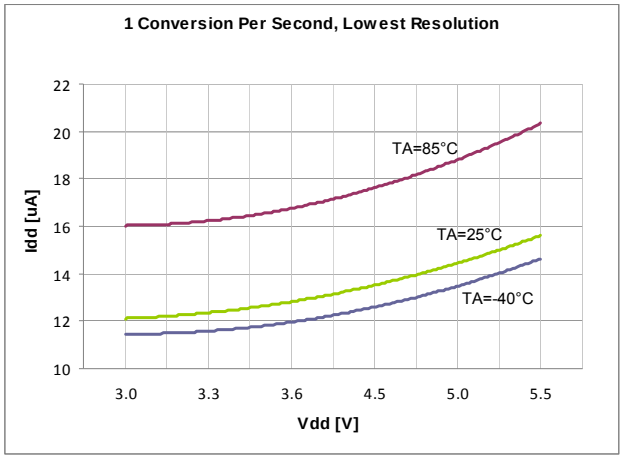


Figure 8.3 IDD Vs VDD

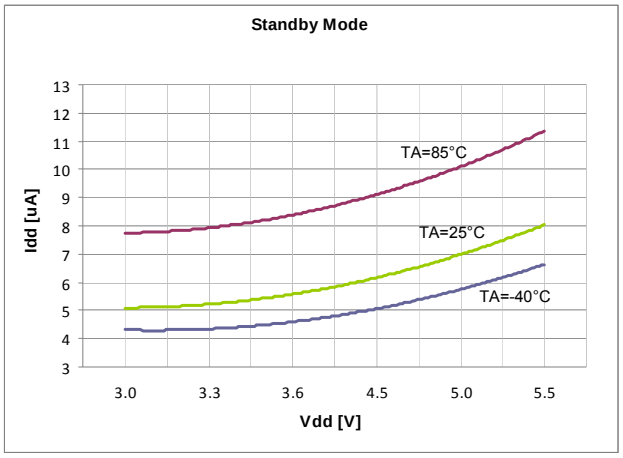


Figure 8.4 ISENSE+ Pin Current Vs VBUS

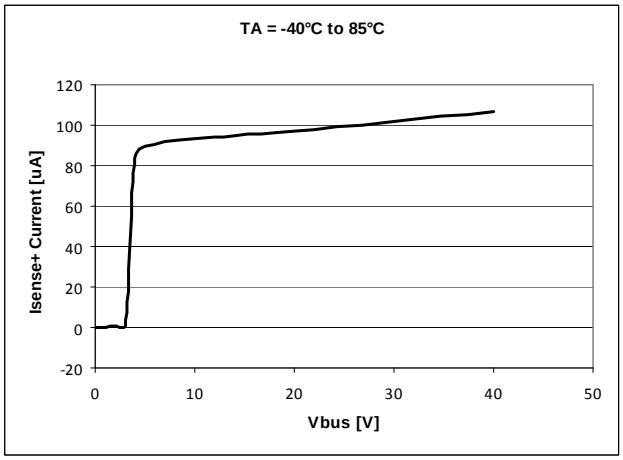


Figure 8.5 ISENSE+ Pin Bias Current

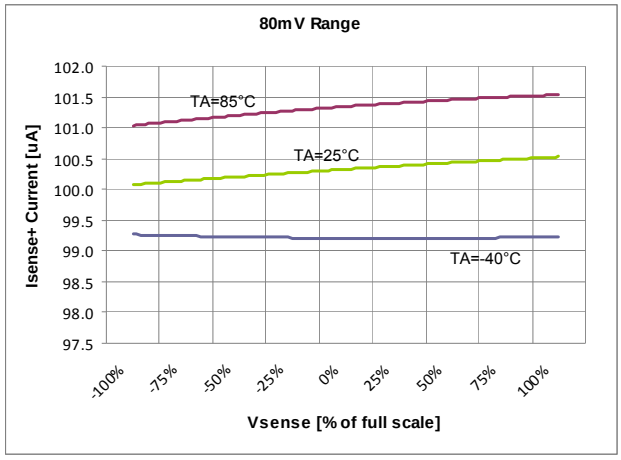


Figure 8.6 ISENSE- Pin Bias Current

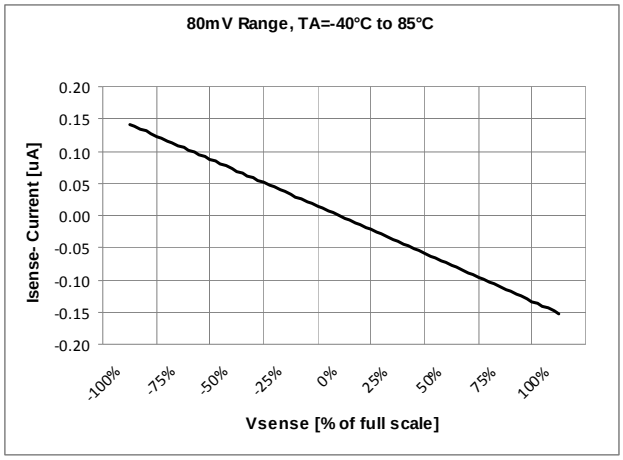


Figure 8.7 ISENSE+ Pin Leakage Current

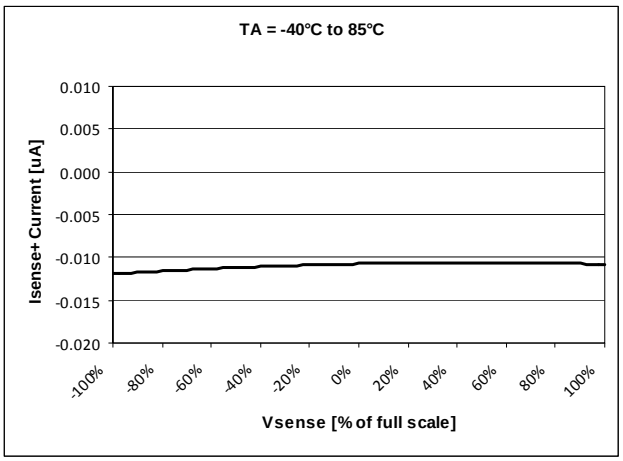


Figure 8.8 ISENSE- Pin Leakage Current

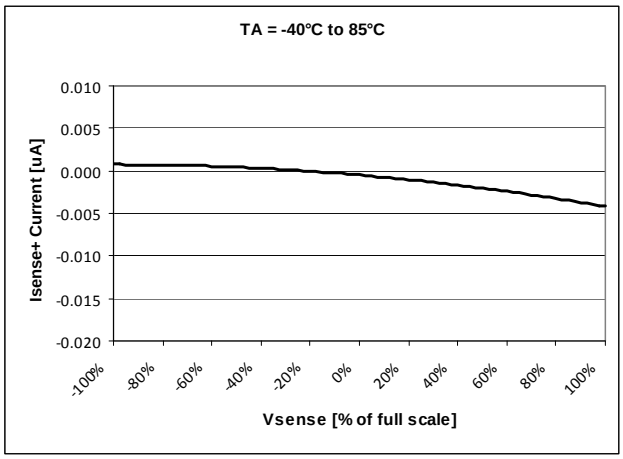
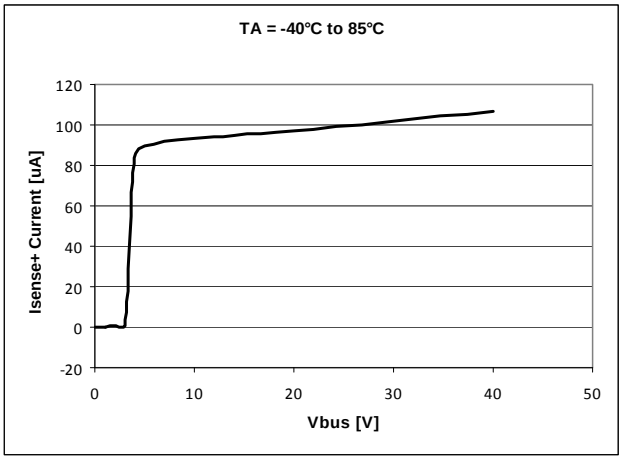


Figure 8.9 ISENSE+ Pin Current Vs VBUS



Chapter 9 Datasheet Revision History

Table 9.1 PAC1720 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (12-08-11)	General Description	Added: “The PAC1720 device is good for measuring dynamic power. The long integration time allows for extending system polling cycles without losing any power consumption information. In addition the alert ensures that transient events are captured between the polling cycles.”
	Table 2.2, "Electrical Specifications"	Changed I_{DD_STBY} from 5µA typ to 5.5µA. I_{SENSE+_LEAK} and I_{SENSE-_LEAK} changed from 0.1 µA typ to 0.01. Added Total Power Ratio Measurement Error (±) (negative range) of 2% FSR max and clarified that 1% FSR max is for positive range.
	Table 2.3, "SMBus Electrical Specifications"	Two rows added for $t_{HD:DAT}$. Also added: Bus Free Time Stop to Start, Start Setup Time, Start Hold Time, Stop Setup Time, Data Setup Time, Clock Low Period, Clock High Period.
	Section 3.1.6, "SMBus and I2C Compliance"	Added: PAC1720 supports I^2C fast mode at 400kHz. This covers the SMBus max time of 100kHz. Added: I^2C devices support Block Read and Block Write differently. I^2C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read / write is transmitted. The PAC1720 supports I^2C formatting only.
	Section 3.3, "I2C Protocols"	Added. Moved descriptions of Block Write and Block Read to this section.
	Chapter 8, Typical Operating Curves	Added.
Rev. 1.0 (10-18-11)	Formal release	