P89V52X2

8-bit 80C51 low power 8 kB flash microcontroller with 256 B RAM, 192 B data EEPROM

Rev. 03 — 4 May 2009 Product data sheet

1. General description

The P89V52X2 is an 80C51 microcontroller with 8 kB flash, 256 B of data RAM, and 192 B of data EEPROM. This device is designed to be a drop in and software compatible replacement for the P87C52, P87C52X2, P89C52, and P89C52X2 devices.

2. Features

2.1 Principal features

- 0 MHz to 40 MHz operating frequency in 12× mode, 20 MHz in 6× mode
- 8 kB of on-chip flash user code memory
- 256 B of RAM
- Enhanced UART
- Three 16-bit timers/counters
- Four 8-bit I/O ports
- Supports 12-clock (default) or 6-clock mode selection via software or In-Circuit Programming (ICP)
- DIP40, PLCC44, and LQFP44 packages
- Six interrupt sources with four priority levels
- Second DPTR register

2.2 Additional features

- Very low power
- Low EMI mode (ALE inhibit)
- Power-down mode with external interrupt wake-up
- Idle mode
- Extended temperature range
- Three security bits
- Programmable clock-out pin

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3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
P89V52X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P89V52X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89V52X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

4. Block diagram

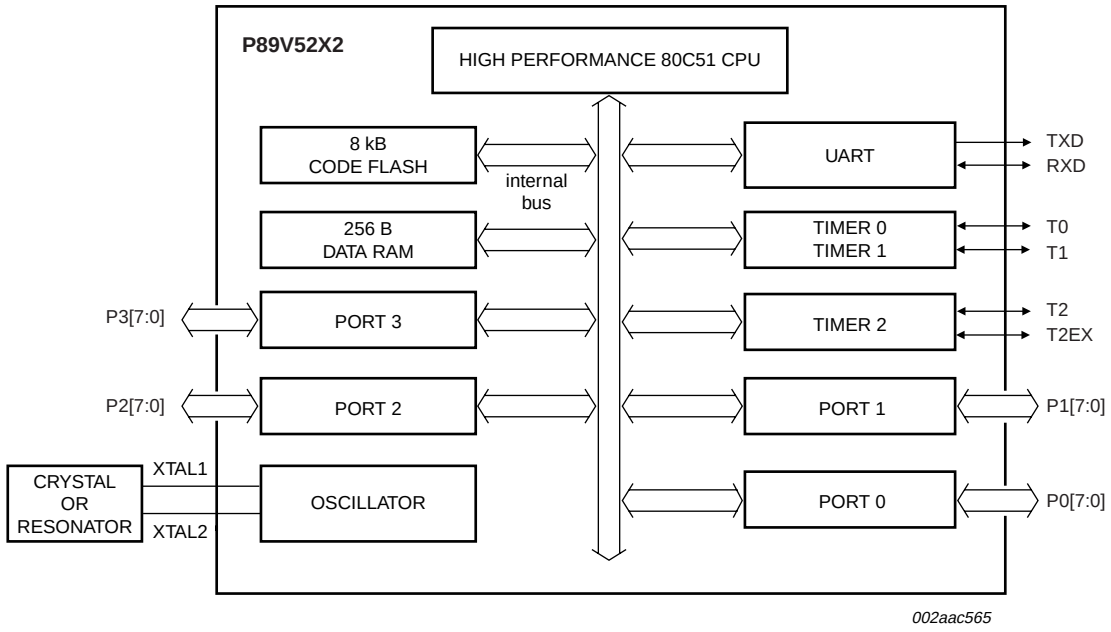

Fig 1. Block diagram

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5. Pinning information

5.1 Pinning

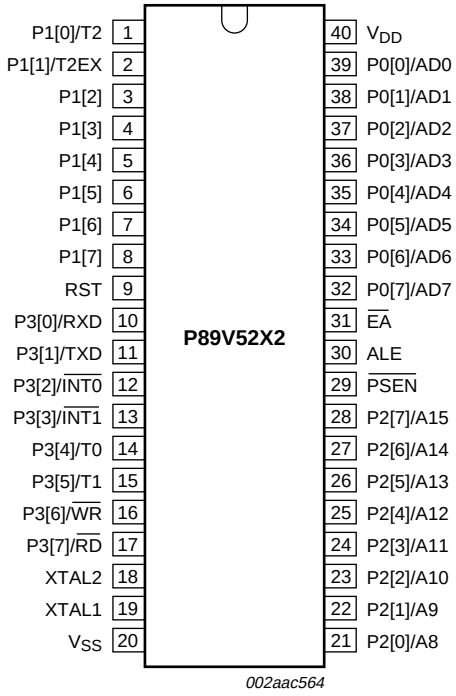

Fig 2. DIP40 pin configuration

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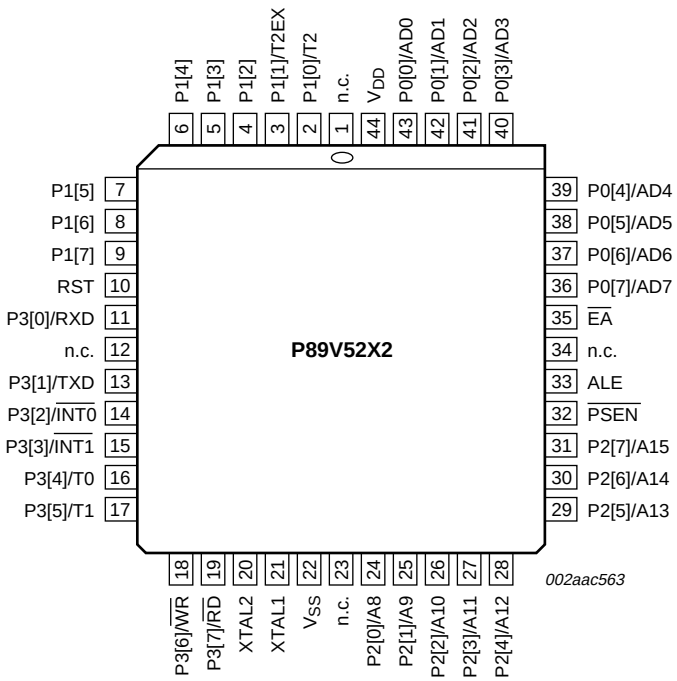

Fig 3. PLCC44 pin configuration

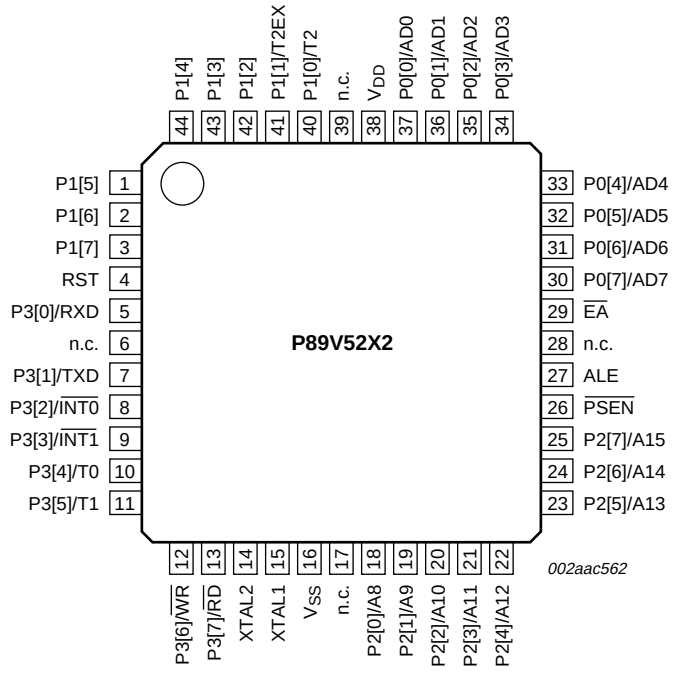

Fig 4. LQFP44 pin configuration

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5.2 Pin description

Table 2. Pin description

Symbol	Pin			Type	Description
	DIP40	LQFP44	PLCC44		
P0[0] to P0[7]				I/O	**Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. External pull-ups are required as a general purpose I/O port.
P0[0]/AD0	39	37	43	I/O	**P0[0] —** Port 0 bit 0.
				I/O	**AD0 —** Address/data bit 0.
P0[1]/AD1	38	36	42	I/O	**P0[1] —** Port 0 bit 1.
				I/O	**AD1 —** Address/data bit 1.
P0[2]/AD2	37	35	41	I/O	**P0[2] —** Port 0 bit 2.
				I/O	**AD2 —** Address/data bit 2.
P0[3]/AD3	36	34	40	I/O	**P0[3] —** Port 0 bit 3.
				I/O	**AD3 —** Address/data bit 3.
P0[4]/AD4	35	33	39	I/O	**P0[4] —** Port 0 bit 4.
				I/O	**AD4 —** Address/data bit 4.
P0[5]/AD5	34	32	38	I/O	**P0[5] —** Port 0 bit 5.
				I/O	**AD5 —** Address/data bit 5.
P0[6]/AD6	33	31	37	I/O	**P0[6] —** Port 0 bit 6.
				I/O	**AD6 —** Address/data bit 6.
P0[7]/AD7	32	30	36	I/O	**P0[7] —** Port 0 bit 7.
				I/O	**AD7 —** Address/data bit 7.
P1[0] to P1[7]				I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. P1[5], P1[6], P1[7] have high current drive of 16 mA.
P1[0]/T2	1	40	2	I/O	**P1[0] —** Port 1 bit 0.
				I	**T2 —** External count input to Timer/Counter 2 or Clock-out from Timer/Counter 2
P1[1]/T2EX	2	41	3	I/O	**P1[1] —** Port 1 bit 1.
				I	**T2EX**: Timer/Counter 2 capture/reload trigger and direction control
P1[2]	3	42	4	I/O	**P1[2] —** Port 1 bit 2.
P1[3]	4	43	5	I/O	**P1[3] —** Port 1 bit 3.
P1[4]	5	44	6	I/O	**P1[4] —** Port 1 bit 4.
P1[5]	6	1	7	I/O	**P1[5] —** Port 1 bit 5.
P1[6]	7	2	8	I/O	**P1[6] —** Port 1 bit 6.

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Table 2. Pin description *...continued*

Symbol	Pin			Type	Description
	DIP40	LQFP44	PLCC44		
P1[7]	8	3	9	I/O	**P1[7] —** Port 1 bit 7.
P2[0] to P2[7]				I/O with internal pull-up	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to '1's.
P2[0]/A8	21	18	24	I/O	**P2[0] —** Port 2 bit 0.
				O	**A8 —** Address bit 8.
P2[1]/A9	22	19	25	I/O	**P2[1] —** Port 2 bit 1.
				O	**A9 —** Address bit 9.
P2[2]/A10	23	20	26	I/O	**P2[2] —** Port 2 bit 2.
				O	**A10 —** Address bit 10.
P2[3]/A11	24	21	27	I/O	**P2[3] —** Port 2 bit 3.
				O	**A11 —** Address bit 11.
P2[4]/A12	25	22	28	I/O	**P2[4] —** Port 2 bit 4.
				O	**A12 —** Address bit 12.
P2[5]/A13	26	23	29	I/O	**P2[5] —** Port 2 bit 5.
				O	**A13 —** Address bit 13.
P2[6]/A14	27	24	30	I/O	**P2[6] —** Port 2 bit 6.
				O	**A14 —** Address bit 14.
P2[7]/A15	28	25	31	I/O	**P2[7] —** Port 2 bit 7.
				O	**A15 —** Address bit 15.
P3[0] to P3[7]				I/O with internal pull-up	**Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups.
P3[0]/RXD	10	5	11	I	**P3[0] —** Port 3 bit 0.
				I	**RXD —** Serial input port.
P3[1]/TXD	11	7	13	O	**P3[1] —** Port 3 bit 1.
				O	**TXD —** Serial output port.
P3[2]/$\overline{\text{INT0}}$	12	8	14	I	**P3[2] —** Port 3 bit 2.
				I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
P3[3]/$\overline{\text{INT1}}$	13	9	15	I	**P3[3] —** Port 3 bit 3.
				I	**$\overline{\text{INT1}}$ —** External interrupt 1 input
P3[4]/T0	14	10	16	I/O	**P3[4] —** Port 3 bit 4.
				I	**T0 —** External count input to Timer/Counter 0.

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Table 2. Pin description *...continued*

Symbol	Pin			Type	Description
	DIP40	LQFP44	PLCC44		
P3[5]/T1	15	11	17	I/O	**P3[5] —** Port 3 bit 5.
				I	**T1 —** External count input to Timer/Counter 1
P3[6]/$\overline{WR}$	16	12	18	O	**P3[6] —** Port 3 bit 6.
				O	**$\overline{WR}$ —** External data memory write strobe
P3[7]/$\overline{RD}$	17	13	19	O	**P3[7] —** Port 3 bit 7.
				O	**$\overline{RD}$ —** External data memory read strobe.
$\overline{PSEN}$	29	26	32	I/O	**Program Store Enable**: $\overline{PSEN}$ is the read strobe for external program memory. When the device is executing from internal program memory, $\overline{PSEN}$ is inactive (HIGH). When the device is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.
RST	9	4	10	I	**Reset**: While the oscillator is running, a HIGH logic state on this pin for two machine cycles will reset the device.
$\overline{EA}$	31	29	35	I	**External Access Enable**: $\overline{EA}$ must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. $\overline{EA}$ must be strapped to V_{DD} for internal program execution.
ALE	30	27	33	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. Normally the ALE[1] is emitted at a constant rate of $\frac{1}{6}$ the crystal frequency[2] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to '1', ALE is disabled.
XTAL1	19	15	21	I	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	14	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	40	38	44	I	**Power supply**
V_{SS}	20	16	22	I	**Ground**

[1] ALE loading issue: When ALE pin experiences higher loading (> 30 pF) during the reset, the microcontroller may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3 kΩ to 50 kΩ to V_{DD}, e.g., for ALE pin.

[2] For 6-clock mode, ALE is emitted at $\frac{1}{3}$ of crystal frequency.

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6. Functional description

6.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

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Table 3. Special function registers[1]

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0
ACC*	Accumulator	E0H	-	-	-	-	-	-	-	-
AUXR	Auxiliary function register	8EH	-	-	-	-	-	-	-	AO
AUXR1	Auxiliary function register 1	A2H	-	-	-		GF2	0	-	DPS
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0
B*	B register	F0H	-	-	-	-	-	-	-	-
CKCON	B register	8FH	-	-	-	-	-	-	-	X2
DPTR	Data Pointer (2 B)									
DPH	Data Pointer HIGH	83H	-	-	-	-	-	-	-	-
DPL	Data Pointer LOW	82H	-	-	-	-	-	-	-	-
FMCON	Flash control register (R)	F4H	BUSY	WE	-	DAP	-	-	SV	ERR
	Flash control register (W)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0
FMDATA	Flash data register	F5H	-	-	-	-	-	-	-	-
FMADRH	Flash memory address HIGH	F6H	-	-	-	-	-	-	-	-
FMADRL	Flash memory address LOW	F7H	-	-	-	-	-	-	-	-
		Bit address	AF	AE	AD	AC	AB	AA	A9	A8
IE*	Interrupt Enable 0	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8
IP*	Interrupt Priority 0	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0
IPH	Interrupt Priority 0 HIGH	B7H	-	-	PT2H	PS0H	PT1H	PX1H	PT0H	PX0H
		Bit address	87	86	85	84	83	82	81	80
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Bit address	97	96	95	94	93	92	91	90
P1*	Port 1	90H	-	-	-	-	-	-	T2EX	T2
		Bit address	A7	A6	A5	A4	A3	A2	A1	A0
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TXD	RXD
PCON	Power Control Register	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

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Table 3. Special function registers[1] *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	-	P
RCAP2H	Timer2 Capture HIGH	CBH	-	-	-	-	-	-	-	-
RCAP2L	Timer2 Capture LOW	CAH	-	-	-	-	-	-	-	-
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**
SCON*	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	Serial Port Data Buffer Register	99H	-	-	-	-	-	-	-	-
SADDR	Serial Port Address Register	A9H	-	-	-	-	-	-	-	-
SADEN	Serial Port Address Enable	B9H	-	-	-	-	-	-	-	-
SP	Stack Pointer	81H	-	-	-	-	-	-	-	-
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**
TCON*	Timer Control Register	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
		Bit address	**CF**	**CE**	**CD**	**CC**	**CB**	**CA**	**C9**	**C8**
T2CON*	Timer2 Control Register	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
T2MOD	Timer2 mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN
TH0	Timer 0 HIGH	8CH	-	-	-	-	-	-	-	-
TH1	Timer 1 HIGH	8DH	-	-	-	-	-	-	-	-
TH2	Timer 2 HIGH	CDH	-	-	-	-	-	-	-	-
TL0	Timer 0 LOW	8AH	-	-	-	-	-	-	-	-
TL1	Timer 1 LOW	8BH	-	-	-	-	-	-	-	-
TL2	Timer 2 LOW	CCH	-	-	-	-	-	-	-	-
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

[1] Unimplemented bits in SFRs (labeled '-') are 'X's (unknown) at all times. Unless otherwise specified, '1's should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

P89V52X2_3

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6.2 Memory organization

The various P89V52X2 memory spaces are as follows:

- DATA

  128 B of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 B of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 B immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89V52X2 has 8 kB of on-chip Code memory.

6.3 System clock and clock options

6.3.1 Clock input options and recommended capacitor values for the oscillator

Shown in Figure 5 and Figure 6 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven. Power consumption can be further reduced by programming the EXTCLK bit (UCFG.0).

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Resonator manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C_1 and C_2 should be adjusted appropriately for each design. Table 4 shows the typical values for C_1 and C_2 vs. resonator type for various frequencies.

Table 4. Recommended values for C_1 and C_2 by crystal type

Resonator	$C_1 = C_2$
Quartz	20 pF to 30 pF
Ceramic	40 pF to 50 pF

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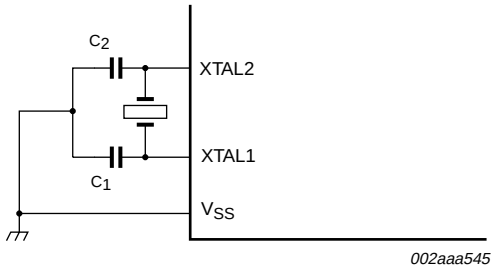

Fig 5. Oscillator characteristics (using the on-chip oscillator)

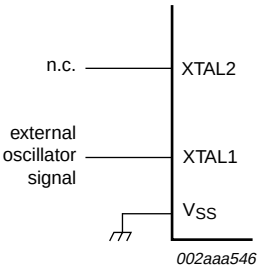

Fig 6. Oscillator characteristics (external clock drive)

6.3.2 Clock control register (CKCON)

By default, the device runs at twelve clocks per machine cycle. The device may be run in 6 clock per machine cycle mode by programming of either a non-volatile bit (FX2) or an SFR bit (Table 5 “Clock modes”). If the FX2 non-volatile bit is programmed the device will run in 6-clock mode and the X2 SFR bit has no effect. If the FX2 bit is erased, then the clock mode is controlled by the X2 SFR bit.

Table 5. Clock modes

FX2 clock mode bit (UCFG.1)	X2 bit (CLKCON.0)	CPU clock mode
erased	0	12-clock mode (default)
erased	1	6-clock mode
programmed	x	6-clock mode

6.4 ALE control

Table 6. AUXR - Auxiliary register (address 8EH) bit allocation

Not bit addressable; Reset value 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	AO

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Table 7. AUXR - Auxiliary register (address 8EH) bit description

Bit	Symbol	Description
7 to 1	-	Reserved for future use. Should be set to '0' by user programs.
0	AO	ALE off: disables/enables ALE. AO = 0 results in ALE emitted at a constant rate of ½ the oscillator frequency. In case of AO = 1, ALE is active only during a MOVX or MOVC.

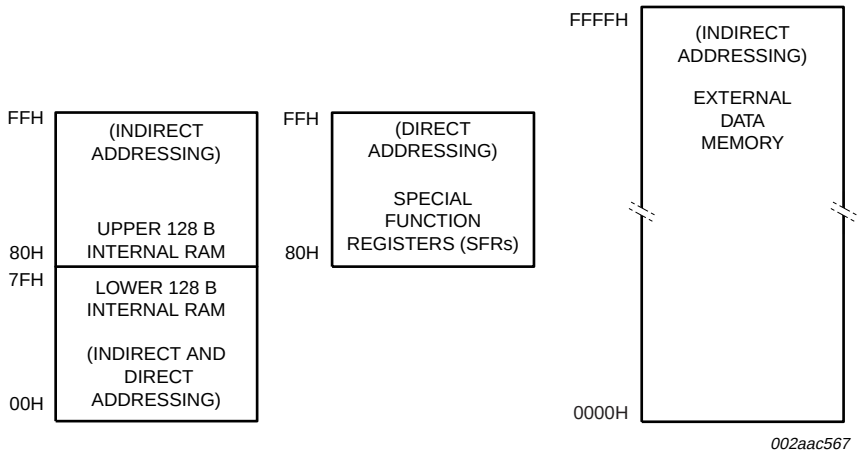

Fig 7. Internal and external data memory structure

6.5 Dual data pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS = 0, DPTR0 is selected; when DPS = 1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1 (see Figure 8).

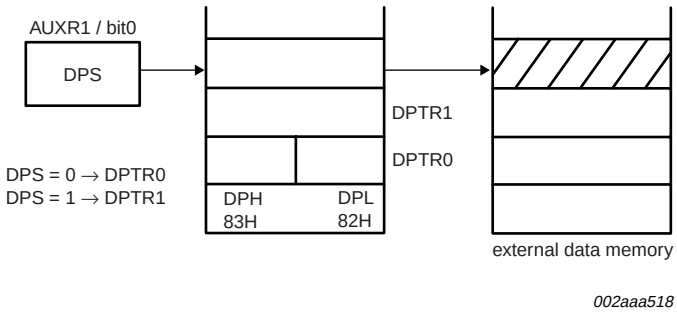

Fig 8. Dual data pointer organization

Table 8. AUXR1 - Auxiliary register 1 (address A2H) bit allocation

Not bit addressable; Reset value 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	GF2	0	-	DPS

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Table 9. AUXR1 - Auxiliary register 1 (address A2H) bit description

Bit	Symbol	Description
7 to 4	-	Reserved for future use. Should be set to '0' by user programs.
3	GF2	General purpose user-defined flag.
2	0	This bit contains a hard-wired '0'. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to '0' by user programs.
0	DPS	Data pointer select. Chooses one of two Data Pointers for use by the program. See text for details.

6.6 Reset

At initial power-up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins HIGH. Powering up the device without a valid reset could cause the device to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power-up are indeterminate.

When power is applied to the device, the RST pin must be held HIGH long enough for the oscillator to start-up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2 kΩ resistor as shown in Figure 9.

During initial power the POF flag in the PCON register is set to indicate an initial power-up condition. The POF flag will remain active until cleared by software.

Following a reset condition, under normal conditions, the device will start executing code from address 0000H in the user's code memory. However if the requirements are met for ICP entry, the device will enter ICP mode.

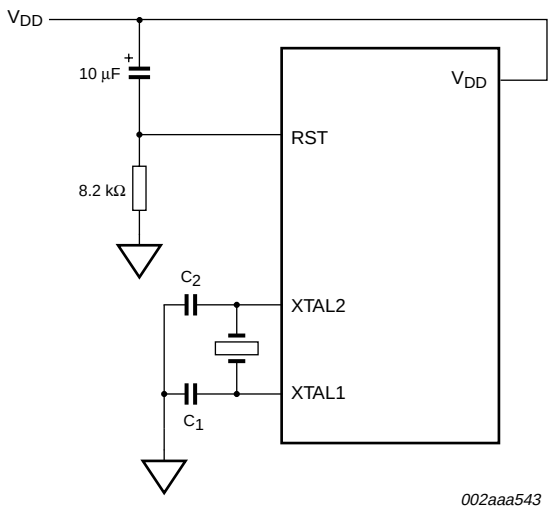

Fig 9. Power-on reset circuit

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6.7 Flash memory

6.7.1 Flash organization

The P89V52X2 program memory consists of an 8 kB block of user code. The flash can be read or written in bytes but may only be erased as an entire block. A chip erase function will erase the entire user code memory and its associated security bits. This flash memory can be erased or programmed using a programmer tool that supports ICP.

6.7.2 Features

- Flash internal program memory.
- Programming and erase over the full operating voltage range.
- Programming with industry-standard commercial programmers.
- 10000 typical erase/program cycles for each byte.
- 100 year minimum data retention.

6.8 Timers/counters 0 and 1

The two 16-bit Timer/Counter registers: Timer 0 and Timer 1 can be configured to operate either as timers or event counters (see Table 10 and Table 11).

In the ‘Timer’ function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of six oscillator periods, the count rate is $\frac{1}{6}$ of the oscillator frequency.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once every machine cycle.

When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register in the machine cycle following the one in which the transition was detected. Since it takes two machine cycles (12 oscillator periods) for 1-to-0 transition to be recognized, the maximum count rate is $\frac{1}{12}$ of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle. In addition to the ‘Timer’ or ‘Counter’ selection, Timer 0 and Timer 1 have four operating modes from which to select.

The ‘Timer’ or ‘Counter’ function is selected by control bits C/T in the Special Function Register TMOD. These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

Table 10. TMOD - Timer/Counter mode control register (address 89H) bit allocation

Not bit addressable; Reset value: 0000 0000B; Reset source(s): any source

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

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Table 11. TMOD - Timer/Counter mode control register (address 89H) bit description

Bit	Symbol	Description
7	T1GATE	Gating control for Timer 1. When set, Timer/Counter is enabled only while the $\overline{INT1}$ pin is HIGH and the TR1 control pin is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.
6	T1C/$\overline{T}$	Timer or Counter select for Timer 1. Cleared for Timer operation (input from CCLK). Set for Counter operation (input from T1 input pin).
5	T1M1	Mode select for Timer 1.
4	T1M0	
3	T0GATE	Gating control for Timer 0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is HIGH and the TR0 control pin is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
2	T0C/$\overline{T}$	Timer or Counter select for Timer 0. Cleared for Timer operation (input from CCLK). Set for Counter operation (input from T0 input pin).
1	T0M1	Mode Select for Timer 0.
0	T0M0	

Table 12. TMOD - Timer/Counter mode control register (address 89H) M1/M0 operating mode

M1	M0	Operating mode	
0	0	0	8048 timer 'TLx' serves as 5-bit prescaler
0	1	1	16-bit Timer/Counter 'THx' and 'TLx' are cascaded; there is no prescaler.
1	0	2	8-bit auto-reload Timer/Counter 'THx' holds a value which is to be reloaded into 'TLx' each time it overflows.
1	1	3	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/Counter 1 stopped.

Table 13. TCON - Timer/Counter control register (address 88H) bit allocation

Bit addressable; Reset value: 0000 0000B; Reset source(s): any reset

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 14. TCON - Timer/Counter control register (address 88H) bit description

Bit	Symbol	Description
7	TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to Timer 1 Interrupt routine, or by software.
6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter 1 on/off.
5	TF0	Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to Timer 0 Interrupt routine, or by software.
4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter 0 on/off.

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Table 14. TCON - Timer/Counter control register (address 88H) bit description *...continued*

Bit	Symbol	Description
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge/LOW-level is detected. Cleared by hardware when the interrupt is processed, or by software.
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/LOW-level that triggers external interrupt 1.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge/LOW-level is detected. Cleared by hardware when the interrupt is processed, or by software.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/LOW-level that triggers external interrupt 0.

6.8.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a fixed divide-by-32 prescaler. Figure 10 shows Mode 0 operation.

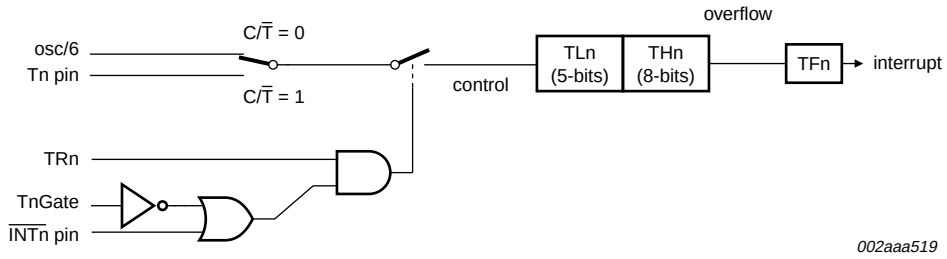

Fig 10. Timer/Counter 0 or 1 in Mode 0 (13-bit counter)

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The count input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the Special Function Register TCON (Figure 8). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1 (see Figure 10). There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

6.8.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register (THn and TLn) are used. See Figure 11.

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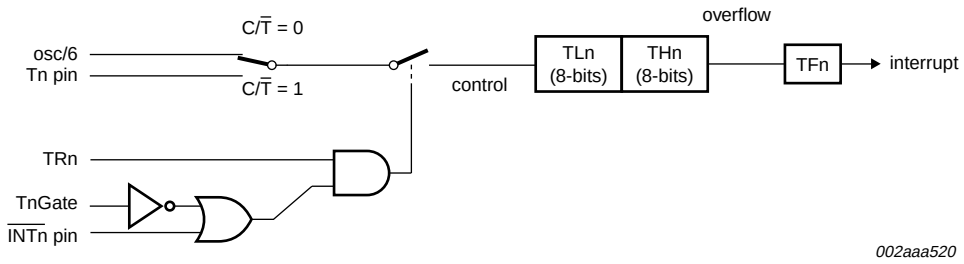

Fig 11. Timer/Counter 0 or 1 in Mode 1 (16-bit counter)

6.8.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TLn) with automatic reload, as shown in Figure 12. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

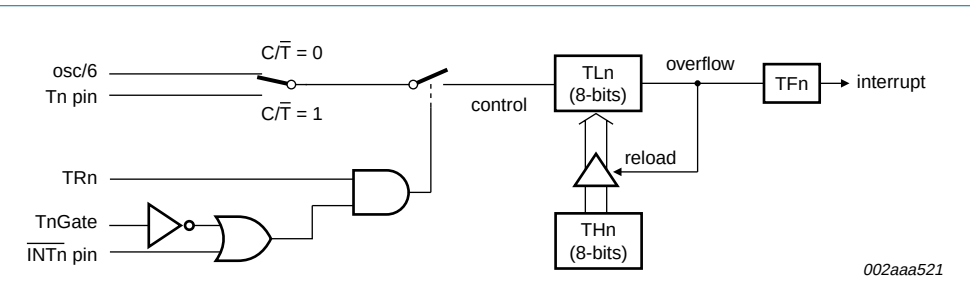

Fig 12. Timer/Counter 0 or 1 in Mode 2 (8-bit auto-reload)

6.8.4 Mode 3

When timer 1 is in Mode 3 it is stopped (holds its count). The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 and Timer 0 is shown in Figure 13. TL0 uses the Timer 0 control bits: T0C/$\overline{T}$, T0GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the 'Timer 1' interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in Mode 3, the P89V52X2 can look like it has an additional Timer.

Note: When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

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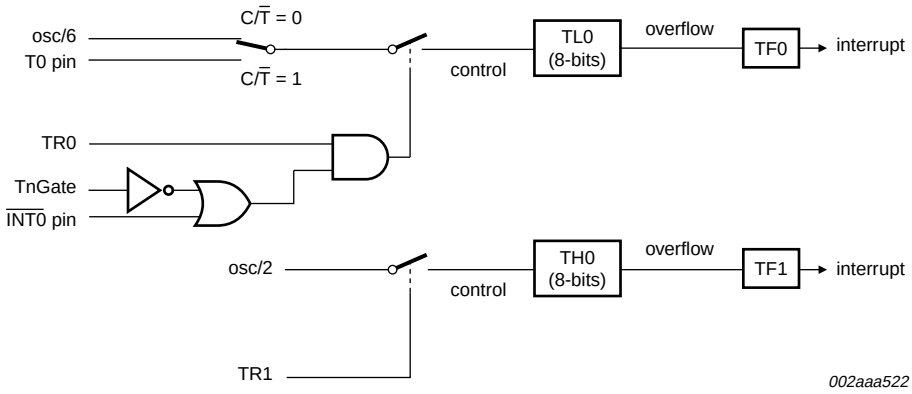

Fig 13. Timer/Counter 0 Mode 3 (two 8-bit counters)

6.9 Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2 in the special function register T2CON. Timer 2 has four operating modes: Capture, Auto-reload (up or down counting), Clock-out, and Baud Rate Generator which are selected according to Table 15 using T2CON (Table 16 and Table 17) and T2MOD (Table 18 and Table 19).

Table 15. Timer 2 operating mode

RCLK+TCLK	CP/$\overline{RL2}$	TR2	T2OE	Mode
0	0	1	0	16-bit auto reload
0	1	1	0	16-bit capture
0	0	1	1	Programmable Clock-Out
1	X	1	0	Baud rate generator
X	X	0	X	off

Table 16. T2CON - Timer/Counter 2 control register (address C8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 17. T2CON - Timer/Counter 2 control register (address C8H) bit description

Bit	Symbol	Description
7	TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1 or when Timer 2 is in Clock-out mode.
6	EXF2	Timer 2 external flag is set when Timer 2 is in capture, reload or baud rate mode, EXEN2 = 1 and a negative transition on T2EX occurs. If Timer 2 interrupt is enabled EXF2 = 1 causes the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
5	RCLK	Receive clock flag. When set, causes the UART to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

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Table 17. T2CON - Timer/Counter 2 control register (address C8H) bit description *...continued*

Bit	Symbol	Description
4	TCLK	Transmit clock flag. When set, causes the UART to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	Start/stop control for Timer 2. A logic '1' enables the timer to run.
1	C/$\overline{T}$2	Timer or counter select. (Timer 2) 0 = internal timer ($f_{osc}/6$) 1 = External event counter (falling edge triggered; external clock's maximum rate = $f_{osc}/12$
0	CP/$\overline{RL}$2	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 18. T2MOD - Timer 2 mode control register (address C9H) bit allocation

Not bit addressable; Reset value: XX00 0000B

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T2OE	DCEN

Table 19. T2MOD - Timer 2 mode control register (address C9H) bit description

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to '0' by user programs.
1	T2OE	Timer 2 Output Enable bit. Used in programmable clock-out mode only.
0	DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down-counter.

6.9.1 Capture mode

In the Capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0 Timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T}$2 in T2CON) which upon overflowing sets bit TF2, the Timer 2 overflow bit.

The capture mode is illustrated in Figure 14.

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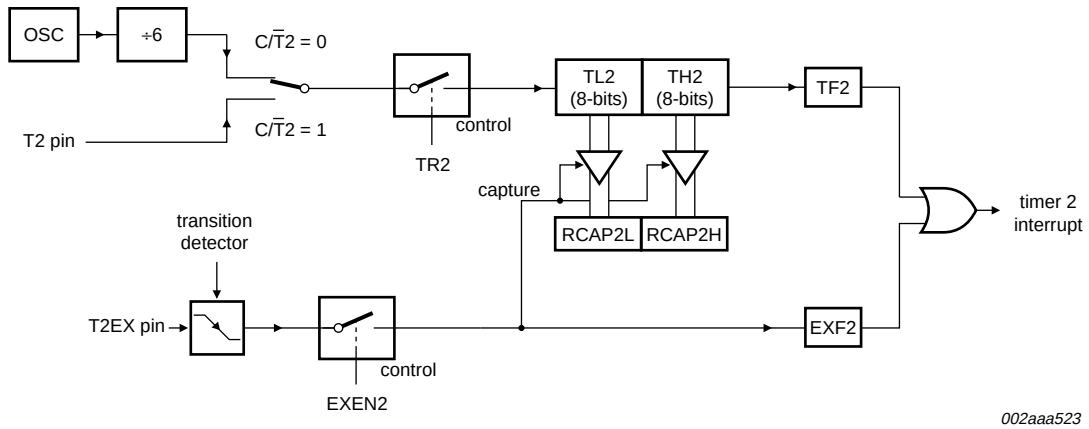

Fig 14. Timer 2 in Capture mode

This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IEN0 register). If EXEN2 = 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively.

In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt). The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt.

There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2 pin transitions or $f_{osc}/6$ pulses. Since once loaded contents of RCAP2L and RCAP2H registers are not protected, once Timer2 interrupt is signalled it has to be serviced before new capture event on T2EX pin occurs. Otherwise, the next falling edge on T2EX pin will initiate reload of the current value from TL2 and TH2 to RCAP2L and RCAP2H and consequently corrupt their content related to previously reported interrupt.

6.9.2 Auto-reload mode (up or down-counter)

In the 16-bit auto-reload mode, Timer 2 can be configured as either a timer or counter (via C/T2 in T2CON), then programmed to count up or down. The counting direction is determined by bit DCEN (Down-counter Enable) which is located in the T2MOD register (see Table 18 and Table 19). When reset is applied, DCEN = 0 and Timer 2 will default to counting up. If the DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 15 shows Timer 2 counting up automatically (DCEN = 0).

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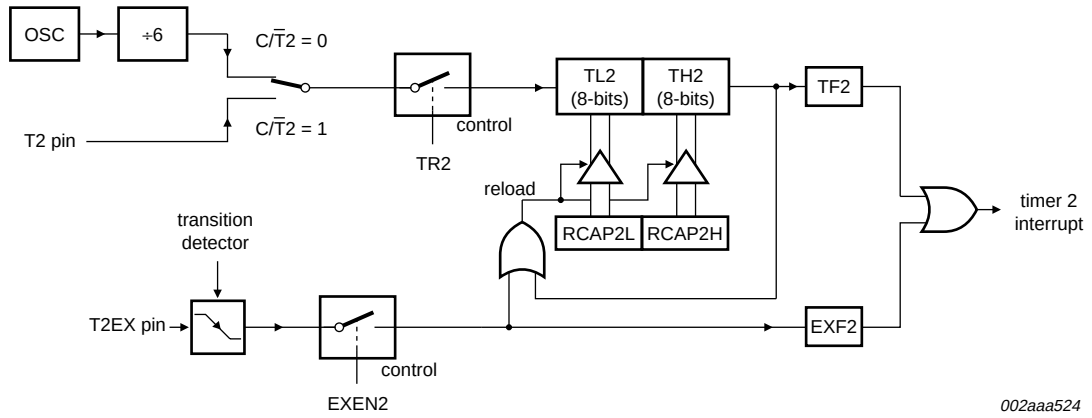

Fig 15. Timer 2 in auto-reload mode (DCEN = 0)

In this mode, there are two options selected by bit EXEN2 in T2CON register. If EXEN2 = 0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

Auto reload frequency when Timer 2 is counting up can be determined from this formula:

$$\frac{SupplyFrequency}{(65536 \angle (RCAP2H, RCAP2L))} \quad (1)$$

Where SupplyFrequency is either f_{osc} (C/$\overline{T2}$ = 0) or frequency of signal on T2 pin (C/$\overline{T2}$ = 1).

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 is ‘1’.

Microcontroller’s hardware will need three consecutive machine cycles in order to recognize falling edge on T2EX and set EXF2 = 1: in the first machine cycle pin T2EX has to be sampled as ‘1’; in the second machine cycle it has to be sampled as ‘0’, and in the third machine cycle EXF2 will be set to ‘1’.

In Figure 16, DCEN = 1 and Timer 2 is enabled to count up or down. This mode allows pin T2EX to control the direction of count. When a logic ‘1’ is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

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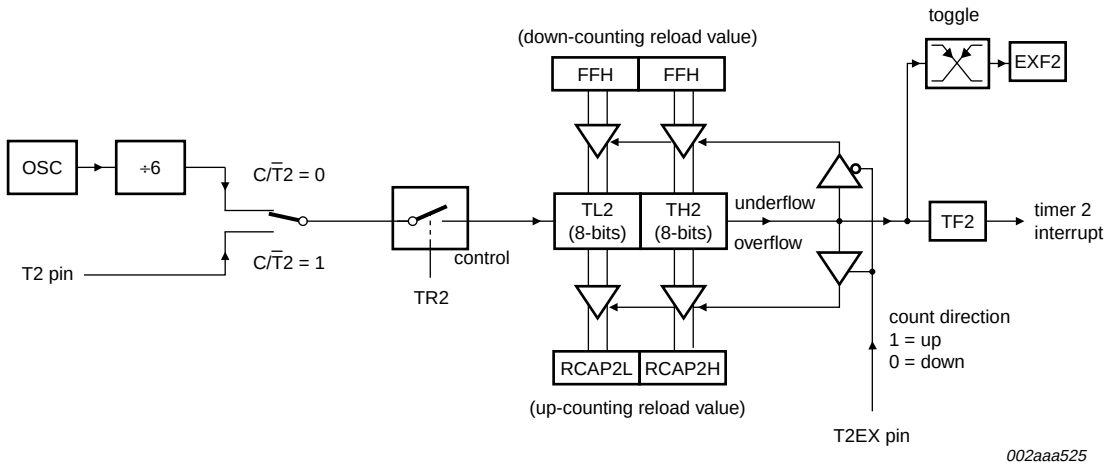

Fig 16. Timer 2 in Auto Reload mode (DCEN = 1)

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2. The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed.

6.9.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1[0]). This pin, besides being a regular I/O pin, has two additional functions. It can be programmed:

1. To input the external clock for Timer/Counter 2, or
2. To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{OscillatorFrequency}{2\times(65536\angle(RCAP2H, RCAP2L))} \quad (2)$$

Where (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 rollovers will not generate an interrupt. This is similar to when it is used as a baud rate generator.

6.9.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART transmit and receive baud rates to be derived from either Timer 1 or Timer 2 (See Section 6.10 for details). When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When TCLK = 1, Timer 2 is

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used as the UART transmit baud rate generator. RCLK has the same effect for the UART receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – Timer 1 or Timer 2.

Figure 17 shows Timer 2 in baud rate generator mode:

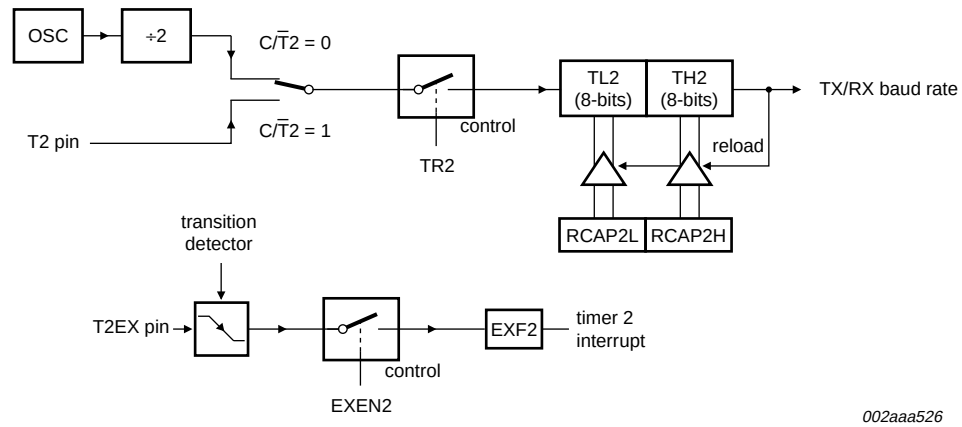

Fig 17. Timer 2 in Baud Rate Generator mode

The baud rate generation mode is like the auto-reload mode, when a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

Modes 1 and 3 Baud Rates = Timer 2 Overflow Rate/16

The timer can be configured for either 'timer' or 'counter' operation. In many applications, it is configured for 'timer' operation (C/$\overline{T}$2 = 0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., $\frac{1}{6}$ the oscillator frequency). As a baud rate generator, it increments at the oscillator frequency. Thus the baud rate formula is as follows:

Modes 1 and 3 Baud Rates =

$$\frac{OscillatorFrequency}{(16 \times (65536 - (RCAP2H, RCAP2L)))} \quad (3)$$

Where: (RCAP2H, RCAP2L) = The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

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When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. Under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers. Table 20 shows commonly used baud rates and how they can be obtained from Timer 2.

6.9.5 Summary of baud rate equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2 (P1[0]) the baud rate is:

Baud rate = Timer 2 overflow rate/16

If Timer 2 is being clocked internally, the baud rate is:

Baud rate = $f_{osc}/(16 \times (65536 - (RCAP2H, RCAP2L)))$

Where f_{osc} = oscillator frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

RCAP2H, RCAP2L = $65536 - f_{osc}/(16 \times \text{baud rate})$

Table 20. Timer 2 generated commonly used baud rates

Rate	Oscillator frequency	Timer 2	
		RCAP2H	RCAP2L
750 kBd	12 MHz	FF	FF
19.2 kBd	12 MHz	FF	D9
9.6 kBd	12 MHz	FF	B2
4.8 kBd	12 MHz	FF	64
2.4 kBd	12 MHz	FE	C8
600 Bd	12 MHz	FB	1E
220 Bd	12 MHz	F2	AF
600 Bd	6 MHz	FD	8F
220 Bd	6 MHz	F9	57

6.10 UART

The UART operates in all standard modes. Enhancements over the standard 80C51 UART include Framing Error detection, and automatic address recognition.

6.10.1 Mode 0

Serial data enters and exits through RXD and TXD outputs the shift clock. Only 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{6}$ of the CPU clock frequency. UART configured to operate in this mode outputs serial clock on TXD line no matter whether it sends or receives data on RXD line.

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6.10.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer $^1/_2$ overflow rate.

6.10.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or (e.g. the parity bit (P, in the PSW) could be moved into TB8). When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either $^1/_{16}$ or $^1/_{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

6.10.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer $^1/_2$ overflow rate.

Table 21. SCON - Serial port control register (address 98H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Table 22. SCON - Serial port control register (address 98H) bit description

Bit	Symbol	Description
7	SM0/FE	The usage of this bit is determined by SMOD0 in the PCON register. If SMOD0 = 0, this bit is SM0, which with SM1, defines the serial port mode. If SMOD0 = 1, this bit is FE (Framing Error). FE is set by the receiver when an invalid stop bit is detected. Once set, this bit cannot be cleared by valid frames but can only be cleared by software. (Note: It is recommended to set up UART mode bits SM0 and SM1 before setting SMOD0 to '1'.)
6	SM1	With SM0, defines the serial port mode (see Table 23 below).
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to '1', then RI will not be activated if the received 9th data bit (RB8) is '0'. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be '0'.
4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
3	TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

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Table 22. SCON - Serial port control register (address 98H) bit description *...continued*

Bit	Symbol	Description
2	RB8	In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is undefined.
1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the stop bit in the other modes, in any serial transmission. Must be cleared by software.
0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or approximately halfway through the stop bit time in all other modes. (See SM2 for exceptions). Must be cleared by software.

Table 23. SCON - Serial port control register (address 98H) SM0/SM1 mode definition

SM0, SM1	UART mode	Baud rate
0 0	0: shift register	CPU clock/6
0 1	1: 8-bit UART	variable
1 0	2: 9-bit UART	CPU clock/32 or CPU clock/16
1 1	3: 9-bit UART	variable

6.10.5 Framing error

Framing error (FE) is reported in the SCON.7 bit if SMOD0 (PCON.6) = 1. If SMOD0 = 0, SCON.7 is the SM0 bit for the UART, it is recommended that SM0 is set up before SMOD0 is set to '1'.

6.10.6 More about UART mode 1

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset to align its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated.

6.10.7 More about UART modes 2 and 3

Reception is performed in the same manner as in mode 1.

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The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF.

6.10.8 Multiprocessor communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed so that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in a way that the 9th bit is ‘1’ in an address byte and ‘0’ in the data byte. With SM2 = 1, no slave will be interrupted by a data byte, i.e. the received 9th bit is ‘0’. However, an address byte having the 9th bit set to ‘1’ will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed or not. The addressed slave will clear its SM2 bit and prepare to receive the data (still 9 bits long) that follow. The slaves that weren’t being addressed leave their SM2 bits set and go on about their business, ignoring the subsequent data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. When UART receives data in mode 1 and SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.10.9 Automatic address recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled for the UART by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the ‘Given’ address or the ‘Broadcast' address. The 9 bit mode requires that the 9th information bit is a ‘1’ to indicate that the received information is an address and not data.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two Special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are ‘don’t care’. The SADEN mask can be logically ANDed with the SADDR to create the ‘Given’ address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others.

This device uses the methods presented in Figure 18 to determine if a ‘Given’ or ‘Broadcast’ address has been received or not.

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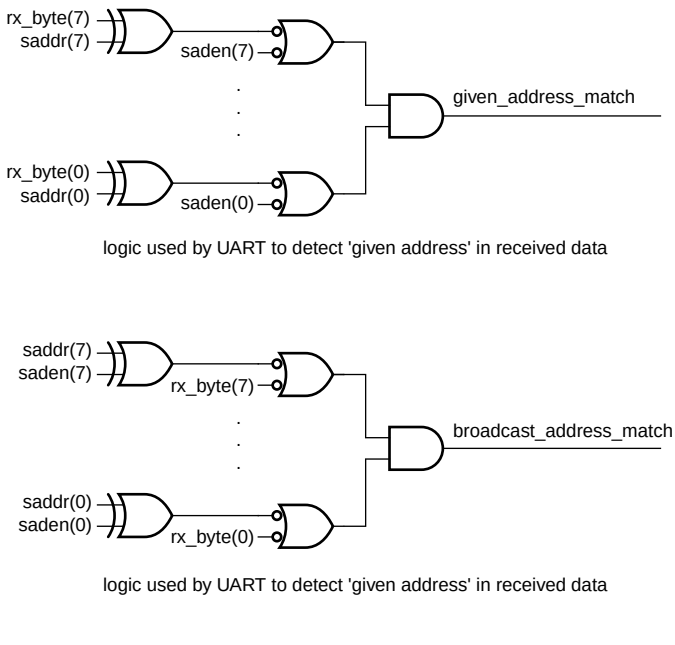

Fig 18. Schemes used by the UART to detect ‘given’ and ‘broadcast’ addresses when multiprocessor communications is enabled

The following examples will help to show the versatility of this scheme.

Example 1, slave 0:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1101} \\ \text{Given} = 1100\ 00\text{X}0 \end{array} \quad (4)$$

Example 2, slave 1:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1110} \\ \text{Given} = 1100\ 000\text{X} \end{array} \quad (5)$$

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a ‘0’ in bit 0 and it ignores bit 1. Slave 1 requires a ‘0’ in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a ‘0’ in bit 1. A unique address for slave 1 would be 1100 0001 since a ‘1’ in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Example 1, slave 0:

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SADDR = 1100 0000
SADEN = 1111 1001
Given = 1100 0XX0 (6)

Example 2, slave 1:

SADDR = 1110 0000
SADEN = 1111 1010
Given = 1110 0X0X (7)

Example 2, slave 2:

SADDR = 1100 0000
SADEN = 1111 1100
Given = 1100 00XX (8)

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2. The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal. Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all 'don't cares' as well as a Broadcast address of all 'don't cares'. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

6.11 Interrupt priority and polling sequence

The device supports six interrupt sources under a four level priority scheme. Table 24 summarizes the polling sequence of the supported interrupts. (See Figure 19).

Table 24. Interrupt polling sequence

Description	Interrupt flag	Vector address	Interrupt enable	Interrupt priority	Service priority	Wake-up Power-down
External Interrupt 0	IE0	0003H	EX0	PX0/H	1 (highest)	yes
T0	TF0	000BH	ET0	PT0/H	2	no
External Interrupt 1	IE1	0013H	EX1	PX1/H	3	yes
T1	TF1	001BH	ET1	PT1/H	4	no
UART	TI/RI	0023H	ES0	PS0/H	5	no
T2	TF2, EXF2	003BH	ET2	PT2/H	6	no

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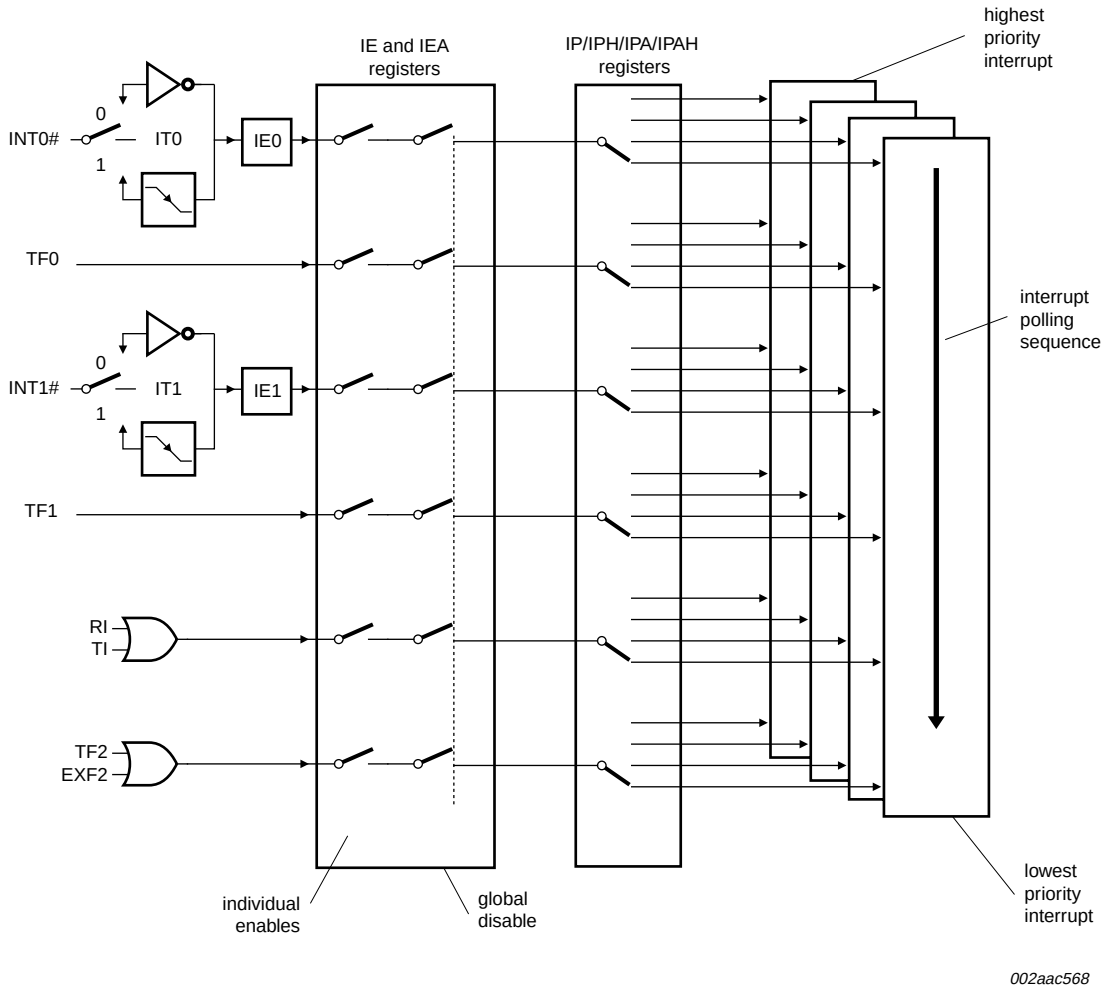

Fig 19. Interrupt structure

Table 25. IE - Interrupt enable register (address A8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Table 26. IE - Interrupt enable register (address A8H) bit description

Bit	Symbol	Description
7	EA	Interrupt Enable Bit: EA = 1 interrupt(s) can be serviced, EA = 0 interrupt servicing disabled.
6	-	Reserved
5	ET2	Timer 2 Overflow Interrupt Enable
4	ES	Serial Port Interrupt Enable
3	ET1	Timer 1 Overflow Interrupt Enable.

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Table 26. IE - Interrupt enable register (address A8H) bit description *...continued*

Bit	Symbol	Description
2	EX1	External Interrupt 1 Enable.
1	ET0	Timer 0 Overflow Interrupt Enable.
0	EX0	External Interrupt 0 Enable.

Table 27. IP - Interrupt priority low register (address B8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	PT2	PS	PT1	PX1	PT0	PX0

Table 28. IP - Interrupt priority low register (address B8H) bit description

Bit	Symbol	Description
7:6	-	Reserved
5	PT2	Timer 2 Interrupt Priority Low Bit.
4	PS	Serial Port Interrupt Priority Low Bit.
3	PT1	Timer 1 Interrupt Priority Low Bit.
2	PX1	External Interrupt 1 Priority Low Bit.
1	PT0	Timer 0 Interrupt Priority Low Bit.
0	PX0	External Interrupt 0 Priority Low Bit.

Table 29. IPH - Interrupt priority high register (address B7H) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Table 30. IPH - Interrupt priority high register (address B7H) bit description

Bit	Symbol	Description
7:6	-	Reserved
5	PT2H	Timer 2 Interrupt Priority High Bit.
4	PSH	Serial Port Interrupt Priority High Bit.
3	PT1H	Timer 1 Interrupt Priority High Bit.
2	PX1H	External Interrupt 1 Priority High Bit.
1	PT0H	Timer 0 Interrupt Priority High Bit.
0	PX0H	External Interrupt 0 Priority High Bit.

6.12 Power-saving modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and Power-down, see Table 31.

6.12.1 Idle mode

Idle mode is entered setting the IDL bit in the PCON register. In Idle mode, the program counter is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

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The device exits Idle mode through either a system interrupt or a hardware reset. Exiting Idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits Idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the Idle mode. A hardware reset starts the device similar to a power-on reset.

6.12.2 Power-down mode

The Power-down mode is entered by setting the PD bit in the PCON register. In the Power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during Power-down, the minimum V_{DD} level is 2.0 V.

The device exits Power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits Power-down. Holding the external interrupt pin LOW restarts the oscillator, the signal must hold LOW at least 1024 clock cycles before bringing back HIGH to complete the exit. Upon interrupt signal restored to logic V_{IH}, the interrupt service routine program execution resumes beginning at the instruction immediately following the instruction which invoked Power-down mode. A hardware reset starts the device similar to power-on reset.

To exit properly out of Power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

Table 31. Power-saving modes

Mode	Initiated by	State of device	Exited by
Idle mode	Software (set IDL bit in PCON) MOV PCON, #01H;	CLK is running. Interrupts, serial port and timers/counters are active. Program Counter is stopped. ALE and $\overline{PSEN}$ signals at a HIGH-level during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits Idle mode, after the interrupt service routine RETI instruction, program resumes execution beginning at the instruction following the one that invoked Idle mode. A hardware reset restarts the device similar to a power-on reset.
Power-down mode	Software (set PD bit in PCON) MOV PCON, #02H;	CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and $\overline{PSEN}$ signals at a LOW-level during power-down. External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits Power-down mode, after the interrupt service routine RETI instruction program resumes execution beginning at the instruction following the one that invoked Power-down mode. A hardware reset restarts the device similar to a power-on reset.

6.13 Data EEPROM

The P89V52X2 contains 192 B of data EEPROM organized into three pages of 64 B each. This memory can be erased in 64 byte pages (using a Page Erase command) or erased and written as bytes. The P89V52X2 flash reliably stores memory contents even after 100000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. P89V52X2 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

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The data EEPROM must be mapped into the code memory address space in order to read, erase, or program the data EEPROM. The memory is read using the MOVC instruction.

6.13.1 Features

- ICP with industry-standard commercial programmers
- IAP-Lite allows individual and multiple bytes of data EEPROM to be programmed under control of the end application.
- Programming and erase over the full operating voltage range
- Programming/Erase using ICP or IAP-Lite
- Program or erases requires 2 ms, 4 ms, or 6 ms, depending on the operation
- Programmable security for the data in each page
- > 100000 typical erase/program cycles for each byte
- Data EEPROM mapped into code space for quick MOVC reading

6.13.2 Register interface

Erasing, programming, and mapping operations are performed in the application under the control of the microcontroller's firmware using four SFRs and an internal 64-byte 'page register'. These SFRs are:

- FMCON (Flash Control Register). When read, this is the status register. When written, this is a command register. Note that the status bits are cleared to logic 0s when the command is written.
- FMADRL, FMADRH (Flash memory address low, Flash memory address high). Used to specify the byte address within the page register or specify the page within user code memory (for programming, erase, and reading the data EEPROM is mapped into the user address space (see Table 32).
- FMDATA (Flash Data Register). Accepts data to be loaded into the page register.

Data is read by mapping the data EEPROM into the code memory space and using the MOVC instruction.

6.13.3 Mapping the data EEPROM into code space

In order to read, erase, or program the data EEPROM must be mapped into the code memory address space. This is accomplished by writing the MAP command (09H) to FMCON. The data EEPROM may be unmapped by writing the UNMAP command (0AH) to FMCON. The mapping of the data EEPROM pages into code memory space is shown in Table 32.

Table 32. Data EEPROM page addresses

Data EEPROM page	Start address	End address
0	FF00H	FF3FH
1	FF40H	FF7FH
2	FF80H	FFBFH

6.13.4 Reading the data EEPROM

Reading the data EEPROM can be achieved by performing the following sequence:

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- Map the data EEPROM into code memory space if not already mapped.
- Write the data EEPROM byte address into the DPTR.
- Use the MOVC instruction to read the data EEPROM.

6.13.5 Erasing a complete page (64 B)

A complete page can be erased by performing the following sequence:

- Map the data EEPROM into code memory space if not already mapped.
- Write the lower 8-bits of the data EEPROM page's start address into FMADRL.
- Write the ERS_DP command (33H) to FMCON.

Once the ERS_DP command is written to FMCON, code execution will stall until the operation is completed, approximately 6 ms.

6.13.6 Data EEPROM programming and erasing using the page register

In addition to page erase, a 64 B page register is included which allows from 1 B to 64 B of a given page to be programmed or erase/programmed at the same time, substantially reducing overall programming time. Two programming operations are provided:

- Program only operation. This operation used the PROG (48H) command and programs the contents of the page register into the data EEPROM page. This operation requires that the bytes being programmed have been previously erased. This operation requires approximately 2 ms to complete.
- Erase and Program operation. This operation uses the EP (68H) command to both erase and program the bytes previously loaded into the page register. This command is often useful to erase and reprogram a single byte of data. This operation requires approximately 4 ms to complete.

The page register consists of 64 B and an update flag for each byte. When a LOAD command is issued to FMCON the page register contents and all of the update flags will be cleared. When FMDATA is written, the value written to FMDATA will be stored in the page register at the location specified by the lower 6 bits of FMADRL. In addition, the update flag for that location will be set. FMADRL will auto-increment to the next location. Auto-increment after writing to the last byte in the page register will 'wrap-around' to the first byte in the page register, but will not affect FMADRL[7:6]. Bytes loaded into the page register do not have to be continuous. Any byte location can be loaded into the page register by changing the contents of FMADRL prior to writing to FMDATA. However, each location in the page register can only be written once following each LOAD command. Attempts to write to a page register location more than once should be avoided.

FMADRH and FMADRL[7:6] are used to specify a page in the code memory space. When the PROG command is written to FMCON, the locations within the data EEPROM page that correspond to updated locations in the page register will have their contents programmed with the contents of their corresponding locations in the page register. Only the bytes that were loaded into the page register will be programmed in the data EEPROM array. Other bytes within the data EEPROM array will not be affected. The EP command works similarly except that If the EP command is written, the corresponding bytes in the data EEPROM will be erased prior to being programmed. This is often useful for erasing and programming a small number of bytes or even a single byte.

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Writing either the PROG or EP command to FMCON will start the program or erase-program process and place the CPU in a program-idle state. The CPU will remain in this idle state until the program or erase-program cycle is completed. Interrupts will NOT be serviced until the cycle is completed.

Erase-program or programming of a single byte (or multiple bytes) in the data EEPROM array is accomplished using the following steps:

- Write the LOAD command (00H) to FMCON. The LOAD command will clear all locations in the page register and their corresponding update flags.
- Write the address within the page register to FMADRL. Since the loading the page register uses FMADRL[5:0], and since the erase-program or program command uses FMADRH and FMADRL[7:6], the user can write the byte location within the page register (FMADRL[5:0]) and the code memory page address (FMADRH and FMADRL[7:6]) at this time.
- Write the data to be programmed to FMDATA. This will increment FMADRL pointing to the next byte in the page register.
- Write the address of the next byte to be programmed to FMADRL, if desired. (This is not needed for contiguous bytes since FMADRL is auto-incremented). All bytes to be programmed must be within the same page.
- Write the data for the next byte to be programmed to FMDATA.
- Repeat writing of FMADRL and/or FMDATA until all desired bytes have been loaded into the page register.
- Write the page address mapped into user code memory to FMADRH and FMADRL[7:6], if not previously included when writing the page register address to FMADRL[5:0].
- Write the EP (68H) or PROG (48H) command to FMCON, starting the erase-program or program cycle.
- Read FMCON to check status. If aborted, repeat starting with the LOAD command.

Table 33. Flash Memory Control register (FMCON - address F4H) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol (R)	BUSY	WE	-	DAP	-	-	SV	ERR
Symbol (W)	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0
Reset	0	0	0	0	0	0	0	0

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Table 34. Flash Memory Control register (FMCON - address E4H) bit description

Bit	Symbol	Access	Description
0	ERR	R	Set when either of the following conditions occur: • Device was reset before the operation was completed. • Attempt made to access data EEPROM while Data Access Protect (DAP) is set. • An error occurs in the device's internal high voltage circuits.
	FMCMD.0	W	Command byte bit 0.
1	SV	R	Security violation. Set when an attempt is made to program, erase, or CRC a secured page. The specific cause of the security violation depends on the operation: • **PROG or EP**: CSEC.0 = 1 or DPxSEC.1 = 1 for the page addressed by FMADRH/L. • **ERS_G**: Any DPxSEC.0 = 1. • **ERS_DP**: DPxSEC.2 = 1 for addressed page while in execution mode. • **CRC_DP**: DPxCSEC.0 = 1 and DPxSEC.1 = 0.
	FMCMD.1	W	Command byte bit 1
2	-	R	Reserved
	FMCMD.2	W	Command byte bit 2.
3	-	R	Reserved
	FMCMD.3	W	Command byte bit 3.
4	DAP	R	Data Access Protect. When set, access to the data EEPROM is unmapped and thus prohibited. Set by the MAP command. Cleared by the UNMAP command.
	FMCMD.4	W	Command byte bit 4.
5	-	R	Reserved
	FMCMD.5	W	Command byte bit 5.
6	WE	R	When set, indicates that data EEPROM writes during program execution are enabled.
	FMCMD.6	W	Command byte bit 6.
7	BUSY	R	Indicates that a program, erase, CRC calculation or similar operation is in progress. Note that this bit is usable only in ICP mode since the CPU is stalled whenever this bit is set in execution mode.
	FMCMD.7	W	Command byte bit 7.

An assembly language routine to load the page register and perform an erase/program operation is shown below. This code assumes the data EEPROM has been mapped into user code space.

```
;*************************************************
;*    pgm user code          *
;*************************************************
;*
;                                                *

;* Inputs:                                                    *
;*R3 = number of bytes to program (byte)          *
;*R4 = page address MSB(byte)                     *
;*R5 = page address LSB(byte)                     *
;*R7 = pointer to data buffer in RAM(byte)        *
;* Outputs:                                                   *
;*R7 = status (byte)                                 *
;* C = clear on no error, set on error            *
;*************************************************
```


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```
LOAD     EQU     00H
EP       EQU     68H

PGM_USER:
          MOV     FMCON,#LOAD   ;load command, clears page register
          MOV     FMADRH,R4     ;get high address
          MOV     FMADRL,R5     ;get low address
          MOV     A,R7          ;
          MOV     R0,A          ;get pointer into R0
 LOAD_PAGE:
          MOV     FMDAT,@R0     ;write data to page register
          INC     R0             ;point to next byte
          DJNZ    R3,LOAD_PAGE  ;do until count is zero
          MOV     FMCON,#EP     ;else erase & program the page

          MOV     R7,FMCON      ;copy status for return
          MOV     A,R7          ;read status
          ANL     A,#0FH        ;save only four lower bits
          JNZ     BAD            ;
          CLR     C              ;clear error flag if good
          RET                    ;and return
BAD:
          SETB    C             ;set error flag
          RET                    ;and return
```

A C-language routine to load the page register and perform an erase/program operation is shown below. This code assumes the data EEPROM has been mapped into user code space.

```
#include <REGV52.H>
unsigned char idata dbytes[64];// data buffer
unsigned char Fm_stat;// status result
bit PGM_USER (unsigned char, unsigned char);
bit prog_fail;
void main ()
{
     prog_fail=PGM_USER(0x1F,0xC0);
}

bit PGM_USER (unsigned char page_hi, unsigned char page_lo)
          {
                    #define LOAD0x00// clear page register, enable loading
                    #define EP0x68// erase & program page
                    unsigned char i;// loop count

           FMCON = LOAD;//load command, clears page reg
           FMADRH = page_hi;//
           FMADRL = page_lo;//write my page address to addr regs

           for(i=0;i<64;i=i+1)
               {
```


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```
                    FMDATA = dbytes[i];
                }
            FMCON = EP;//erase & prog page command
            Fm_stat = FMCON;//read the result status
            if ((Fm_stat & 0x0F)!=0) prog_fail=1; else prog_fail=0;
            return(prog_fail);
    }
```

6.13.7 Data EEPROM write enable

The data EEPROM has a Write Enable mechanism to help prevent against inadvertent writes. If the WE bit (FMCON.6) is set writes to the data EEPROM are enabled. When cleared, writes are disabled. This bit only affects execution mode. The WE bit is set when:

- The disable write enable bit, DISWE (UCFG.2) = 1
- In ICP mode
- The SET_WE (08H) command is written to FMCON followed by the key value (96H) being written to FMDATA

The WE bit is cleared following any reset. The WE bit may also be cleared by writing the CLR_WE (0BH) command to FMCON.

6.13.8 Data EEPROM security bits

The data EEPROM security bits protects each data EEPROM page. The data EEPROM page security bits and their effects are shown in Table 35.

Table 35. DPxSEC - Data page X security register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	XERSx	PWRx	MOVCx

Table 36. DPxSEC - Data page X security register bit description

Bit	Symbol	Description
7 to 3	-	Reserved
2	XERSx	Execution Erase Protect x. When programmed = 1, cannot be erased with ERS_DP command in execution mode. ERS_DP can be used in ICP mode.
1	PWRx	Page Write Protect x. When programmed = 1, data EEPROM cannot be erased or programmed using PROG or EP commands.
0	MOVCx	When programmed = 1, prevents instructions fetched from off-chip from reading the contents of the data EEPROM and returns FFH. CRC_DP are disabled if the corresponding Page Write Protect is disabled.

6.13.9 Summary of data EEPROM commands

Table 37 is a summary of the FMCON commands related to the data EEPROM.

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Table 37. Summary of data EEPROM commands

Mnemonic	Value (hex)	Description
CLR_WE	0B	Clear the WE bit
CRC_DP	1D	Calculate CRC on selected data EEPROM page
EP	68	Erase and Program data EEPROM page
ERS_DP	33	Erase data EEPROM page
LOAD	00	Reset and clear page register
MAP	09	Map data EEPROM into upper end of user code space
PROG	48	Program data EEPROM page
SET_WE	08	Set the WE bit if followed by writing key value to FMDATA
UNMAP	0A	Unmap data EEPROM from user code space

6.14 User configuration bytes

This device contains some non-volatile bytes which allow the user to configure the device. These bytes are programmed or read using the configuration read or write command (CONF) with a programmer that supports ICP. The user configuration bytes, their CONF address are shown in Table 38.

Table 38. User configuration bytes

Configuration byte	CONF address	Function
UCFG	00H	6x/12x selection, ext clk select, disable WE
CSEC	01H	Code security
DP0SEC	02H	Data EEPROM, page 0, security
DP1SEC	03H	Data EEPROM, page 1, security
DP2SEC	04H	Data EEPROM, page 2, security
MFG_ID	10H	Manufacturer signature byte
DEVIC_ID	11H	Device id signature byte
DERIV_ID	12H	Derivative id signature byte

6.15 UCFG

The user configuration bits in the UCFG register allow the user to configure some of the operating characteristics of the device and are shown in Table 39.

Table 39. UCFG - User configuration register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	ENW	FX2	EXTCLK

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Table 40. UCFG - User configuration register bit description

Bit	Symbol	Description
7 to 3	-	Reserved
2	ENW	Enable Write. When programmed = 1, forces the WE bit to be set.
1	FX2	Force X2. When programmed = 1, the device is in 6-clock mode. When erased = 0, the mode depends on the state of the X2 bit in CKCON.
0	EXTCLK	External Clock. When programmed = 1, disables the XTAL block when using an external digital clock source.

6.16 Code security (CSEC) bits

The code security bits protect against software piracy and prevent the contents of the flash from being read by unauthorized parties. The code security bits and their effects are shown in Table 41.

Table 41. CSEC - Code security register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INTEXEC	PROT

Table 42. CSEC - Code security register bit description

Bit	Symbol	Description
7 to 2	-	Reserved
1	INTEXEC	Internal execution only. When programmed, if the internal address space is exceeded, the address will rollover into internal space (upper address bits are ignored) for MOVC and instruction fetches. MOVC will access the data EEPROM when the address >= FF00H.
0	PROT	Protect. When programmed, prohibits further erasing or programming of code memory. MOVC instructions executed from external code memory are disabled from fetching code bytes from internal code memory.

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7. Limiting values

Table 43. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	V_{DD} + 0.5	V
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	15	mA
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

8. Static characteristics

Table 44. Static characteristics

T_{amb} = –40 °C to +85 °C; V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$n_{endu(fl)}$	endurance of flash memory	JEDEC Standard A117	[1]	10000	-		cycles
$t_{ret(fl)}$	flash memory retention time	JEDEC Standard A103	[1]	100	-		years
I_{latch}	I/O latch-up current	JEDEC Standard 78	[1]	100 + I_{DD}	-		mA
V_{IL}	LOW-level input voltage			–0.5	-	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	6.0	V
V_{OL}	LOW-level output voltage	V_{DD} = 4.5 V	[2][3][4]		-		
		I_{OL} = 3.2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	V_{DD} = 2.7 V, ports 1, 2, 3	[5]		-		
		I_{OH} = –20 µA		V_{DD} – 0.7	-	-	V
		V_{DD} = 4.5 V, ports 1, 2, 3	[5]		-		
		I_{OH} = –30 µA		V_{DD} – 0.7	-	-	V
		V_{DD} = 4.5 V, Port 0 in External Bus mode, ALE, $\overline{PSEN}$			-		
		I_{OH} = –3.2 mA		V_{DD} – 0.7	-	-	V
I_{IL}	LOW-level input current	V_I = 0.4 V, ports 1, 2, 3		–1	-	–50	µA
I_{THL}	HIGH-LOW transition current	V_I = 2 V, ports 1, 2, 3	[6]	-	-	–650	µA
I_{LI}	input leakage current	0.45 V < V_I < V_{DD} – 0.3 V, port 0		-	-	±10	µA

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Table 44. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{pd}	pull-down resistance	on pin RST		40	-	225	kΩ
C_{iss}	input capacitance	@ 1 MHz, T_{amb} = 25 °C, V_I = 0 V	[7]	-	-	15	pF
$I_{DD(oper)}$	operating supply current	f_{osc} = 12 MHz		-	-	3	mA
		f_{osc} = 40 MHz		-	-	7	mA
$I_{DD(idle)}$	Idle mode supply current	f_{osc} = 12 MHz		-	-	1.7	mA
		f_{osc} = 40 MHz		-	-	3	mA
$I_{DD(pd)}$	Power-down mode supply current	minimum V_{DD} = 2 V		-	-	15	µA

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

a) Maximum I_{OL} per 8-bit port: 26 mA

b) Maximum I_{OL} total for all outputs: 71 mA

c) If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[3] Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

[4] Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[5] Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{DD} − 0.7 specification when the address bits are stabilizing.

[6] Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_I is approximately 2 V.

[7] Pin capacitance is characterized but not tested. $\overline{EA}$ = 25 pF (max).

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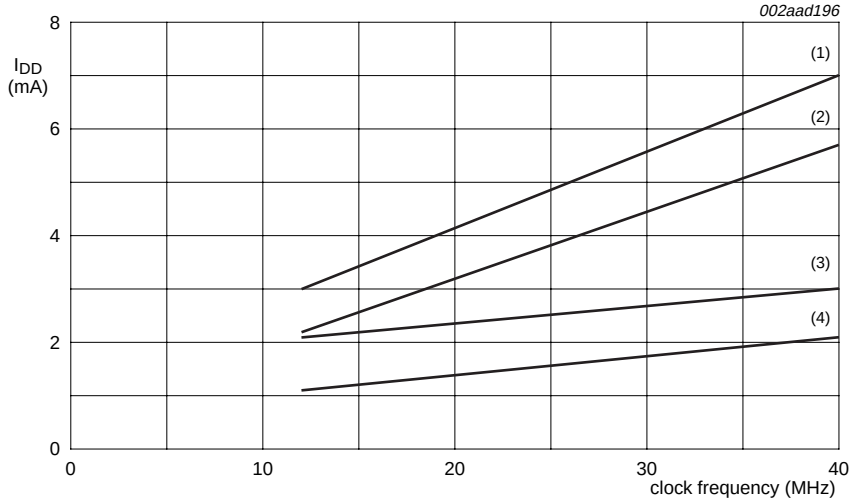

(1) Maximum $I_{DD(oper)}$

(2) Typical $I_{DD(oper)}$

(3) Maximum $I_{DD(idle)}$

(4) Typical $I_{DD(idle)}$

Fig 20. I_{DD} vs. frequency

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9. Dynamic characteristics

Table 45. Dynamic characteristics

Over operating conditions: load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{osc}	oscillator frequency	12-clock mode	0	40	MHz
		6-clock mode	0	20	MHz
t_{LHLL}	ALE pulse width		$2T_{cy(clk)} - 15$	-	ns
t_{AVLL}	address valid to ALE LOW time		$T_{cy(clk)} - 15$	-	ns
t_{LLAX}	address hold after ALE LOW time		$T_{cy(clk)} - 15$	-	ns
t_{LLIV}	ALE LOW to valid instruction in time		-	$4T_{cy(clk)} - 45$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW time		$T_{cy(clk)} - 15$	-	ns
t_{PLPH}	$\overline{PSEN}$ pulse width		$3T_{cy(clk)} - 15$	-	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in time		-	$3T_{cy(clk)} - 55$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$ time		0	-	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$ time		-	$T_{cy(clk)} - 20$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid time		$T_{cy(clk)} - 8$	-	ns
t_{AVIV}	address to valid instruction in time		-	$5T_{cy(clk)} - 60$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float time		-	10	ns
t_{RLRH}	$\overline{RD}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	ns
t_{WLWH}	$\overline{WR}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in time		-	$5T_{cy(clk)} - 50$	ns
t_{RHDX}	data hold after $\overline{RD}$ time		0	-	ns
t_{RHDZ}	data float after $\overline{RD}$ time		-	$2T_{cy(clk)} - 12$	ns
t_{LLDV}	ALE LOW to valid data in time		-	$8T_{cy(clk)} - 50$	ns
t_{AVDV}	address to valid data in time		-	$9T_{cy(clk)} - 75$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW time		$3T_{cy(clk)} - 15$	$3T_{cy(clk)} + 15$	ns
t_{AVWL}	address to $\overline{RD}$ or $\overline{WR}$ LOW time		$4T_{cy(clk)} - 30$	-	ns
t_{WHQX}	data hold after $\overline{WR}$ time		$T_{cy(clk)} - 20$	-	ns
t_{QVWH}	data output valid to $\overline{WR}$ HIGH time		$7T_{cy(clk)} - 50$	-	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float time		-	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH time		$T_{cy(clk)} - 15$	$T_{cy(clk)} + 15$	ns

[1] $T_{cy(clk)} = 1/f_{osc}$.

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9.1 Explanation of symbols

Each timing symbol has 5 characters. The first character is always a 't' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A — Address

C — Clock

D — Input data

H — Logic level HIGH

I — Instruction (program memory contents)

L — Logic level LOW or ALE

P — $\overline{\text{PSEN}}$

Q — Output data

R — $\overline{\text{RD}}$ signal

T — Time

V — Valid

W — $\overline{\text{WR}}$ signal

X — No longer a valid logic level

Z — High impedance (Float)

Example:

t_{AVLL} = Address valid to ALE LOW time

t_{LLPL} = ALE LOW to $\overline{\text{PSEN}}$ LOW time

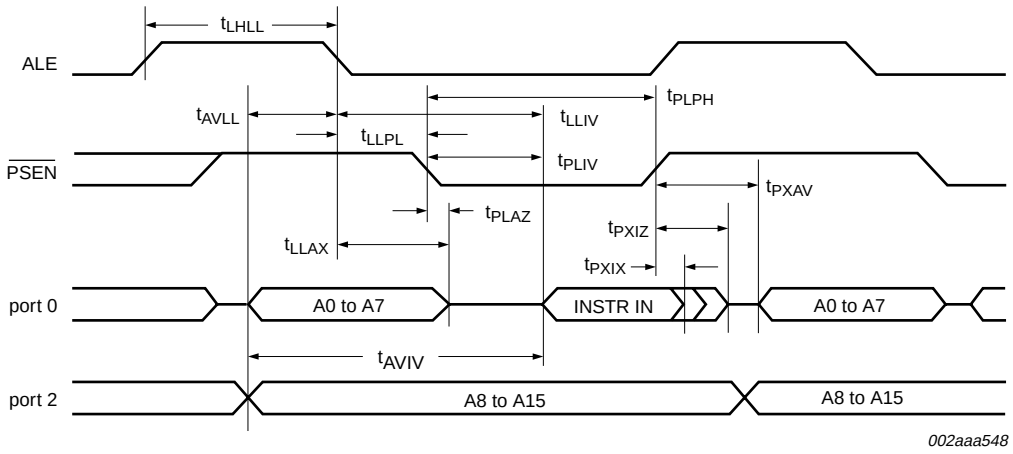

Fig 21. External program memory read cycle

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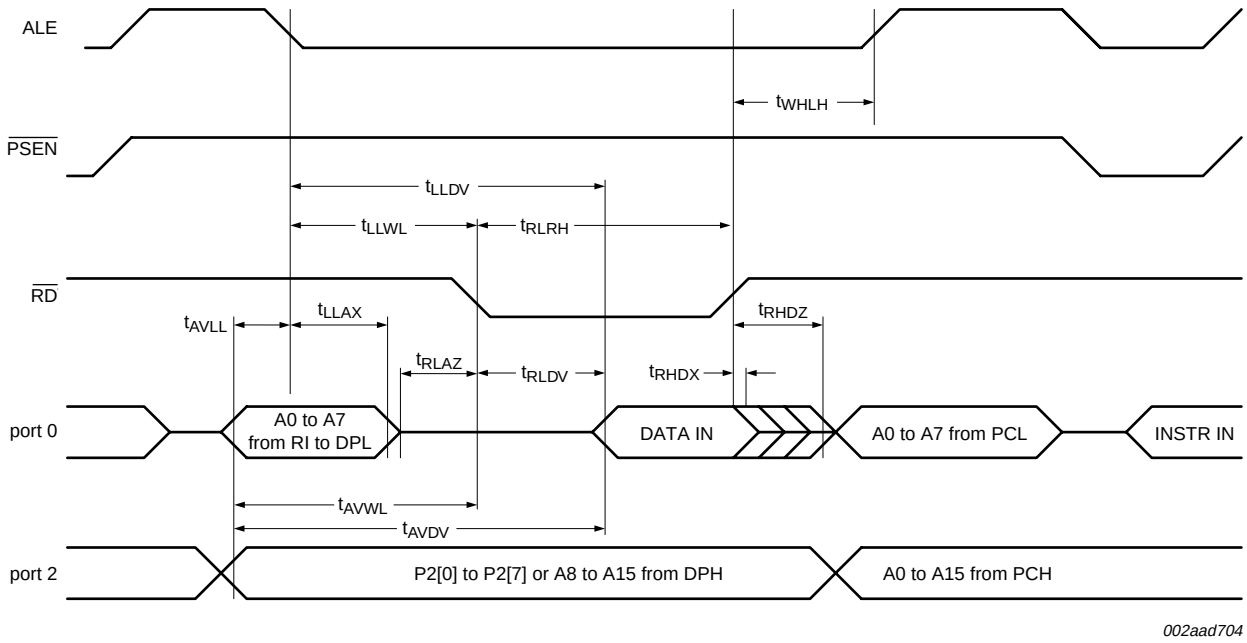

Fig 22. External data memory read cycle

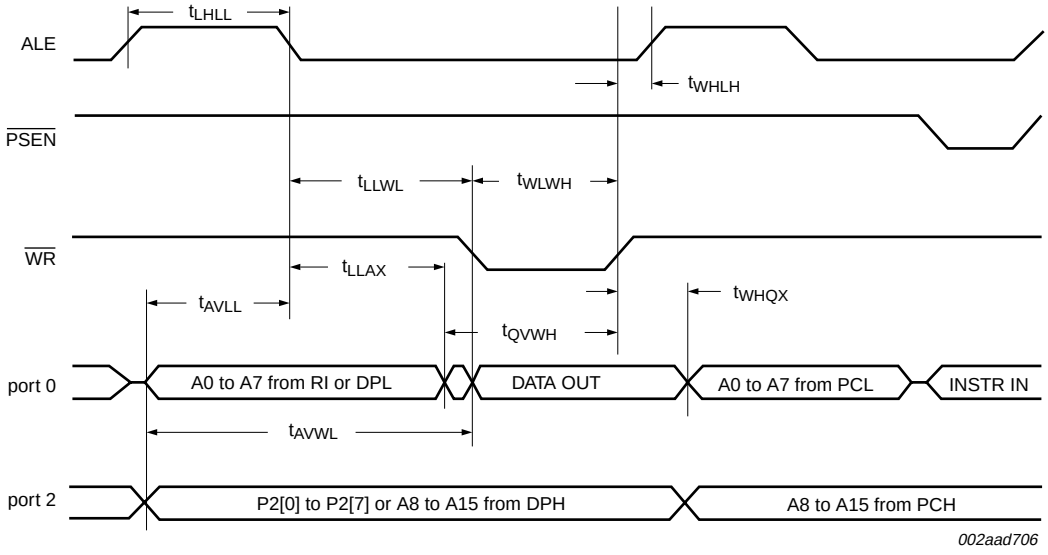

Fig 23. External data memory write cycle

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Table 46. External clock drive

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	40	MHz
$T_{cy(clk)}$	clock cycle time	25	-	-	-	ns
t_{CHCX}	clock HIGH time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	10	-	-	ns
t_{CHCL}	clock fall time	-	10	-	-	ns

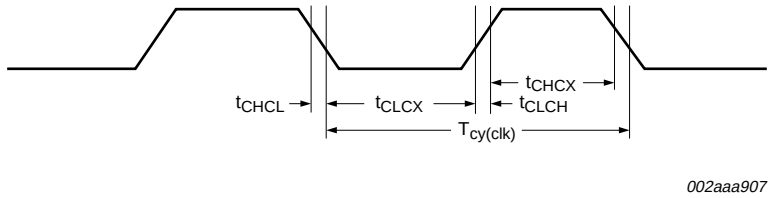

Fig 24. External clock drive waveform (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

Table 47. Serial port timing

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	0.3	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	117	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	0	-	$2T_{cy(clk)} - 15$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	117	-	$10T_{cy(clk)} - 133$	ns

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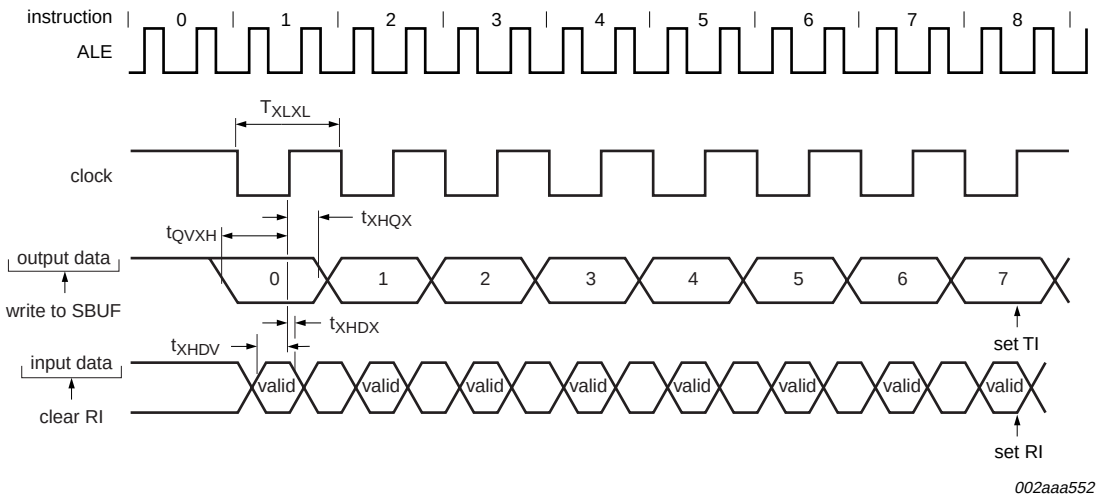


Fig 25. Shift register mode timing waveforms

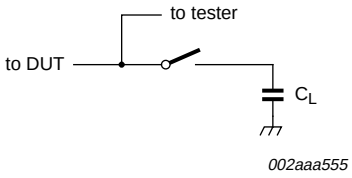
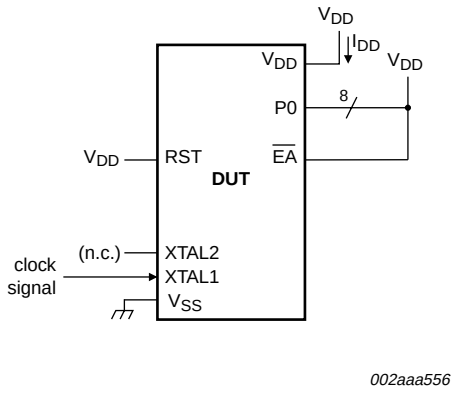


Fig 26. Test load example



All other pins disconnected

Fig 27. I_{DD} test condition, active mode

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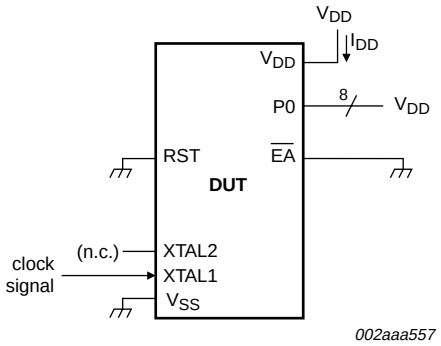
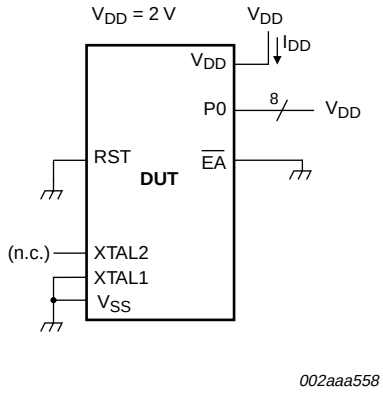


All other pins disconnected

Fig 28. I_{DD} test condition, Idle mode



All other pins disconnected

Fig 29. I_{DD} test condition, Power-down mode

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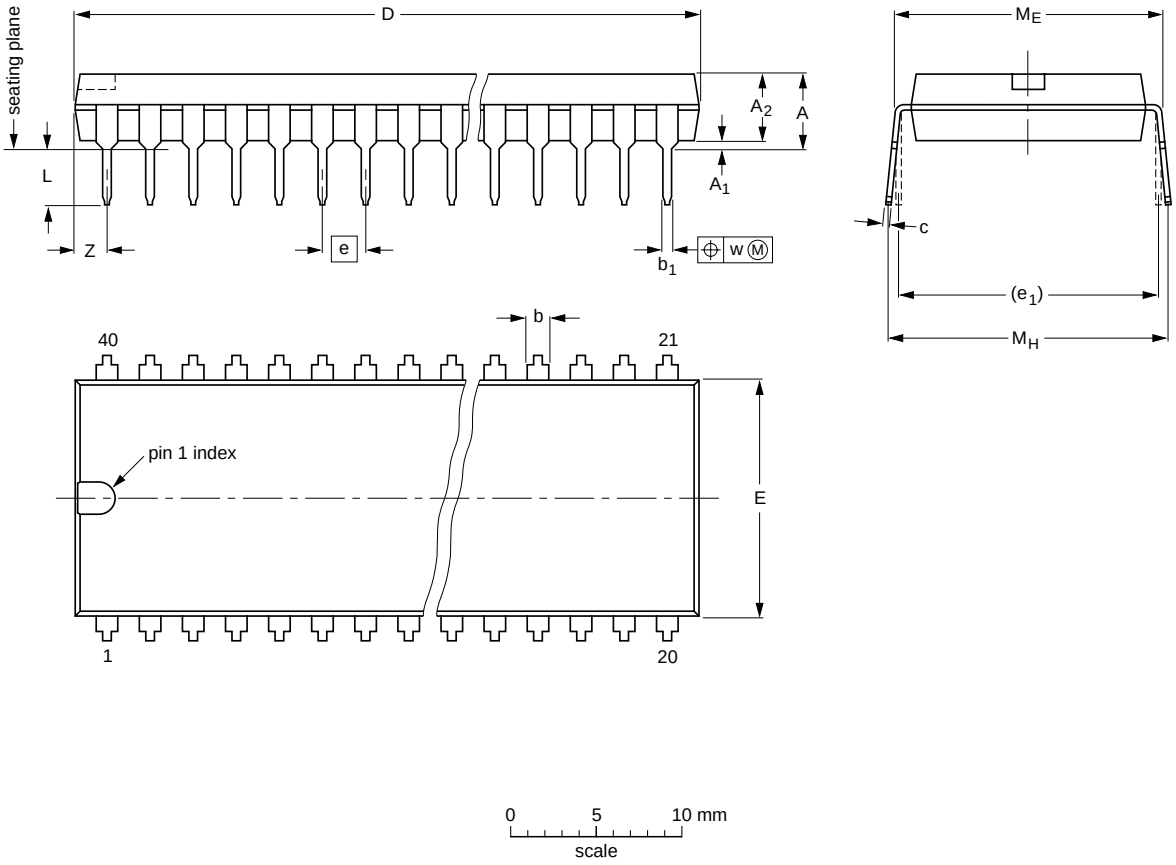
10. Package outline

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4	1.70 1.14	0.53 0.38	0.36 0.23	52.5 51.5	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.02	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.1	0.6	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT129-1	051G08	MO-015	SC-511-40			~~99-12-27~~ 03-02-13

Fig 30. Package outline SOT129-1 (DIP40)

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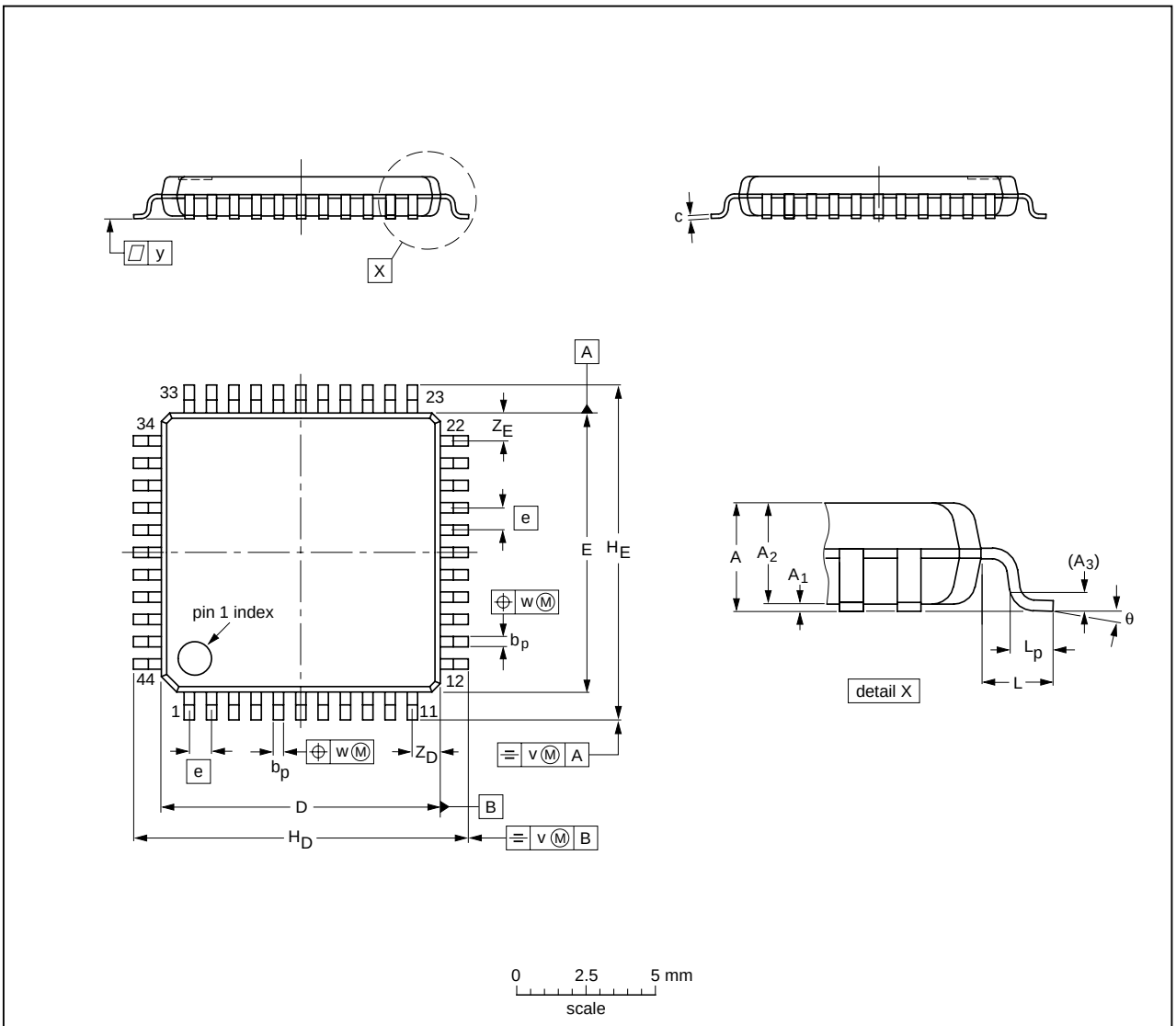
LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm **SOT389-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.14 0.85	1.14 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT389-1	136E08	MS-026				~~00-01-19~~ 02-06-07

Fig 31. Package outline SOT389-1 (LQFP44)

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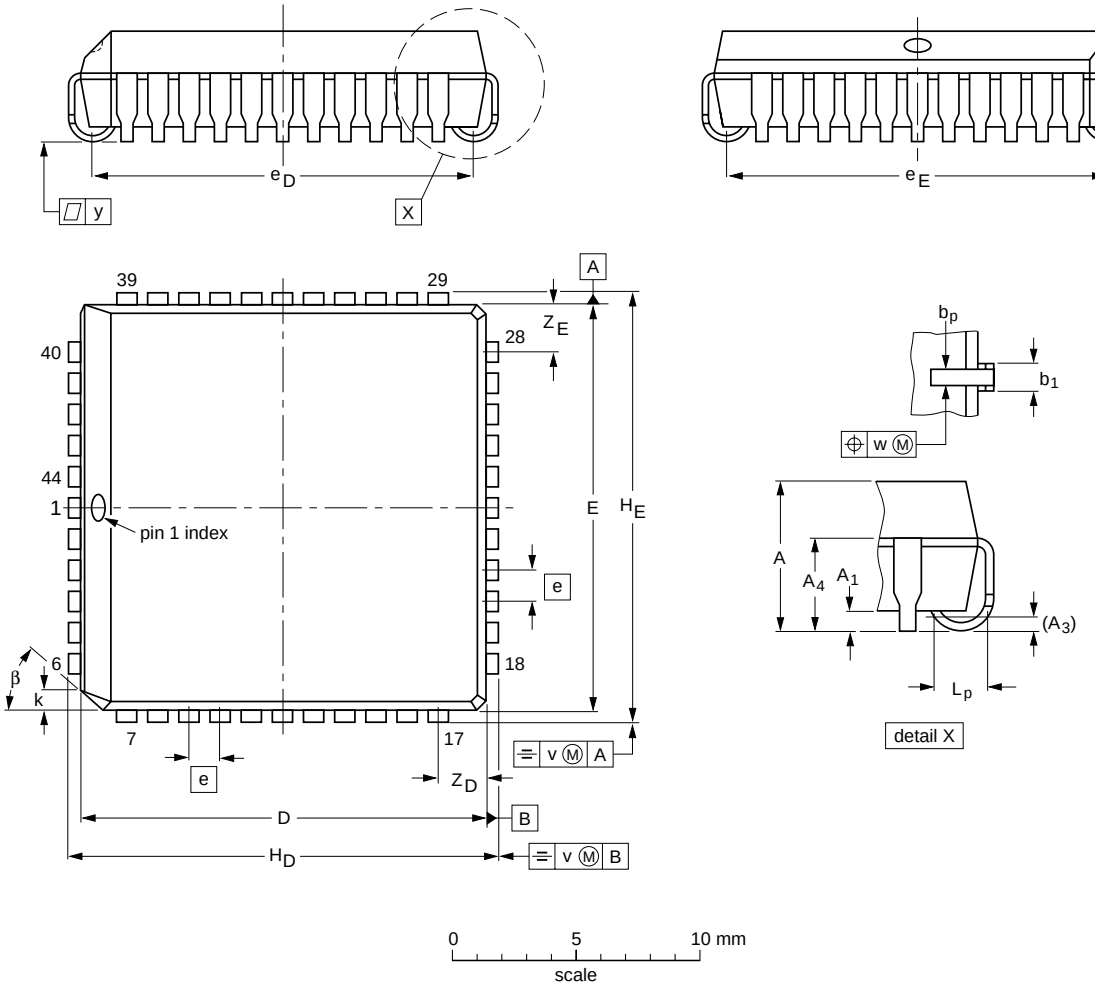
PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 32. Package outline SOT187-2 (PLCC44)

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11. Abbreviations

Table 48. Acronym list

Acronym	Description
CRC	Cyclic Redundancy Check
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
IAP	In-Application Programming
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PWM	Pulse Width Modulator
RC	Resistance-Capacitance
RETI	Return From Interrupt
SFR	Special Function Register
UART	Universal Asynchronous Receiver/Transmitter

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12. Revision history

Table 49. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89V52X2_3	20090504	Product data sheet	-	P89V52X2_2
Modifications:	• Table 44: replaced $V_{th(HL)}$ with V_{IL} • Table 44: V_{IH}, removed 'XTAL1, RST' from conditions			
P89V52X2_2	20080522	Product data sheet	-	P89V52X2_1
Modifications:	• Table 3: added registers FMCON, FMDATA, FMADRH and FMADRL • Table 33: changed address of register FMCON to F4H • Figure 1: corrected XTAL pin names • Figure 21: deleted superfluous arrows • Figure 22: added right arrow to t_{RLRH} • Figure 23: deleted unwanted lines from DATA OUT			
P89V52X2_1	20080403	Product data sheet	-	-

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