



# P3A9606JK

Dual bidirectional I3C/I<sup>2</sup>C-bus and SPI voltage-level translator

Rev. 2.0 — 4 January 2023

Product data sheet

## 1 General description

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The P3A9606JK is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation for traditional I<sup>2</sup>C-bus/SMBus applications, 12.5 MHz I3C-bus applications and also higher speed SPI applications (with two devices). It features two 1-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins (V<sub>CCA</sub> and V<sub>CCB</sub>). V<sub>CCA</sub> can be supplied at any voltage between 0.72 V and 1.98 V and V<sub>CCB</sub> can be supplied at any voltage between 0.72 V and 1.98 V, making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V and 1.8 V). V<sub>CCA</sub> must be ≤ V<sub>CCB</sub> to ensure proper operation.

P3A9606JK can be used for both open drain as well as push-pull application which allows for level translation applications using I3C, I<sup>2</sup>C and SPI protocols.

Pins An are referenced to V<sub>CCA</sub> and pins Bn are referenced to V<sub>CCB</sub>. The active HIGH OE pin is referenced to V<sub>CCA</sub> and controllable by a signal in either V<sub>CCA</sub> or V<sub>CCB</sub> domain. A LOW level at pin OE causes the outputs to be in a high-impedance OFF-state. This device is fully specified for partial power-down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2 Features and benefits

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- Wide supply voltage range:
  - V<sub>CCA</sub>: 0.72 V to 1.98 V and V<sub>CCB</sub>: 0.72 V to 1.98 V; V<sub>CCA</sub> ≤ V<sub>CCB</sub>
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 1.98 V and are overvoltage tolerant to 1.98 V
- Provided voltage level translation for I3C, I<sup>2</sup>C-bus, SMBus and SPI devices
- ESD protection:
  - HBM JESD22-A114E Class 2 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Available in X2SON8 package
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



### 3 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
P3A9606JK	Tx <sup>[1]</sup>	X2SON8	super thin small outline package, no leads; 8 terminals; 0.35 mm pitch; 1.35 mm x 1.0 mm x 0.32 mm body	SOT2015-1

[1] "x" changes based on date code.

#### 3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3A9606JK	P3A9606JKZ	X2SON8	Reel 13" Q1/T1 *standard mark SMD with SSB <sup>[1]</sup>	20000	T <sub>amb</sub> = -40 °C to +125 °C

[1] This packing method uses a Static Shielding Bag (SSB) solution. Material should be kept in the sealed bag between uses.

### 4 Block diagram

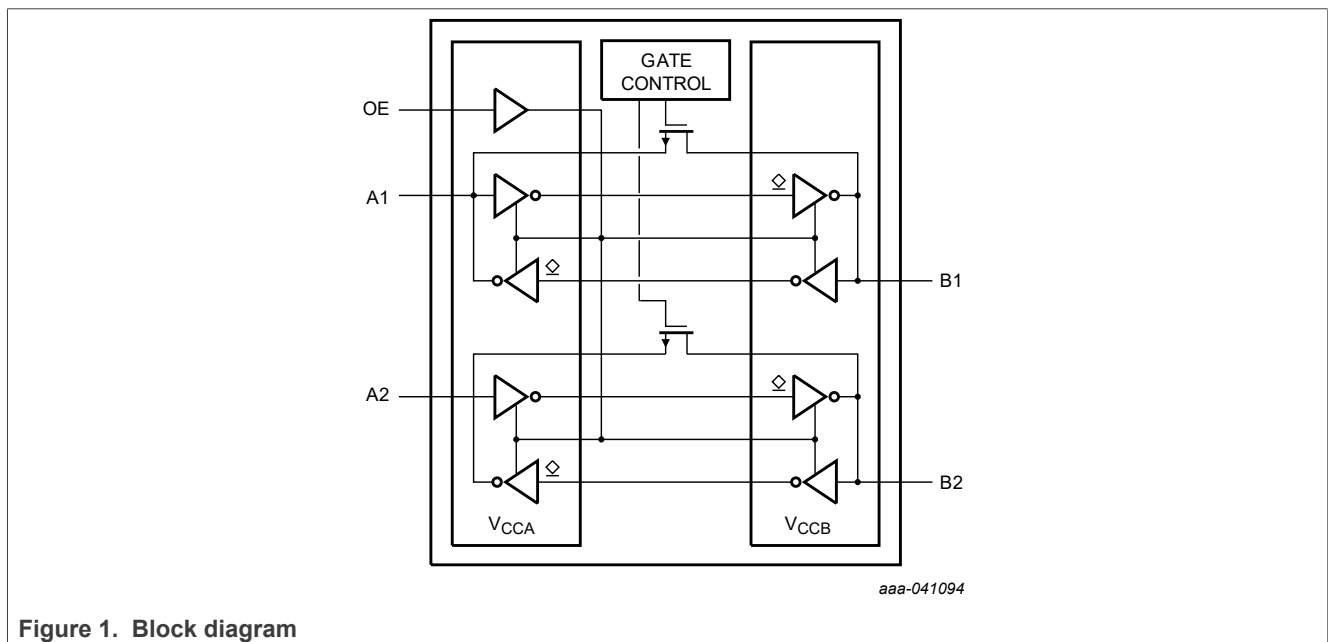
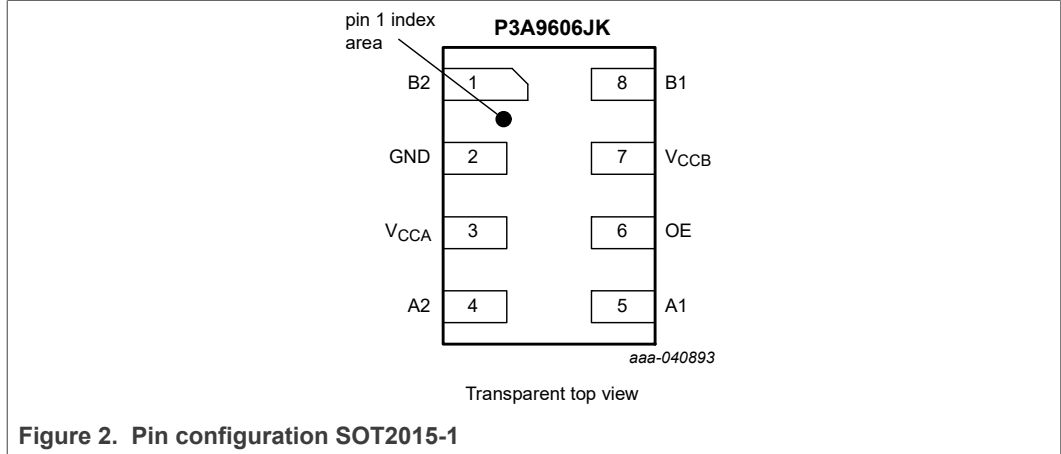


Figure 1. Block diagram

## 5 Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B2, B1	1, 8	B port - data input or output (referenced to V <sub>CCB</sub> )
GND	2	ground (0 V)
V <sub>CCA</sub>	3	supply voltage A
A2, A1	4, 5	A port - data input or output (referenced to V <sub>CCA</sub> )
OE	6	output enable input (active HIGH, referenced to V <sub>CCA</sub> ); signal can be from V <sub>CCA</sub> or V <sub>CCB</sub> domain
V <sub>CCB</sub>	7	supply voltage B

## 6 Functional description

Table 4. Function table <sup>[1]</sup>

Supply voltage		Input	Input/output
V <sub>CCA</sub>	V <sub>CCB</sub>	OE <sup>[2]</sup>	
0.72 V to 1.98 V	0.72 V to 1.98 V	L	disconnected
0.72 V to 1.98 V	0.72 V to 1.98 V	H	A1 = B1; A2 = B2
GND <sup>[3]</sup>	GND <sup>[3]</sup>	X	disconnected

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

[2] V<sub>IL</sub> and V<sub>IH</sub> are referenced to V<sub>CCA</sub>. The OE can be controlled by an external device that is powered by either V<sub>CCA</sub> or V<sub>CCB</sub>. As V<sub>CCB</sub> is required to be greater than V<sub>CCA</sub>, the OE pin has been designed to withstand a voltage equal to V<sub>CCB</sub> (up to 1.98 V per recommended functional voltage range).

[3] When either V<sub>CCA</sub> or V<sub>CCB</sub> is at GND level, the device goes into Power-down mode.

## 7 Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCA</sub>	supply voltage A	V <sub>CCA</sub> ≤ V <sub>CCB</sub>	-0.5	2.5	V
V <sub>CCB</sub>	supply voltage B	V <sub>CCA</sub> ≤ V <sub>CCB</sub>	-0.5	2.5	V
V <sub>I</sub>	input voltage	A port, B port and OE	<sup>[1]</sup> -0.5	2.5	V
V <sub>O</sub>	output voltage	Active mode	<sup>[1][2][3]</sup> -0.5	V <sub>CCO</sub> + 0.25	V
		Power-down or 3-state mode	<sup>[1]</sup> -0.5	2.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CCO</sub>	<sup>[2]</sup> -	±50	mA
I <sub>CC</sub>	supply current	I <sub>CC(A)</sub> or I <sub>CC(B)</sub>	-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	-	125	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V<sub>CCO</sub> is the supply voltage associated with the output.

[3] V<sub>CCO</sub> + 0.25 V should not exceed 2.5 V.

## 8 Recommended operating conditions

**Table 6. Recommended operating conditions<sup>[1]</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCA</sub>	supply voltage A	V <sub>CCA</sub> ≤ V <sub>CCB</sub>	0.72	1.98	V
V <sub>CCB</sub>	supply voltage B	V <sub>CCA</sub> ≤ V <sub>CCB</sub>	0.72	1.98	V
V <sub>I</sub>	input voltage	A port, B port and OE	0	1.98	V
V <sub>O</sub>	output voltage	Power-down or 3-state mode; V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V			
		A port	0	1.98	V
		B port	0	1.98	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
T <sub>J</sub>	junction temperature <sup>[2]</sup>		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V	-	<5.3	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V<sub>CC1</sub> or both at GND.

[2] The T<sub>J</sub> limits shall be supported by proper thermal PCB design taking the power consumption and the thermal resistance as listed in [Table 7](#) into account.

## 9 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Value (typ)	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient	X2SON8 package	114.9	°C/W
$\Psi_{(j-t)}$	Junction to top characterization	X2SON8 package	1.6	°C/W

## 10 Static characteristics

Table 8. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	A port; $V_{CCA} = 1.2\text{ V}$ ; $I_O = -15\text{ }\mu\text{A}$	-	1.05	-	V
$V_{OL}$	LOW-level output voltage	A port; $V_{CCA} = 1.2\text{ V}$ ; $I_O = 20\text{ }\mu\text{A}$	-	0.09	-	V
$I_I$	input leakage current	OE input; $V_I = 0\text{ V}$ or $1.98\text{ V}$ ; $V_{CCA} = 0.72\text{ V}$ to $1.98\text{ V}$ ; $V_{CCB} = 0.72\text{ V}$ to $1.98\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V}$ to $V_{CCO}$ ; $V_{CCA} = 0.72\text{ V}$ to $1.98\text{ V}$ ; $V_{CCB} = 0.72\text{ V}$ to $1.98\text{ V}$	[1]	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V}$ to $1.98\text{ V}$ ; $V_{CCA} = 0\text{ V}$ ; $V_{CCB} = 0\text{ V}$ to $1.98\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V}$ to $1.98\text{ V}$ ; $V_{CCB} = 0\text{ V}$ ; $V_{CCA} = 0\text{ V}$ to $1.98\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 0\text{ V}$ or $V_{CCI}$ ; $I_O = 0\text{ A}$	[2]			
		$I_{CC(A)}$ ; $V_{CCA} = 0.72\text{ V}$ ; $V_{CCB} = 0.72\text{ V}$ to $1.98\text{ V}$	-	0.05	-	$\mu\text{A}$
		$I_{CC(B)}$ ; $V_{CCA} = 0.72\text{ V}$ ; $V_{CCB} = 0.72\text{ V}$ to $1.98\text{ V}$	-	3.3	-	$\mu\text{A}$
		$I_{CC(A)} + I_{CC(B)}$ ; $V_{CCA} = 0.72\text{ V}$ ; $V_{CCB} = 0.72\text{ V}$ to $1.98\text{ V}$	-	3.5	-	$\mu\text{A}$
$C_I$	input capacitance	OE input; $V_{CCA} = 0.72\text{ V}$ to $1.98\text{ V}$ ; $V_{CCB} = 0.72\text{ V}$ to $1.98\text{ V}$	-	1.0	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CCA} = 0.72\text{ V}$ to $1.98\text{ V}$ ; $V_{CCB} = 0.72\text{ V}$ to $1.98\text{ V}$	-	4.0	-	pF
		B port; $V_{CCA} = 0.72\text{ V}$ to $1.98\text{ V}$ ; $V_{CCB} = 0.72\text{ V}$ to $1.98\text{ V}$	-	4.0	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output.

[2]  $V_{CCI}$  is the supply voltage associated with the input.

Dual bidirectional I<sup>3</sup>C/I<sup>2</sup>C-bus and SPI voltage-level translator

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).<sup>[1]</sup>

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Max	Min	Max		
V <sub>IH</sub>	HIGH-level input voltage	A port or B port						
		V <sub>CCA</sub> = 0.72 V to 0.9 V; V <sub>CCB</sub> = 0.72 V to 0.9 V	<sup>[1]</sup>	0.75V <sub>CCI</sub>	-	0.75V <sub>CCI</sub>	-	V
		V <sub>CCA</sub> = 0.9 V to 1.98 V; V <sub>CCB</sub> = 0.9 V to 1.98 V	<sup>[1]</sup>	0.7V <sub>CCI</sub>	-	0.7V <sub>CCI</sub>	-	V
		OE input						
		V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V		0.65V <sub>CCA</sub>	-	0.65V <sub>CCA</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	A or B port						
		V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V		-	0.3V <sub>CCA</sub>	-	0.3V <sub>CCA</sub>	V
		OE input						
		V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V		-	0.3V <sub>CCA</sub>	-	0.3V <sub>CCA</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub> = -15 μA	<sup>[2]</sup> <sup>[3]</sup>					
		A port; V <sub>CCA</sub> = 0.72 V to 1.98 V		V <sub>CCO</sub> - 0.195	-	V <sub>CCO</sub> - 0.195	-	V
		B port; V <sub>CCB</sub> = 0.72 V to 1.98 V		V <sub>CCO</sub> - 0.195	-	V <sub>CCO</sub> - 0.195	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = 20 μA	<sup>[2]</sup>					
		A port; V <sub>CCA</sub> = 0.72 V to 1.98 V		-	0.3	-	0.3	V
		B port; V <sub>CCB</sub> = 0.72 V to 1.98 V		-	0.3	-	0.3	V
I <sub>I</sub>	input leakage current	OE input; V <sub>I</sub> = 0 V to 1.98 V; V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V		-	±2	-	±5	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V	<sup>[2]</sup>	-	±2	-	±10	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 1.98 V; V <sub>CCA</sub> = 0 V; V <sub>CCB</sub> = 0 V to 1.98 V		-	±2	-	±10	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 1.98 V; V <sub>CCB</sub> = 0 V; V <sub>CCA</sub> = 0 V to 1.98 V		-	±2	-	±10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A	<sup>[1]</sup>					
		I <sub>CC(A)</sub> OE = LOW; V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V		-	5	-	15	μA

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Table 9. Static characteristics...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).<sup>[1]</sup>

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
		OE = HIGH; V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V	-	6	-	20	μA
		V <sub>CCA</sub> = 1.98 V; V <sub>CCB</sub> = 0 V	-	3.5	-	15	μA
		V <sub>CCA</sub> = 0 V; V <sub>CCB</sub> = 1.98 V	-	-2	-	-15	μA
		I <sub>CC(B)</sub>					
		OE = LOW; V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V	-	8	-	29	μA
		OE = HIGH; V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V	-	11	-	36	μA
		V <sub>CCA</sub> = 1.98 V; V <sub>CCB</sub> = 0 V	-	-2	-	-15	μA
		V <sub>CCA</sub> = 0 V; V <sub>CCB</sub> = 1.98 V	-	6	-	20	μA
		I <sub>CC(A)</sub> + I <sub>CC(B)</sub>					
		OE = LOW; V <sub>CCA</sub> = 0.72 V to 1.98 V; V <sub>CCB</sub> = 0.72 V to 1.98 V	-	16	-	56	μA

[1] V<sub>CCI</sub> is the supply voltage associated with the input.

[2] V<sub>CCO</sub> is the supply voltage associated with the output.

[3] The V<sub>OH</sub> min can be calculated by V<sub>CCO</sub> - I<sub>O</sub> x 10 kΩ x 1.3. The 1.3 factor is for the design margin. In this case, I<sub>O</sub> = 15 μA and R<sub>UP</sub> = 10 kΩ then V<sub>OH</sub> min = V<sub>CCO</sub> - 0.195 V.

## 11 Dynamic characteristics

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C <sup>[1]</sup>

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 4](#); for waveform see [Figure 3](#).

Symbol	Parameter	Conditions	V <sub>CCB</sub>			V <sub>CCB</sub>			Unit
			1.2 V ± 10 %			1.8 V ± 10 %			
			Min	Typ	Max	Min	Typ	Max	
V <sub>CCA</sub> = 0.8 V ± 10 %									
t <sub>pd</sub>	propagation delay	A to B; C <sub>L</sub> = 15 pF	2.1	5.6	7.7	1.7	3.9	5.3	ns
		B to A; C <sub>L</sub> = 15 pF	1.2	10.6	19.9	0.5	9.6	17.2	ns
t <sub>en</sub>	enable time	OE to A, B; C <sub>L</sub> = 15 pF	16	125	150	16	120	160	ns
t <sub>dis</sub> <sup>[2]</sup>	disable time	OE to A; no external load <sup>[3]</sup>	10		25	10		25	ns
		OE to B; no external load <sup>[3]</sup>	10		25	10		25	ns
		OE to A; C <sub>L</sub> = 15 pF			50			50	ns
		OE to B; C <sub>L</sub> = 15 pF			50			50	ns
t <sub>t</sub>	transition time	A port; C <sub>L</sub> = 15 pF	2.1	8.5	17.5	1.5	9	15.4	ns
		B port; C <sub>L</sub> = 15 pF	1.1	4	5.8	0.7	1.5	2.1	ns
t <sub>sk(o)</sub>	output skew time	delta between channels <sup>[4]</sup>	0	0.2	0.4	0	0.2	0.4	ns
t <sub>w</sub>	pulse width	data inputs	37			37			ns
f <sub>data</sub>	data rate		0.064		26	0.064		26	Mbps

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

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- [2] Guaranteed by design.
- [3] Delay between OE going LOW and when the outputs are actually disabled.
- [4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

**Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 4](#); for waveform see [Figure 3](#).

Symbol	Parameter	Conditions	V <sub>CCB</sub>			V <sub>CCB</sub>			Unit
			1.2 V ± 10 %			1.8 V ± 10 %			
			Min	Typ	Max	Min	Typ	Max	
V <sub>CCA</sub> = 1.2 V ± 10 %									
t <sub>pd</sub>	propagation delay	A to B; C <sub>L</sub> = 15 pF	1.5	4.5	6.1	1.0	2.5	3.5	ns
		B to A; C <sub>L</sub> = 15 pF	1.1	3.9	5.3	0.6	2.8	3.9	ns
t <sub>pdC</sub>	propagation delay	A to B; C <sub>L</sub> = 80 pF	NA	NA	NA	2.5	4.9	7	ns
		B to A; C <sub>L</sub> = 30 pF	NA	NA	NA	0.9	3.4	5	ns
t <sub>en</sub>	enable time	OE to A, B; C <sub>L</sub> = 15 pF	10	50	100	10	50	100	ns
t <sub>dis</sub> [2]	disable time	OE to A; no external load [3]	10		25	10		25	ns
		OE to B; no external load [3]	10		25	10		25	ns
		OE to A; C <sub>L</sub> = 15 pF			50	-		50	ns
		OE to B; C <sub>L</sub> = 15 pF			50	-		50	ns
t <sub>t</sub>	transition time	A port; C <sub>L</sub> = 15 pF	0.8	2.6	3.5	0.6	1.5	2.5	ns
		B port; C <sub>L</sub> = 15 pF	1.1	3.6	5.1	0.6	1.3	2.2	ns
t <sub>tc</sub>	transition time	A port; C <sub>L</sub> = 30 pF	NA	NA	NA	1.0	2.2	3.6	ns
		B port; C <sub>L</sub> = 80 pF	NA	NA	NA	2.5	4.3	6.3	ns
t <sub>sk(o)</sub>	output skew time	delta between channels [4]	0.0	0.1	0.2	0.0	0.1	0.3	ns
t <sub>W</sub>	pulse width	data inputs	15			13.5			ns
f <sub>data</sub>	data rate		0.064		52	0.064		52	Mbps

- [1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [2] Guaranteed by design.
- [3] Delay between OE going LOW and when the outputs are actually disabled.
- [4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

**Table 12. Dynamic characteristics for temperature range -40 °C to +85 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 4](#); for waveforms see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	V <sub>CCB</sub>			Unit
			1.8 V ± 10 %			
			Min	Typ	Max	
V <sub>CCA</sub> = 1.8 V ± 10 %						
t <sub>pd</sub>	propagation delay	A to B; C <sub>L</sub> = 15 pF	1	2.5	3.4	ns
		B to A; C <sub>L</sub> = 15 pF	0.7	2.3	3	ns
t <sub>en</sub>	enable time	OE to A, B; C <sub>L</sub> = 15 pF	8	25	50	ns
t <sub>dis</sub> [2]	disable time	OE to A; no external load [3]	10		25	ns
		OE to B; no external load [3]	10		25	ns
		OE to A; C <sub>L</sub> = 15 pF			50	ns
		OE to B; C <sub>L</sub> = 15 pF			50	ns
t <sub>t</sub>	transition time	A port; C <sub>L</sub> = 15 pF	0.5	1.2	1.7	ns
		B port; C <sub>L</sub> = 15 pF	0.7	1.7	2.5	ns
t <sub>sk(o)</sub>	output skew time	delta between channels [4]	0	0.1	0.2	ns
t <sub>W</sub>	pulse width	data inputs	13.5			ns
f <sub>data</sub>	data rate		0.064		52	Mbps

- [1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [2] Guaranteed by design.
- [3] Delay between OE going LOW and when the outputs are actually disabled.
- [4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.



Dual bidirectional I3C/I<sup>2</sup>C-bus and SPI voltage-level translator

**Table 13. Dynamic characteristics for temperature range -40 °C to +125 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 4](#); for waveform see [Figure 3](#).

Symbol	Parameter	Conditions	V <sub>CCB</sub>			V <sub>CCB</sub>			Unit
			1.2 V ± 10 %			1.8 V ± 10 %			
			Min	Typ	Max	Min	Typ	Max	
V <sub>CCA</sub> = 0.8 V ± 10 %									
t <sub>pd</sub>	propagation delay	A to B; C <sub>L</sub> = 15 pF	2.1	5.6	7.7	1.7	3.9	5.3	ns
		B to A; C <sub>L</sub> = 15 pF	1.2	10.6	19.9	0.5	9.6	17.2	ns
t <sub>en</sub>	enable time	OE to A, B; C <sub>L</sub> = 15 pF	16	125	150	16	120	160	ns
t <sub>dis</sub> [2]	disable time	OE to A; no external load [3]	10		25	10		25	ns
		OE to B; no external load [3]	10		25	10		25	ns
		OE to A; C <sub>L</sub> = 15 pF			50			50	ns
		OE to B; C <sub>L</sub> = 15 pF			50			50	ns
t <sub>t</sub>	transition time	A port; C <sub>L</sub> = 15 pF	2.1	8.5	17.5	1.5	9	15.4	ns
		B port; C <sub>L</sub> = 15 pF	1.1	4	5.8	0.7	1.5	2.1	ns
t <sub>sk(o)</sub>	output skew time	delta between channels [4]	0	0.2	0.4	0	0.2	0.4	ns
t <sub>W</sub>	pulse width	data inputs	37			37			ns
f <sub>data</sub>	data rate		0.064		26	0.064		26	Mbps

- [1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [2] Guaranteed by design.
- [3] Delay between OE going LOW and when the outputs are actually disabled.
- [4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

**Table 14. Dynamic characteristics for temperature range -40 °C to +125 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 4](#); for waveforms see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	V <sub>CCB</sub>			V <sub>CCB</sub>			Unit
			1.2 V ± 10 %			1.8 V ± 10 %			
			Min	Typ	Max	Min	Typ	Max	
V <sub>CCA</sub> = 1.2 V ± 10 %									
t <sub>pd</sub>	propagation delay	A to B; C <sub>L</sub> = 15 pF	1.5	4.5	6.2	1.0	2.5	3.6	ns
		B to A; C <sub>L</sub> = 15 pF	1.1	3.9	5.4	0.6	2.8	4.0	ns
t <sub>pdC</sub>	propagation delay	A to B; C <sub>L</sub> = 80 pF	NA	NA	NA	2.5	4.9	7.4	ns
		B to A; C <sub>L</sub> = 30 pF	NA	NA	NA	0.9	3.4	5.3	ns
t <sub>en</sub>	enable time	OE to A, B; C <sub>L</sub> = 15 pF	10	50	100	10	50	100	ns
t <sub>dis</sub> [2]	disable time	OE to A; no external load [3]	10		25	10		25	ns
		OE to B; no external load [3]	10		25	10		25	ns
		OE to A; C <sub>L</sub> = 15 pF			50	-		50	ns
		OE to B; C <sub>L</sub> = 15 pF			50	-		50	ns
t <sub>t</sub>	transition time	A port; C <sub>L</sub> = 15 pF	0.8	2.6	3.5	0.6	1.5	2.6	ns
		B port; C <sub>L</sub> = 15 pF	1.1	3.6	5.1	0.6	1.3	2.3	ns
t <sub>tc</sub>	transition time	A port; C <sub>L</sub> = 30 pF	NA	NA	NA	1.0	2.2	3.8	ns
		B port; C <sub>L</sub> = 80 pF	NA	NA	NA	2.5	4.3	6.9	ns
t <sub>sk(o)</sub>	output skew time	delta between channels [4]	0	0.1	0.2	0	0.1	0.3	ns
t <sub>W</sub>	pulse width	data inputs	15			13.5			ns
f <sub>data</sub>	data rate		0.064		52	0.064		52	Mbps

- [1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [2] Guaranteed by design.
- [3] Delay between OE going LOW and when the outputs are actually disabled.
- [4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

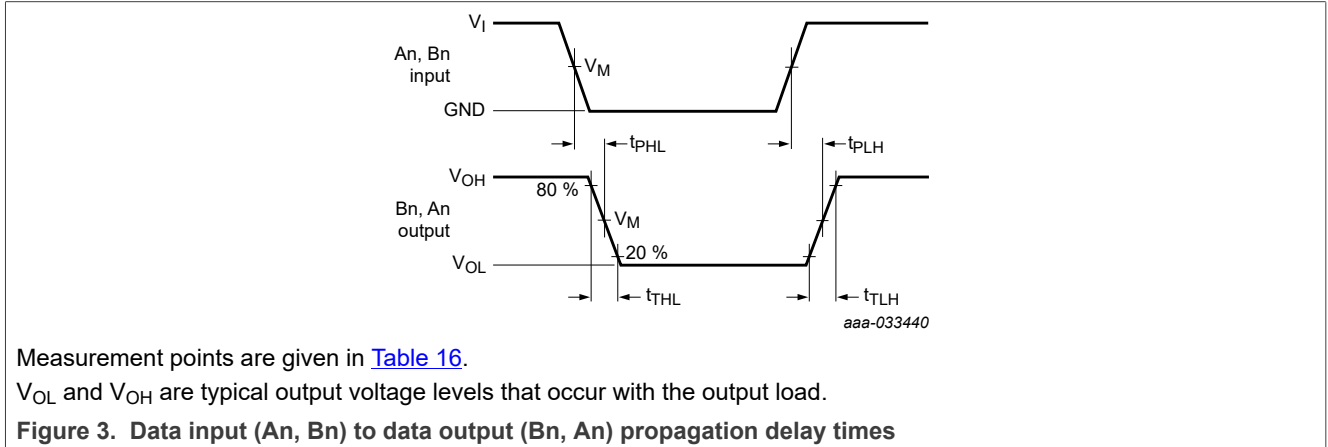
**Table 15. Dynamic characteristics for temperature range -40 °C to +125 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 4](#); for waveforms see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	V <sub>CCB</sub>			Unit
			1.8 V ± 10 %			
			Min	Typ	Max	
V <sub>CCA</sub> = 1.8 V ± 10 %						
t <sub>pd</sub>	propagation delay	A to B; C <sub>L</sub> = 15 pF	1	2.5	3.5	ns
		B to A; C <sub>L</sub> = 15 pF	0.7	2.3	3.1	ns
t <sub>en</sub>	enable time	OE to A, B; C <sub>L</sub> = 15 pF	8	25	50	ns
t <sub>dis</sub> [2]	disable time	OE to A; no external load [3]	10		25	ns
		OE to B; no external load [3]	10		25	ns
		OE to A; C <sub>L</sub> = 15 pF			50	ns
		OE to B; C <sub>L</sub> = 15 pF			50	ns
t <sub>t</sub>	transition time	A port; C <sub>L</sub> = 15 pF	0.5	1.2	1.7	ns
		B port; C <sub>L</sub> = 15 pF	0.7	1.7	2.6	ns
t <sub>sk(o)</sub>	output skew time	delta between channels [4]	0	0.1	0.2	ns
t <sub>W</sub>	pulse width	data inputs	13.5			ns
f <sub>data</sub>	data rate		0.064		52	Mbps

- [1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [2] Guaranteed by design.
- [3] Delay between OE going LOW and when the outputs are actually disabled.
- [4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

## 12 Waveforms



**Table 16. Measurement points**

V<sub>CCI</sub> is the supply voltage associated with the input and V<sub>CCO</sub> is the supply voltage associated with the output.

Supply voltage	Input	Output		
V <sub>CCO</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
0.8 V ± 10 %	0.5V <sub>CCI</sub>	0.5V <sub>CCO</sub>	V <sub>OL</sub> + 0.08 V	V <sub>OH</sub> - 0.08 V
1.2 V ± 10 %	0.5V <sub>CCI</sub>	0.5V <sub>CCO</sub>	V <sub>OL</sub> + 0.12 V	V <sub>OH</sub> - 0.12 V
1.8 V ± 10 %	0.5V <sub>CCI</sub>	0.5V <sub>CCO</sub>	V <sub>OL</sub> + 0.18 V	V <sub>OH</sub> - 0.18 V

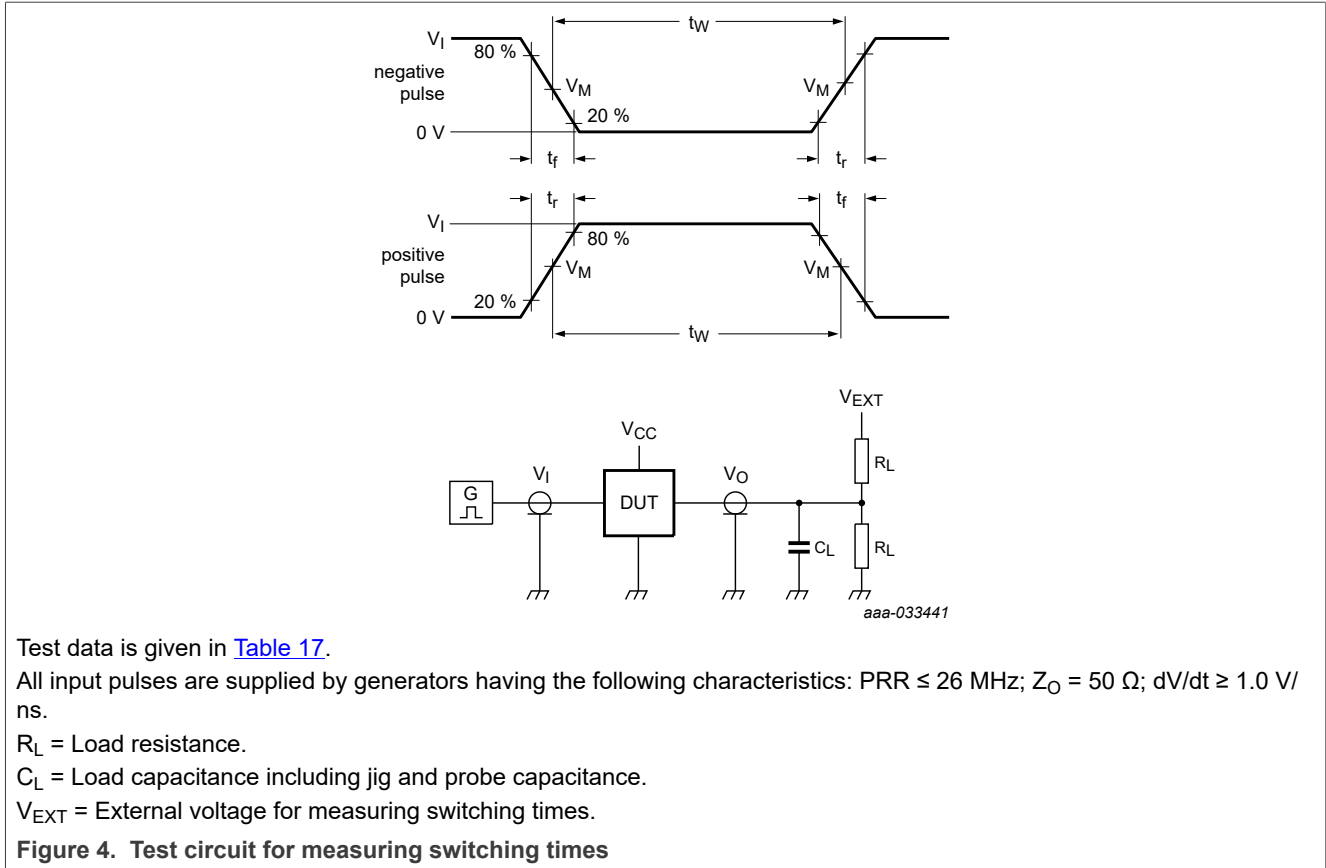


Table 17. Test data

Supply voltage		Input		Load		V <sub>EXT</sub>		
V <sub>CCA</sub>	V <sub>CCB</sub>	V <sub>I</sub> [1]	Δt/ΔV	C <sub>L</sub>	R <sub>L</sub> [2]	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub> [3]
0.72 V to 1.98 V	0.72 V to 1.98 V	V <sub>CCI</sub>	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V <sub>CCO</sub>

[1] V<sub>CCI</sub> is the supply voltage associated with the input.  
 [2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R<sub>L</sub> = 1 MΩ; for measuring enable and disable times, R<sub>L</sub> = 50 kΩ.  
 [3] V<sub>CCO</sub> is the supply voltage associated with the output.

### 13 Application information

#### 13.1 Applications

Voltage level-translation applications. The P3A9606JK can be used to interface between devices or systems operating at different supply voltages. See [Figure 5](#), [Figure 6](#), [Figure 7](#) and [Figure 8](#) for a typical operating circuit using the P3A9606JK.

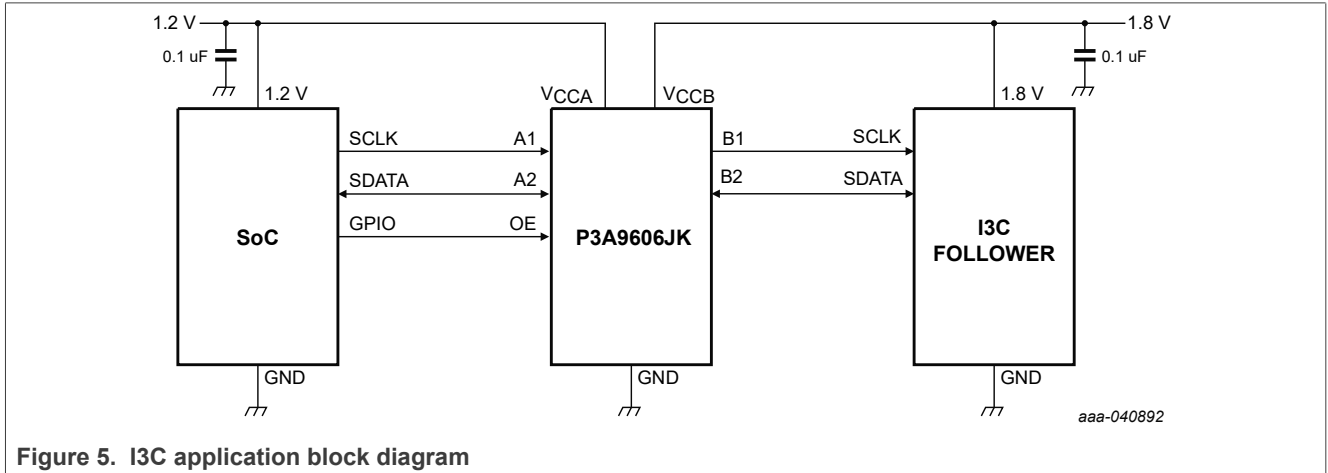


Figure 5. I3C application block diagram

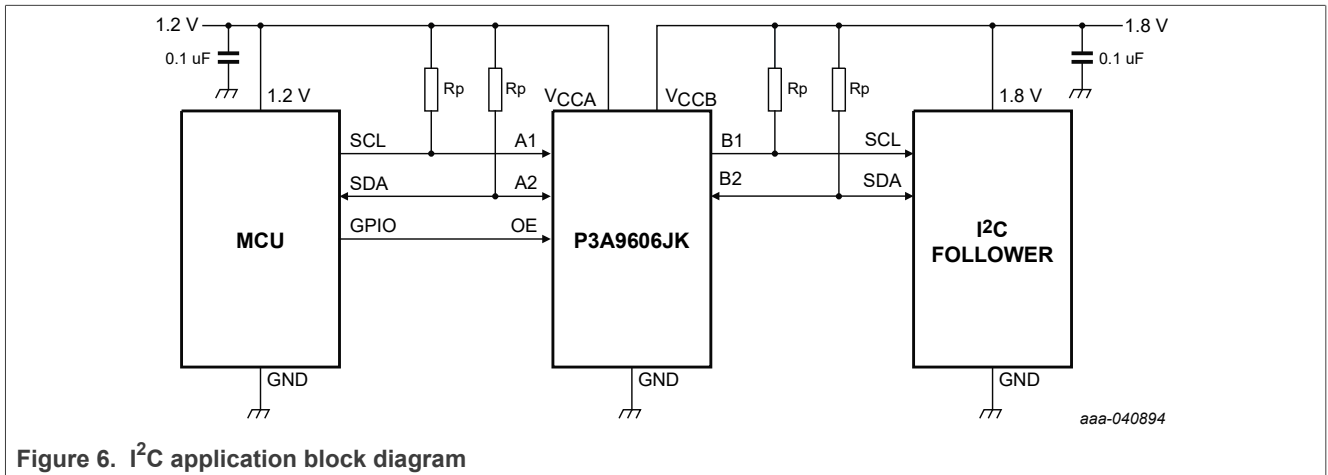


Figure 6. I<sup>2</sup>C application block diagram

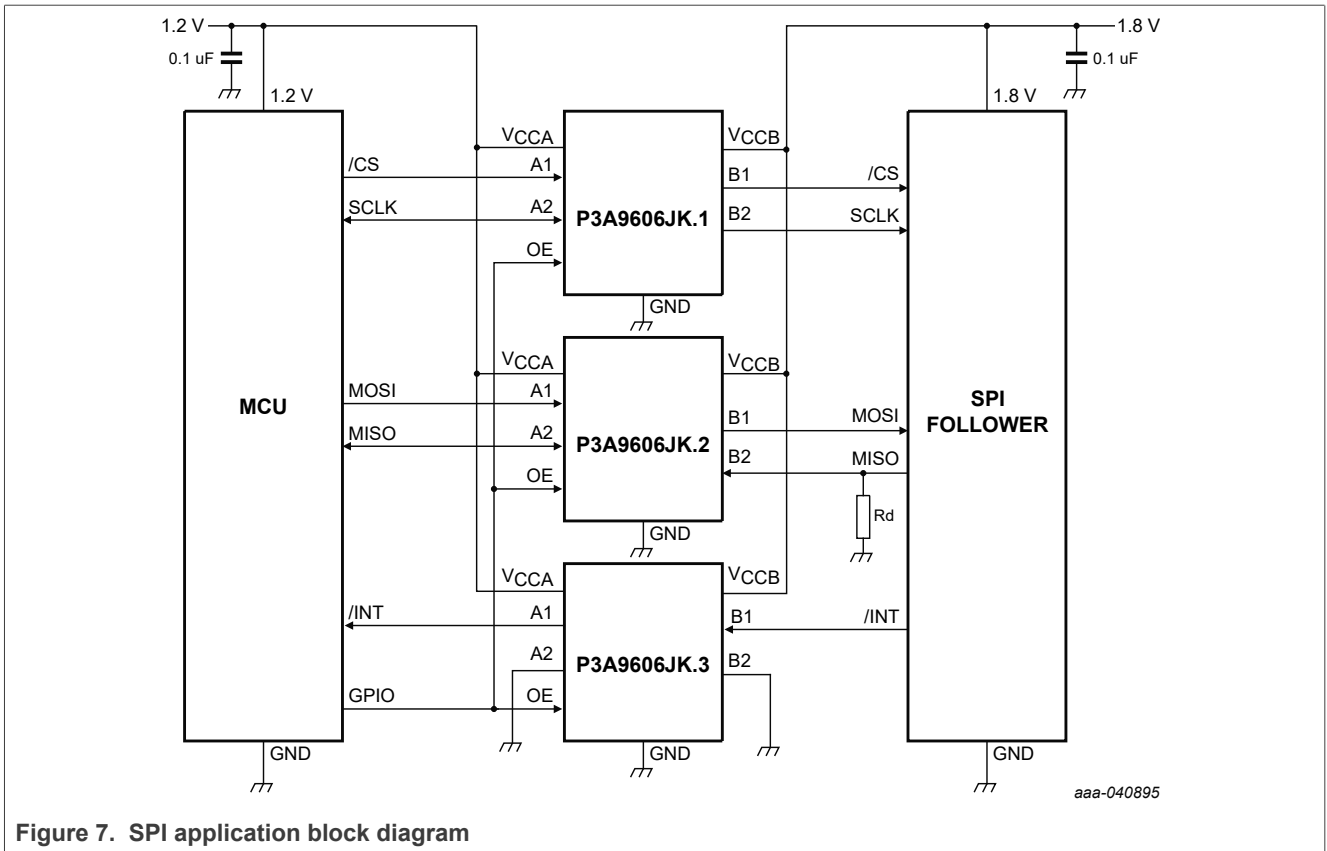


Figure 7. SPI application block diagram

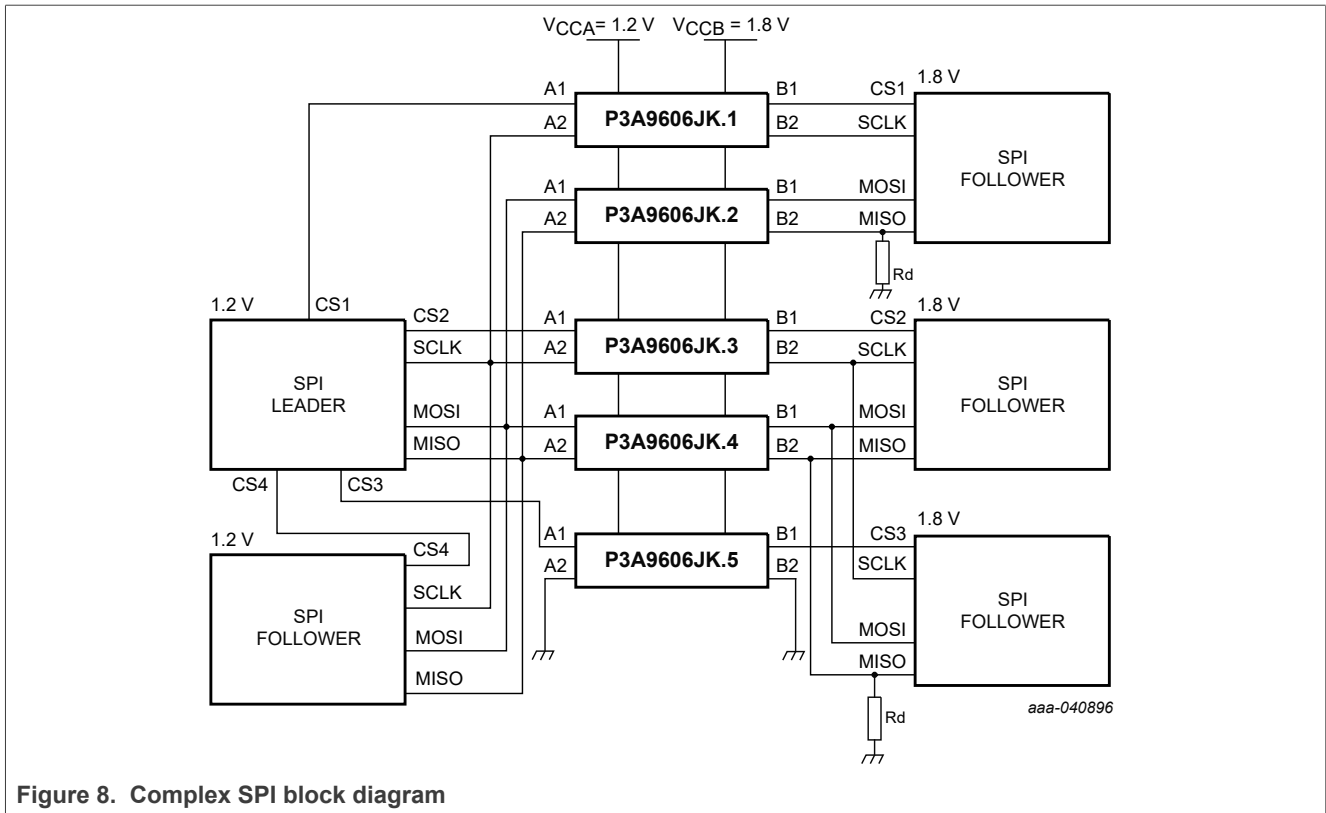


Figure 8. Complex SPI block diagram

### 13.2 Architecture

The architecture uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high), N-Channel Pass gate transistor and a pull-up resistor (to provide DC-bias and drive capabilities) to meet these requirements. The design is directionless and does not need direction control signal. The implementation supports both low speed Open-drain operation as well as high speed push-pull operation. The N-Channel Pass device will be on only during Low input cycle and will be off during High input cycle.

### 13.3 Input driver requirements

The continuous DC- current sinking or sourcing capability is determined by the external system-level; open-drain or push-pull drivers that are interfaced to the P3A9606JK IO pins.

The high bandwidth of these IO circuits used to facilitate this fast change from an input to an output and an output to an input, they have a modest sourcing capability of hundreds of micro-amperes, as determined by the pull-up resistor.

The fall time of a signal depends on the edge-rate and output impedance of the external driving the P3A9606JK data IOs, as well as the capacitive loading at the data lines.

### 13.4 Power-up and power-down

During operation, ensure that  $V_{CCA} \leq V_{CCB}$  at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. There is no special power-up sequencing required. The

P3A9606JK includes circuitry that disables all output ports and puts the device into a power-down mode when either  $V_{CCA}$  or  $V_{CCB}$  is switched off.

### 13.5 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND, OE pin should not be left floating in any condition.

OE  $V_{IL}$  and  $V_{IH}$  are referenced to  $V_{CCA}$ . The OE can be controlled by an external device that is powered by either  $V_{CCA}$  or  $V_{CCB}$ . As  $V_{CCB}$  is required to be greater than  $V_{CCA}$ , the OE pin has been designed to withstand a voltage equal to  $V_{CCB}$  (up to 1.98 V per recommended functional voltage range).

### 13.6 Layout guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies and should be placed as close as possible to  $V_{CCA}$ ,  $V_{CCB}$ , and GND pins.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 8 ns, ensuring that any reflection encounters low impedance at the source driver.

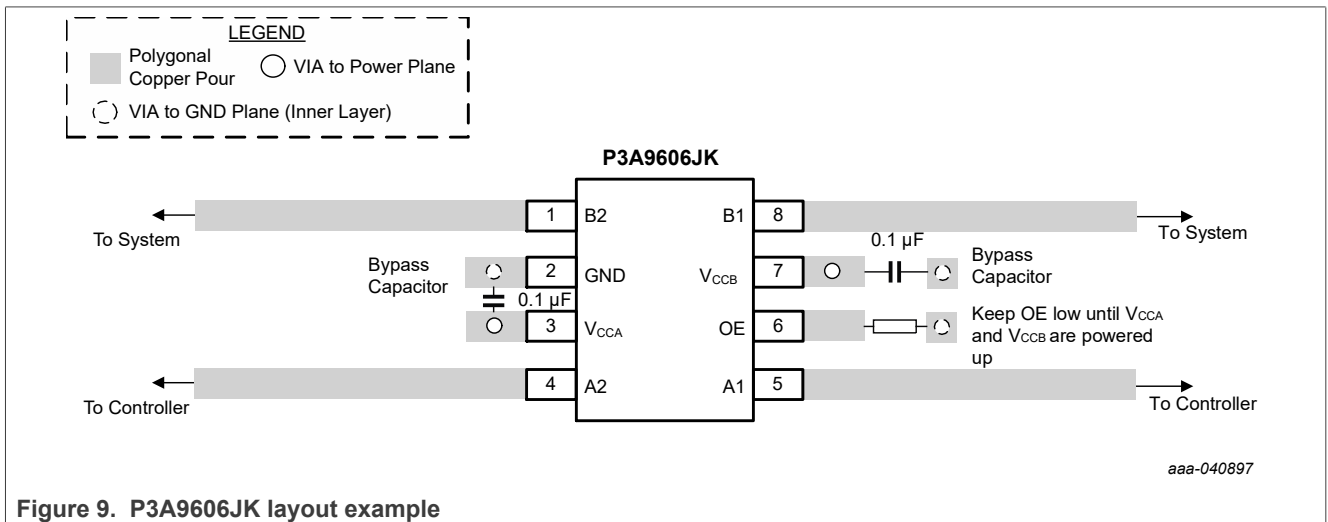


Figure 9. P3A9606JK layout example

14 Package outline

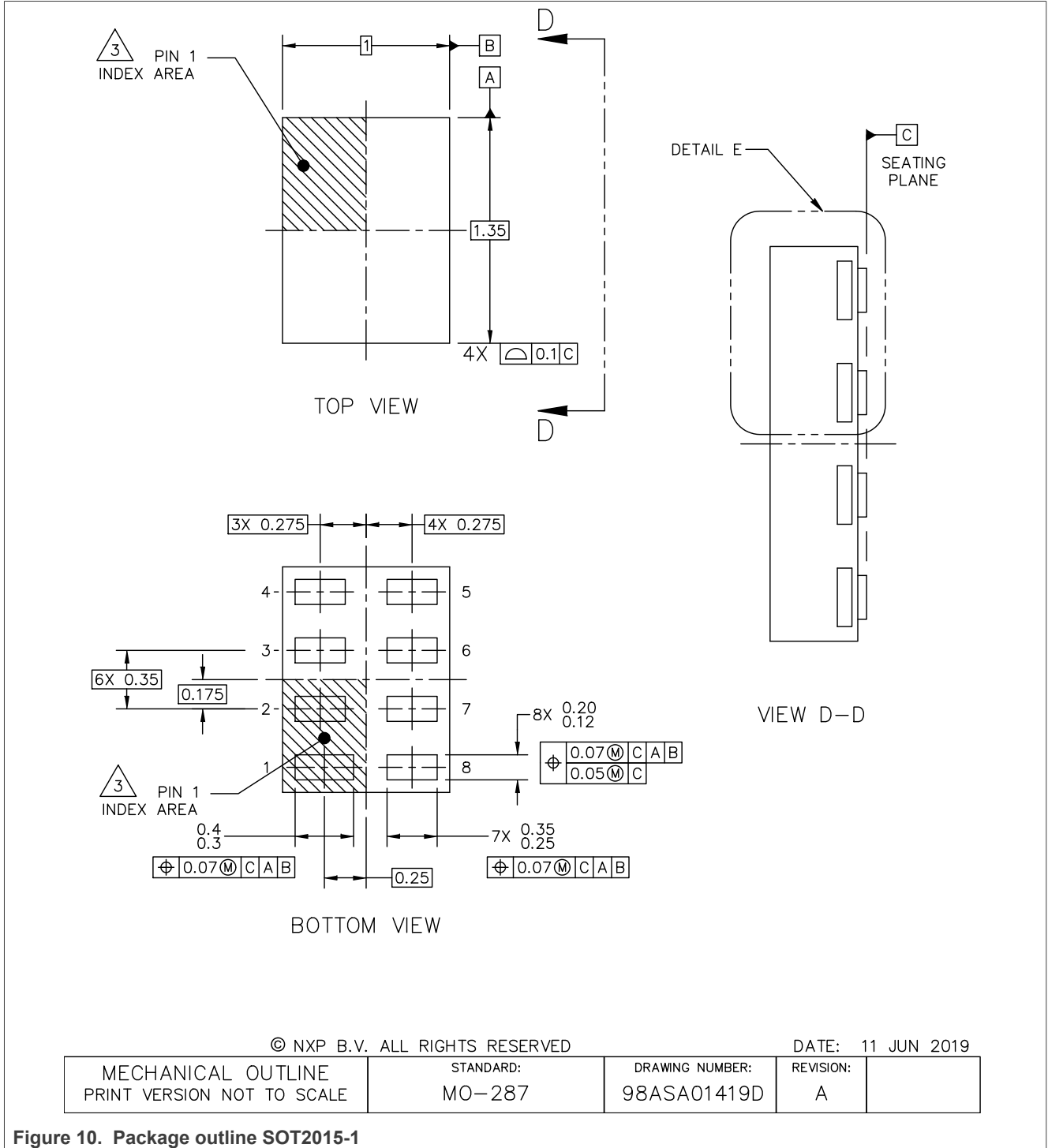


Figure 10. Package outline SOT2015-1



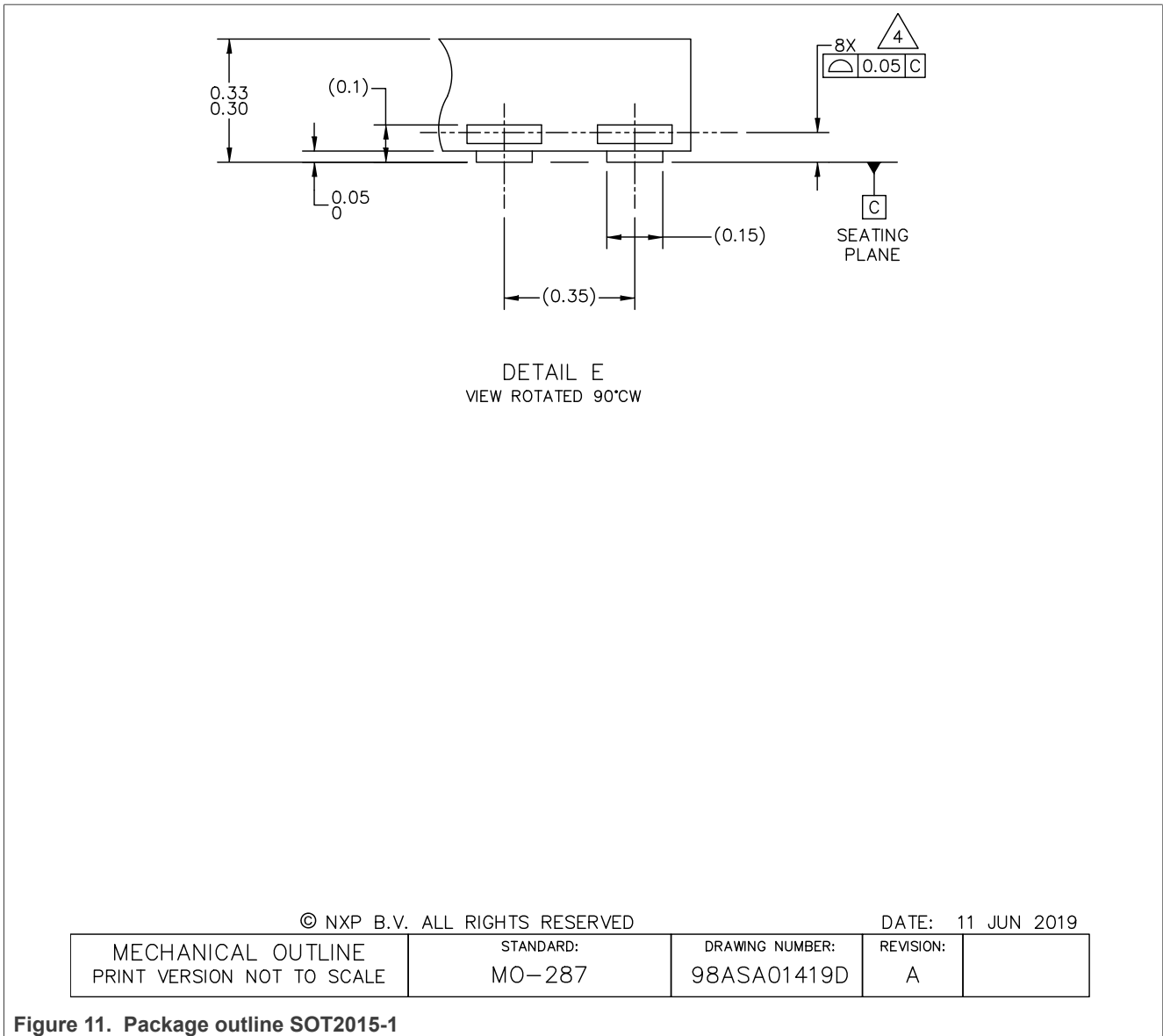
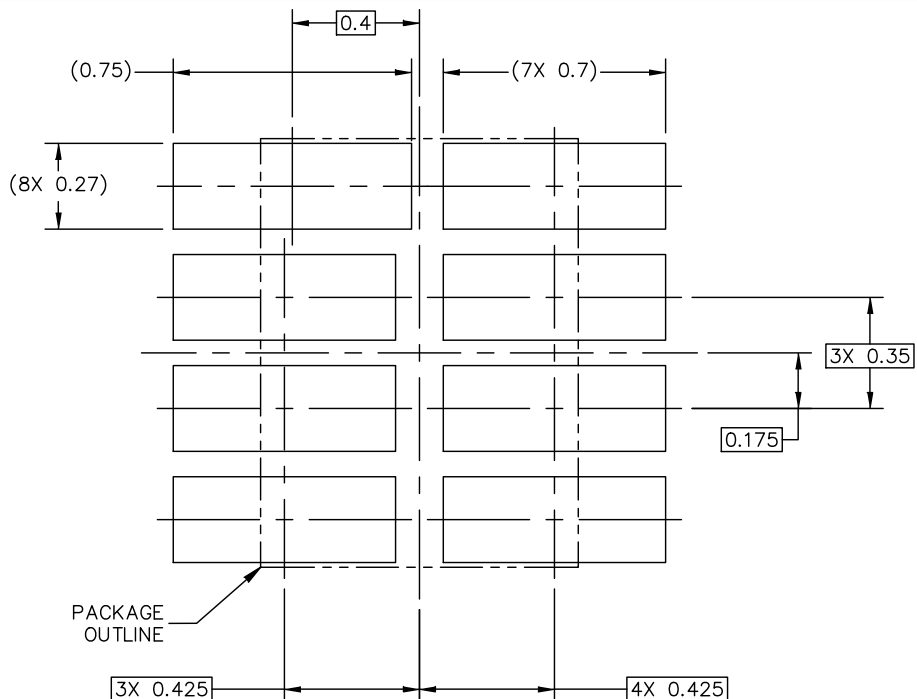


Figure 11. Package outline SOT2015-1

15 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

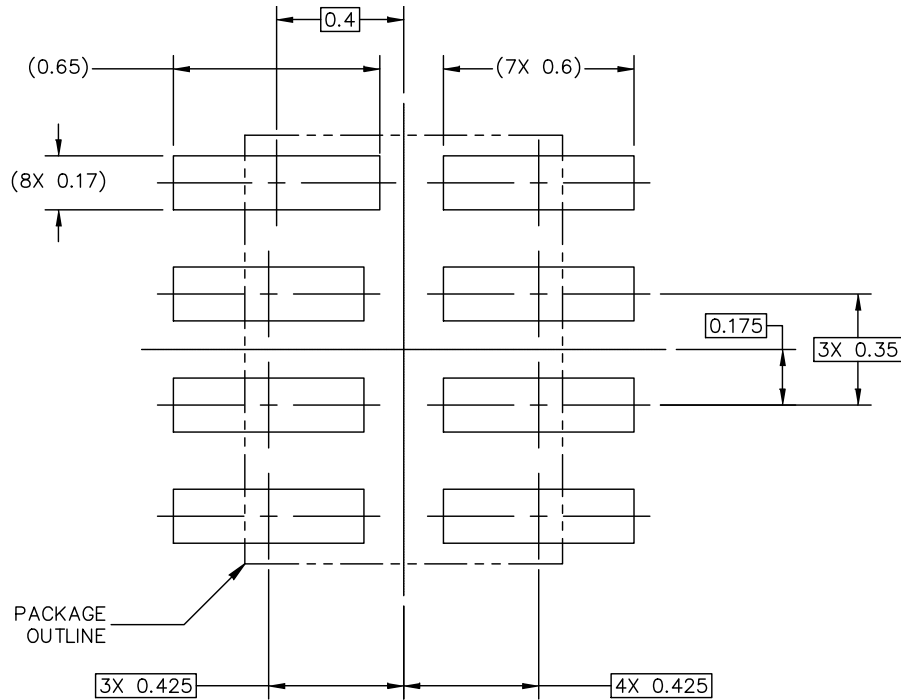
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Figure 12. Soldering footprint for SOT2015-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

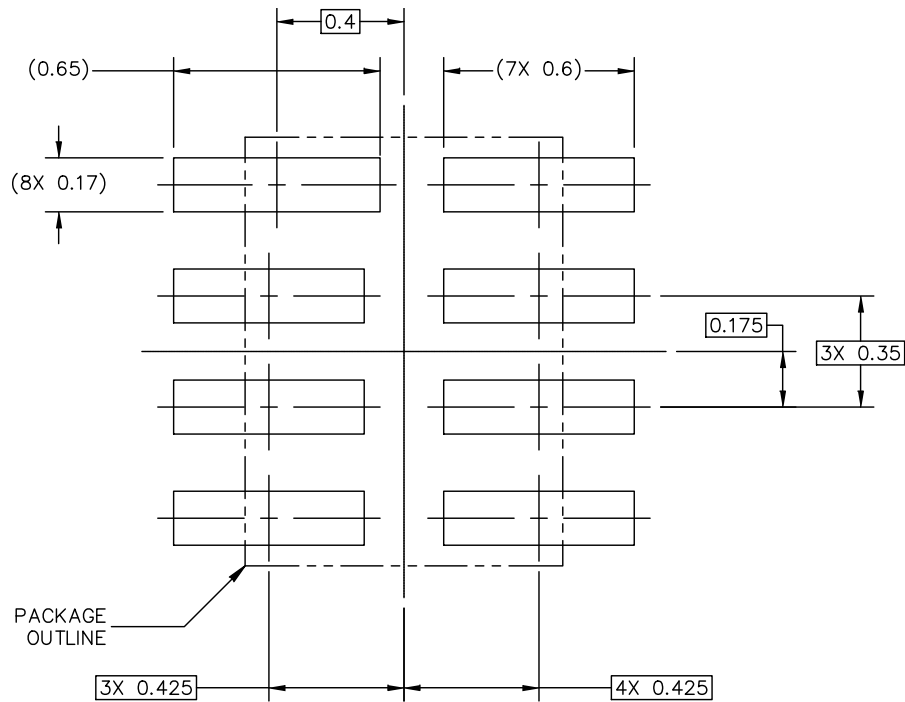
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Figure 13. Soldering footprint for SOT2015-1



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 14. Soldering footprint for SOT2015-1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS.
5. MIN METAL GAP SHOULD BE 0.15 MM.

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Figure 15. Soldering footprint for SOT2015-1

## 16 Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
PRR	Pulse Repetition Rate

## 17 Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P3A9606JK v.2.0	20230104	Product data sheet	202212010I	P3A9606JK v.1.0
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 8</a>: Updated V<sub>OH</sub> and V<sub>OL</sub> conditions and logic levels to meet I<sup>3</sup>C spec.</li> <li>• <a href="#">Table 9</a>: Updated V<sub>IH</sub> min values for V<sub>CCA</sub> = 0.9 V to 1.98 V; V<sub>CCB</sub> = 0.9 V to 1.98 V.</li> </ul>			
P3A9606JK v.1.0	20210510	Product data sheet	-	-

## 18 Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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