Burr-Brown Products
from Texas Instruments

SBOS206E − DECEMBER 2001 − REVISED FEBRUARY 2007

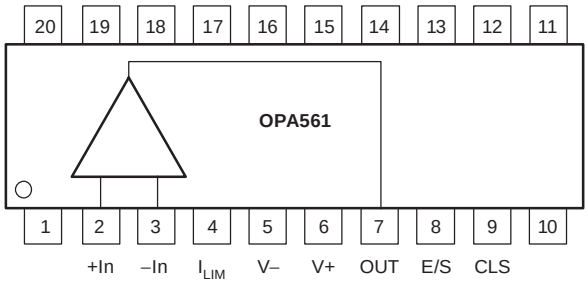
High-Current, High-Speed OPERATIONAL AMPLIFIER

FEATURES

- 1.2A OUTPUT CURRENT
- 12V_{PP} OUTPUT VOLTAGE
- WIDE POWER RANGE:
  - Single Supply: +7V to +15V
  - Dual Supply: ±3.5V to ±7.5V
- FULLY PROTECTED:
  - Thermal Shutdown
  - Adjustable Current Limit
- OUTPUT DISABLE CONTROL
- 17MHz GAIN-BANDWIDTH PRODUCT
- 50V/µs SLEW RATE
- 1MHz FULL-POWER BANDWIDTH
- THERMALLY ENHANCED HTSSOP-20 PowerPAD™ PACKAGE

APPLICATIONS

- POWER-LINE COMMUNICATIONS
- VALVE-ACTUATOR DRIVERS
- POWER SUPPLIES
- TEST EQUIPMENT
- TEC DRIVERS
- LASER DIODE DRIVERS



HTSSOP−20

NOTE: Pins 1, 10, and 11−20 are not connected.
Flag must be connected to V–.

DESCRIPTION

The OPA561 is a low-cost, high-current operational amplifier capable of driving up to 1.2A pulses into reactive loads. This monolithic integrated circuit provides high reliability in demanding line-carrier communications, laser diode drivers, and motor control applications. The high slew rate provides 1MHz full-power bandwidth and excellent linearity.

The OPA561 operates from either a single supply in the range of 7V to 15V or dual power supplies of ±3.5V to ±7.5V for design flexibility. In single-supply operation, the input common-mode range extends below ground. At maximum output current, a wide output swing provides a 12Vp-p capability with a nominal 15V supply.

The OPA561 is internally protected against over-temperature conditions and current overloads. In addition, the OPA561 is designed to provide an accurate, user-selected, current limit. The current limit can be adjusted from 0.2A to 1.2A with a low-power resistor/potentiometer or DAC (Digital-to-Analog Converter). The high-speed characteristics of the current control loop provide accuracy even under pulsed load conditions.

The Enable/Status (E/S) pin performs two functions: it can be monitored to determine if the device is in thermal shutdown (active LOW), and it can also be forced LOW to disable the output, disconnecting the load.

The OPA561 is available in the miniature, HTSSOP-20 PowerPAD power package. This surface-mount package is thermally enhanced and has a very low thermal resistance. Operation is specified over the extended industrial temperature range, −40°C to +125°C.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V− to V+	16V
Input Voltage Range	(V−) −0.4V to (V+) + 0.5V
Input Shutdown Voltage	(V−) −0.4V to (V−) + 0.5V
Operating Temperature	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA561PWP	HTSSOP-20	PWP	−40°C to +125°C	OPA561	OPA561PWP OPA561PWP/2K	Rails, 70 Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

BOLDFACE limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

At T_{CASE} = +25°C, V_S = 15V, load connected to V_S/2, and E/S enabled, unless otherwise noted.

PARAMETER		CONDITIONS	OPA561 MIN	OPA561 TYP	OPA561 MAX	UNITS
OFFSET VOLTAGE		V_S = 12V				
Input Offset Voltage	V_{OS}	V_{CM} = 0V		±1	±20	mV
vs Temperature	**dV_{OS}/dT**			**±50**		**µV/°C**
vs Power Supply	PSRR	V_{CM} = 0V, V_S = 7V to 16V		25	150	µV/V
INPUT BIAS CURRENT(1)						
Input Bias Current	I_B	V_{CM} = 0V		10	100	pA
Input Offset Current	I_{OS}	V_{CM} = 0V		10	100	pA
NOISE						
Input Voltage Noise Density	e_n	f = 1kHz		83		nV/√Hz
		f = 10kHz		32		nV/√Hz
		f = 100kHz		14		nV/√Hz
Current Noise	i_n	f = 1kHz		4		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	Linear Operation	(V−) − 0.1		(V+) − 3	V
Common-Mode Rejection Ratio	CMRR	V_S = 15V, V_{CM} = (V−) − 0.1V to (V+) − 3V	70	80		dB
INPUT IMPEDANCE						
Differential				$1.8 \cdot 10^{11}$ || 10		Ω || pF
Common-Mode				$1.8 \cdot 10^{11}$ || 18.5		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_O = $10V_{PP}$, R_L = 5Ω	80	100		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	R_L = 5Ω		17		MHz
Slew Rate	SR	G = 1, 10V Step, R_L = 5Ω		50		V/µs
Full-Power Bandwidth		G = +2, V_{OUT} = 10Vp-p		1		MHz
Settling Time: ±0.1%		G = −1, 10V Step		1		µs
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, R_L = 5Ω, G = +2, V_O = $10V_{PP}$		0.02		%
		f = 1MHz		3		%

(1) High-speed test at T_J = +25°C.
(2) See text for more information on current limit accuracy.
(3) Transient load transition time must be ≥ 200ns.
(4) 402kΩ pull-up resistor to V+ can be used to permanently enable the OPA561.

ELECTRICAL CHARACTERISTICS (continued)

BOLDFACE limits apply over the specified temperature range, T_A = −40°C to +125°C.

At T_{CASE} = +25°C, V_S = 15V, load connected to V_S/2, and E/S enabled, unless otherwise noted.

PARAMETER		CONDITIONS	OPA561 MIN	OPA561 TYP	OPA561 MAX	UNITS
OUTPUT						
Voltage Output, Positive		I_O = 0.5A	(V+) − 1	(V+) − 0.7		V
Negative		I_O = −0.5A	(V−) + 1	(V−) + 0.7		V
Positive		I_O = 1A	(V+) − 1.5	(V+) − 1.2		V
Negative		I_O = −1A	(V−) + 1.5	(V−) + 1.2		V
Maximum Continuous Current Output, dc				1.2		A
Output Impedance	Z_O	G = +2, f = 100kHz		0.05		Ω
Ouput Current Limit Range				±0.2 to ±1.2		A
Current Limit Tolerance(2)		R_{CL} = 2kΩ (I_{LIM} = ±1A)		±50		mA
Asymmetry		Comparing Positive and Negative Limits		10		%
Current Limit Overshoot(3)		V = 5V Pulse (200ns t_r), G = +2		50		%
Output Disabled						
Output Resistance				10		MΩ
Output Capacitance				140		pF
OUTPUT ENABLE/STATUS AND FLAG PINS						
Shutdown Input Mode						
$V_{E/S}$ HIGH (output enabled)(4)		E/S Pin Open or Forced HIGH	(V−) + 2		(V−) + 5	V
$V_{E/S}$ LOW (output disabled)		E/S Pin Forced LOW	(V−) − 0.4		(V−) + 0.8	V
$I_{E/S}$ HIGH (output enabled)		E/S Pin Indicates HIGH		20		µA
$I_{E/S}$ LOW (output disabled)		E/S Pin Indicates LOW		0.1		µA
Output Disable Time				50		ns
Output Enable Time				3		µs
Thermal Shutdown Status						
Normal Operation		Sourcing 20µA	(V−) + 2			V
Thermally Shutdown					(V−) + 0.8	V
Current Limit Status						
Normal Operation		Sourcing 20µA	(V−) + 0.8			V
Current Limit Flagged					(V−) + 2	V
Junction Temperature at Shutdown				+160		°C
Reset Temperature from Shutdown				+140		°C
POWER SUPPLY						
Specified Voltage	V_S			15		V
Operating Voltage Range, (V+) − (V−)			7		16	V
Quiescent Current	I_Q	I_{LIM} Connected to V−, I_Q = 0		50	60	mA
vs Temperature				**60**	**70**	**mA**
Quiescent Current in Shutdown Mode		I_{LIM} Connected to V−			250	µA
TEMPERATURE RANGE						
Specified Junction Temperature Range			−40		+125	°C
Storage Range			−65		+150	°C
Thermal Resistance						
HTSSOP-20 PowerPAD	θ_{JC}			1.4		°C/W
θ_{JA}		2oz. Trace and 9in^2 Copper Pad with Solder		32		°C/W
θ_{JA}		Without Heatsink		100		°C/W

(1) High-speed test at T_J = +25°C.

(2) See text for more information on current limit accuracy.

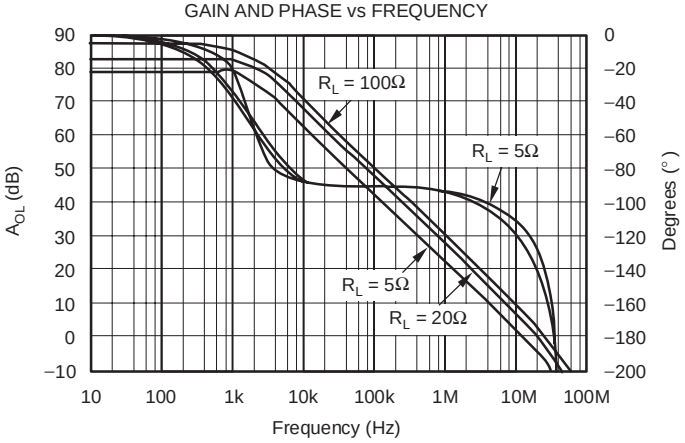
(3) Transient load transition time must be ≥ 200ns.

(4) 402kΩ pull-up resistor to V+ can be used to permanently enable the OPA561.

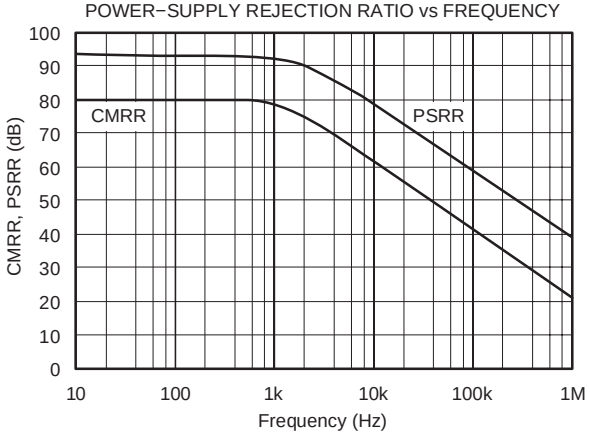
TYPICAL CHARACTERISTICS

At T_{CASE} = +25°C, V_S = 15V, and E/S enabled, unless otherwise noted.

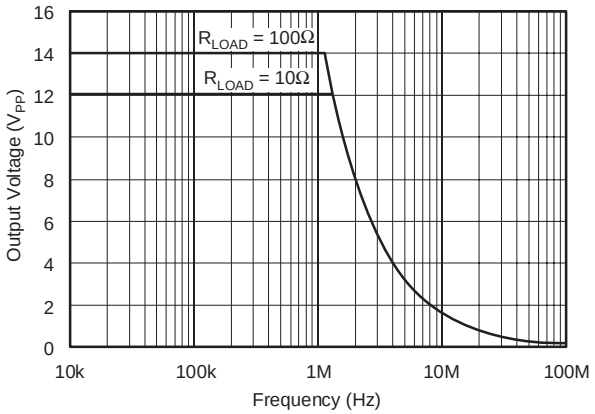
GAIN AND PHASE vs FREQUENCY



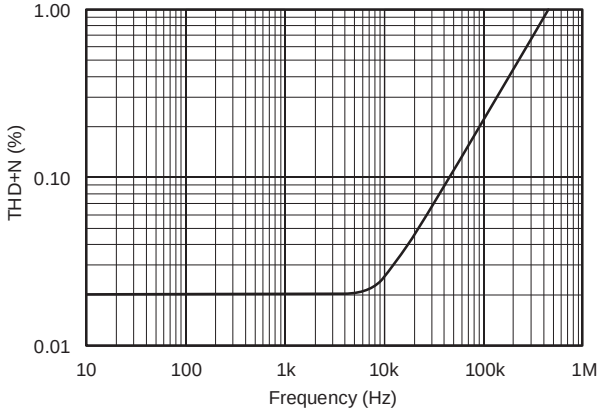
COMMON−MODE REJECTION RATIO,
POWER−SUPPLY REJECTION RATIO vs FREQUENCY



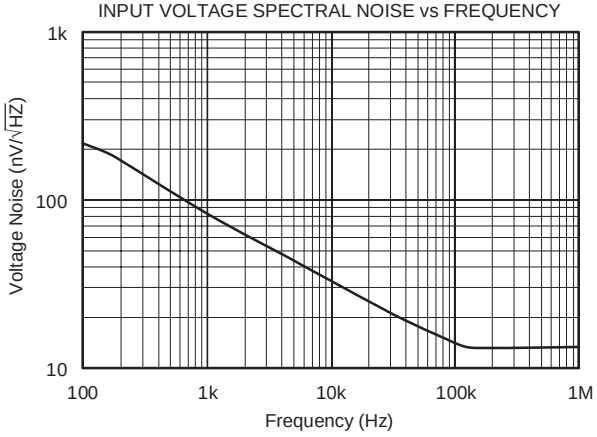
MAXIMUM OUTPUT AMPLITUDE vs FREQUENCY



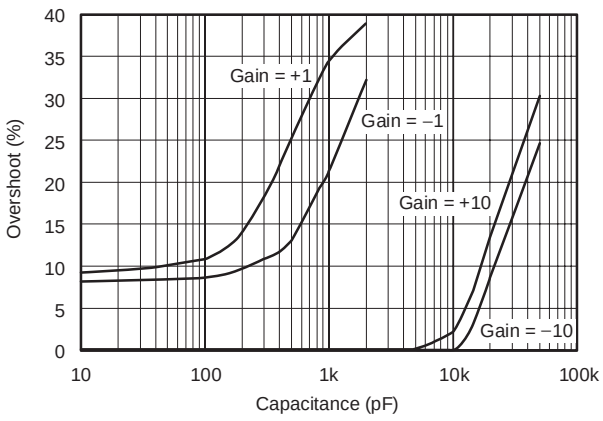
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY
(Unity Gain Follower, Load = 5Ω)



INPUT VOLTAGE SPECTRAL NOISE vs FREQUENCY



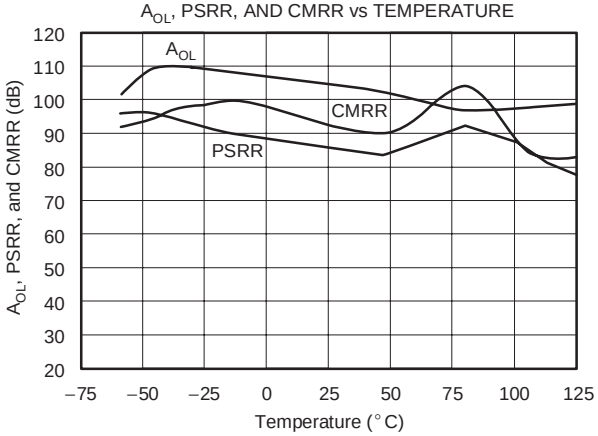
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



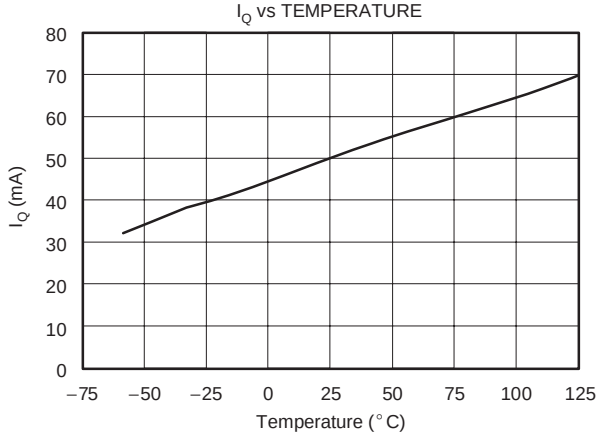
TYPICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = 15V, and E/S enabled, unless otherwise noted.

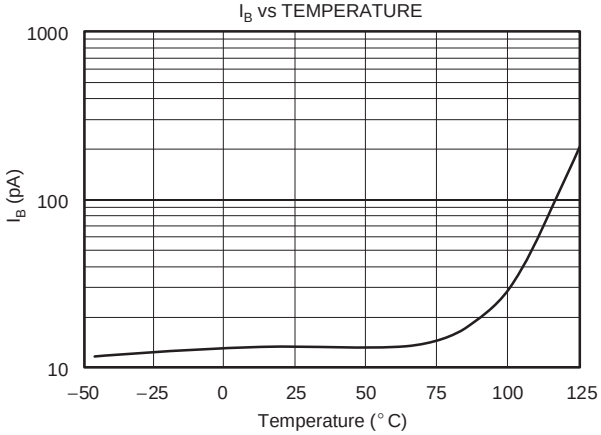
A_{OL}, PSRR, AND CMRR vs TEMPERATURE



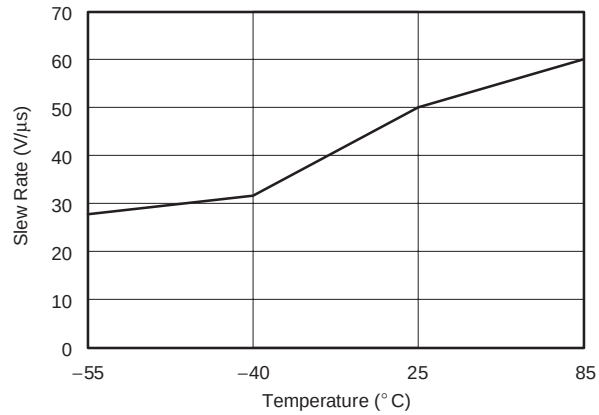
I_Q vs TEMPERATURE



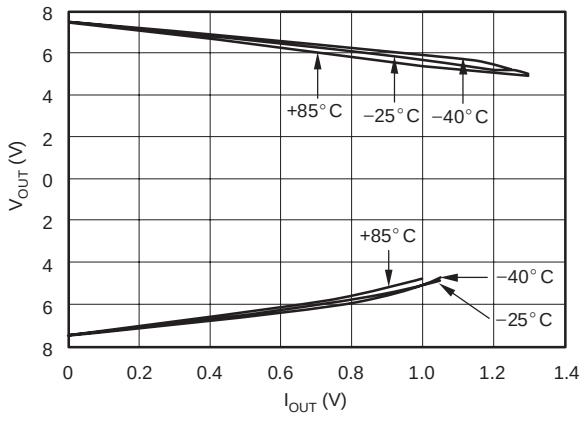
I_B vs TEMPERATURE



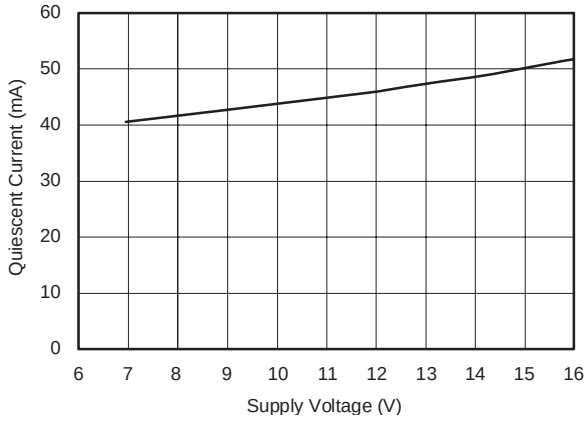
SLEW RATE vs TEMPERATURE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



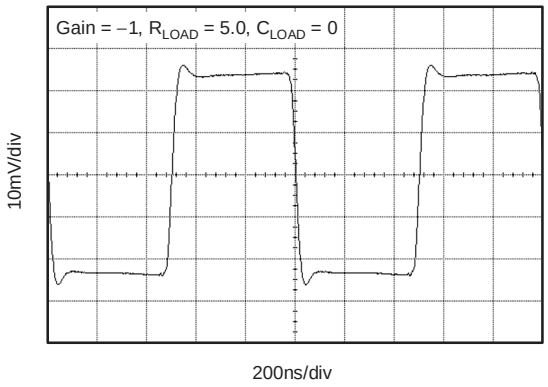
QUIESCENT CURRENT vs SUPPLY VOLTAGE



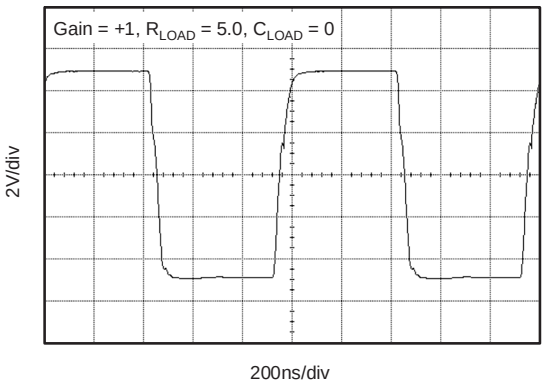
TYPICAL CHARACTERISTICS (continued)

At T_{CASE} = +25°C, V_S = 15V, and enabled, unless otherwise noted.

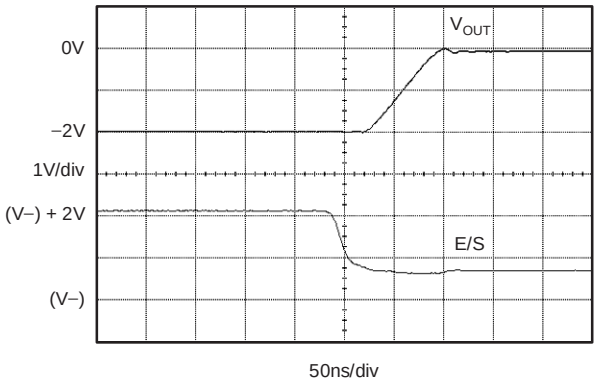
SMALL−SIGNAL STEP RESPONSE



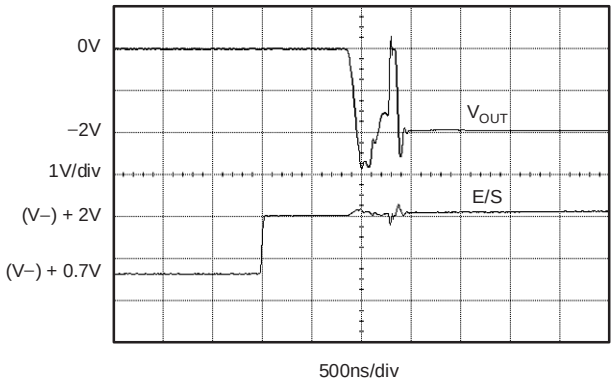
LARGE−SIGNAL STEP RESPONSE



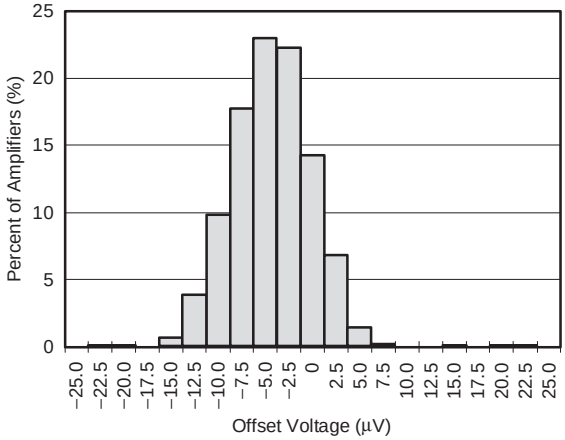
SHUTDOWN RESPONSE
R_L = 5Ω



ENABLE RESPONSE
R_L = 5Ω



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



APPLICATIONS INFORMATION

Figure 1 shows the OPA561 connected as a basic noninverting amplifier. However, the OPA561 can be used in virtually any op amp configuration.

Power-supply terminals should be bypassed with low series impedance capacitors. The technique of using a ceramic and tantalum type in parallel is recommended. Power-supply wiring should have low series impedance.

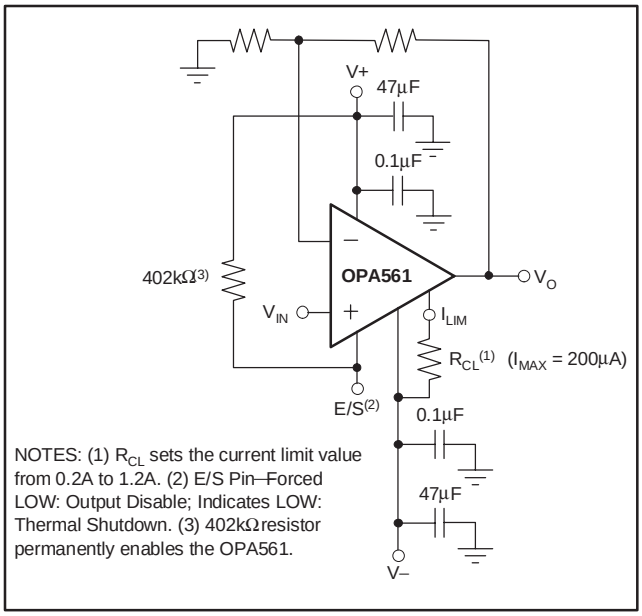


Figure 1. Basic Circuit Connections

POWER SUPPLIES

The OPA561 operates from single (+7V to +15V) or dual (±3.5V to ±7.5V) supplies with excellent performance. Power-supply voltages do not need to be equal. For example, the positive supply could be set to 10V with the negative supply at –5V, or vice-versa. Most behaviors remain unchanged throughout the operating voltage range. Parameters that vary significantly with operating voltage are shown in the typical characteristics.

ADJUSTABLE CURRENT LIMIT

The OPA561's accurate, user-defined, current limit can be set from 0.2A to 1.2A by controlling the input to the I_{LIM} pin. Unlike other designs that use a power resistor in series with the output current path, the OPA561 senses the load internally. This allows the current limit to be set with low-power components. In contrast, other designs require one or two expensive power resistors that can handle the full output current (1.2A in this case).

Current Limit Accuracy

Separate circuits monitor the positive and negative currents. Each output is compared to a single internal reference that is set by the external current limit resistor (or voltage). The OPA561 employs a patented circuit technique to achieve an accurate and stable current limit. The output current limit has an accuracy of up to 5% on the 1A current limit. Due to internal matching limitations, the positive and negative current limits can be slightly different. However, the values are typically within 10% of each other.

Setting the Current Limit

Leaving the I_{LIM} pin open could damage the part. Connecting I_{LIM} directly to V− programs the maximum output current limit, typically 1.2A. The simplest method for adjusting the current limit (I_{LIM}) uses a resistor or potentiometer connected between the I_{LIM} pin and V− according to Equation 1:

$$I_{LIM} = \left(\frac{1.2V}{R_{CL} + 10k\Omega}\right) \times 10,000 \quad (1)$$

This external resistor determines a small internal current which sets the desired output current limit. Alternatively, the output current limit can be set by applying a voltage to the I_{LIM} pin. Figure 2 shows a simplified schematic of the OPA561's current limit.

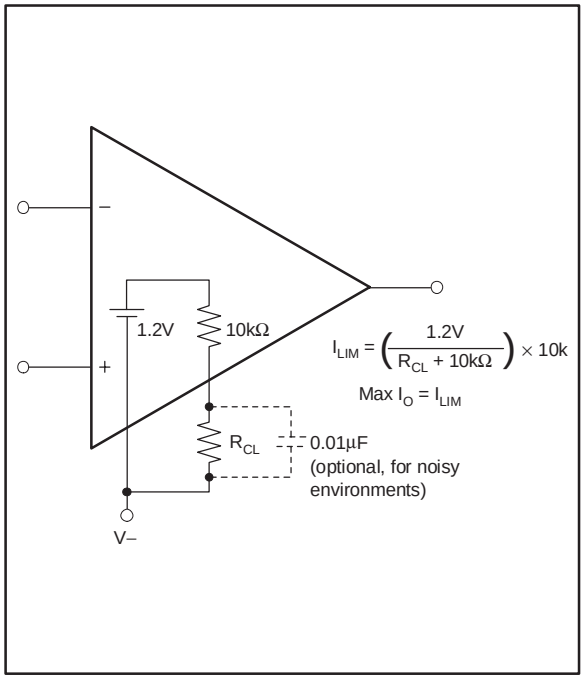


Figure 2. Adjustable Current Limit—Resistor Method

ENABLE/STATUS (E/S) PIN

The Enable/Status Pin provides two unique functions: 1) output disable by forcing the pin LOW and 2) thermal shutdown indication by monitoring the voltage level at the pin. One or both of these functions can be utilized on the same device. For normal operation (output enabled), the E/S pin must be pulled HIGH (at least 2V above V−). A small value capacitor connected between the E/S pin and V− may be appropriate for noisy applications. To enable the OPA561 permanently, the E/S pin can be tied to V+ through a 402kΩ pull-up resistor.

Output Disable

The shutdown pin is referenced to the negative supply (V−). Therefore, shutdown operation is slightly different in single-supply and dual-supply applications.

In single-supply operation, V− typically equals common ground. Therefore, the shutdown logic signal and the OPA561's shutdown pin are referenced to the same potential. In this configuration, the logic pin and the OPA561 enable can simply be tied together. Shutdown occurs for voltage levels of < 0.8V. The OPA561 is enabled at logic levels > 2V.

In dual-supply operation, the logic pin is still referenced to a logic ground. However, the shutdown pin of the OPA561 is still referenced to V−. To shutdown the OPA561, the voltage level of the logic signal needs to be level shifted using an optocoupler, as shown in Figure 3.

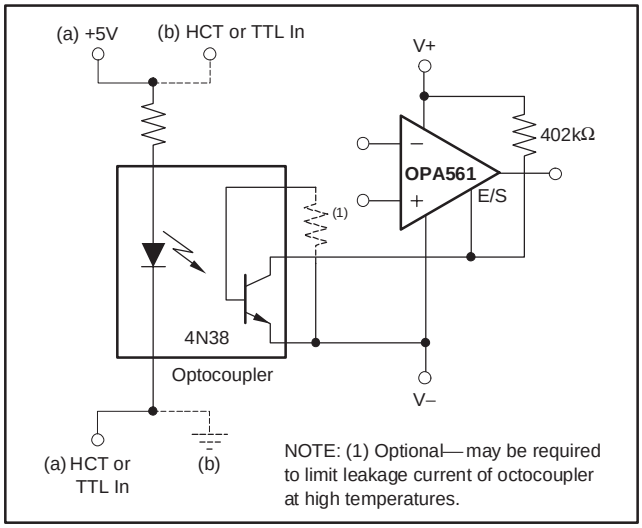


Figure 3. Shutdown Configuration for Dual Supplies

To disable the output, the E/S pin is pulled LOW, no greater than 0.8V above V−. This function can be used to conserve power during idle periods. The typical time required to shut down the output is 50ns. To return the output to an enabled state, the E/S pin should be pulled to at least 2.0V above V−. Typically, the output is enabled within 3µs. It should be noted that pulling the E/S pin HIGH (output enabled) does not disable the internal thermal shutdown.

Ensuring Microcontroller Compatibility

Not all microcontrollers output the same logic state after power-up or reset. 8051-type microcontrollers, for example, output logic HIGH levels on their ports while other models power up with logic LOW levels after reset.

In configuration (a) as shown in Figure 3, the shutdown signal is applied on the cathode side of the photodiode within the optocoupler. A high logic level causes the OPA561 to be enabled, and a low logic level shuts the OPA561 down. In configuration (b) of Figure 3, with the logic signal applied on the anode side, a high level causes the OPA561 to shutdown and low level enables the op amp.

OVER-CURRENT FLAG

The OPA561 features an over-current status flag (CLS, Pin 9) that can be monitored to see if the load exceeds the current limit. The output signal of the over current limit flag is compatible to standard logic. The CLS signal is referenced to V−. A voltage level of less than (V−) + 0.8V indicates normal operation and a level of greater than (V−) + 2 indicates that the OPA561 is in current limit. The flag is HIGH as long as the output of the OPA561 is in current limit. At very low signal frequencies, typically < 1kHz, both the upper (sourcing current) and lower current limit (sinking current) are monitored. At frequencies > 1kHz, due to internal circuit limitations, the flag output signal for the upper current limit becomes delayed and shortened. The flag signal for the lower current limit is unaffected by this behavior. As the signal frequency increases further, only the lower current limit (sinking current) is output on pin 9.

OUTPUT STAGE COMPENSATION

The complex load impedances common in power op amp applications can cause output stage instability. For normal operation, output compensation circuitry is typically not required. However, if the OPA561 is intended to be driven into current limit, an R/C network (snubber) may be required. A snubber circuit may also enhance stability when driving large capacitive loads (> 1000pF) or inductive loads (motors, loads separated from the amplifier by long cables). Typically, 3Ω to 10Ω in series with 0.01µF to 0.1µF is adequate. Some variations in circuit value may be required with certain loads.

OUTPUT PROTECTION

Reactive and EMF-generation loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in Figure 4. Schottky rectifier diodes with a 3A or greater continuous rating are recommended.

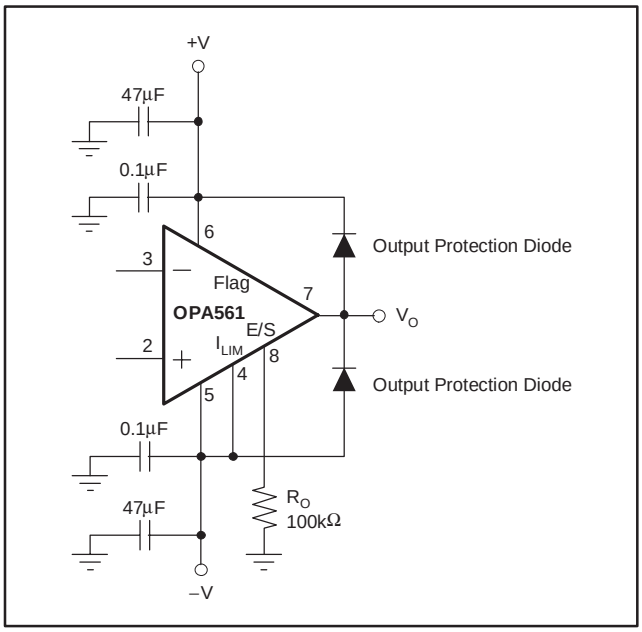


Figure 4. Output Protection Diode

THERMAL PROTECTION

The OPA561 has thermal sensing circuitry that helps protect the amplifier from exceeding temperature limits. Power dissipated in the OPA561 will cause the junction temperature to rise. Internal thermal shutdown circuitry shuts down the output when the die temperature reaches approximately 160°C, resetting when the die has cooled to 140°C. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the amplifier, but may have an undesirable effect on the load. Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable, long-term, continuous operation, junction temperature should be limited to +125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loading and signal conditions. For good, long-term reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a junction temperature of +125°C at the maximum expected ambient condition.

The internal protection circuitry of the OPA561 was designed to protect against overload conditions; it was not intended to replace proper heatsinking. Continuously running the OPA561 into thermal shutdown can degrade reliability. The E/S pin can be monitored to determine if shutdown has occurred. During normal operation the voltage on the E/S pin is typically above (V−) + 2V. During shutdown, the voltage drops to less than (V−) + 0.8V.

POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. For DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Dissipation with ac signals is lower. Application Bulletin AB−039 (SBOA022) explains how to calculate or measure power dissipation with unusual signals and loads, and can be dowloaded from www.ti.com.

HEATSINK AREA

The relationship between thermal resistance and power dissipation can be expressed as:

where:

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

θ_{JA} = Junction-to-Ambient Thermal Resistance (°C/W)

P_D = Power Dissipation (W)

To appropriately determine required heatsink area, required power dissipation should be calculated and the relationship between power dissipation and thermal resistance should be considered to minimize shutdown conditions and allow for proper long-term operation (junction temperature of +125°C). Once the heatsink area has been selected, worst-case load conditions should be tested to ensure proper thermal protection.

For applications with limited board size, refer to Figure 5 for the approximate thermal resistance relative to heatsink area. Increasing heatsink area beyond $2in^2$ provides little improvement in thermal resistance. To achieve the 32°C/W stated in the Electrical Characteristics, a copper plane size of $9in^2$ was used. The HTSSOP-20 PowerPAD package is well suited for continuous power levels from 2W to 4W, depending on ambient temperature and heatsink area. Higher power levels may be achieved in applications with a low on/off duty cycle, such as remote meter reading.

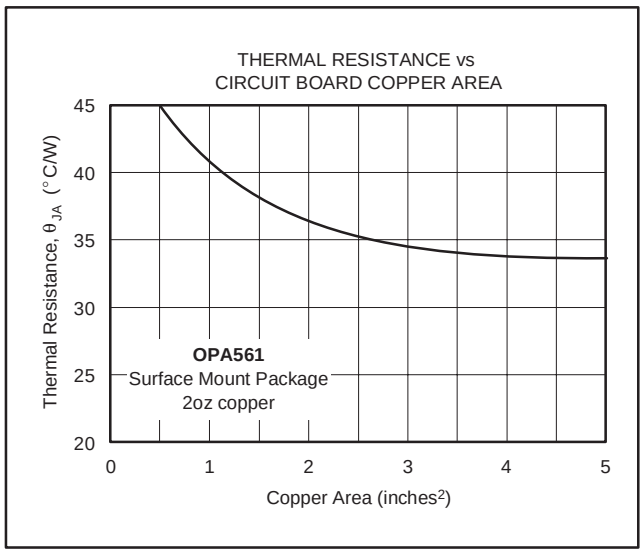


Figure 5. Thermal Resistance vs Circuit Board Copper Area

AMPLIFIER MOUNTING

What is PowerPAD?

The OPA561 uses the HTSSOP-20 PowerPAD package, a thermally enhanced, standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC, as shown in Figure 6. This provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package. The thermal pad on the bottom of the IC must be soldered directly to the PCB, using the PCB as a heatsink. In addition, through the use of thermal vias, the thermal pad can be directly connected to a ground plane or special heatsink structure designed into the PCB.

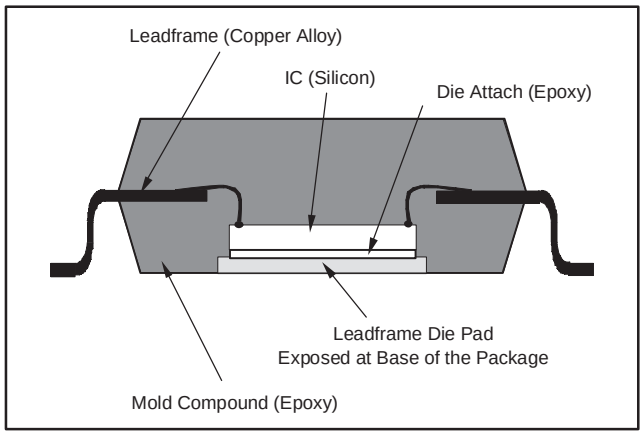


Figure 6. Section View of a PowerPAD Package

Soldering the PowerPAD to the PCB is always recommended, even with applications that have low power dissipation. It provides the necessary connection between the leadframe die and the PCB. The PowerPAD must be connected to the most negative supply of the device.

PowerPAD Assembly Process

1. Prepare the PCB with a top side etch pattern, as shown in the attached Thermal Land Pattern mechanical drawing. There should be etch for the leads as well as etch for the thermal land.
2. Place the recommended number of holes (or thermal vias) in the area of the thermal pad as shown on the attached Land Pattern mechanical. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. It is recommended, but not required, to place a small number of the holes under the package and outside the thermal pad area. These holes provide additional heat path between the copper land and ground plane and are 25 mils in diameter. They may be larger because they are not in the area to be soldered, so wicking is not a problem.
4. Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology; see Figure 7. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.

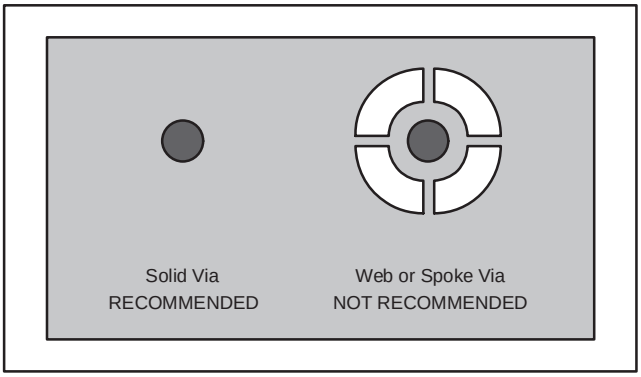


Figure 7. Via Connection

6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area. The thermal pad area should leave the 13 mil holes exposed. The larger 25 mil holes outside the thermal pad area should be covered with solder mask.
7. Apply solder paste to the exposed thermal pad area and all of the package terminals.
8. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For detailed information on the PowerPAD package including thermal modeling considerations and repair procedures, please see Technical Brief SLMA002, *PowerPAD Thermally Enhanced Package*, available at www.ti.com.

LAYOUT GUIDELINES

The OPA561 is a high-speed power amplifier that requires proper layout for best performance. Figure 8 shows an example of proper layout.

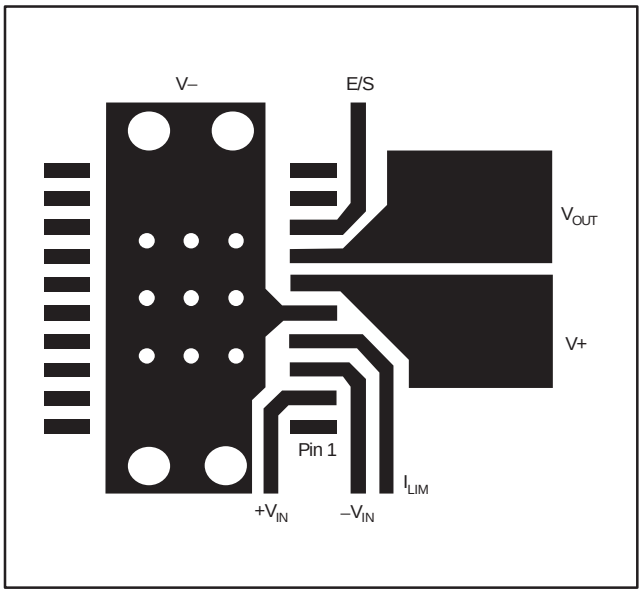


Figure 8. OPA561 Example Layout

Keep power-supply leads as short as possible. This will keep inductance low and resistive losses at a minimum. A minimum 18 gauge wire thickness is recommended for power-supply leads. The wire length should be < 8 inches.

Proper power-supply bypassing with low ESR capacitors is essential to achieve good performance. A parallel combination of small ceramic (around 100nF) and bigger (47µF) non-ceramic bypass capacitors will provide low impedance over a wide frequency range. Bypass capacitors should be placed as close as practical to the power-supply pins of the OPA561.

PCB traces conducting high currents, such as from output to load or from the power-supply connector to the power-supply pins of the OPA561 should be kept as wide and as short as possible. This will keep inductance low and also resistive losses to a minimum.

The holes in the landing pattern for the OPA561 are for the thermal vias that connect the PowerPAD of the OPA561 to the heatsink area on the printed circuit board (see attached Land Pattern mechanical drawing). The additional larger vias further enhance the heat conduction into the heatsink area. All traces conducting high currents are very wide for lowest inductance and minimal resistive losses. Note that the negative supply (V−) pin on the OPA561 is connected through the PowerPAD. This allows for maximum trace width for V_{OUT} and the positive power supply (V+).

APPLICATIONS CIRCUITS

The high output current and low supply of the OPA561 makes it a good candidate for driving laser diodes and thermo electric coolers. Figure 9 shows the OPA561 configured as a laser diode driver.

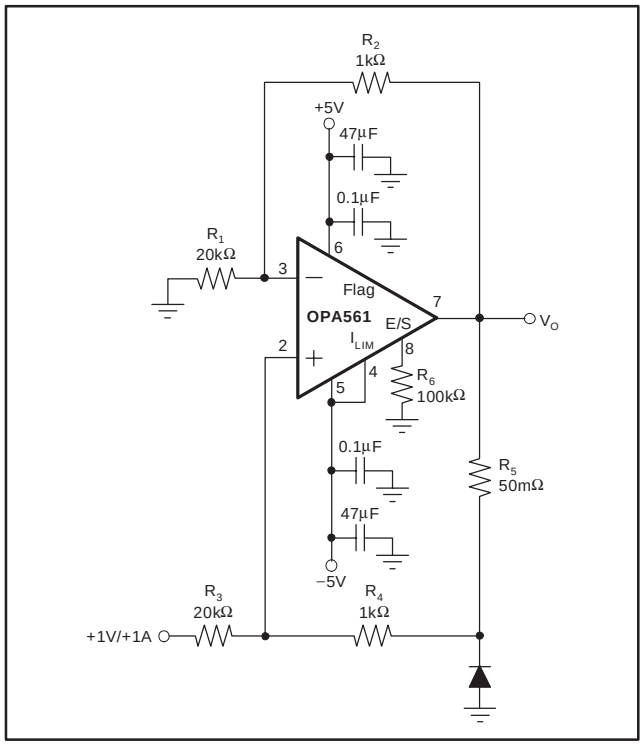


Figure 9. Laser Diode Driver

PROGRAMMABLE POWER SUPPLY

Figure 10 shows the OPA561 configured with the MSP430, REF3030, and DAC7513 as a space-saving, low-cost, programmable power-supply solution. This solution features low-voltage operation, small-size packages, (DAC7513 in SOT23-8, REF3030 in SOT23-3) and low cost.

POWER-LINE COMMUNICATION MODEM

The OPA561 is well suited to drive AC power lines for low-speed communications applications. It provides an easily implemented, reliable solution that is superior to discrete power transistor circuits. Advantages include:

1. Fully Integrated Solution
2. Integrated Shutdown Circuitry for Send-and-Receive Switching
3. Thermal Shutdown
4. Adjustable Current Limit
5. Shutdown Flag
6. Power Savings
7. Small PowerPAD package

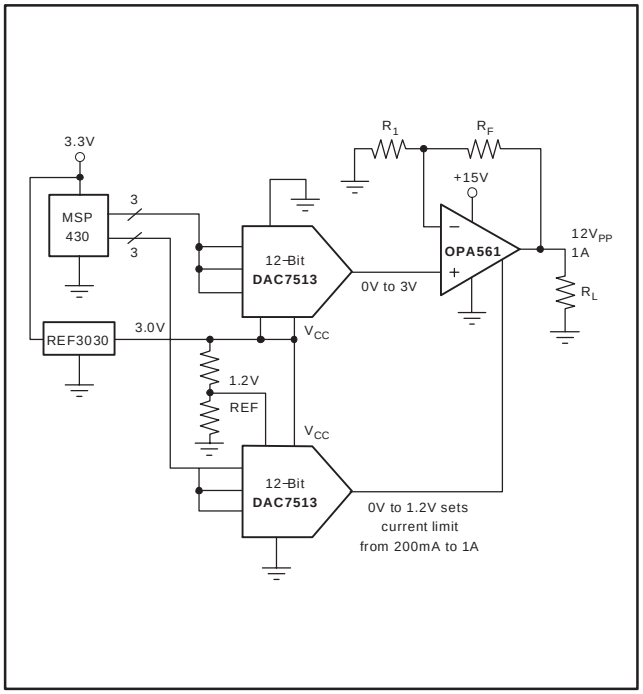


Figure 10. Programmable Power Supply

Typically such a system consists of a microcontroller, a modem IC and the power line interface circuitry. See Figure 11 for the half-duplex power line communication system.

It uses a synchronous FSK-modem, capable of 600 and 1200-baud data rates, and supports two different FSK channels in the 60kHz to 80kHz range. A microcontroller such as the MSP430 is used to control the modem IC.

The OPA561 analog interface circuitry drives the FSK modem signals on the AC power line. It filters the transmit signal (ATO) from the ST7536 to suppress the 2nd-harmonic distortion of the transmit signal. It also amplifies the ATO signal and provides the very low output impedance necessary to properly drive the line. The impedance of a typical power line at 70kHz ranges from 1Ω to 100Ω. The OPA561 is ideal for this type of load. The transformer provides isolation and additional filtering. C_9 prevents 50/60Hz current from flowing in the transformer. This capacitor must be chosen carefully for proper voltage rating and safety characteristics.

The receive input signal is amplified (G = 100) and applied to the modem IC. The OPA561 is disabled in receive mode to avoid loading the line.

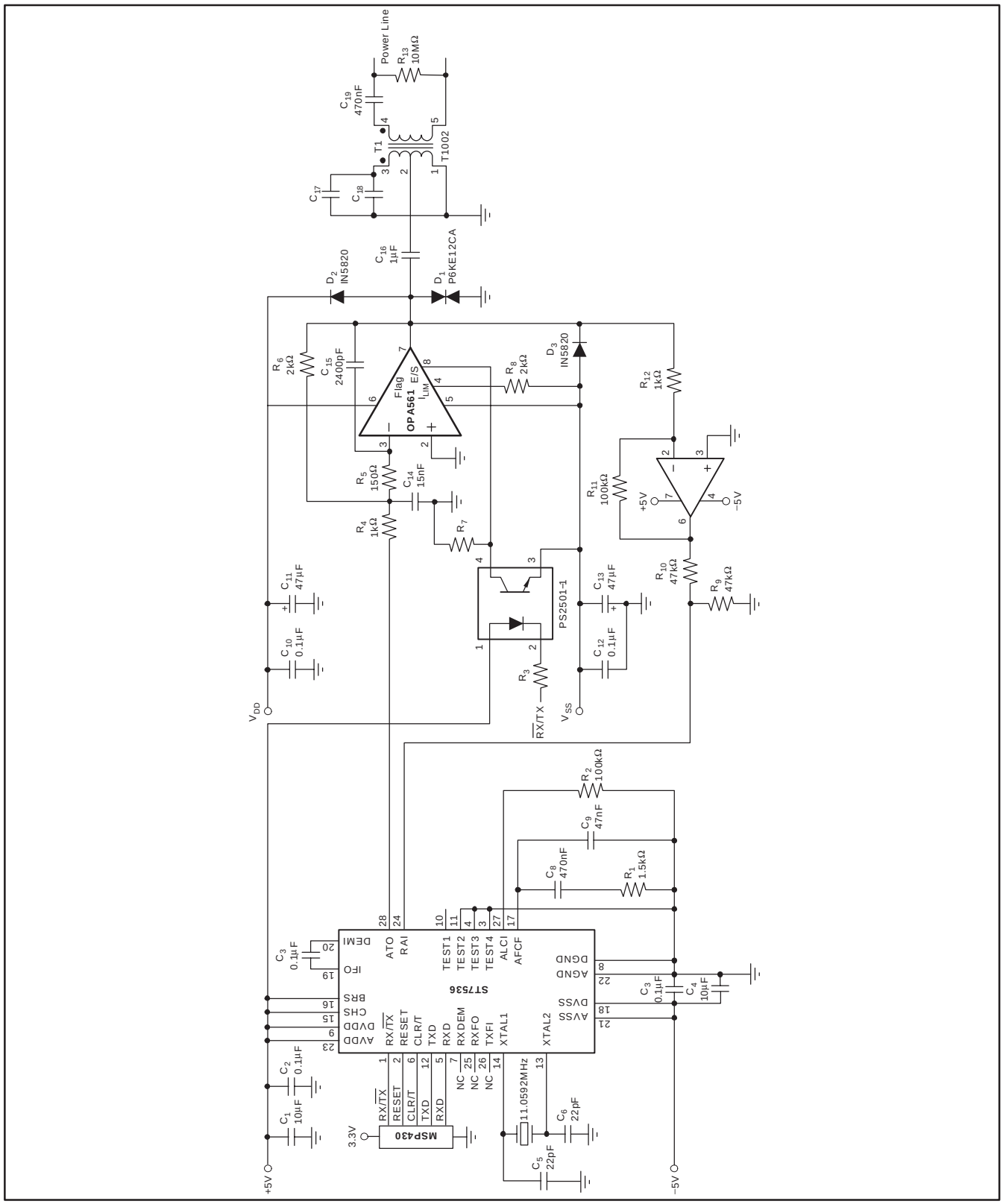


Figure 11. Power Line Communication Driver

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA561PWP	NRND	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA561	
OPA561PWP/2K	NRND	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA561	
OPA561PWP/2KG4	NRND	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA561	
OPA561PWPG4	NRND	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA561	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

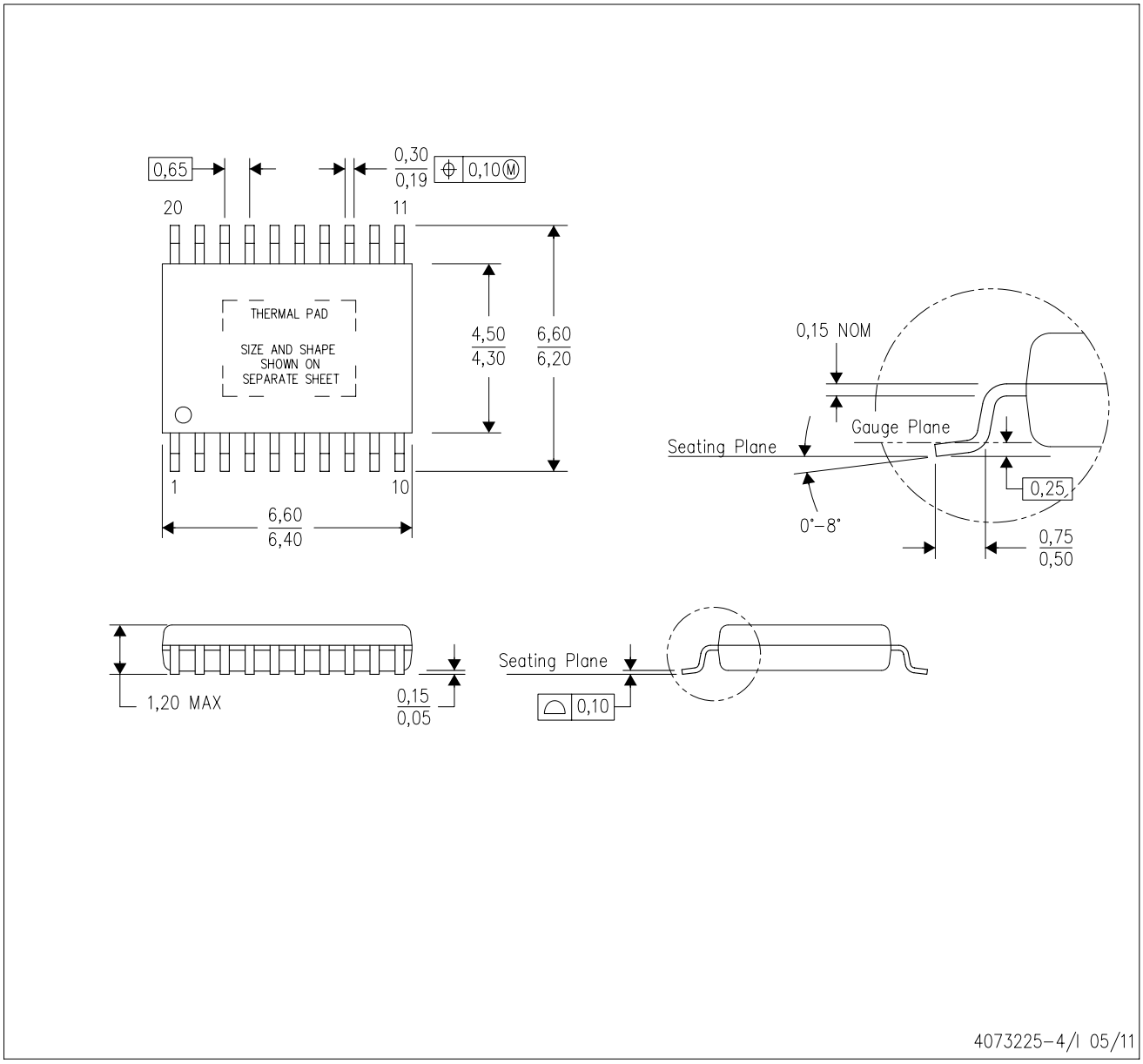
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

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