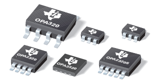


Precision, 20MHz, 0.9pA, Low-Noise, RRIO, CMOS Operational Amplifier with Shutdown

Check for Samples: OPA320, OPA2320, OPA320S, OPA2320S

FEATURES

- **Precision with Zero-Crossover Distortion:**
  - **Low Offset Voltage: 150µV (max)**
  - **High CMRR: 114dB**
  - **Rail-to-Rail I/O**
- **Low Input Bias Current: 0.9pA (max)**
- **Low Noise: 7nV/√Hz at 10kHz**
- **Wide Bandwidth: 20MHz**
- **Slew Rate: 10V/µs**
- **Quiescent Current: 1.45mA/ch**
- **Single-Supply Voltage Range: 1.8V to 5.5V**
- **OPA320S, OPA2320S:**
  - **I_Q in Shutdown Mode: 0.1µA**
- **Unity-Gain Stable**
- **Small Packages:**
  - **SOT23, MSOP, DFN**

APPLICATIONS

- **High-Z Sensor Signal Conditioning**
- **Transimpedance Amplifiers**
- **Test and Measurement Equipment**
- **Programmable Logic Controllers (PLCs)**
- **Motor Control Loops**
- **Communications**
- **Input/Output ADC/DAC Buffers**
- **Active Filters**

DESCRIPTION

The OPA320 (single) and OPA2320 (dual) are a new generation of precision, low-voltage CMOS operational amplifiers optimized for very low noise and wide bandwidth while operating on a low quiescent current of only 1.45mA.

The OPA320 series is ideal for low-power, single-supply applications. Low-noise (7nV/√Hz) and high-speed operation also make them well-suited for driving sampling analog-to-digital converters (ADCs). Other applications include signal conditioning and sensor amplification.

The OPA320 features a linear input stage with zero-crossover distortion that delivers excellent common-mode rejection ratio (CMRR) of typically 114dB over the full input range. The input common-mode range extends 100mV beyond the negative and positive supply rails. The output voltage typically swings within 10mV of the rails.

In addition, the OPAx320 have a wide supply voltage range from 1.8V to 5.5V with excellent PSRR (106dB) over the entire supply range, making them suitable for precision, low-power applications that run directly from batteries without regulation.

The OPA320 (single version) is available in a SOT23-5 package; the OPA320S shut-down single version is available in an SOT23-6 package. The dual OPA2320 is offered in SO-8, MSOP-8, and DFN-8 packages, and the OPA2320S (dual with shut-down) in an MSOP-10 package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA320, OPA320S, OPA2320, OPA2320S	UNIT
Supply voltage, V_S = (V+) – (V–)		6	V
Signal input pins	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short-circuit current(3)		Continuous	mA
Operating temperature, T_A		–40 to +150	°C
Storage temperature, T_{STG}		–65 to +150	°C
Junction temperature, T_J		+150	°C
ESD ratings	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V or ±0.9V to ±2.75V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2, and $\overline{\text{SHDN x}}$ = V_{S+}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA320, OPA320S, OPA2320, OPA2320S MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			40	150	μV
vs Temperature	**dV_{OS}/dT**	**V_S = +5.5V**		**1.5**	**5**	**μV/°C**
vs Power supply	PSR	V_S = +1.8V to +5.5V		5	20	μV/V
Over temperature		**V_S = +1.8V to +5.5V**		**15**		**μV/V**
Channel separation		At 1kHz		130		dB
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-mode rejection ratio	CMRR	V_S = 5.5V, (V–) – 0.1V < V_{CM} < (V+) + 0.1V	100	114		dB
Over temperature			**96**			**dB**
INPUT BIAS CURRENT						
Input bias current	I_B			±0.2	±0.9	pA
Over temperature		**T_A = –40°C to +85°C**			**±50**	**pA**
		OPA2320, OPA2320S, T_A = –40°C to +125°C			**±400**	**pA**
		OPA320, OPA320S, T_A = –40°C to +125°C			**±600**	**pA**
Input offset current	I_{OS}			±0.2	±0.9	pA
Over temperature		**T_A = –40°C to +85°C**			**±50**	**pA**
		T_A = –40°C to +125°C			**±400**	**pA**
NOISE						
Input voltage noise		f = 0.1Hz to 10Hz		2.8		μV_{PP}
Input voltage noise density	e_n	f = 1kHz		8.5		nV/√Hz
		f = 10kHz		7		nV/√Hz
Input current noise density	i_n	f = 1kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
Differential				5		pF
Common-mode				4		pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{OL}	0.1V < V_O < (V+) – 0.1V, R_L = 10kΩ	114	132		dB
		0.1V < V_O < (V+) – 0.1V, R_L = 10kΩ	**100**	**130**		**dB**
		0.2V < V_O < (V+) – 0.2V, R_L = 2kΩ	108	123		dB
		0.2V < V_O < (V+) – 0.2V, R_L = 2kΩ	**96**	**130**		**dB**
Phase margin	PM	V_S = 5V, C_L = 50pF		47		Degrees
FREQUENCY RESPONSE		**V_S = 5.0V, C_L = 50pF**				
Gain bandwidth product	GBP	Unity gain		20		MHz
Slew rate	SR	G = +1		10		V/μs
Settling time	t_S	To 0.1%, 2V step, G = +1		0.25		μs
		To 0.01%, 2V step, G = +1		0.32		μs
		To 0.0015%, 2V step, G = +1 (1)		0.5		μs
Overload recovery time		V_{IN} × G > V_S		100		ns
Total harmonic distortion + noise (2)	THD+N	V_O = $4V_{PP}$, G = +1, f = 10kHz, R_L = 10kΩ		0.0005		%
		V_O = $2V_{PP}$, G = +1, f = 10kHz, R_L = 600Ω		0.0011		%

(1) Based on simulation.
(2) Third-order filter; bandwidth = 80kHz at –3dB.

ELECTRICAL CHARACTERISTICS: V_S = +1.8V to +5.5V or ±0.9V to ±2.75V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, $V_{OUT} = V_S/2$, and $\overline{\text{SHDN x}} = V_{S+}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA320, OPA320S, OPA2320, OPA2320S			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage output swing from both rails	V_O	R_L = 10kΩ		10	20	mV
		R_L = 2kΩ		25	35	mV
Over temperature		**R_L = 10kΩ**			**30**	**mV**
		R_L = 2kΩ			**45**	**mV**
Short-circuit current	I_{SC}	V_S = 5.5V		±65		mA
Capacitive load drive	C_L		See Typical Characteristics			
Open-loop output resistance	R_O	I_O = 0mA, f = 1MHz		90		Ω
SHUTDOWN(3)						
Quiescent current per amplifier	I_{QSD}	All amplifiers disabled, $\overline{\text{SHDN}}$ = V–		0.1	0.5	µA
		OPA2320S only, $\overline{\text{SHDN A}} = V_{S–}$, $\overline{\text{SHDN B}} = V_{S+}$		1.6		mA
		OPA2320S only, $\overline{\text{SHDN A}} = V_{S+}$, $\overline{\text{SHDN B}} = V_{S–}$		1.6		mA
High-level input voltage	V_{IH}	Amplifier enabled, $V_{S–}$ + 0.7 [(V_{S+}) + |$V_{S–}$|]	0.7 × V_{S+}		5.5	V
Low-level input voltage	V_{IL}	Amplifier disabled, $V_{S–}$ + 0.3 [(V_{S+}) + |$V_{S–}$|]			0.3 × V_{S+}	V
Amplifier enable time(4)	t_{ON}	G = 1, V_{OUT} = 0.1 × $V_S/2$, full shutdown(5)		20		µs
		OPA2320S only, partial shutdown(5)		6		
Amplifier disable time(4)	t_{OFF}	G = 1, V_{OUT} = 0.1 × $V_S/2$		3		µs
$\overline{\text{SHDN}}$ pin input bias current (per pin)		V_{IH} = 5V		0.13		µA
		V_{IL} = 0V		0.04		µA
POWER SUPPLY						
Specified voltage range	V_S		1.8		5.5	V
Quiescent current per amplifier	I_Q					
OPA320, OPA320S		I_O = 0mA, V_S = +5.5V		1.5	1.75	mA
Over temperature		**I_O = 0mA, V_S = +5.5V**			**1.85**	**mA**
OPA2320, OPA2320S		I_O = 0mA, V_S = +5.5V		1.45	1.6	mA
Over temperature		**I_O = 0mA, V_S = +5.5V**			**1.7**	**mA**
Power-on time		V+ = 0V to 5V, to 90% I_Q level		28		µs
TEMPERATURE						
Specified range			–40		+125	°C
Operating range			–40		+150	°C

(3) Specified by design and characterization; not production tested.
(4) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time between the 50% point of the signal applied to the $\overline{\text{SHDN}}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(5) Full shutdown refers to the dual OPA2320S having both A and B channels disabled ($\overline{\text{SHDN A}} = \overline{\text{SHDN B}} = V_{S–}$). For partial shutdown, only one $\overline{\text{SHDN}}$ pin is exercised; in this mode, the internal biasing and oscillator remain operational and the enable time is shorter.

THERMAL INFORMATION: OPA320, OPA320S

THERMAL METRIC[(1)]		OPA320	OPA320S	UNITS
		DBV (SOT23)	DBV (SOT23)	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	219.3	177.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	107.5	108.9	
θ_{JB}	Junction-to-board thermal resistance	57.5	27.4	
ψ_{JT}	Junction-to-top characterization parameter	7.4	13.3	
ψ_{JB}	Junction-to-board characterization parameter	56.9	26.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

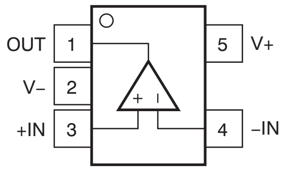
THERMAL INFORMATION: OPA2320, OPA2320S

THERMAL METRIC[(1)]		OPA2320			OPA2320S	UNITS
		D (SO)	DGK (MSOP)	DRG (DFN)	DGS (MSOP)	
		8 PINS	8 PINS	8 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	122.6	174.8	50.6	171.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	67.1	43.9	54.9	43.0	
θ_{JB}	Junction-to-board thermal resistance	64.0	95.0	25.2	91.4	
ψ_{JT}	Junction-to-top characterization parameter	13.2	2.0	0.6	1.9	
ψ_{JB}	Junction-to-board characterization parameter	63.4	93.5	25.3	89.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	5.7	N/A	

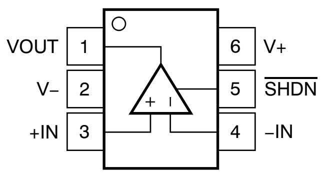
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

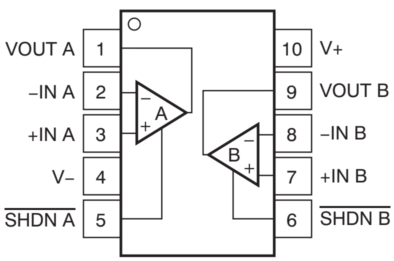
DBV PACKAGE
SOT23-5
(TOP VIEW)



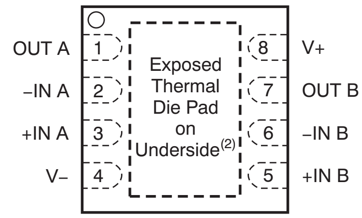
DBV PACKAGE
SOT23-6
(TOP VIEW)



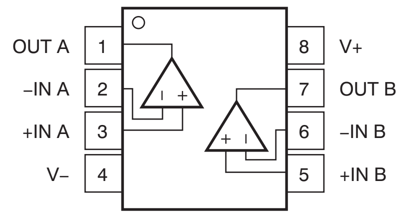
DGS PACKAGE
MSOP-10
(TOP VIEW)



DRG PACKAGE
DFN-8
(TOP VIEW)



D, DGK PACKAGES
SO-8, MSOP-8
(TOP VIEW)



(1) No internal connection.
(2) Connect thermal pad to V–.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

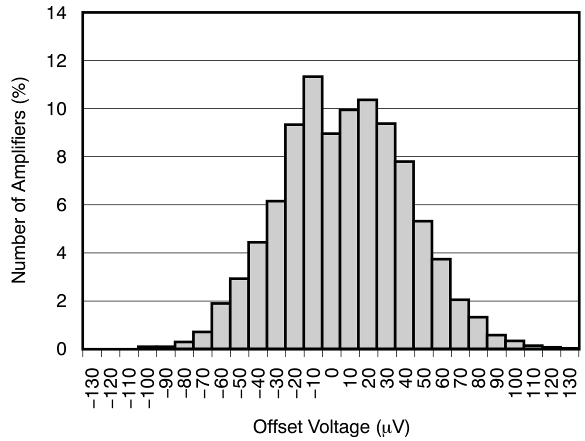


Figure 1.

OFFSET VOLTAGE DRIFT DISTRIBUTION

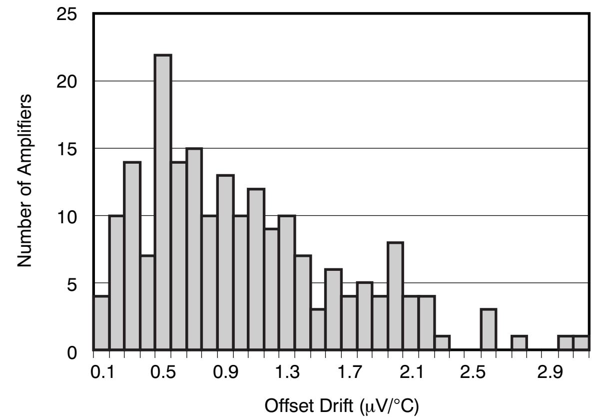


Figure 2.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

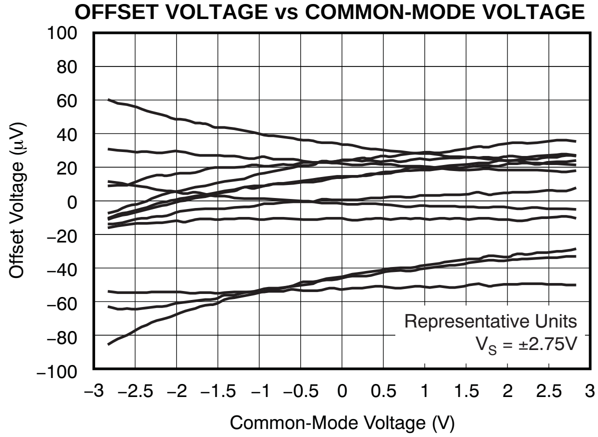


Figure 3.

OPEN-LOOP GAIN/PHASE vs FREQUENCY

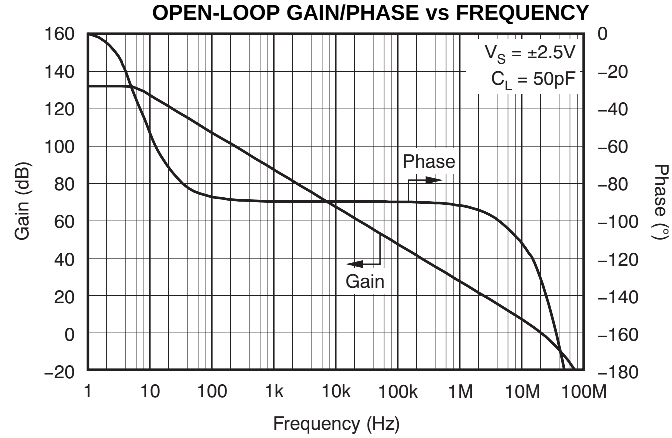


Figure 4.

OPEN-LOOP GAIN vs TEMPERATURE

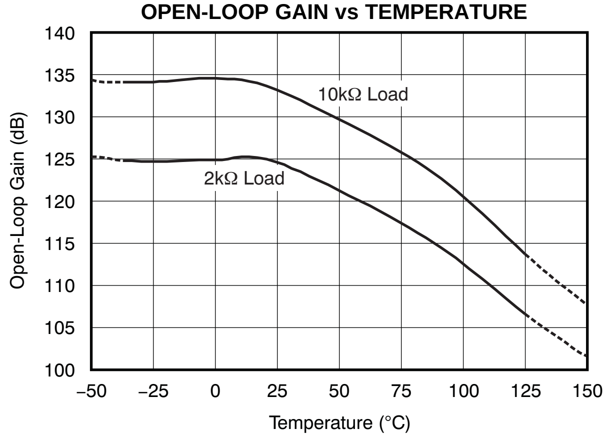


Figure 5.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

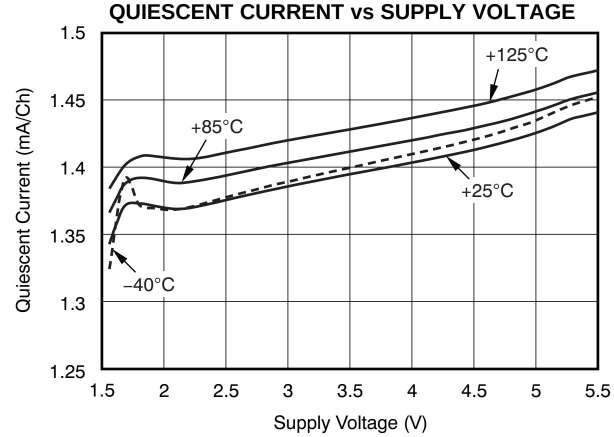


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ, unless otherwise noted.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

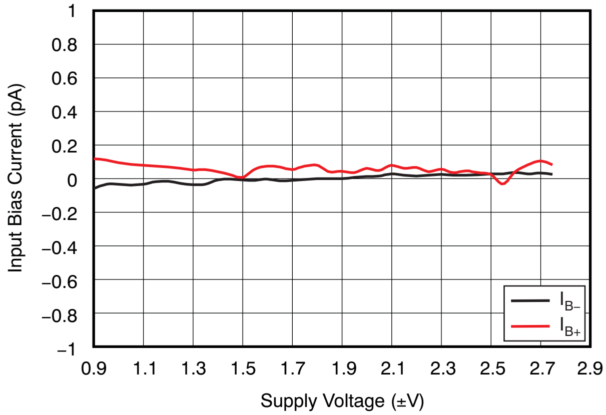


Figure 7.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

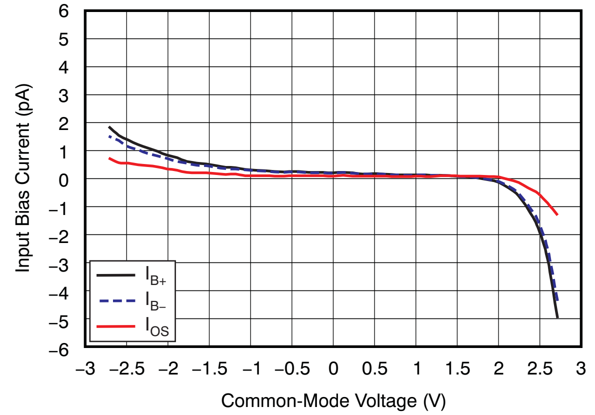


Figure 8.

INPUT BIAS CURRENT DISTRIBUTION

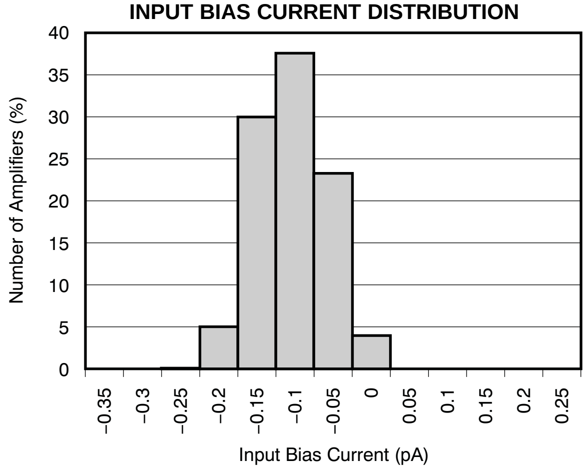


Figure 9.

INPUT BIAS CURRENT vs TEMPERATURE

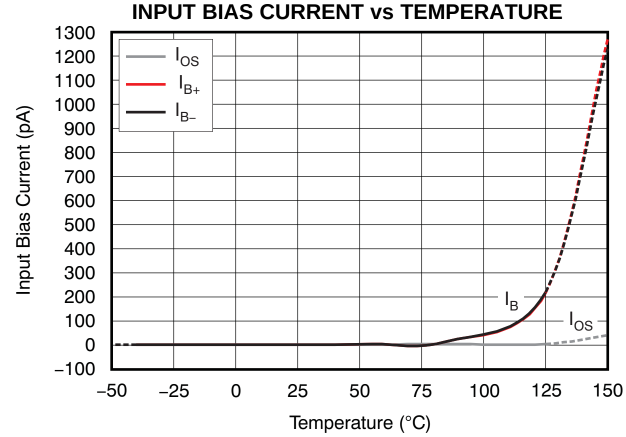


Figure 10.

CMRR AND PSRR vs FREQUENCY

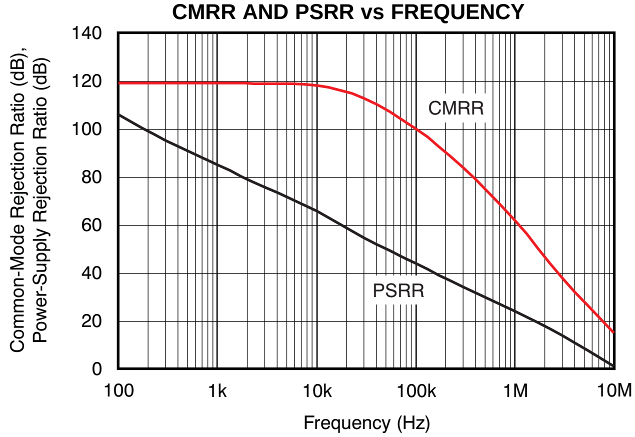


Figure 11.

CMRR AND PSRR vs TEMPERATURE

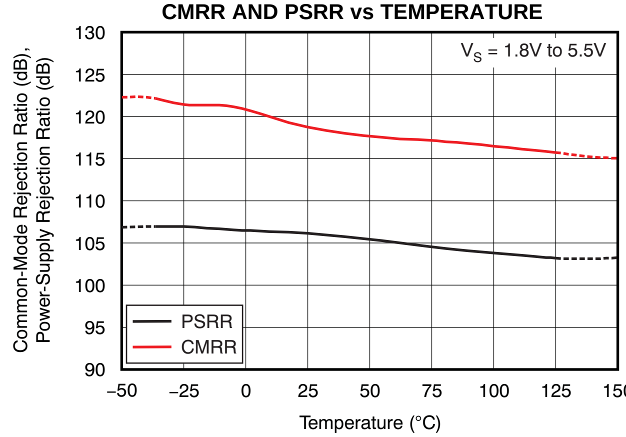


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ, unless otherwise noted.

INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

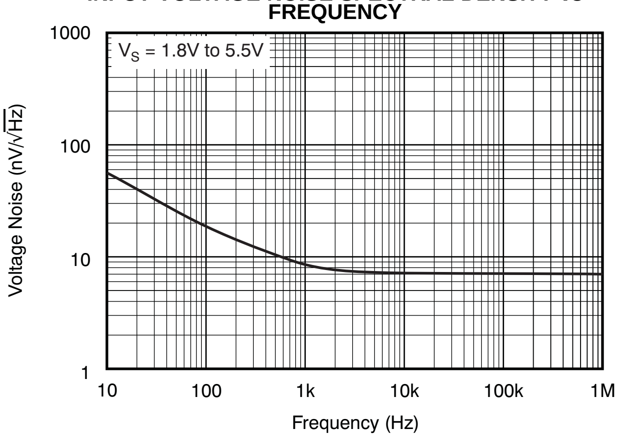


Figure 13.

0.1Hz TO 10Hz INPUT VOLTAGE NOISE

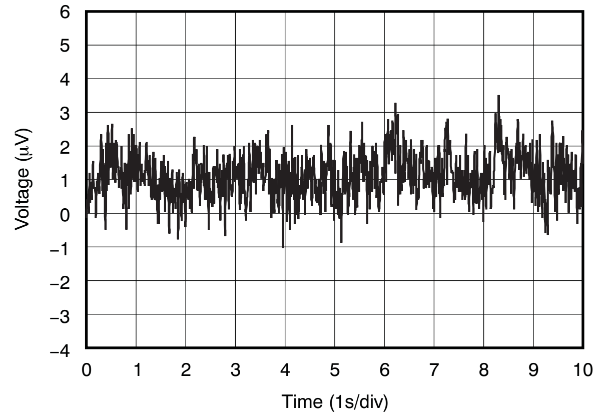


Figure 14.

CLOSED-LOOP GAIN vs FREQUENCY

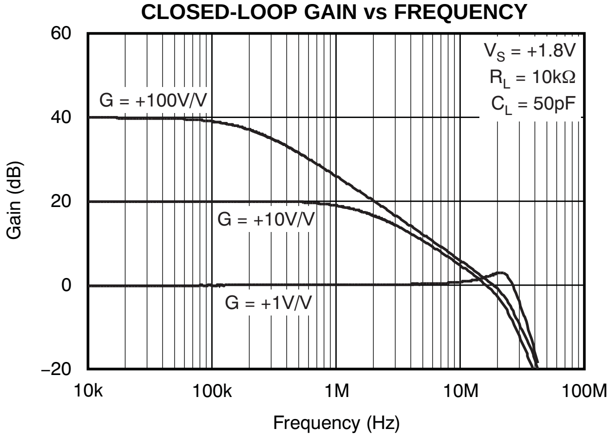


Figure 15.

CLOSED-LOOP GAIN vs FREQUENCY

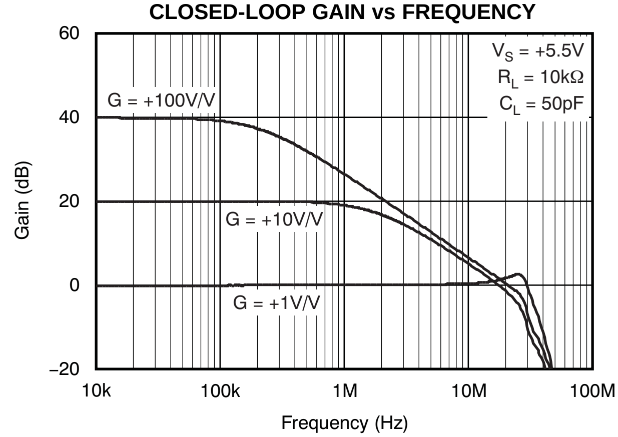


Figure 16.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

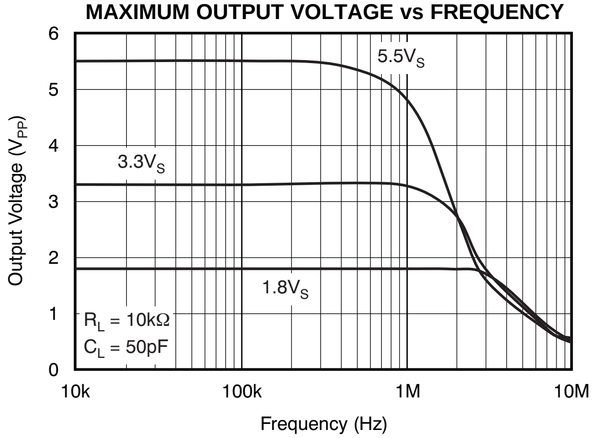


Figure 17.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (MSOP-8)

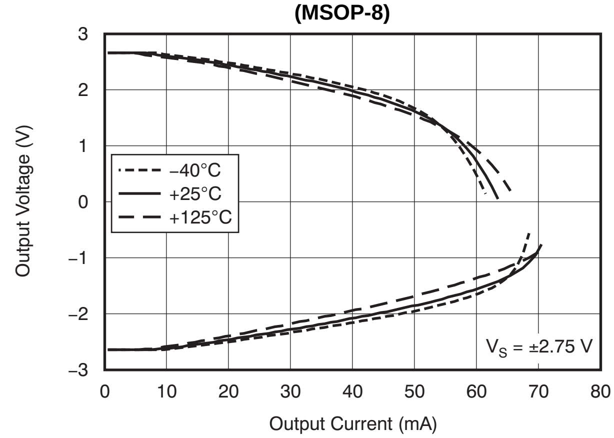


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ, unless otherwise noted.

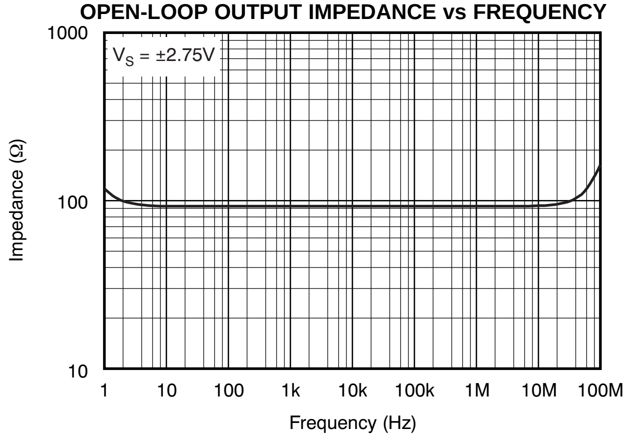


Figure 19.

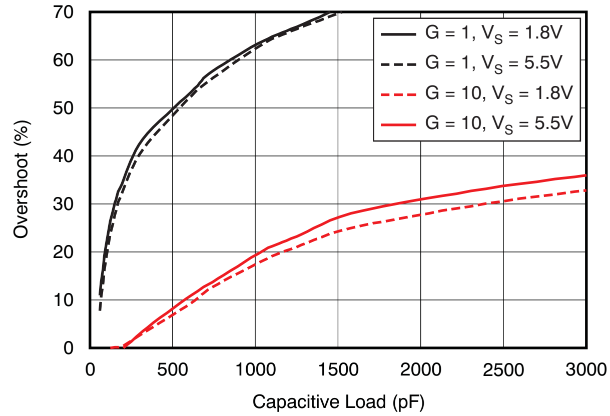


Figure 20.

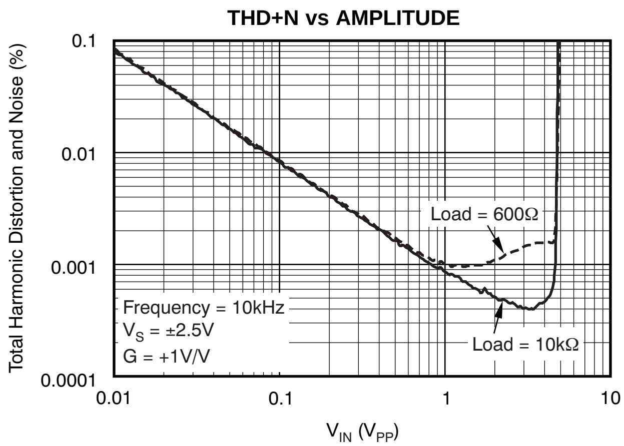


Figure 21.

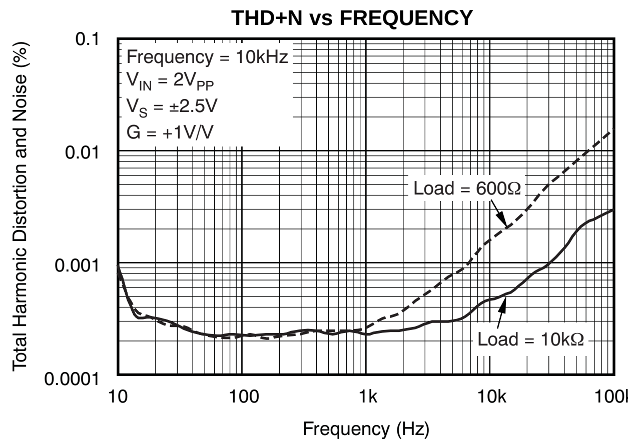


Figure 22.

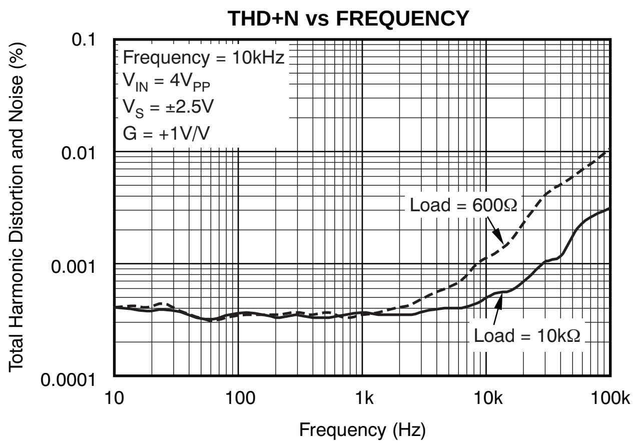


Figure 23.

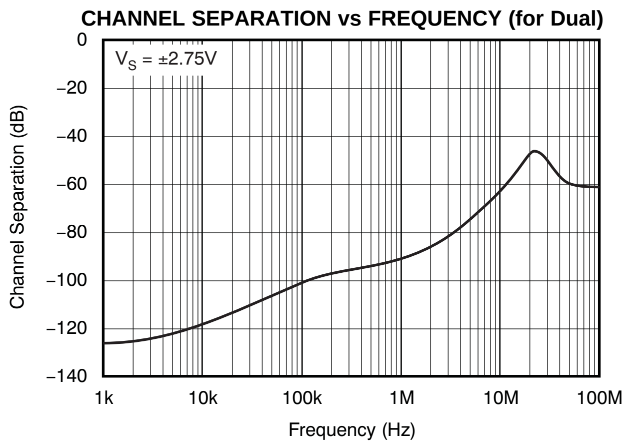


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ, unless otherwise noted.

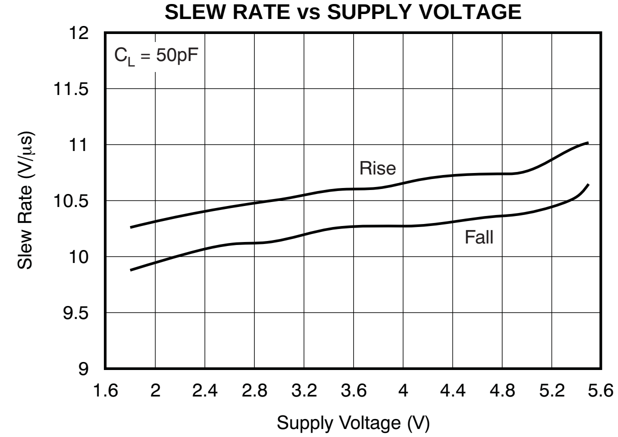


Figure 25.

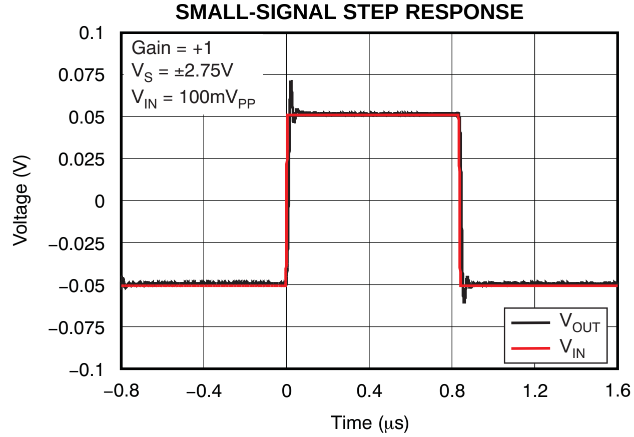


Figure 26.

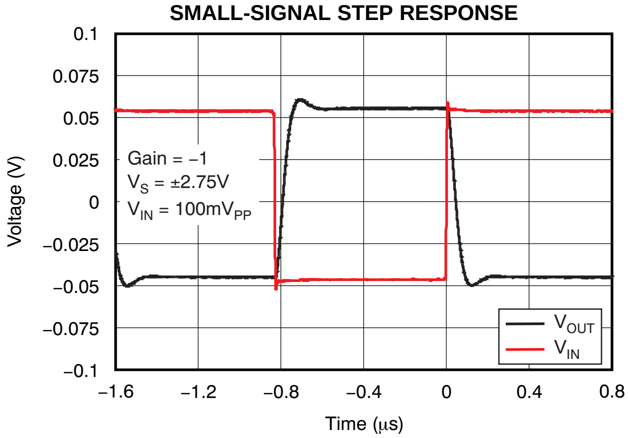


Figure 27.

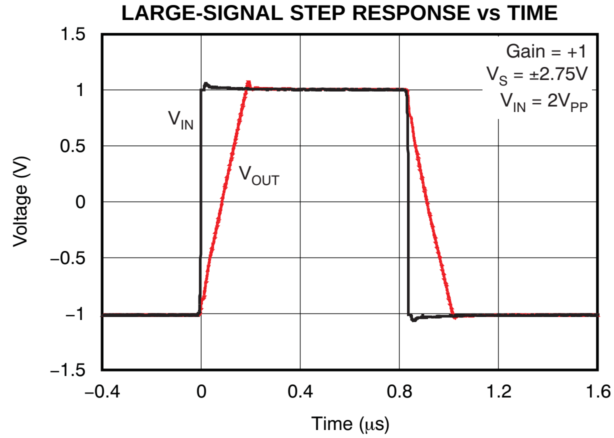


Figure 28.

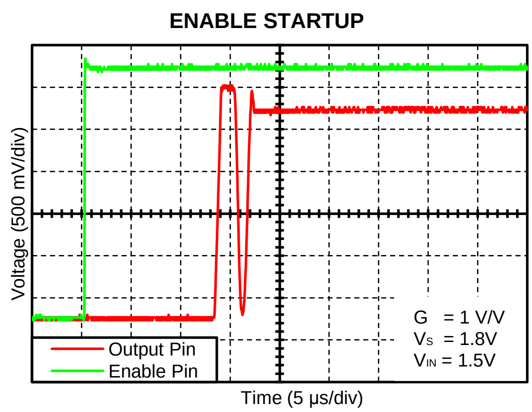


Figure 29.

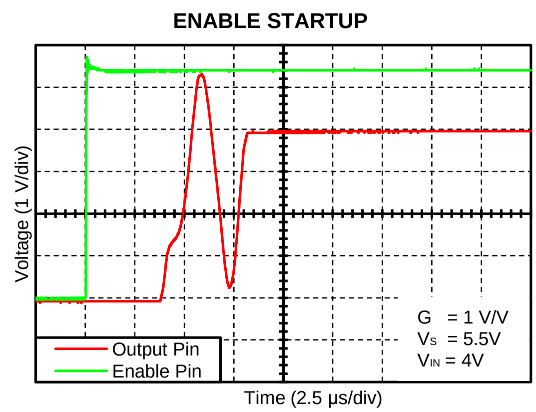


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ, unless otherwise noted.

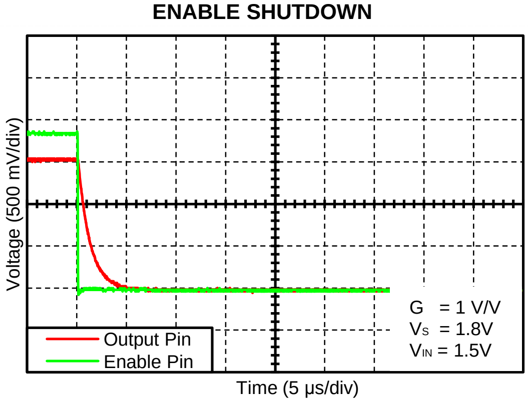


Figure 31.

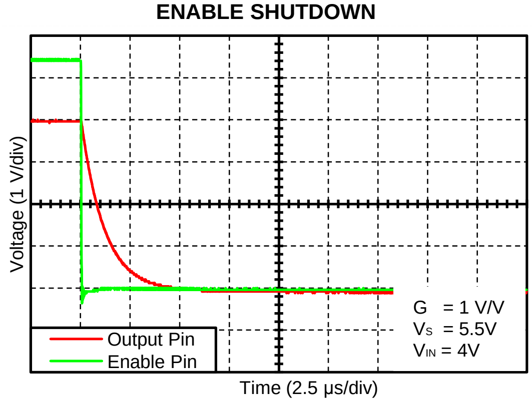


Figure 32.

APPLICATION INFORMATION

OPERATING VOLTAGE

The OPA320 series op amps are unity-gain stable and can operate on a single-supply voltage (1.8V to 5.5V), or a split supply voltage (±0.9V to ±2.75V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001μF to 0.1μF). The OPA320 amplifiers are fully specified from +1.8V to +5.5V and over the extended temperature range of –40°C to +125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

INPUT AND ESD PROTECTION

The OPA320 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, provided that the current is limited to 10mA as stated in the Absolute Maximum Ratings. Many input signals are inherently current-limited to less than 10mA; therefore, a limiting resistor is not required. Figure 33 shows how a series input resistor (R_S) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

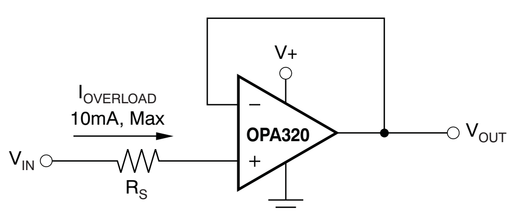


Figure 33. Input Current Protection

RAIL-TO-RAIL INPUT

The OPA320 product family features true rail-to-rail input operation, with supply voltages as low as ±0.9V (1.8V). The design of the OPA320 amplifiers include an internal charge-pump that powers the amplifier input stage with an internal supply rail at approximately 1.6V above the external supply (V_{S+}). This internal supply rail allows the single differential input pair to operate and remain very linear over a very wide input common-mode range. A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary input stage operational amplifiers. This topology allows the OPA320 to provide superior common-mode performance (CMRR > 110dB, typical) over the entire common-mode input range, which extends 100mV beyond both power-supply rails. When driving analog-to-digital converters (ADCs), the highly linear V_{CM} range of the OPA320 assures maximum linearity and lowest distortion.

PHASE REVERSAL

The OPA320 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. Figure 34 shows the input voltage exceeding the supply voltage without any phase reversal.

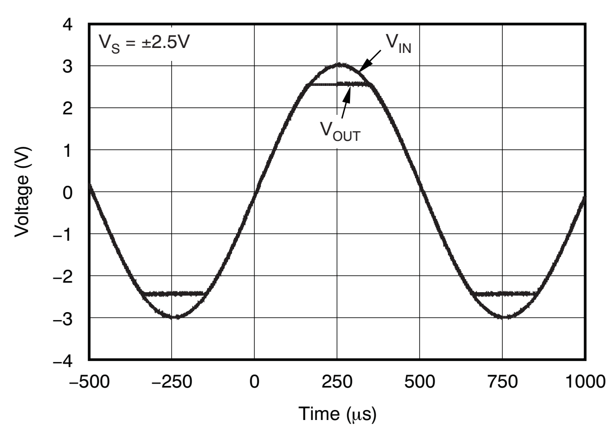
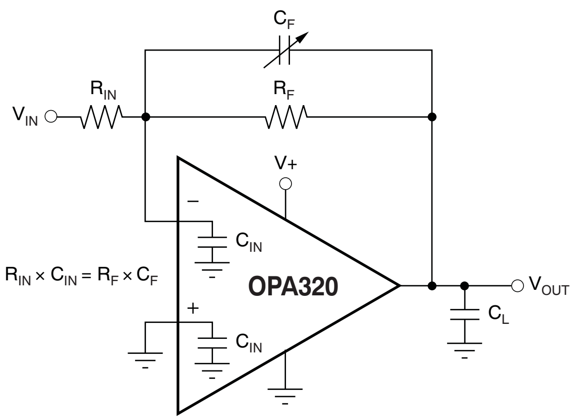


Figure 34. No Phase Reversal

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 35. This capacitor compensates for the zero created by the feedback network impedance and the OPA320 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.



NOTE: Where C_{IN} is equal to the OPA320 input capacitance (approximately 9pF) plus any parasitic layout capacitance.

Figure 35. Feedback Capacitor Improves Dynamic Performance

It is suggested that a variable capacitor be used for the feedback capacitor because input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 35, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA320 (typically 9pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$R_{IN} \times C_{IN} = R_F \times C_F$

Where:

C_{IN} is equal to the OPA320 input capacitance (sum of differential and common-mode) plus the layout capacitance.

The capacitor value can be adjusted until optimum performance is obtained.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA320 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cut-off frequency of approximately 580MHz (–3dB), with a roll-off of 20dB per decade.

OUTPUT IMPEDANCE

The open-loop output impedance of the OPA320 common-source output stage is approximately 90Ω. When the op amp is connected with feedback, this value is reduced significantly by the loop gain. For example, with 130dB (typ) of open-loop gain, the output impedance is reduced in unity-gain to less than 0.03Ω. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPA320 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This in turn prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA320 has excellent capacitive load drive capability for an op amp with its bandwidth.

CAPACITIVE LOAD AND STABILITY

The OPA320 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA320 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (+1V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA320 remains stable with a pure capacitive load up to approximately 1nF.

The equivalent series resistance (ESR) of some very large capacitors (C_L > 1µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 37. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor (R_S), typically 10Ω to 20Ω, in series with the output, as shown in Figure 36.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider may be insignificant. For instance, with a load resistance, R_L = 10kΩ and R_S = 20Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600Ω, which the OPA320 is able to drive, the error increases to 7.5%.

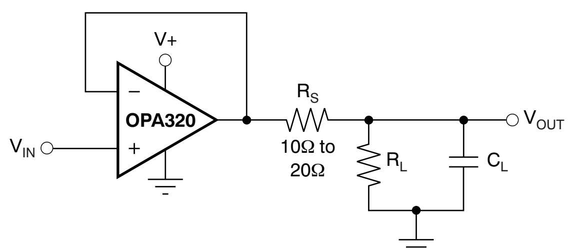


Figure 36. Improving Capacitive Load Drive

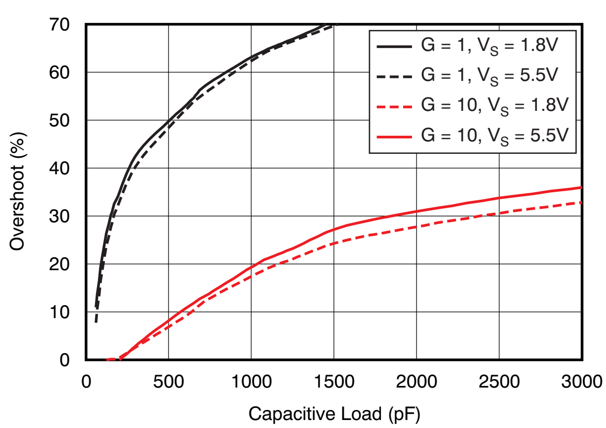


Figure 37. Small-Signal Overshoot versus Capacitive Load (100mV$_{PP}$output step)

OVERLOAD RECOVERY TIME

Overload recovery time is the time it takes the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 38 and Figure 39 show the positive and negative overload recovery times of the OPA320, respectively. In both cases, the time elapsed before the OPA320 comes out of saturation is less than 100ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

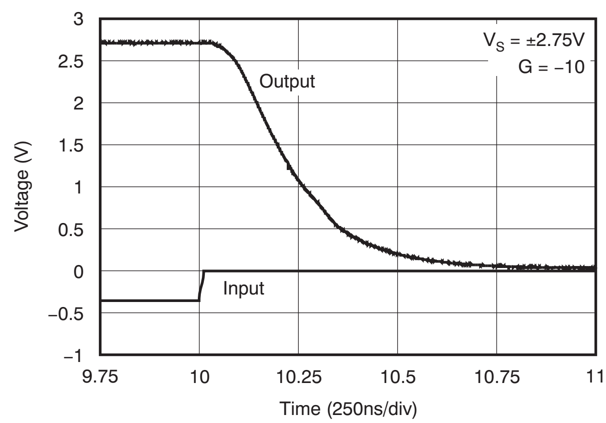


Figure 38. Positive Recovery Time

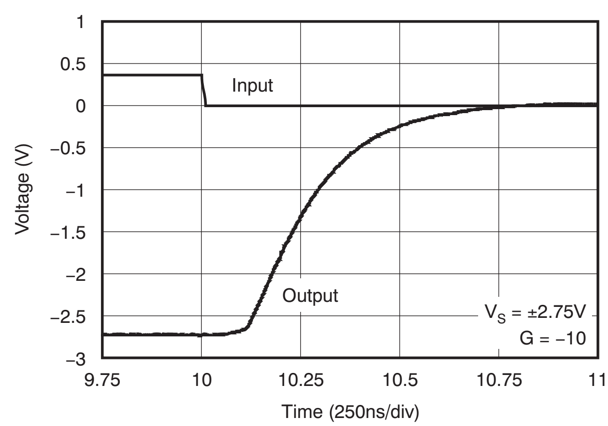


Figure 39. Negative Recovery Time

GENERAL LAYOUT GUIDELINES

The OPA320 is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed circuit board (PCB) layout practices are required. The bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

LEADLESS DFN PACKAGE

The OPA320 series uses the DFN style package (also known as SON), which is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes PCB space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low height (0.8mm).

DFN packages are physically small, have a smaller routing area, improved thermal performance, reduced electrical parasitics, and a pinout scheme that is consistent with other commonly-used packages (such as SO and MSOP). Additionally, the absence of external leads eliminates bent-lead issues.

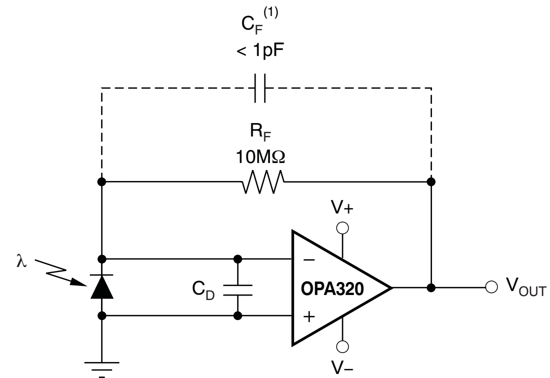
The DFN package can easily be mounted using standard PCB assembly techniques. See Application Report, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com. **The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V–).**

APPLICATION EXAMPLES

TRANSIMPEDANCE AMPLIFIER

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPA320 an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 40, are the expected diode capacitance (C_D), which should include the parasitic input common-mode and differential-mode input capacitance (4pF + 5pF for the OPA320); the desired transimpedance gain (R_F); and the gain-bandwidth (GBW) for the OPA320 (20MHz). With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response. C_F includes the stray capacitance of R_F, which is 0.2pF for a typical surface-mount resistor.



(1) C_F is optional to prevent gain peaking. It includes the stray capacitance of R_F.

Figure 40. Dual-Supply Transimpedance Amplifier

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole should be set to:

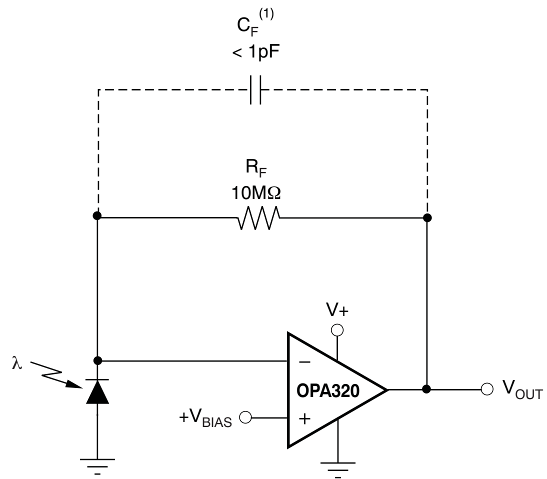
$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \quad (1)$$

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}} \quad (Hz) \quad (2)$$

For even higher transimpedance bandwidth, consider the high-speed CMOS OPA380 (90MHz GBW), OPA354 (100MHz GBW), OPA300 (180MHz GBW), OPA355 (200MHz GBW), or OPA656/57 (400MHz GBW).

For single-supply applications, the +IN input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in Figure 41. This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.



(1) C_F is optional to prevent gain peaking. It includes the stray capacitance of R_F.

Figure 41. Single-Supply Transimpedance Amplifier

For additional information, refer to Application Bulletin (SBOA055), *Compensate Transimpedance Amplifiers Intuitively*, available for download at www.ti.com.

OPTIMIZING THE TRANSIMPEDANCE CIRCUIT

To achieve the best performance, components should be selected according to the following guidelines:

1. For lowest noise, select R_F to create the total required gain. Using a lower value for R_F and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by R_F increases with the square-root of R_F, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce its capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the R_F to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, refer to the Application Bulletins *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060), and *Noise Analysis for High-Speed Op Amps* (SBOA066), available for download at the TI web site.

HIGH-IMPEDANCE SENSOR INTERFACE

Many sensors have high source impedances that may range up to 10MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 42, where ($V_{IN+} = V_S - I_{BIAS} \times R_S$). The last term, $I_{BIAS} \times R_S$, shows the voltage drop across R_S. To prevent errors introduced to the system as a result of this voltage, an op amp with very low input bias current must be used with high impedance sensors. This low current keeps the error contribution by $I_{BIAS} \times R_S$ less than the input voltage noise of the amplifier, so that it does not become the dominant noise factor. The OPA320 series of op amps feature very low input bias current (typically 200fA), and are therefore ideal choices for such applications.

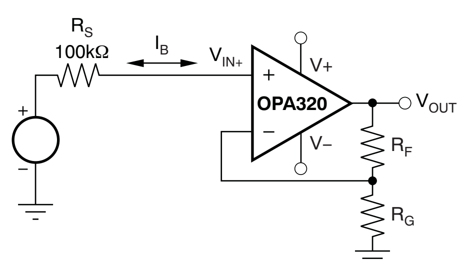


Figure 42. Noise as a Result of I_{BIAS}

DRIVING ADCS

The OPA320 series op amps are well-suited for driving sampling analog-to-digital converters (ADCs) with sampling speeds up to 1MSPS. The zero-crossover distortion input stage topology allows the OPA320 to drive ADCs without degradation of differential linearity and THD.

The OPA320 can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. Figure 44 shows the OPA320 configured to drive the ADS8326.

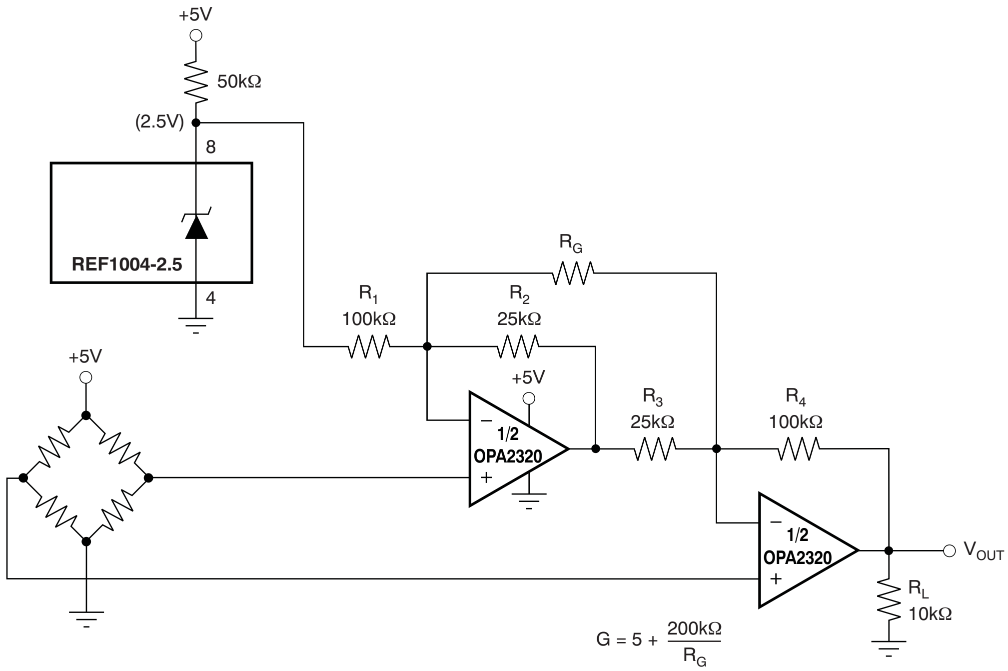
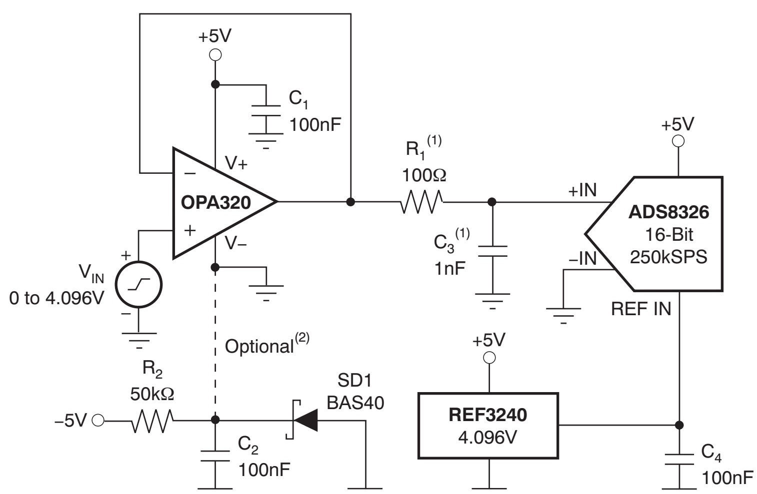


Figure 43. Two Op Amp Instrumentation Amplifier with Improved High-Frequency Common-Mode Rejection



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3V supply to allow output swing to true ground potential.

Figure 44. Driving the ADS8326

ACTIVE FILTER

The OPA320 is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 45 shows a 500kHz, second-order, low-pass filter using the multiple−feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

1. adding an inverting amplifier;
2. adding an additional second-order MFB stage; or
3. using a noninverting filter topology, such as the Sallen-Key (shown in Figure 46).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

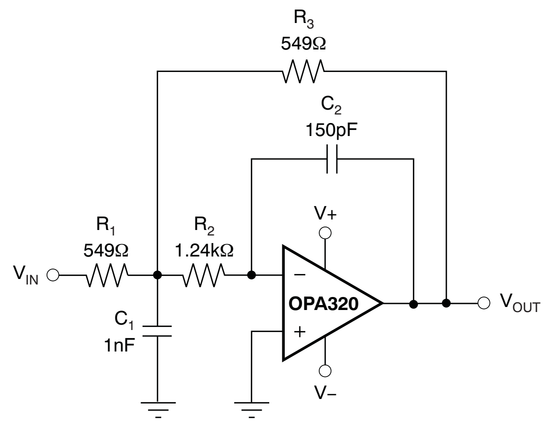


Figure 45. Second-Order Butterworth 500kHz Low-Pass Filter

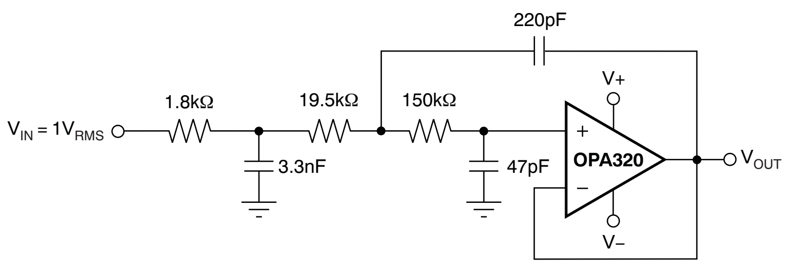


Figure 46. OPA320 Configured as a Three-Pole, 20kHz, Sallen-Key Filter

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2320AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2320A	Samples
OPA2320AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OCLQ	Samples
OPA2320AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OCLQ	Samples
OPA2320AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2320A	Samples
OPA2320AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCMQ	Samples
OPA2320AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCMQ	Samples
OPA2320SAIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPAI	Samples
OPA2320SAIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPAI	Samples
OPA320AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAC	Samples
OPA320AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAC	Samples
OPA320SAIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAE	Samples
OPA320SAIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAE	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

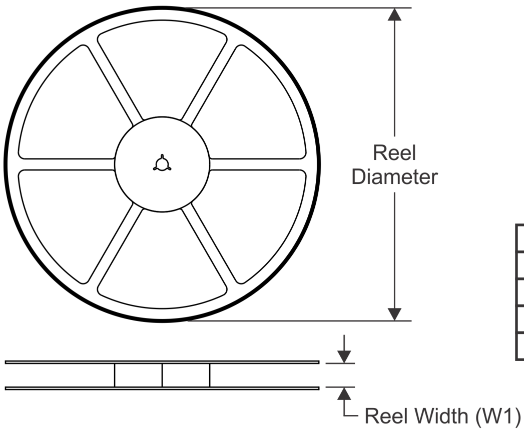
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

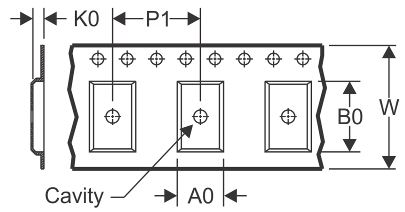
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

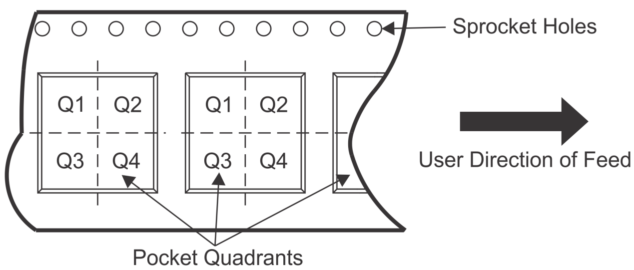


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

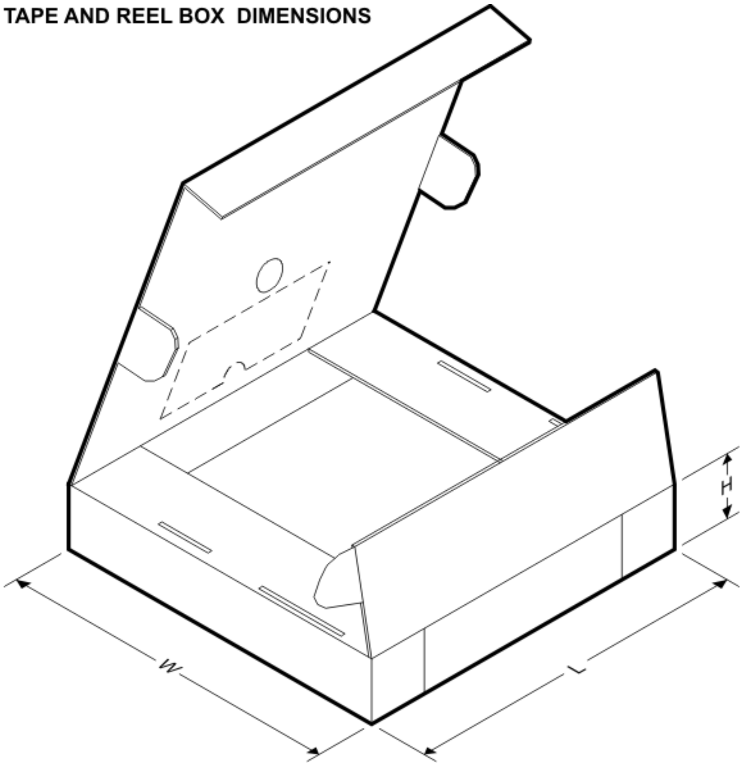
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2320AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2320AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2320AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2320AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2320AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2320AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2320SAIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2320SAIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA320AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

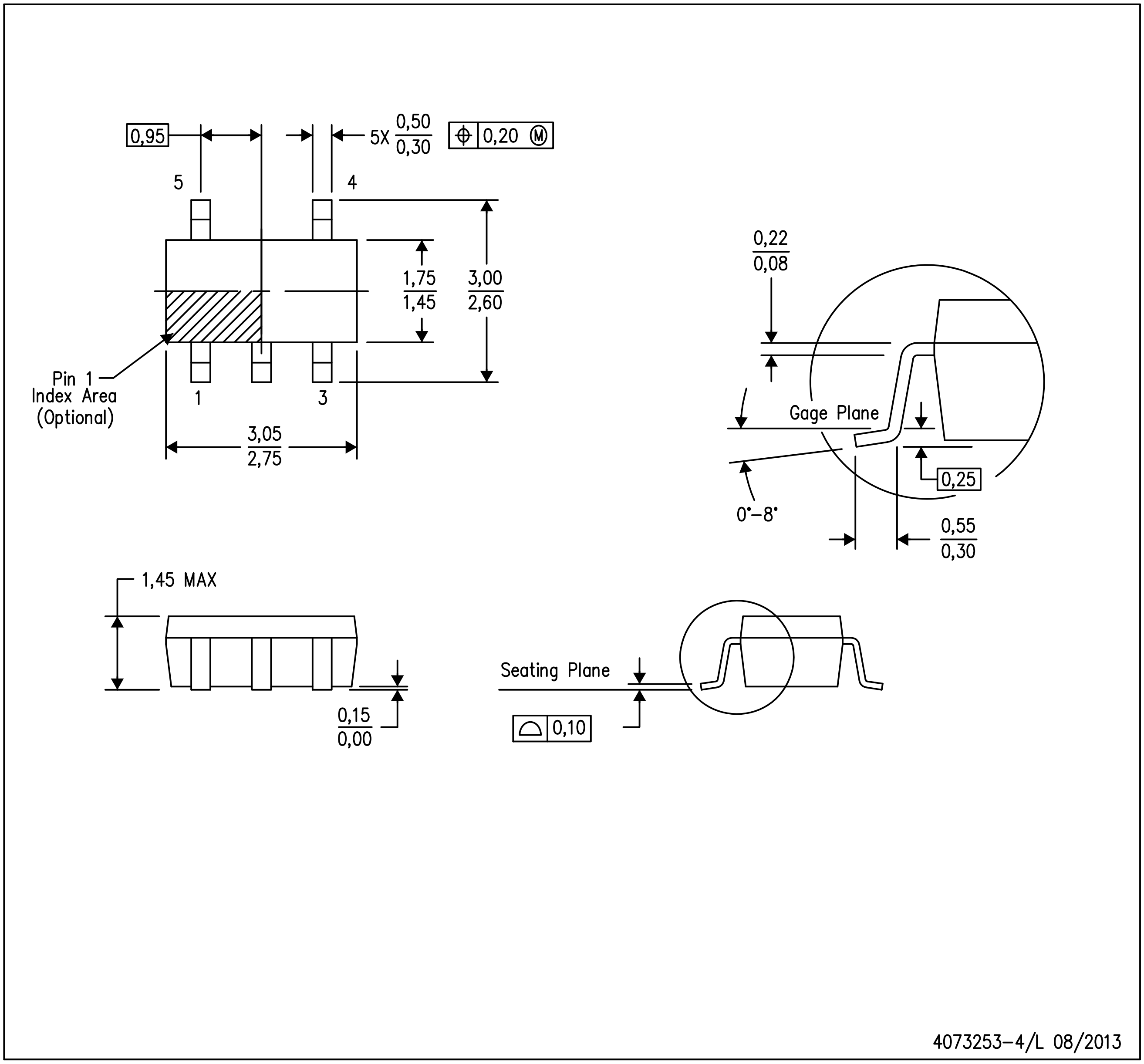
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

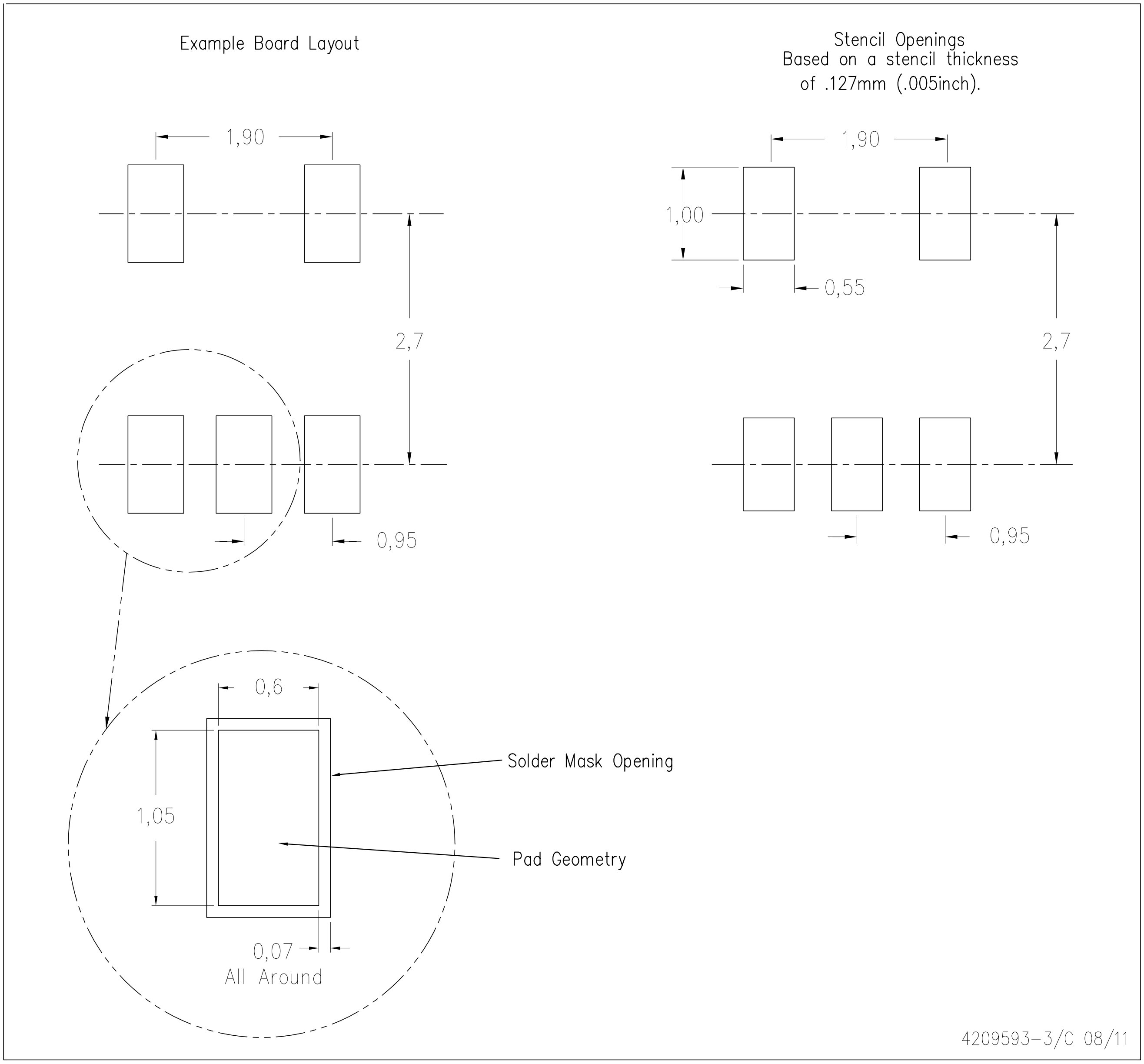
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2320AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2320AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2320AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2320AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2320AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA2320AIDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA2320SAIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2320SAIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA320AIDBVT	SOT-23	DBV	5	250	195.0	200.0	45.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



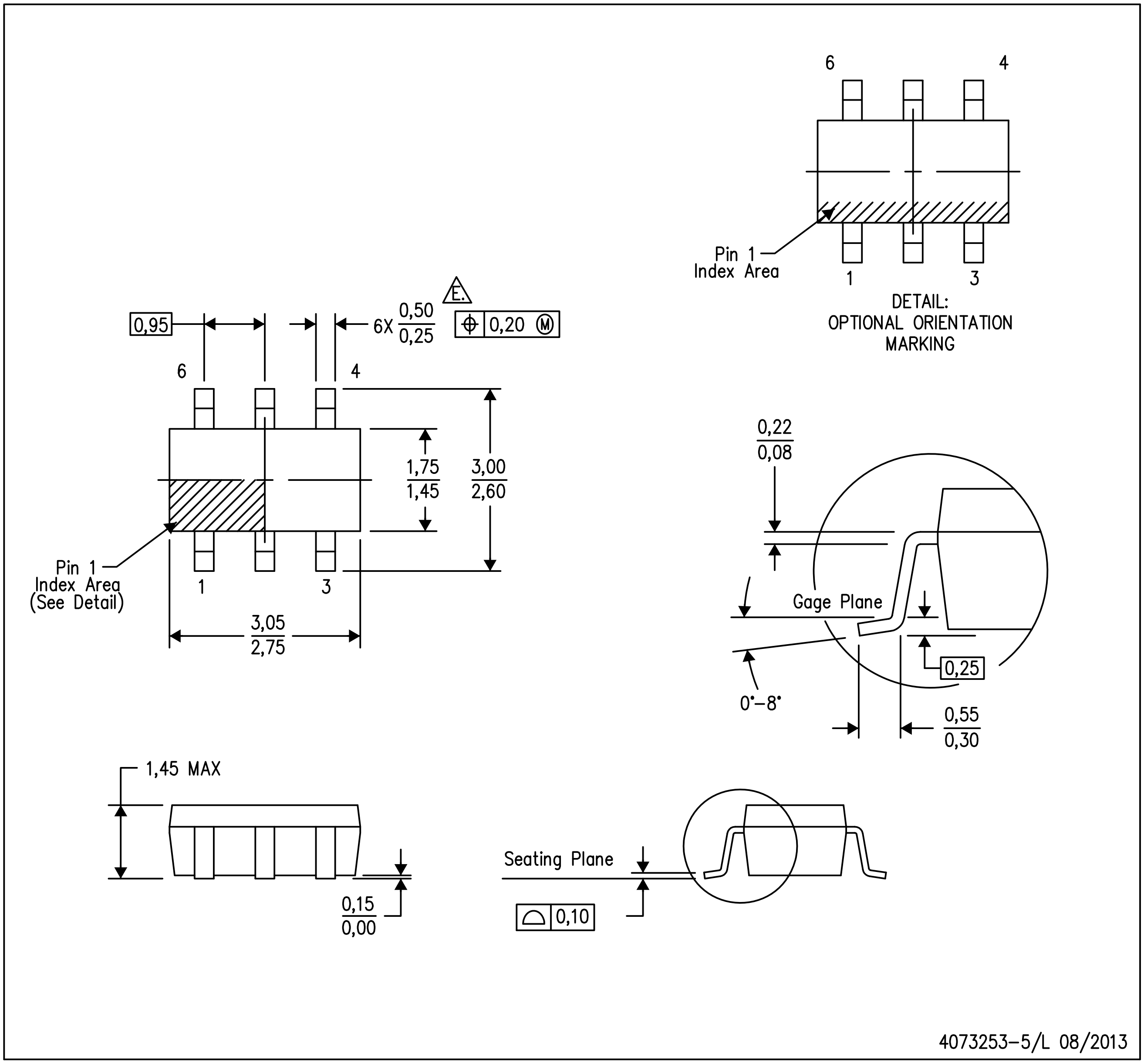
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



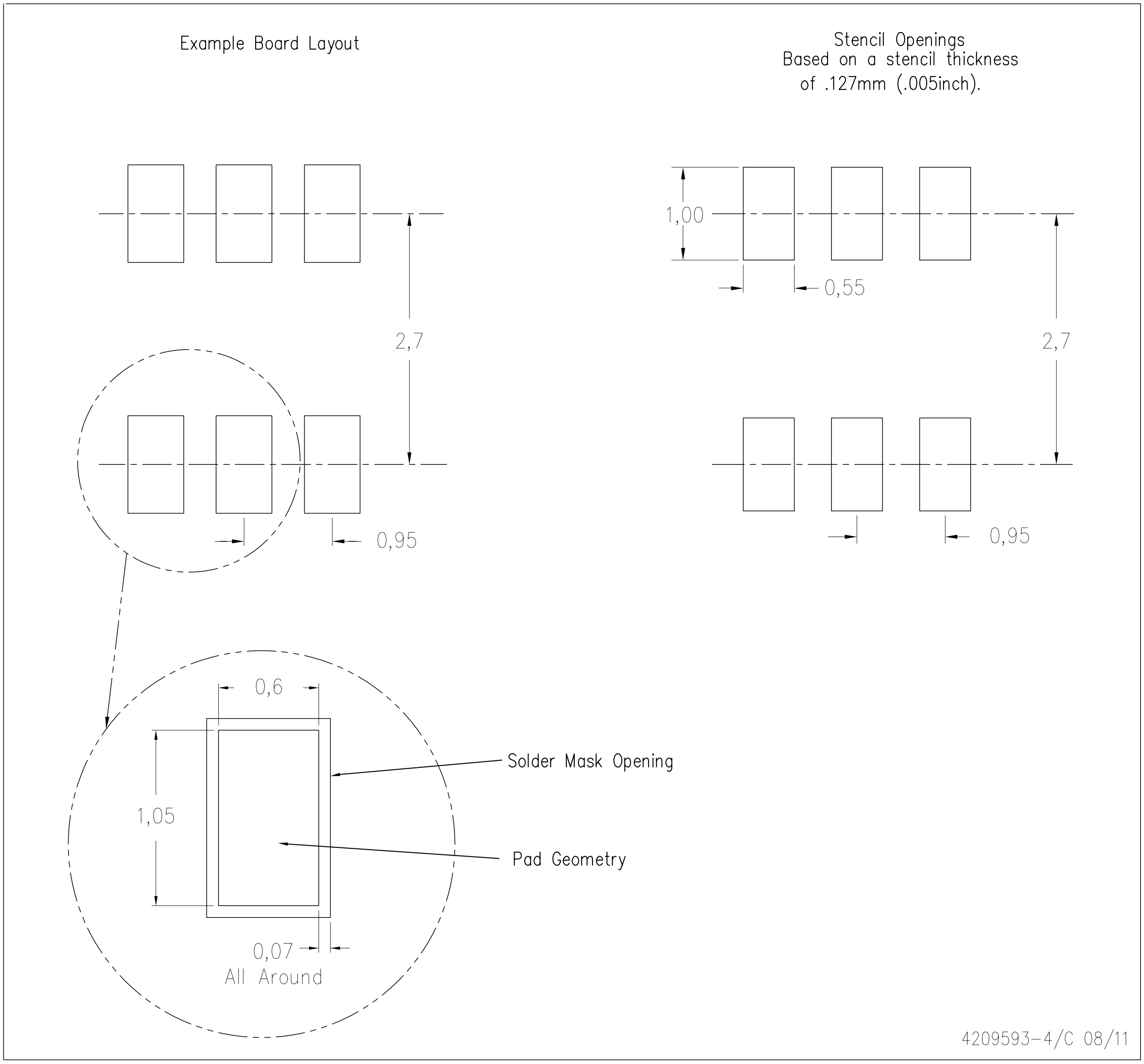
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



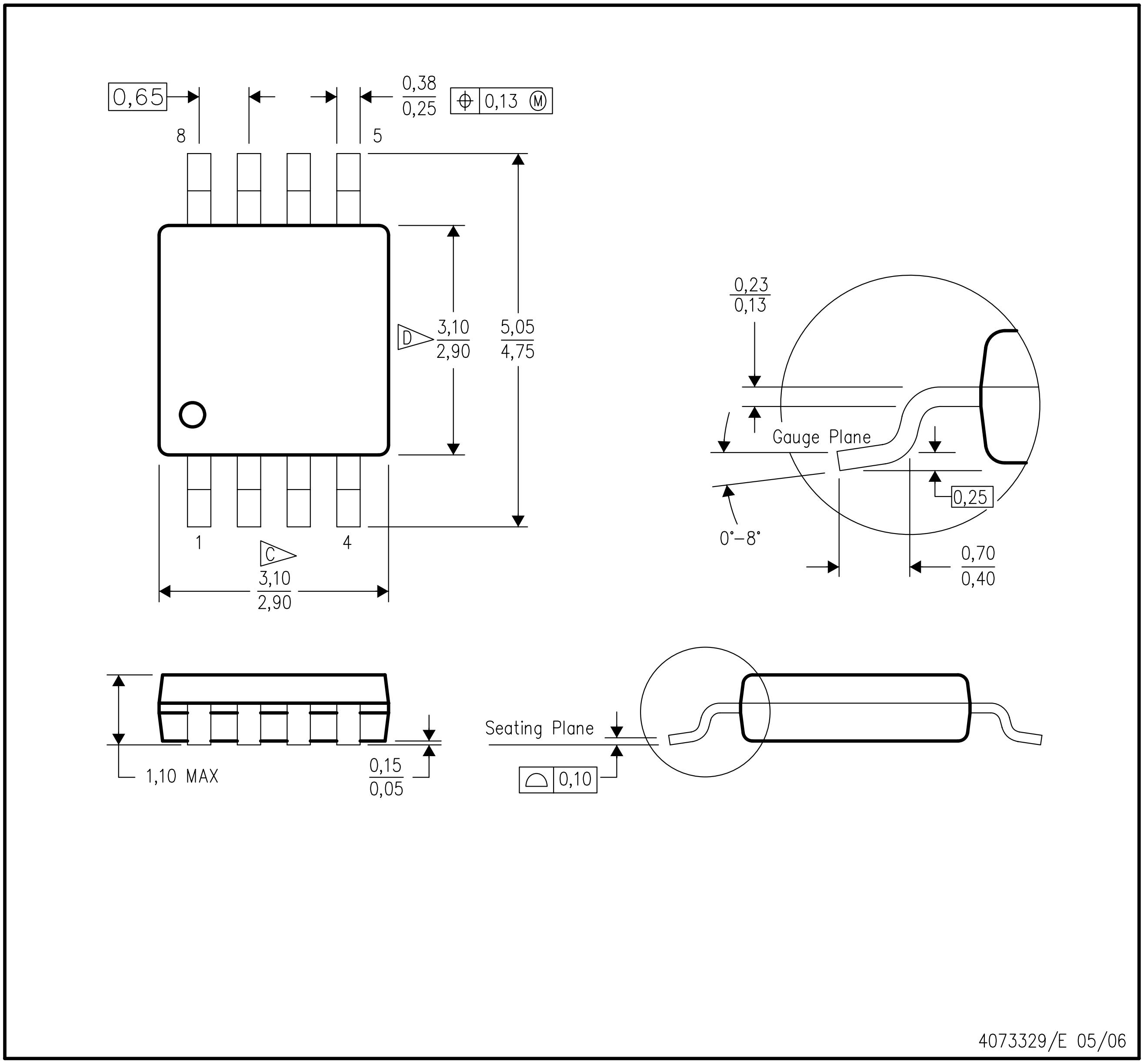
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



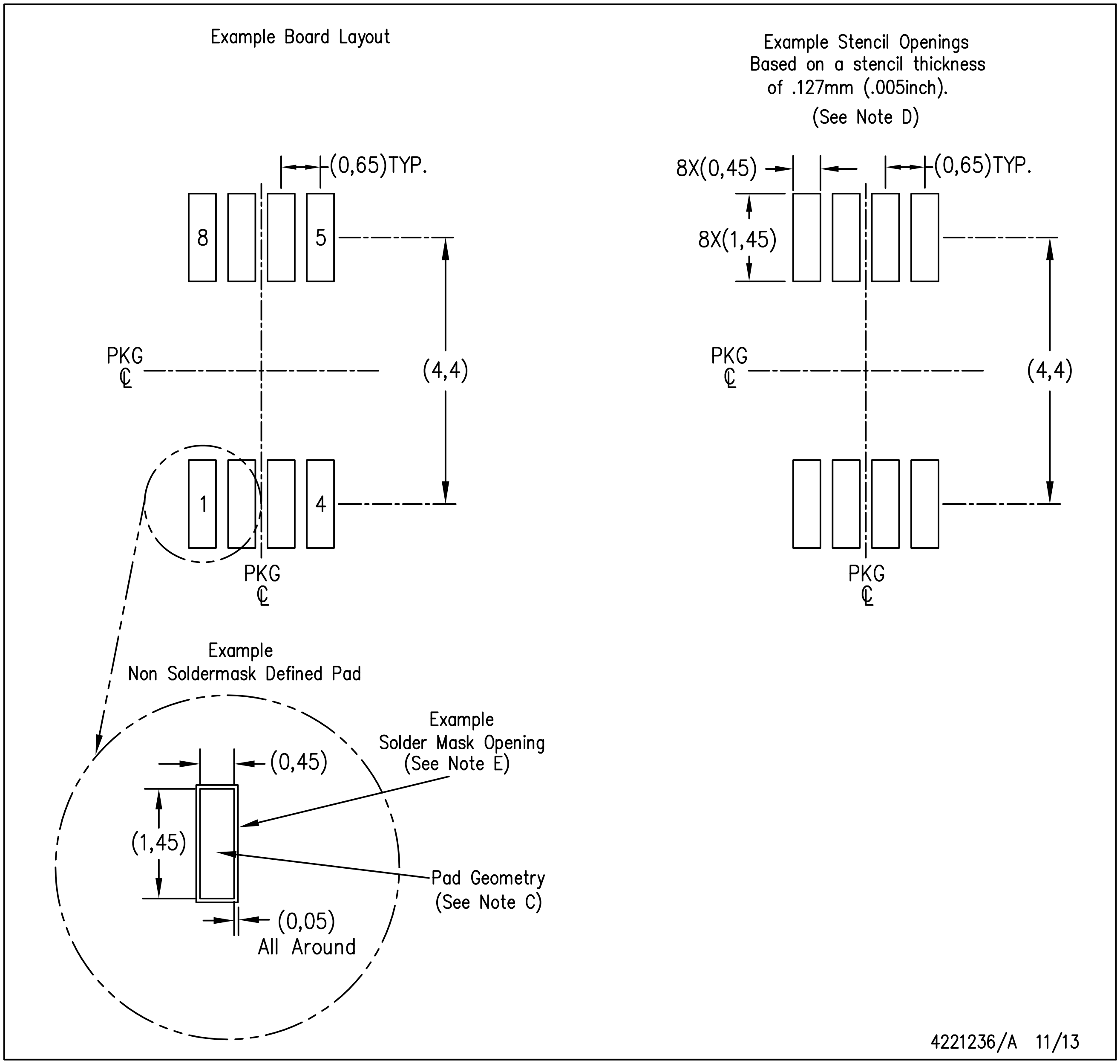
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



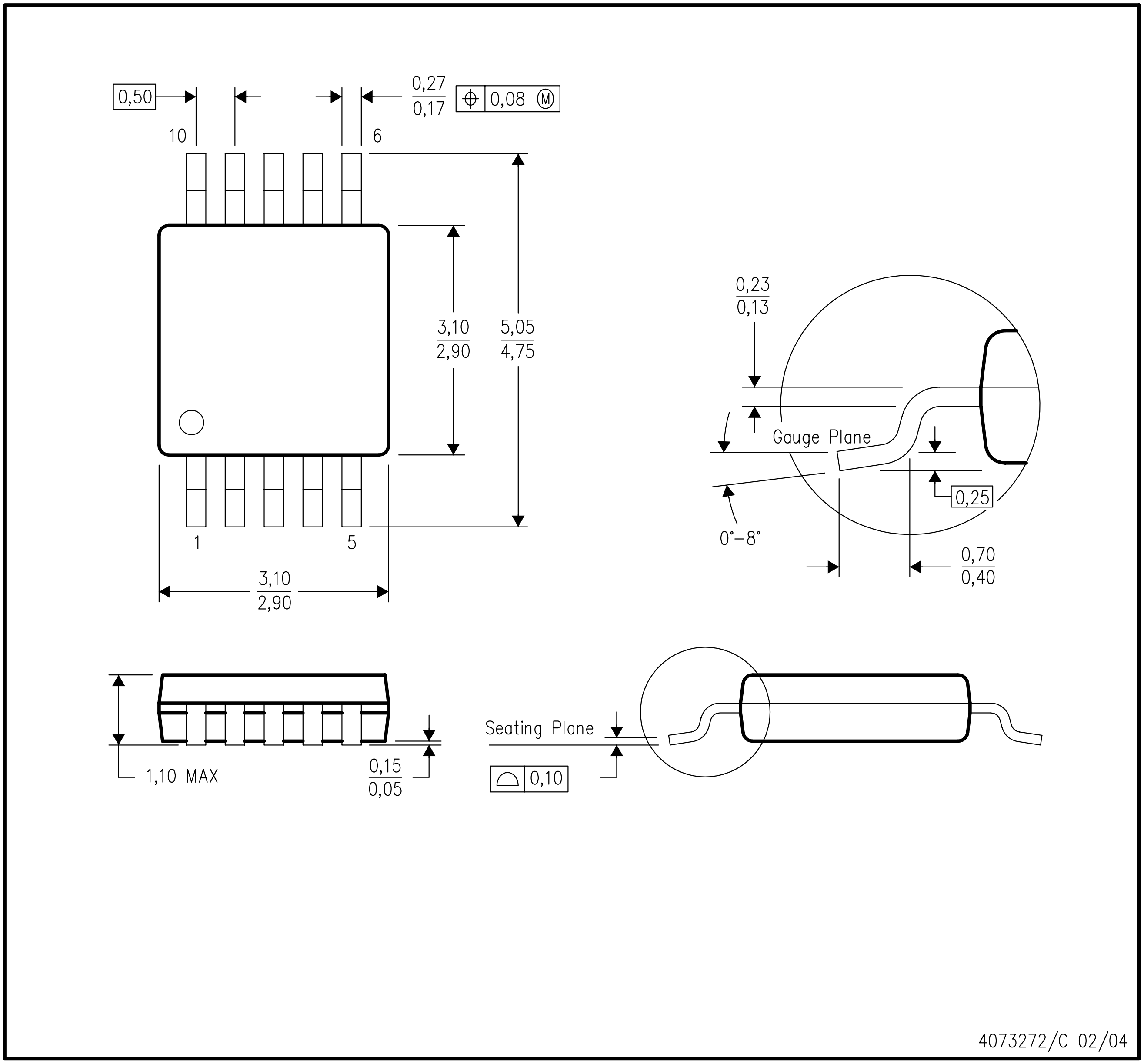
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



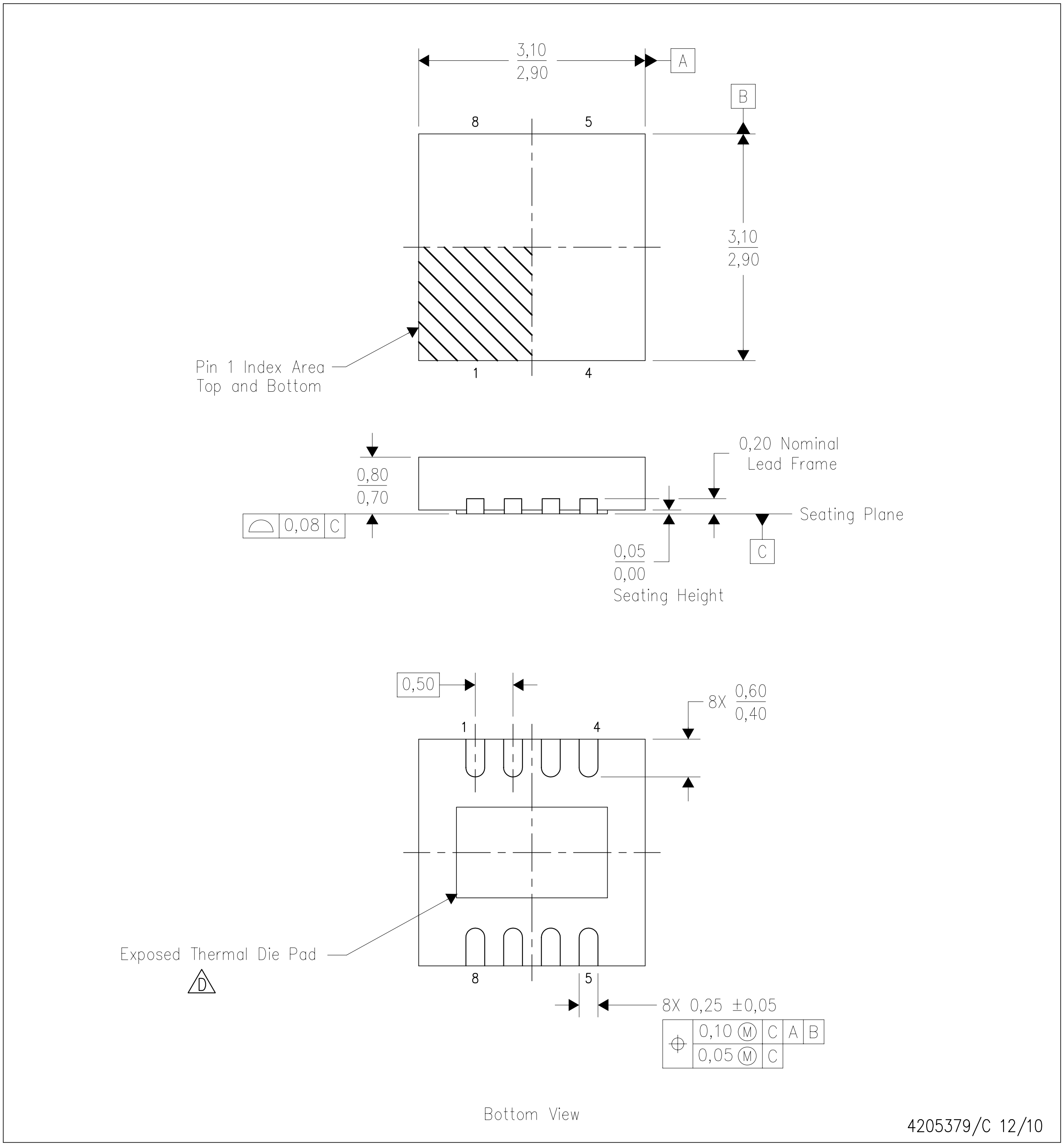
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187 variation BA.

DRG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. JEDEC MO-229 package registration pending.

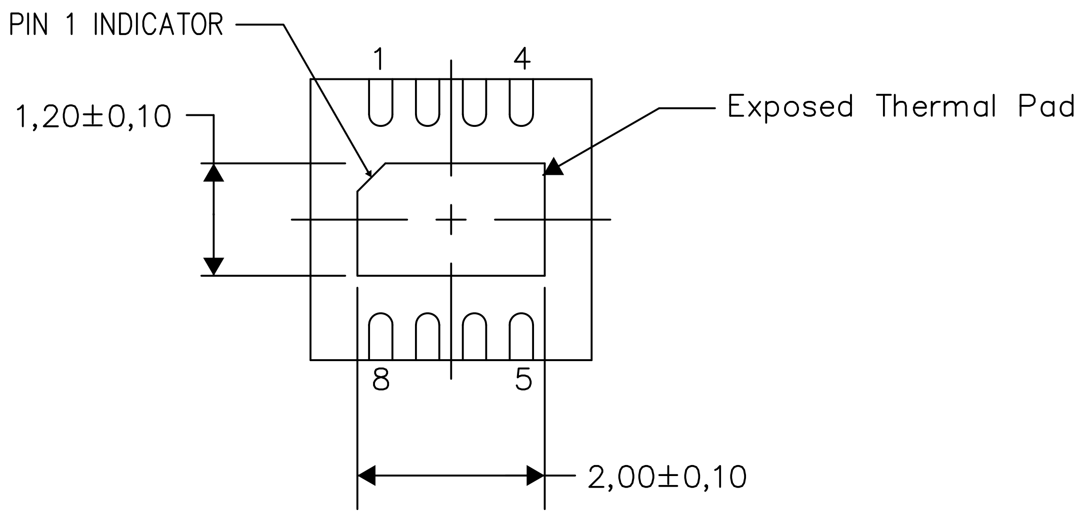
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



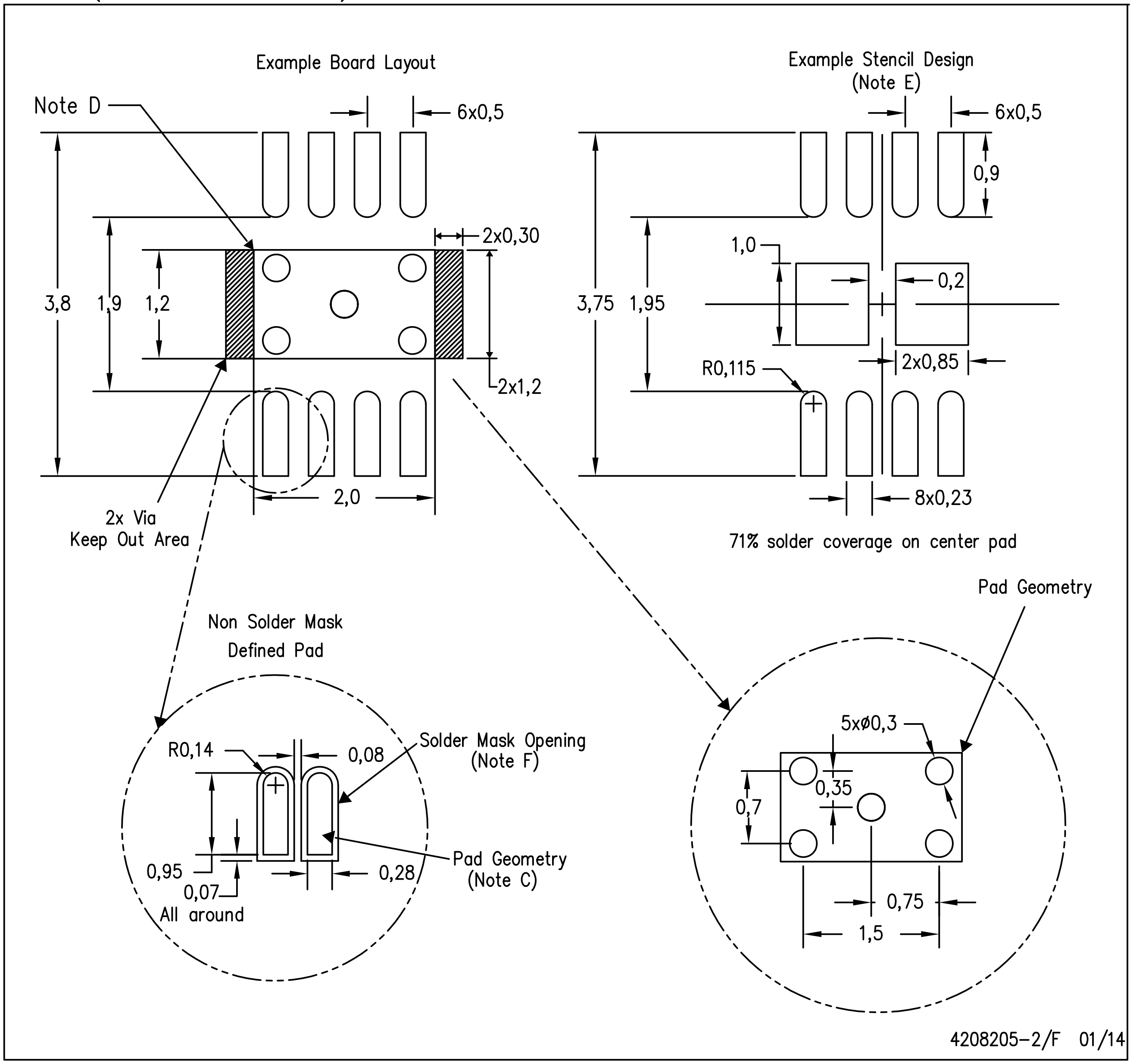
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/H 12/13

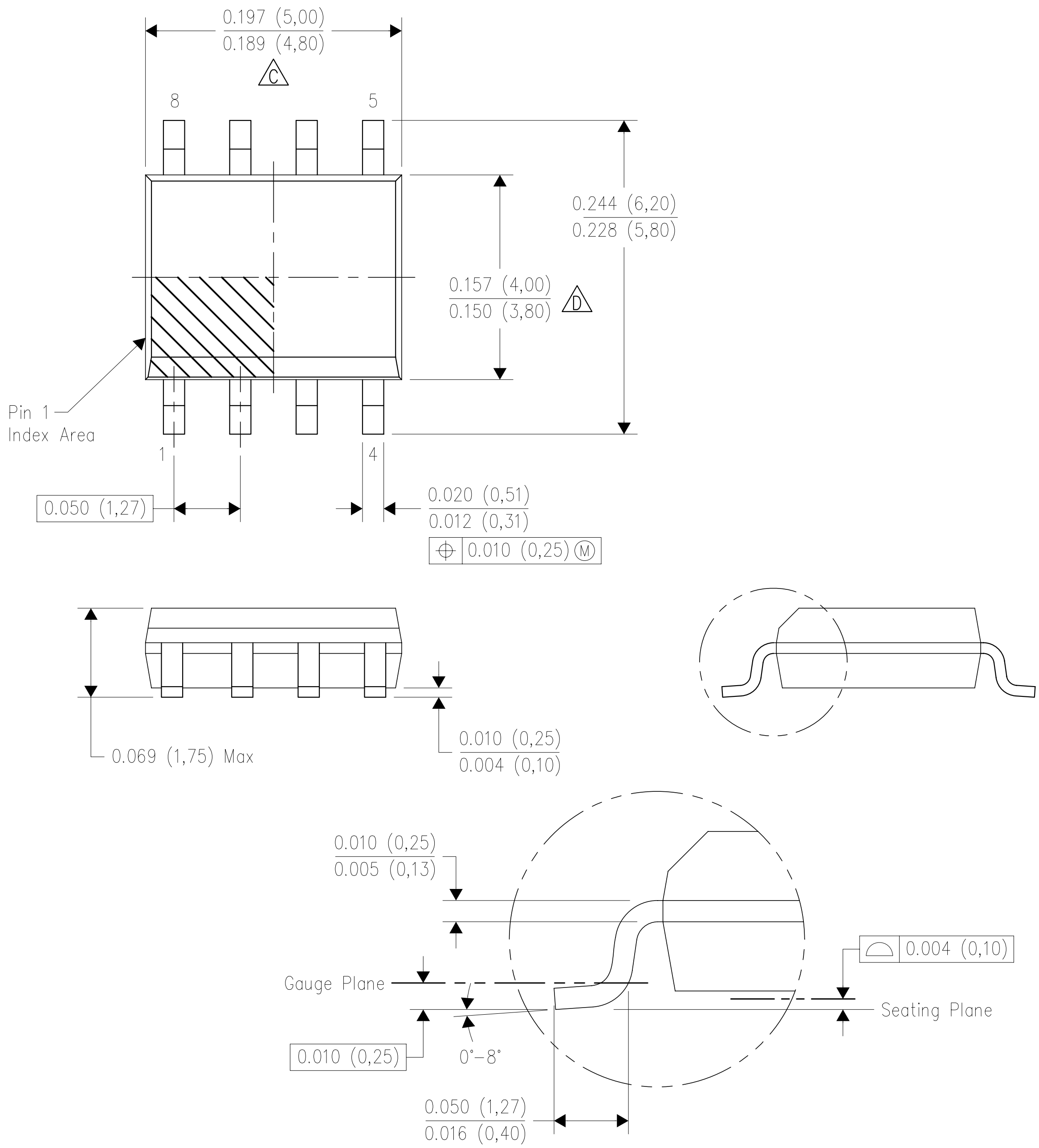
NOTE: All linear dimensions are in millimeters

DRG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-SM-782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

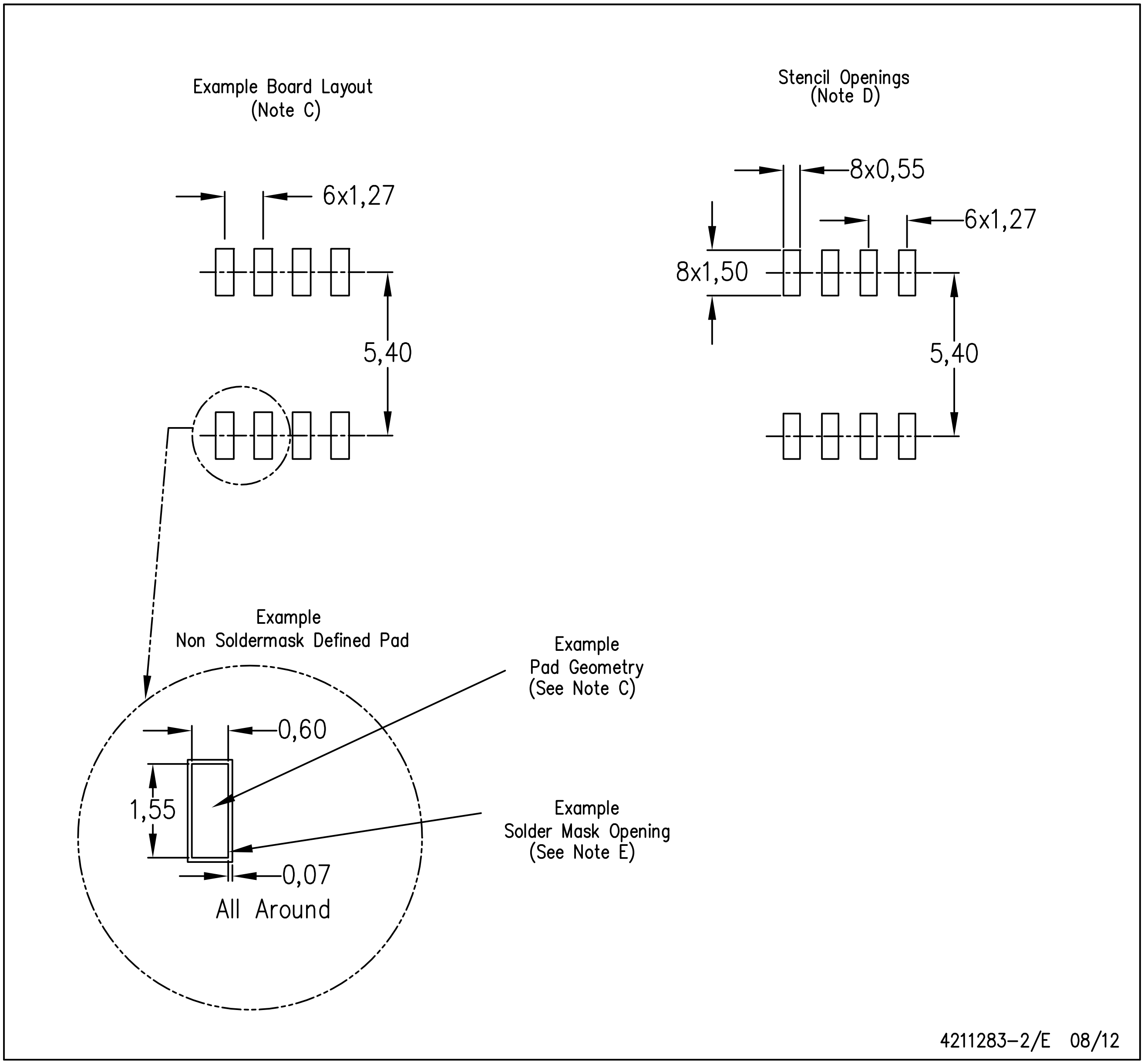
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040047–3/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.