DEVICE SPECIFICATION

OM8373; OM8378

TV signal processor- Closed Caption decoder with embedded μ-Controller

Tentative Device Specification 2004 Jan 15

Version: 1.0 Previous version:

Philips Semiconductors

PHILIPS

TV signal processor- Closed Caption decoder with embedded μ-Controller

OM8373; OM8378

GENERAL DESCRIPTION

The OM8373 and OM8378 combine the functions of a video processor together with a μ-Controller and US Closed Caption decoder. The ICs are intended to be used in economy television receivers with 110° picture tubes.

The ICs have supply voltages of 8 V and 3.3 V and they are mounted in a SDIP-64 envelope.

The features are given in the following feature list.

FEATURES

TV-signal processor

- Vision IF circuit suitable for negative modulation with alignment-free PLL demodulator
- Internal (switchable) time-constant for the IF-AGC circuit
- The mono intercarrier sound circuit has a selective FM-PLL demodulator which can be switched to the different FM sound frequencies (4.5/5.5/6.0/6.5 MHz). The quality of this system is such that the external band-pass filters can be omitted.
- Source selection between the 'internal' CVBS and an external CVBS or Y/C signal
- 1 external audio input.
- Integrated chrominance trap circuit
- Integrated luminance delay line with adjustable delay time
- Picture improvement features with peaking (with switchable centre frequency, depeaking, variable positive/negative overshoot ratio and video dependent coring), dynamic skin tone control and blue- and black stretching. All features are available for CVBS, Y/C and YP_BP_R signals.
- Tint control for all internal and external signals
- Integrated chroma band-pass filter with switchable centre frequency
- Only one reference (12 MHz) crystal required for the μ-Controller and the colour decoder
- NTSC or PAL/NTSC colour decoder with automatic search system
- Internal base-band delay line
- Indication of the Signal-to-Noise ratio of the incoming CVBS signal
- A linear RGB/YUV/YP_BP_R input with fast blanking for external RGB/YUV sources. The synchronisation circuit can be connected to the incoming Y signal. The OSD signals are internally supplied from the μ-Controller.
- RGB control circuit with 'Continuous Cathode Calibration', white point and black level off-set adjustment so that the colour temperature of the dark and the light parts of the screen can be chosen independently.
- 2 levels of contrast reduction of main picture possible during OSD/Text insertion ('halftone')
- OSD/Text gain reduction control
- Adjustable 'wide blanking' of the RGB outputs
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Horizontal and vertical geometry processing
- Horizontal and vertical zoom function for 16 : 9 applications
- Horizontal parallelogram and bow correction for large screen picture tubes
- Low-power start-up of the horizontal drive circuit
- Macrovision keying possibility for horizontal synchronisation.

μ-Controller

- 80C51 μ-controller core standard instruction set and timing
- 1 μs machine cycle
- 48Kx8 or 55Kx8-bit late programmed ROM.
- Character ROM size up to 9kx8-bit. The unused character ROM size can be used as additional program ROM.
- 3.5Kx8-bit Auxiliary RAM (up to 1.25KX8-bit required for Display)
- Interrupt controller for individual enable/disable with two level priority
- Two 16-bit Timer/Counter registers
- One 16-bit Timer with 8-bit Pre-scaler
- WatchDog timer
- Auxiliary RAM page pointer
- Standby, Idle and Power Down modes
- 14-bit PWM for Voltage Synthesis Tuning
- 4-bit A/D converter
- 4 pins which can be programmed as general I/O pin, ADC input or PWM (6-bit) output

Data Capture

- Data Capture for Line 21 Data Services
- Signal quality detector for video

Display

- Features of US Closed Caption
- Enhanced OSD modes
- Full screen OSD is supported in 525 and 625 mode
- Serial and Parallel Display Attributes
- Single/Double Width and Height for characters
- Scrolling of display region
- Variable flash rate controlled by software
- Enhanced display features including overlining, underlining and italics
- Soft colours using CLUT with 64 colour palette
- Globally selectable scan lines per row (9/10/13/16/18) and character matrix [12x10, 12x13, 12x16, 16x16, 16x18 (VxH)]
- Globally selectable character spacing
- Fringing (Shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- Special Graphics Characters with two planes, allowing four colours per character
- 16 software redefinable On-Screen display characters

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltages	–	8.0/3.3	–	V
I_P	supply current (V_P = 8 V)	–	135	–	mA
I_P	supply current (V_P = 3.3 V)	–	60	–	mA
Input voltages					
$V_{iVIFrms)}$	video IF amplifier sensitivity (RMS value)	–	75	–	μV
$V_{iAUDIO(rms)}$	external audio input (RMS value)	–	500	–	mV
$V_{iCVBS(p-p)}$	external CVBS/Y input (peak-to-peak value)	–	1.0	–	V
$V_{iCHROMA(p-p)}$	external chroma input voltage (burst amplitude) (peak-to-peak value)	–	0.3	–	V
$V_{iRGB(p-p)}$	RGB inputs (peak-to-peak value)	–	0.7	–	V
$V_{iY(p-p)}$	luminance input signal (peak-to-peak value)	–	1.4 / 1.0	–	V
$V_{iU(p-p)}$ / $V_{iPB(p-p)}$	U / P_B input signal (peak-to-peak value)	–	–1.33 / +0.7	–	V
$V_{iV(p-p)}$ / $V_{iPR(p-p)}$	V / P_R input signal (peak-to-peak value)	–	–1.05 / +0.7	–	V
Output signals					
$V_{o(IFVO)(p-p)}$	demodulated CVBS output (peak-to-peak value)	–	2.0	–	V
$V_{o(CVBSO)(p-p)}$	selected CVBS output (peak-to-peak value)	–	2.0	–	V
$I_{o(AGCOUT)}$	tuner AGC output current range	0	–	5	mA
$V_{oRGB(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	–	2.0	–	V
I_{oHOUT}	horizontal output current	10	–	–	mA
I_{oVERT}	vertical output current (peak-to-peak value)	1	–	–	mA
I_{oEWD}	EW drive output current	1.2	–	–	mA

BLOCK DIAGRAM

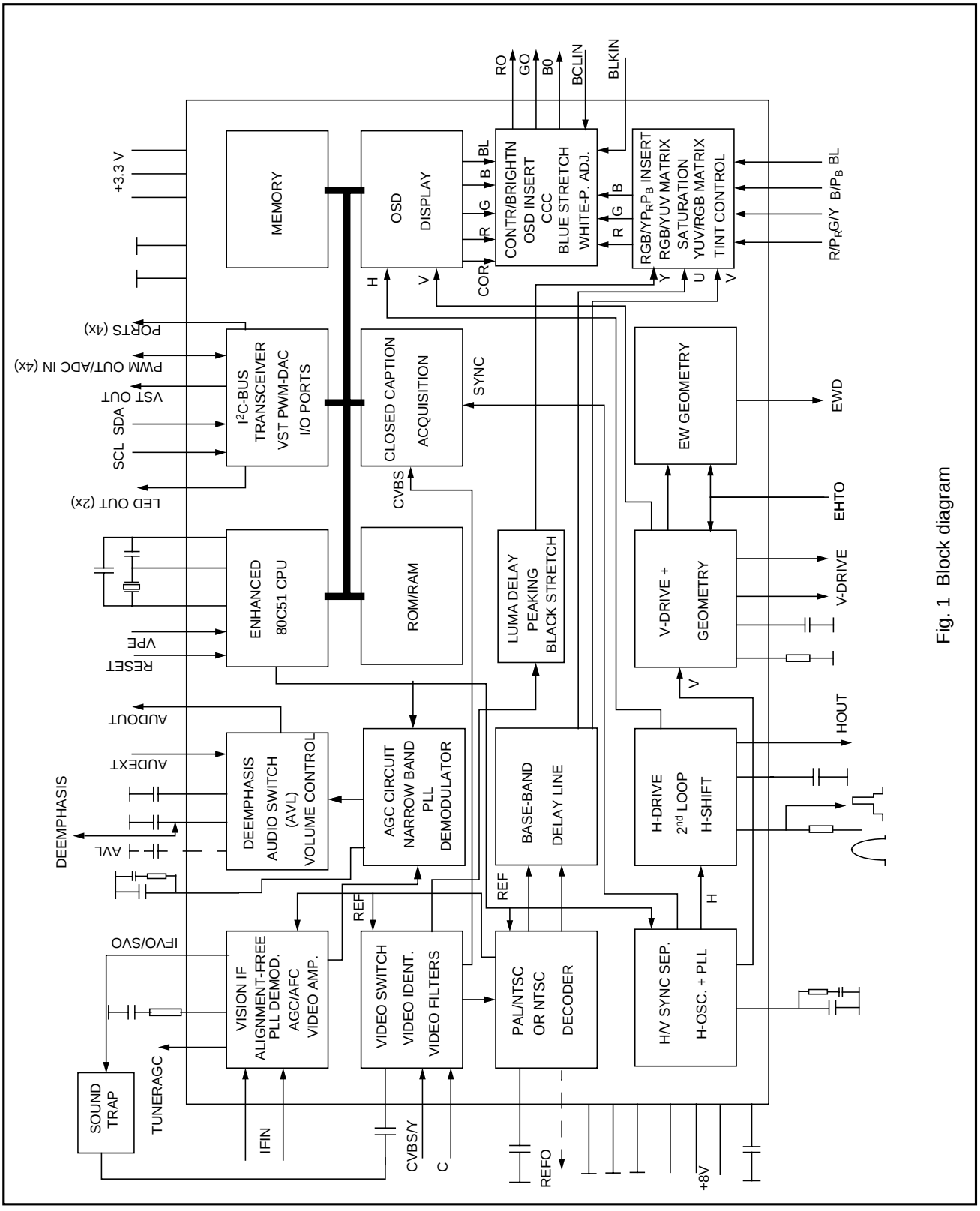


Fig. 1 Block diagram

PINNING

SYMBOL	PIN	DESCRIPTION
P1.3/T1	1	port 1.3 or Counter/Timer 1 input
P1.6/SCL	2	port 1.6 or I^2C-bus clock line
P1.7/SDA	3	port 1.7 or I^2C-bus data line
P2.0/TPWM	4	port 2.0 or Tuning PWM output
P3.0/ADC0/PWM0	5	port 3.0 or ADC0 input or PWM0 output
P3.1/ADC1/PWM1	6	port 3.1 or ADC1 input or PWM1 output
P3.2/ADC2/PWM2	7	port 3.2 or ADC2 input or PWM2 output
P3.3/ADC3/PWM3	8	port 3.3 or ADC3 input or PWM3 output
VSSC/P	9	digital ground for μ-Controller core and periphery
P0.5	10	port 0.5 (8 mA current sinking capability for direct drive of LEDs)
P0.6	11	port 0.6 (8 mA current sinking capability for direct drive of LEDs)
VSSA	12	digital ground of TV-processor
DEC	13	decoupling
VP2	14	2^{nd} supply voltage TV-processor (+8V)
DECDIG	15	supply voltage decoupling of digital circuit of TV-processor
PH2LF	16	phase-2 filter
PH1LF	17	phase-1 filter
GND3	18	ground 3 for TV-processor
DECBG	19	bandgap decoupling
EWD	20	E-W drive output
VDRB	21	vertical drive B output
VDRA	22	vertical drive A output
IFIN1	23	IF input 1
IFIN2	24	IF input 2
IREF	25	reference current input
VSC	26	vertical sawtooth capacitor
AGCOUT	27	tuner AGC output
AUDEEM	28	audio deemphasis
DECSDEM	29	decoupling sound demodulator
GND2	30	ground 2 for TV processor
SNDPLL	31	narrow band PLL filter
AVL/REFO/SNDIF (1)	32	Automatic Volume Levelling / subcarrier reference output / sound IF input
HOUT	33	horizontal output
FBISO	34	flyback input/sandcastle output
AUDEXT	35	external audio input
EHTO	36	EHT/overvoltage protection input
PLLIF	37	IF-PLL loop filter
IFVO/SVO	38	IF video output / selected video output

SYMBOL	PIN	DESCRIPTION
VP1	39	main supply voltage TV processor
CVBS1	40	internal CVBS input
GND	41	ground for TV processor
CVBS3/Y	42	CVBS3/Y input
C	43	chroma input
AUDOUT	44	audio output
INSSW2	45	2^{nd} RGB / YUV insertion input
R2/V/P_RIN	46	2^{nd} R input / V (R-Y) input / P_R input
G2/YIN	47	2^{nd} G input / Y input
B2/U/P_BIN	48	2^{nd} B input / U (B-Y) input / P_B input
BCLIN	49	beam current limiter input
BLKIN	50	black current input / V-guard input
RO	51	Red output
GO	52	Green output
BO	53	Blue output
VDDA	54	analog supply of Teletext decoder and digital supply of TV-processor (3.3 V)
VPE	55	OTP Programming Voltage
VDDC	56	digital supply to core (3.3 V)
OSCGND	57	oscillator ground supply
XTALIN	58	crystal oscillator input
XTALOUT	59	crystal oscillator output
RESET	60	reset
VDDP	61	digital supply to periphery (+3.3 V)
P1.0/INT1	62	port 1.0 or external interrupt 1 input
P1.1/T0	63	port 1.1 or Counter/Timer 0 input
P1.2/INT0	64	port 1.2 or external interrupt 0 input

Note

1. The function of this pin is controlled by the CMB1/CMB0 bits in subaddress 22H and the SIF bit in subaddress 28H. More details can be found in the tables 65 and 93.

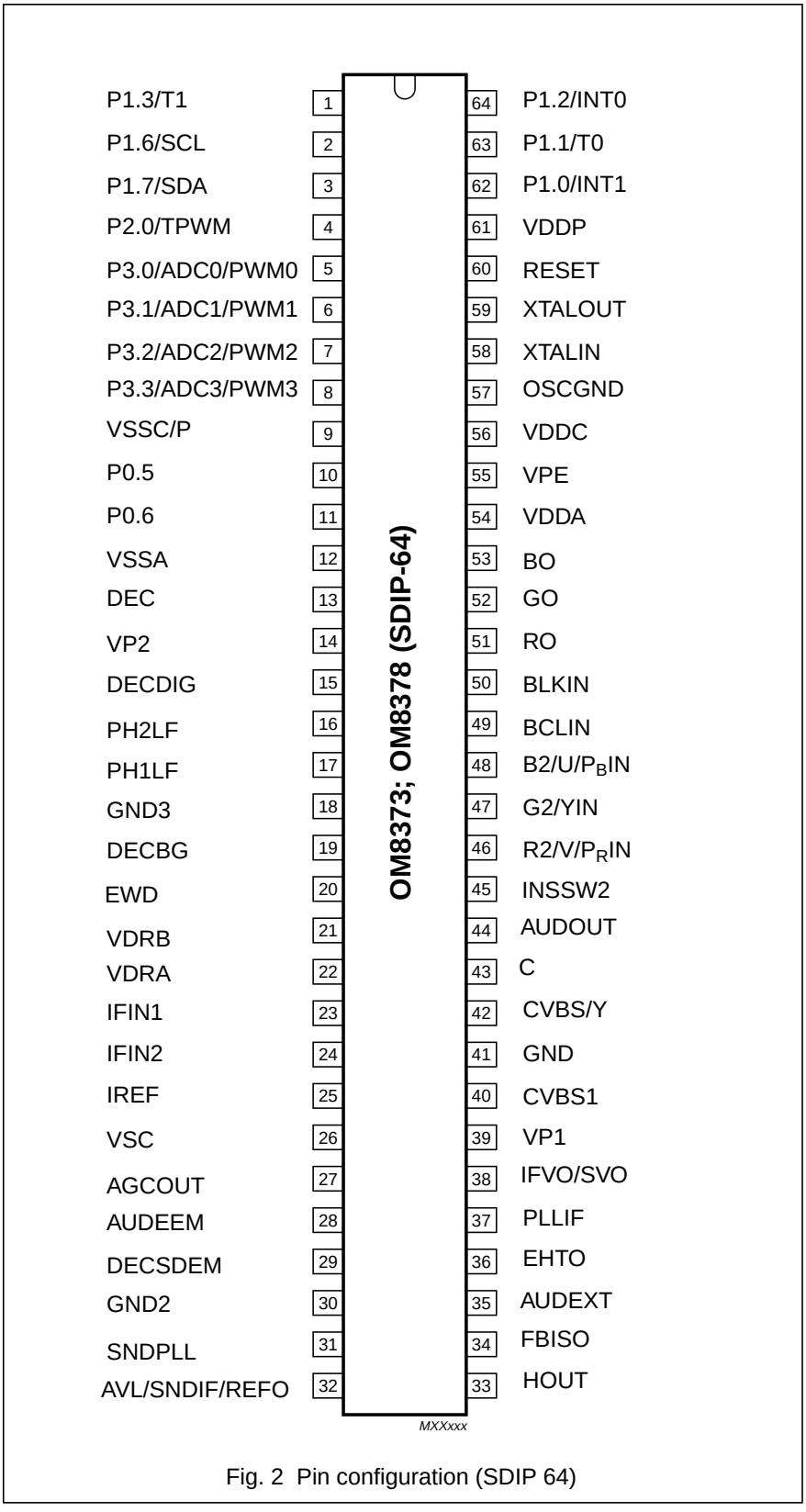


Fig. 2 Pin configuration (SDIP 64)

FUNCTIONAL DESCRIPTION OF THE 80C51

The functionality of the micro-controller used on this device is described here with reference to the industry standard 80C51 micro-controller. A full description of its functionality can be found in the 80C51 based 8-bit micro-controllers - Philips Semiconductors (ref. IC20).

Features of the 80c51

- 80C51 micro-controller core standard instruction set and timing.
- 1μs machine cycle.
- 48K x 8- or 55K x 8-bit Program ROM.
- Maximum of 3.5K x 8-bit Auxiliary RAM (up to 1.25K x 8-bit required for Display).
- 8-Level Interrupt Controller for individual enable/disable with two level priority.
- Two External Interrupts with programmable detection characteristics.
- Two 16-bit Timer/Counters.
- Additional 16-bit Timer with 8-bit Pre-scaler.
- WatchDog Timer.
- Auxiliary RAM Page Pointer.
- Idle, Stand-by and Power-Down modes.
- 13 General I/O.
- Four 6-bit Pulse Width Modulator (PWM) outputs for control of TV analogue signals.
- One 14-bit PWM for Voltage Synthesis tuner control.
- 4-bit ADC with 4 multiplexed inputs.
- 2 high current outputs for directly driving LED's etc.
- I^2C Byte Level bus interface.

Memory Organisation

The device has the capability of a maximum of 55K Bytes of PROGRAM ROM and 3.5K Bytes of DATA RAM. The 3.5K Bytes of DATA RAM are partitoned between display memory and micro-controller auxiliary memory. Up to 1.25K Bytes may be used for display purposes.

RAM Organisation

The Internal Data RAM is organised into two areas, Data Memory and Special Function Registers (SFRs) as shown in Fig.3.

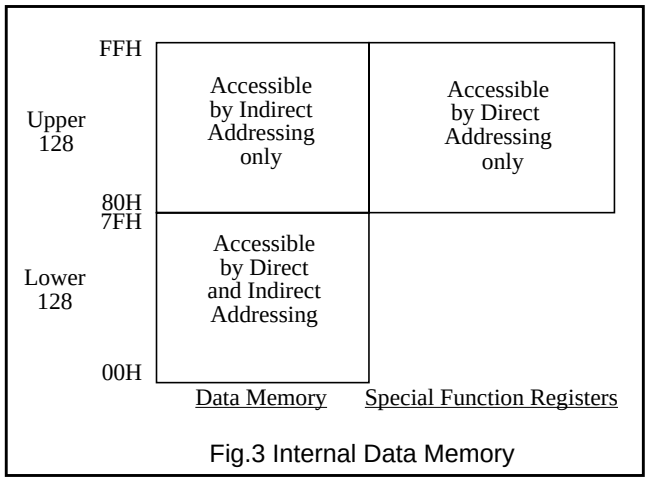


Fig.3 Internal Data Memory

DATA MEMORY

The Data memory is 256 x 8-bits and occupies the address range 00 to FF Hex when using Indirect addressing and 00 to 7F Hex when using direct addressing. The SFRs occupy the address range 80 Hex to FF Hex and are accessible using Direct addressing only. The lower 128 Bytes of Data memory are mapped as shown in Fig.4. The lowest 24 bytes are grouped into 4 banks of 8 registers, the next 16 bytes above the register banks form a block of bit addressable memory space. The upper 128 bytes are not allocated for any special area or functions.

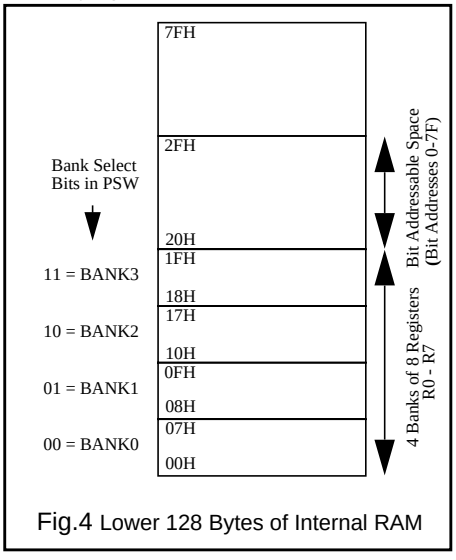


Fig.4 Lower 128 Bytes of Internal RAM

SFR MEMORY

The Special Function Register (SFR) space is used for port latches, counters/timers, peripheral control, data capture and display. These registers can only be accessed

by direct addressing. Sixteen of the addresses in the SFR space are both bit and byte addressable. The bit addressable SFRs are those whose address ends in 0H or 8H. A summary of the SFR map in address order is shown in Table 1.

ADD	R/W	Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
80H	R/W	**P0**	Reserved	P0<6>	P0<5>	Reserved	Reserved	Reserved	Reserved	Reserved
81H	R/W	**SP**	SP<7>	SP<6>	SP<5>	SP<4>	SP<3>	SP<2>	SP<1>	SP<0>
82H	R/W	**DPL**	DPL<7>	DPL<6>	DPL<5>	DPL<4>	DPL<3>	DPL<2>	DPL<1>	DPL<0>
83H	R/W	**DPH**	DPH<7>	DPH<6>	DPH<5>	DPH<4>	DPH<3>	DPH<2>	DPH<1>	DPH<0>
84H	R/W	**IEN1**	-	-	-	-	-	-	-	ET2
85H	R/W	**IP1**	-	-	-	-	-	-	-	PT2
87H	R/W	**PCON**	-	ARD	RFI	WLE	GF1	GF0	PD	IDL
88H	R/W	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89H	R/W	**TMOD**	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
8AH	R/W	**TL0**	TL0<7>	TL0<6>	TL0<5>	TL0<4>	TL0<3>	TL0<2>	TL0<1>	TL0<0>
8BH	R/W	**TL1**	TL1<7>	TL1<6>	TL1<5>	TL1<4>	TL1<3>	TL1<2>	TL1<1>	TL1<0>
8CH	R/W	**TH0**	TH0<7>	TH0<6>	TH0<5>	TH0<4>	TH0<3>	TH0<2>	TH0<1>	TH0<0>
8DH	R/W	**TH1**	TH1<7>	TH1<6>	TH1<5>	TH1<4>	TH1<3>	TH1<2>	TH1<1>	TH1<0>
90H	R/W	**P1**	P1<7>	P1<6>	Reserved	Reserved	P1<3>	P1<2>	P1<1>	P1<0>
91H	R/W	**TP2L**	TP2L<7>	TP2L<6>	TP2L<5>	TP2L<4>	TP2L<3>	TP2L<2>	TP2L<1>	TP2L<0>
92H	R/W	**TP2H**	TP2H<7>	TP2H<6>	TP2H<5>	TP2H<4>	TP2H<3>	TP2H<2>	TP2H<1>	TP2H<8>
93H	R/W	**TP2PR**	TP2PR<7>	TP2PR<6>	TP2PR<5>	TP2PR<4>	TP2PR<3>	TP2PR<2>	TP2PR<1>	TP2PR<0>
94H	R/W	**TP2CRL**	-	-	-	-	-	-	TP2CRL<1>	TP2CRL<0>
96H	R/W	**P0CFGA**	Reserved	P0CFGA<6>	P0CFGA<5>	Reserved	Reserved	Reserved	Reserved	Reserved
97H	R/W	**P0CFGB**	Reserved	P0CFGB<6>	P0CFGB<5>	Reserved	Reserved	Reserved	Reserved	Reserved
98H	R/W	**SADB**	-	-	-	DC_COMP	SAD<3>	SAD<2>	SAD<1>	SAD<0>
9CH	R	**TP2CL**	TP2CL<7>	TP2CL<6>	TP2CL<5>	TP2CL<4>	TP2CL<3>	TP2CL<2>	TP2CL<1>	TP2CL<0>
9DH	R	**TP2CH**	TP2CH<7>	TP2CH<6>	TP2CH<5>	TP2CH<4>	TP2CH<3>	TP2CH<2>	TP2CH<1>	TP2CH<0>
9EH	R/W	**P1CFGA**	P1CFGA<7>	P1CFGA<6>	Reserved	Reserved	P1CFGA<3>	P1CFGA<2>	P1CFGA<1>	P1CFGA<0>
9FH	R/W	**P1CFGB**	P1CFGB<7>	P1CFGB<6>	Reserved	Reserved	P1CFGB<3>	P1CFGB<2>	P1CFGB<1>	P1CFGB<0>
A0H	R/W	**P2**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	P2<0>
A1H	R	**TXT31**	-	-	-	-	GPF1<11>	GPF1<10>	GPF1<9>	GPF1<8>
A2H	R	**TXT32**	GPF1<11>	GPF2<11>	GPF2<10>	GPF2<9>	GPF2<8>	GPF2<7>	GPF2<6>	GPF2<5>
A3H	R	**TXT33**	GPF3<7>	GPF3<6>	GPF3<5>	GPF3<4>	GPF3<3>	GPF3<2>	GPF3<1>	GPF3<0>
A4H	R	**TXT34**	-	-	-	-	GPF3<11>	GPF3<10>	GPF3<9>	GPF3<8>
A6H	R/W	**P2CFGA**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	P2CFGA<0>

Table 1 SFR Map

ADD	R/W	Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A7H	R/W	**P2CFGB**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	P2CFGB<0>
A8H	R/W	**IE**	EA	EBUSY	ES2	ECC	ET1	EX1	ET0	EX0
B0H	R/W	**P3**	Reserved	Reserved	Reserved	Reserved	P3<3>	P3<2>	P3<1>	P3<0>
B4H	R/W	**TXT20**	DRCS ENABLE	OSD PLANES	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
B5H	R/W	**TXT21**	DISP LINE<1>	DISP LINES<0>	CHAR SIZE<1>	CHAR SIZE<0>	Reserved	CC ON	I2C PORT EN	Reserved
B6H	R	**TXT22**	GPF1<7>	GPF1<6>	GPF1<5>	GPF1<4>	GPF1<3>	GPF1<2>	GPF1<1>	GPF1<0>
B7H	R/W	**CCLIN**	0	0	0	CS<4>	CS<3>	CS<2>	CS<1>	CS<0>
B8H	R/W	**IP**	0	PBUSY	PES2	PCC	PT1	PX1	PT0	PX0
B9H	R/W	**TXT17**	0	FORCE ACQ<1>	FORCE ACQ<0>	FORCE DISP<1>	FORCE DISP<0>	Reserved	Reserved	Reserved
BEH	R/W	**P3CFGA**	Reserved	Reserved	Reserved	Reserved	P3CFGA<3>	P3CFGA<2>	P3CFGA<1>	P3CFGA<0>
BFH	R/W	**P3CFGB**	Reserved	Reserved	Reserved	Reserved	P3CFGB<3>	P3CFGB<2>	P3CFGB<1>	P3CFGB<0>
C1H	R/W	**TXT1**	Reserved	Reserved	Reserved	Reserved	Reserved	FIELD POLARITY	Reserved	Reserved
C5H	R/W	**TXT5**	Reserved	Reserved	CORB OUT	CORB IN	Reserved	Reserved	Reserved	Reserved
C7H	R/W	**TXT7**	Reserved	CURSOR ON	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
C9H	R/W	**TXT9**	Reserved	Reserved	Reserved	R<4>	R<3>	R<2>	R<1>	R<0>
CAH	R/W	**TXT10**	CHAR 16/12	-	C<5>	C<4>	C<3>	C<2>	C<1>	C<0>
CCH	R	**TXT12**	525/$\overline{625}$ SYNC	GPF2<4>	GPF2<3>	GPF2<2>	GPF2<1>	GPF2<0>	1	VIDEO SIGNAL QUALITY
D0H	R/W	**PSW**	C	AC	F0	RS1	RS0	OV	-	P
D2H	R/W	**TDACL**	TD<7>	TD<6>	TD<5>	TD<4>	TD<3>	TD<2>	TD<1>	TD<0>
D3H	R/W	**TDACH**	TPWE	1	TD<13>	TD<12>	TD<11>	TD<10>	TD<9>	TD<8>
D5H	R/W	**PWM0**	PW0E	1	PW0V<5>	PW0V<4>	PW0V<3>	PW0V<2>	PW0V<1>	PW0V<0>
D6H	R/W	**PWM1**	PW1E	1	PW1V<5>	PW1V<4>	PW1V<3>	PW1V<2>	PW1V<1>	PW1V<0>
D7H	R	**CCDAT1**	CCD1<7>	CCD1<6>	CCD1<5>	CCD1<4>	CCD1<3>	CCD1<2>	CCD1<1>	CCD1<0>
D8H	R/W	**S1CON**	CR<2>	ENSI	STA	STO	SI	AA	CR<1>	CR<0>
D9H	R	**S1STA**	STAT<4>	STAT<3>	STAT<2>	STAT<1>	STAT<0>	0	0	0
DAH	R/W	**S1DAT**	DAT<7>	DAT<6>	DAT<5>	DAT<4>	DAT<3>	DAT<2>	DAT<1>	DAT<0>
DBH	R/W	**S1ADR**	ADR<6>	ADR<5>	ADR<4>	ADR<3>	ADR<2>	ADR<1>	ADR<0>	GC
DCH	R/W	**PWM3**	PW3E	1	PW3V<5>	PW3V<4>	PW3V<3>	PW3V<2>	PW3V<1>	PW3V<0>
E0H	R/W	**ACC**	ACC<7>	ACC<6>	ACC<5>	ACC<4>	ACC<3>	ACC<2>	ACC<1>	ACC<0>
E4H	R/W	**PWM2**	PW2E	1	PW2V<5>	PW2V<4>	PW2V<3>	PW2V<2>	PW2V<1>	PW2V<0>

Table 1 SFR Map

ADD	R/W	Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
E5H	R/W	**TXT37**	0	0	TV LINE SPACE<2>	TV LINE SPACE<1>	TV LINE SPACE<0>	CHAR SPACE<2>	CHAR SPACE<1>	CHAR SPACE<1>
E7H	R	**CCDAT2**	CCD2<7>	CCD2<6>	CCD2<5>	CCD2<4>	CCD2<3>	CCD2<2>	CCD2<1>	CCD2<0>
E8H	R/W	**SAD**	VHI	CH<1>	CH<0>	ST	Reserved	Reserved	Reserved	Reserved
F0H	R/W	**B**	B<7>	B<6>	B<5>	B<4>	B<3>	B<2>	B<1>	B<0>
F8H	R	**TXT13**	Reserved	DRAM INIT	525 DISPLAY	Reserved	Reserved	Reserved	Reserved	Reserved
FAH	R/W	**XRAMP**	XRAMP<7>	XRAMP<6>	XRAMP<5>	XRAMP<4>	XRAMP<3>	XRAMP<2>	XRAMP<1>	XRAMP<0>
FBH	R/W	**ROMBK**	STANDBY	IIC_LUT<1>	IIC_LUT<0>	Reserved	Reserved	Reserved	Reserved	Reserved
FDH	R	**TEST**	TEST<7>	TEST<6>	TEST<5>	TEST<4>	TEST<3>	TEST<2>	TEST<1>	TEST<0>
FEH	W	**WDTKEY**	WKEY<7>	WKEY<6>	WKEY<5>	WKEY<4>	WKEY<3>	WKEY<2>	WKEY<1>	WKEY<0>
FFH	R/W	**WDT**	WDV<7>	WDV<6>	WDV<5>	WDV<4>	WDV<3>	WDV<2>	WDV<1>	WDV<0>

Table 1 SFR Map

A description of each of the SFR bits is shown in Table 2, The SFRs are in alphabetical order.

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
ACC	ACC<7>	ACC<6>	ACC<5>	ACC<4>	ACC<3>	ACC<2>	ACC<1>	ACC<0>	**00H**
ACC<7:0>	Accumulator value.								
B	B<7>	B<6>	B<5>	B<4>	B<3>	B<2>	B<1>	B<0>	**00H**
B<7:0>	B Register value.								
CCDAT1	CCD1<7>	CCD1<6>	CCD1<5>	CCD1<4>	CCD1<3>	CCD1<2>	CCD1<1>	CCD1<0>	**00H**
CCD1<7:0>	Closed Caption first data byte.								
CCDAT2	CCD2<7>	CCD2<6>	CCD2<5>	CCD2<4>	CCD2<3>	CCD2<2>	CCD2<1>	CCD2<0>	**00H**
CCD2<7:0>	Closed Caption second data byte.								
CCLIN	0	0	0	CS<4>	CS<3>	CS<2>	CS<1>	CS<0>	**15H**
CS<4:0>	Closed Caption Slice line using 525 line number.								
DPH	DPH<7>	DPH<6>	DPH<5>	DPH<4>	DPH<3>	DPH<2>	DPH<1>	DPH<0>	**00H**
DPH<7:0>	Data Pointer High byte, used with DPL to address display and auxiliary memory.								
DPL	DPL<7>	DPL<6>	DPL<5>	DPL<4>	DPL<3>	DPL<2>	DPL<1>	DPL<0>	**00H**
DPL<7:0>	Data pointer low byte, used with DPH to address display and auxiliary memory.								
IE	EA	EBUSY	ES2	ECC	ET1	EX1	ET0	EX0	**00H**
EA	Disable all interrupts (0), or use individual interrupt enable bits (1).								
EBUSY	Enable BUSY Interrupt.								
ES2	Enable I^2C Interrupt.								

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
ECC	Enable Closed Caption Interrupt.								
ET1	Enable Timer 1 Interrupt.								
EX1	Enable External Interrupt 1.								
ET0	Enable Timer 0 Interrupt.								
EX0	Enable External Interrupt 0.								
IEN1	-	-	-	-	-	-	-	ET2	**00H**
ET2	Enable Timer 2 Interrupt.								
IP	-	PBUSY	PES2	PCC	PT1	PX1	PT0	PX0	**00H**
PBUSY	Priority EBUSY Interrupt.								
PES2	Priority ES2 Interrupt.								
PCC	Priority ECC Interrupt.								
PT1	Priority Timer 1 Interrupt.								
PX1	Priority External Interrupt 1.								
PT0	Priority Timer 0 Interrupt.								
PX0	Priority External Interrupt 0.								
IP1	-	-	-	-	-	-	-	PT2	**00H**
PT2	Priority Timer 2 Interrupt.								
P0	Reserved	P0<6>	P0<5>	Reserved	Reserved	Reserved	Reserved	Reserved	**60H**
P0<6:5>	Port 0 I/O register connected to external pins.								
P1	P1<7>	P1<6>	Reserved	Reserved	P1<3>	P1<2>	P1<1>	P1<0>	**CFH**
P1<7:6>	Port 1 I/O register connected to external pins.								
P1<3:0>	Port 1 I/O register connected to external pins.								
P2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	P2<0>	**3FH**
P2<0>	Port 2 I/O register connected to external pins.								
P3	Reserved	Reserved	Reserved	Reserved	P3<3>	P3<2>	P3<1>	P3<0>	**0FH**
P3<3:0>	Port 3 I/O register connected to external pins.								
P0CFGA	Reserved	P0CFGA<6>	P0CFGA<5>	Reserved	Reserved	Reserved	Reserved	Reserved	**FFH**
P0CFGB	Reserved	P0CFGB<6>	P0CFGB<5>	Reserved	Reserved	Reserved	Reserved	Reserved	**00H**
P0CFGB<x>/P0CFGA<x> = 00	MODE 0 Open Drain.								
P0CFGB<x>/P0CFGA<x> = 01	MODE 1 Quasi Bi-Directional.								
P0CFGB<x>/P0CFGA<x> = 10	MODE2 High Impedance.								
P0CFGB<x>/P0CFGA<x> = 11	MODE3 Push Pull.								
P1CFGA	P1CFGA<7>	P1CFGA<6>	Reserved	Reserved	P1CFGA<3>	P1CFGA<2>	P1CFGA<1>	P1CFGA<0>	**FFH**

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
P1CFGB	P1CFGB<7>	P1CFGB<6>	Reserved	Reserved	P1CFGB<3>	P1CFGB<2>	P1CFGB<1>	P1CFGB<0>	**00H**
P1CFGB<x>/P1CFGA<x> = 00	MODE 0 Open Drain.								
P1CFGB<x>/P1CFGA<x> = 01	MODE 1 Quasi Bi-Directional.								
P1CFGB<x>/P1CFGA<x> = 10	MODE2 High Impedance.								
P1CFGB<x>/P1CFGA<x> = 11	MODE3 Push Pull.								
P2CFGA	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	P2CFGA<0>	**FFH**
P2CFGB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	P2CFGB<0>	**00H**
P2CFGB<x>/P2CFGA<x> = 00	MODE 0 Open Drain.								
P2CFGB<x>/P2CFGA<x> = 01	MODE 1 Quasi Bi-Directional.								
P2CFGB<x>/P2CFGA<x> = 10	MODE2 High Impedance.								
P2CFGB<x>/P2CFGA<x> = 11	MODE3 Push Pull.								
P3CFGA	Reserved	Reserved	Reserved	Reserved	P3CFGA<3>	P3CFGA<2>	P3CFGA<1>	P3CFGA<0>	**FFH**
P3CFGB	Reserved	Reserved	Reserved	Reserved	P3CFGB<3>	P3CFGB<2>	P3CFGB<1>	P3CFGB<0>	**00H**
P3CFGB<x>/P3CFGA<x> = 00	MODE 0 Open Drain.								
P3CFGB<x>/P3CFGA<x> = 01	MODE 1 Quasi Bi-directional.								
P3CFGB<x>/P3CFGA<x> = 10	MODE2 High Impedance.								
P3CFGB<x>/P3CFGA<x> = 11	MODE3 Push Pull.								
PCON	-	ARD	RFI	WLE	GF1	GF0	PD	IDL	**00H**
ARD	Auxiliary RAM Disable, All MOVX instructions access the external data memory. ‘0’ : Enable ‘1’ : Disable								
RFI	Disable ALE during internal access to reduce Radio Frequency Interference. ‘0’ : Enable ‘1’ : Disable								
WLE	Watch Dog Timer enable. ‘0’ : Disable ‘1’ : Enable								
GF1	General purpose flag.								
GF0	General purpose flag.								
PD	Power-down activation bit.								
IDL	Idle mode activation bit.								
PSW	C	AC	F0	RS<1>	RS<0>	OV	-	P	**00H**
C	Carry Bit.								
AC	Auxiliary Carry bit.								
F0	Flag 0, General purpose flag.								

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
RS<1:0>	Register Bank selector bits. RS<1:0> = 00, Bank0 (00H - 07H). RS<1:0> = 01, Bank1 (08H - 0FH). RS<1:0> = 10, Bank2 (10H - 17H). RS<1:0> = 11, Bank3 (18H - 1FH).								
OV	Overflow flag.								
P	Parity bit.								
PWM0	PW0E	1	PW0V<5>	PW0V<4>	PW0V<3>	PW0V<2>	PW0V<1>	PW0V<0>	**40H**
PW0E	0 - Disable Pulse Width Modulator 0. 1 - Enable Pulse Width Modulator 0.								
PW0V<5:0>	Pulse Width Modulator high time.								
PWM1	PW1E	1	PW1V<5>	PW1V<4>	PW1V<3>	PW1V<2>	PW1V<1>	PW1V<0>	**40H**
PW1E	0 - Disable Pulse Width Modulator 1. 1 - Enable Pulse Width Modulator 1.								
PW1V<5:0>	Pulse Width Modulator high time.								
PWM2	PW2E	1	PW2V<5>	PW2V<4>	PW2V<3>	PW2V<2>	PW2V<1>	PW2V<0>	**40H**
PW2E	0 - Disable Pulse Width Modulator 2. 1 - Enable Pulse Width Modulator 2.								
PW2V<5:0>	Pulse Width Modulator high time.								
PWM3	PW3E	1	PW3V<5>	PW3V<4>	PW3V<3>	PW3V<2>	PW3V<1>	PW3V<0>	**40H**
PW3E	0 - Disable Pulse Width Modulator 3. 1 - Enable Pulse Width Modulator 3.								
PW3V<5:0>	Pulse Width Modulator high time.								
ROMBK	STANDBY	IIC_LUT<1>	IIC_LUT<0>	Reserved	Reserved	Reserved	Reserved	Reserved	**00H**
STANDBY	0 - Disable Stand-by Mode 1 - Enable Stand-by Mode								
IIC_LUT<1:0>	IIC Lookup table selection: IIC_LUT<1:0>=00, 558 Normal Mode. IIC_LUT<1:0>=01, 558 Fast Mode. IIC_LUT<1:0>=10, 558 Slow Mode. IIC_LUT<1:0>=11, Reserved.								
S1ADR	ADR<6>	ADR<5>	ADR<4>	ADR<3>	ADR<2>	ADR<1>	ADR<0>	GC	**00H**
ADR<6:0>	I2C Slave Address.								
GC	0 - Disable I^2C general call address. 1 - Enable I^2C general call address.								
S1CON	CR<2>	ENSI	STA	STO	SI	AA	CR<1>	CR<0>	**00H**
CR<2:0>	Clock rate bits. Refer to section on I^2C.								

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
ENSI	0 - Disable I^2C interface. 1 - Enable I^2C interface.								
STA	START flag. When this bit is set in slave mode, the hardware checks the I2C bus and generates a START condition if the bus is free or after the bus becomes free. If the device operates in master mode it will generate a repeated START condition.								
STO	STOP flag. If this bit is set in a master mode a STOP condition is generated. A STOP condition detected on the I2C bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. In this case no STOP condition is generated to the I2C bus, but the hardware releases the SDA and SCL lines and switches to the not selected receiver mode. The STOP flag is cleared by the hardware.								
SI	Serial Interrupt flag. This flag is set and an interrupt request is generated, after any of the following events occur: -A START condition is generated in master mode. -The own slave address has been received during AA=1. -The general call address has been received while S1ADR.GC and AA=1. -A data byte has been received or transmitted in master mode (even if arbitration is lost). -A data byte has been received or transmitted as selected slave. A STOP or START condition is received as selected slave receiver or transmitter While the SI flag is set, SCL remains LOW and the serial transfer is suspened.SI must be reset by software.								
AA	Assert Acknowledge flag. When this bit is set, an acknowledge is returned after any one of the following conditions -Own slave address is received. -General call address is received(S1ADR.GC=1). -A data byte is received, while the device is programmed to be a master receiver. -A data byte is received, while the device is selected slave receiver. When the bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.								
S1DAT	DAT<7>	DAT<6>	DAT<5>	DAT<4>	DAT<3>	DAT<2>	DAT<1>	DAT<0>	**00H**
DAT<7:0>	I^2C Data.								
S1STA	STAT<4>	STAT<3>	STAT<2>	STAT<1>	STAT<0>	0	0	0	**F8H**
STAT<4:0>	I^2C Interface Status.								
SAD	VHI	CH<1>	CH<0>	ST	Reserved	Reserved	Reserved	Reserved	**00H**
VHI	0 - Analogue input voltage less than or equal to DAC voltage. 1 - Analogue input voltage greater then DAC voltage.								
CH<1:0>	ADC Input channel select. CH<1:0> = 00,ADC3. CH<1:0> = 01,ADC0. CH<1:0> = 10,ADC1. CH<1:0> = 11,ADC2.								
ST	Initiate voltage comparison between ADC input Channel and SADB<3:0> value. Note: Set by Software and reset by Hardware.								
SADB	-	-	-	DC_COMP	SAD<3>	SAD<2>	SAD<1>	SAD<0>	**00H**
DC_COMP	0 - Disable DC Comparator mode. 1 - Enable DC Comparator mode.								
SAD<3:0>	4-bit SAD value.								
SP	SP<7>	SP<6>	SP<5>	SP<4>	SP<3>	SP<2>	SP<1>	SP<0>	**07H**
SP<7>	Stack Pointer.								
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	**00H**

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
TF1	Timer 1 overflow Flag. Set by hardware on Timer/Counter overflow.Cleared by hardware when processor vectors to interrupt routine.								
TR1	Timer 1 Run control bit. Set/Cleared by software to turn Timer/Counter on/off.								
TF0	Timer 0 overflow Flag. Set by hardware on Timer/Counter overflow.Cleared by hardware when processor vectors to interrupt routine.								
TR0	Timer 0 Run control bit. Set/Cleared by software to turn Timer/Counter on/off.								
IE1	Interrupt 1 Edge flag (both edges generate flag). Set by hardware when external interrupt edge detected.Cleared by hardware when interrupt processed.								
IT1	Interrupt 1 Type control bit. Set/Cleared by Software to specify edge/low level triggered external interrupts.								
IE0	Interrupt 0 Edge l flag. Set by hardware when external interrupt edge detected.Cleared by hardware when interrupt processed.								
IT0	Interrupt 0 Type flag.Set/Cleared by Software to specify falling edge/low level triggered external interrupts.								
TDACH	TPWE	1	TD<13>	TD<12>	TD<11>	TD<10>	TD<9>	TD<8>	**40H**
TPWE	0 - Disable Tuning Pulse Width Modulator. 1 - Enable Tuning Pulse Width Modulator.								
TD<13:8>	Tuning Pulse Width Modulator High Byte.								
TDACL	TD<7>	TD<6>	TD<5>	TD<4>	TD<3>	TD<2>	TD<1>	TD<0>	**00H**
TD<7:0>	Tuning Pulse Width Modulator Low Byte.								
TH0	TH0<7>	TH0<6>	TH0<5>	TH0<4>	TH0<3>	TH0<2>	TH0<1>	TH0<0>	**00H**
TH0<7:0>	Timer 0 high byte.								
TH1	TH1<7>	TH1<6>	TH1<5>	TH1<4>	TH1<3>	TH1<2>	TH1<1>	TH1<0>	**00H**
TH1<7:0>	Timer 1 high byte.								
TL0	TL0<7>	TL0<6>	TL0<5>	TL0<4>	TL0<3>	TL0<2>	TL0<1>	TL0<0>	**00H**
TL0<7:0>	Timer 0 low byte.								
TL1	TL1<7>	TL1<6>	TL1<5>	TL1<4>	TL1<3>	TL1<2>	TL1<1>	TL1<0>	**00H**
TL1<7:0>	Timer 1 low byte.								
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	**00H**
	Timer / Counter 1				Timer / Counter 0				
GATE	Gating Control Timer /Counter 1.								
C/T	Counter/Timer 1 selector.								
M1,M0	Mode control bits Timer/Counter 1. M1,M0 = 00, 8 bit timer or 8 bit counter with divide by 32 pre-scaler. M1,M0 = 01, 16 bit time interval or event counter. M1,M0 = 10, 8 bit time interval or event counter with automatic reload upon overflow. Reload value stored in TH1. M1,M0 = 11, stopped.								
GATE	Gating control Timer/Counter 0.								
C/T	Counter/Timer 0 selector.								

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
M1,M0	Mode Control bits Timer/Counter 0. M1,M0 = 00, 8 bit timer or 8 bit counter with divide by 32 pre-scaler. M1,M0 = 01, 16 bit time interval or event counter. M1,M0 = 10, 8 bit time interval or event counter with automatic reload upon overflow. Reload value stored in TH0. M1,M0 = 11, one 8 bit time interval or event counter and one 8 bit time interval counter.								
TP2H	TP2H<7>	TP2H<6>	TP2H<5>	TP2H<4>	TP2H<3>	TP2H<2>	TP2H<1>	TP2H<0>	**00H**
TP2H<7:0>	Timer 2 high byte.								
TP2L	TP2L<7>	TP2L<6>	TP2L<5>	TP2L<4>	TP2L<3>	TP2L<2>	TP2L<1>	TP2L<0>	**00H**
TP2L<7:0>	Timer 2 low byte.								
TP2CH	TP2CH<7>	TP2CH<6>	TP2CH<5>	TP2CH<4>	TP2CH<3>	TP2CH<2>	TP2CH<1>	TP2CH<0>	**00H**
TP2CH<7:0>	Timer 2 high byte current value.								
TP2CL	TP2CL<7>	TP2CL<6>	TP2CL<5>	TP2CL<4>	TP2CL<3>	TP2CL<2>	TP2CL<1>	TP2CL<0>	**00H**
TP2CL<7:0>	Timer 2 low byte current value.								
TP2PR	TP2PR<7>	TP2PR<6>	TP2PR<5>	TP2PR<4>	TP2PR<3>	TP2PR<2>	TP2PR<1>	TP2PR<0>	**00H**
TP2H<7:0>	Timer 2 Pre-scaler.								
TP2CRL	-	-	-	-	-	-	TP2CRL<1>	TP2CRL<0>	**00H**
TP2CRL<0>	Timer 2 Control. 0 - Timer 2 disabled. 1 - Timer 2 enabled.								
TP2CRL<1>	Timer 2 Status. 0 - No Overflow. 1 - Overflow.								
TXT1	Reserved	Reserved	Reserved	Reserved	Reserved	FIELD POLARITY	Reserved	Reserved	**00H**
FIELD POLARIY	0 - Vsync pulse in first half of line during even field. 1 - Vsync pulse in second half of line during even field.								
TXT5	Reserved	Reserved	COR OUT	COR IN	Reserved	Reserved	Reserved	Reserved	**00H**
COR OUT	0 - COR not active outside OSD boxes. 1 - COR active outside OSD boxes.								
COR IN	0 - COR not active inside OSD boxes. 1 - COR active inside OSD boxes.								
TXT7	Reserved	CURSOR ON	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**00H**
CURSOR ON	0 - Disable display of cursor. 1 - Display cursor at position given by TXT9 and TXT10.								
TXT9	-	-	-	R<4>	R<3>	R<2>	R<1>	R<0>	**00H**
R<4:0>	Cursor ROW position.								
TXT10	CHAR 16/12	-	C<5>	C<4>	C<3>	C<2>	C<1>	C<0>	**00H**

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
CHAR 16/12	Character Matrix width: 0 - 12 pixel wide matrix. 1 - 16 pixel wide matrix.								
C<5:0>	Cursor COLUMN position.								
TXT12	625/525 SYNC	GPF2<4>	GPF2<3>	GPF2<2>	GPF2<1>	GPF2<0>	1	VIDEO SIGNAL QUALITY	**xxxxxx1xB**
625/525 SYNC	0 - 625 line CVBS signal is being received. 1 - 525 line CVBS signal is being received.								
GPF2<4:0>	Mask programmable identification for character set.								
VIDEO SIGNAL QUALITY	0 - Acquisition can not be synchronised to CVBS input. 1 - Acquisition can be synchronised to CVBS input.								
TXT13	Reserved	DRAM INIT	525 DISPLAY	Reserved	Reserved	Reserved	Reserved	Reserved	**XXH**
DRAM INIT	DRAM Memory Initialisation: 0 - DRAM Memory may be accessed. 1 - DRAM Memory being initialised.								
525 DISPLAY	0 - 625 Line synchronisation for Display. 1 - 525 Line synchronisation for Display.								
TXT17	Reserved	FORCE ACQ<1>	FORCE ACQ<0>	FORCE DISP<1>	FORCE DISP<0>	Reserved	Reserved	Reserved	**00H**
FORCE ACQ<1:0>	00 - Automatic Selection. 01 - Force 525 timing. 10 - Force 625 timing. 11 - Not Valid (default to 625 timing).								
FORCE DISP<1:0>	00 - Automatic Selection. 01 - Force Display to 525 mode (9 lines per row). 10 - Force Display to 625 mode (10 lines per row). 11 - Not Valid (default to 625).								
TXT20	DRCS ENABLE	OSD PLANES	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**00H**
DRCS ENABLE	0 - Normal OSD characters used. 1 - Re-map column 8 to DRCS.								
OSD PLANES	0 - Character code column 8 defined as single plane characters. 1 - Character code column 8 defined as double plane characters (special graphics characters).								
TXT21	DISP LINES<1>	DISP LINES<0>	CHAR SIZE<1>	CHAR SIZE<0>	Reserved	CC ON	I2C PORT EN	Reserved	**02H**
DISP LINES<1:0>	The number of display lines per character row. 00 - 10 lines per character (defaults to 9 lines in 525 mode). 01 - 13 lines per character. 10 - 16 lines per character. 11 - 18 lines per character.								

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
CHAR SIZE<1:0>	Character matrix size. 00 - 10 lines per character matrix. 01 - 13 lines per character matrix. 10 - 16 lines per character matrix. 11 - 18 lines per character matrix. NOTE: Character matrix width defined by TXT10.CHAR16/12.								
CCON	0 - Closed Caption acquisition off. 1 - Closed Caption acquisition on.								
I2C PORT EN	0 - Disable I2C PORT. 1 - Enable I2C PORT selection (P1.7/SDA0, P1.6/SCL0).								
TXT22	GPF1<7>	GPF1<6>	GPF1<5>	GPF1<4>	GPF1<3>	GPF1<2>	GPF1<1>	GPF1<0>	**XXH**
GPF1<7:0>	General purpose register, bits defined by mask programmable bits.								
GPF1<6>	0 - Painter Extended Fonts disabled. 1 - Painter Extended Fonts enabled.								
GPF1<5>	Reserved.								
GPF1<4> (Used for software only)	Reserved.								
GPF1<3>	0 - PWM0, PWM1, PWM2 & PWM3 output on Port 3.0 to Port 3.3 respectively. 1 - PWM0, PWM1, PWM2 & PWM3 output on Port 2.1 to Port 2.4 respectively.(not available on SDIP64)								
GPF1<2>	0 - Closed Caption acquisition disabled. 1 - Closed Caption acquisition enabled.								
GPF1<1>	Reserved.								
GPF<0> (Polarity reversed in P_Leader standalone)	0 - Standalone (Painter) mode. 1 - TV processor mode.								
TXT31	-	-	-	-	GPF1<11>	GPF1<10>	GPF1<9>	GPF1<8>	**XXH**
GPF1<11:8>	General purpose register, bits defined by mask programmable location.								
GPF1<10>	Reserved.								
GPF1<9:8>	Reserved.								
TXT32	GPF1<11>	GPF2<11>	GPF2<10>	GPF2<9>	GPF2<8>	GPF2<7>	GPF2<6>	GPF2<5>	**XXH**
GPF2<11:5>	Mask programmable bits available for TV processor configuration.								
TXT33	GPF3<7>	GPF3<6>	GPF3<5>	GPF3<4>	GPF3<3>	GPF3<2>	GPF3<1>	GPF3<0>	**XXH**
GPF3<7:0>	Mask programmable bits available for TV processor configuration.								
TXT34	-	-	-	-	GPF3<11>	GPF3<10>	GPF3<9>	GPF3<8>	**XXH**
GPF3<11:8>	Mask programmable bits available for TV processor configuration.								
TXT37	0	0	TV LINE SPACE<2>	TV LINE SPACE<1>	TV LINE SPACE<0>	CHAR SPACE<2>	CHAR SPACE<1>	CHAR SPACE<0>	**00H**
TV LINE SPACE<2:0>	No. of TV Lines between character row (0-7 TV Lines). NOTE: Works in addition to TV display lines per character row (TXT21).								

Table 2 SFR Bit description

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
CHAR SPACE<2:0>	Horizontal spacing between characters: 000 - No space. 001 - 1 pixel space. 010 - 2 pixel space. 011 - 3 pixel space. 100 - 4 pixel space. 101 to 111 - Reserved.								
WDT	WDV<7>	WDV<6>	WDV<5>	WDV<4>	WDV<3>	WDV<2>	WDV<1>	WDV<0>	**00H**
WDV<7:0>	Watch Dog Timer period.								
WDTKEY	WKEY<7>	WKEY<6>	WKEY<5>	WKEY<4>	WKEY<3>	WKEY<2>	WKEY<1>	WKEY<0>	**00H**
WKEY<7:0>	Watch Dog Timer Key. Note: Must be set to 55H to disable Watch dog timer when active.								
XRAMP	XRAMP<7>	XRAMP<6>	XRAMP<5>	XRAMP<4>	XRAMP<3>	XRAMP<2>	XRAMP<1>	XRAMP<0>	**00H**
XRAMP<7:0>	Internal RAM access upper byte address.								

Table 2 SFR Bit description

External (Auxiliary + Display) Memory
The normal 80C51 external memory area has been mapped internally to the device, this means that the MOVX instruction accesses data memory internal to the device. The movx memory map is shown in Fig.5.

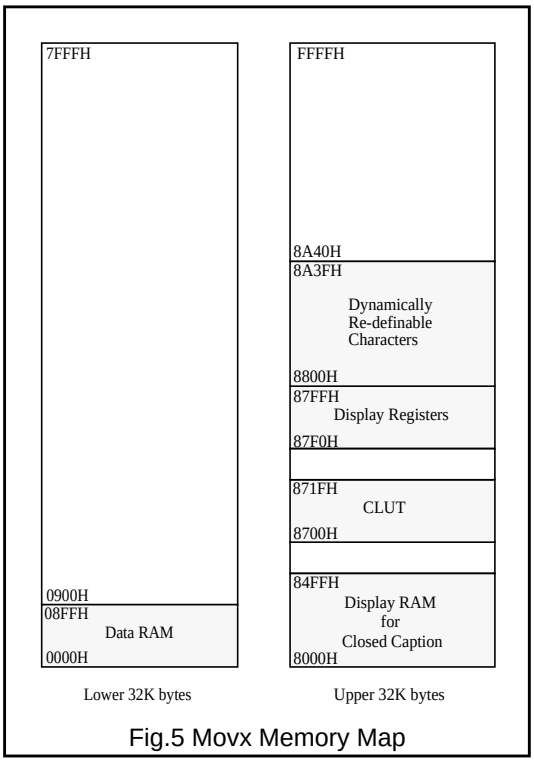


Fig.5 Movx Memory Map

Auxiliary RAM Page Selection
The Auxiliary RAM page pointer is used to select one of the 256 pages within the movx address space, not all pages are allocated, refer to Fig.6. A page consists of 256 consecutive bytes. XRAMP only works on internal MOVX memory.

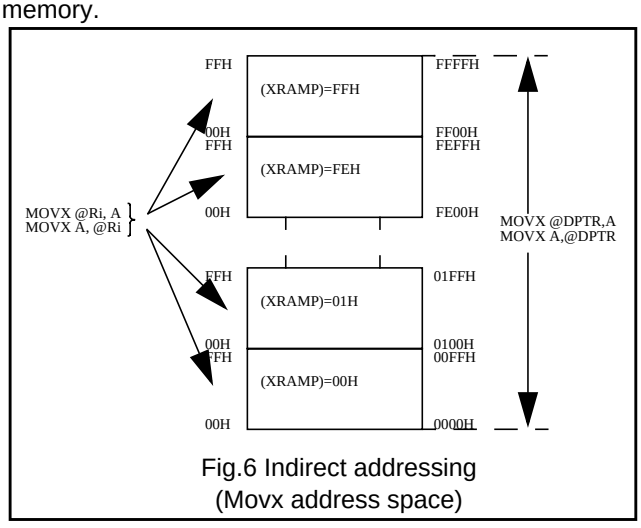


Fig.6 Indirect addressing (Movx address space)

Power-on Reset
Power on reset is generated internally to the TV processor, hence no external reset circuitry is required. The TV processor die shall generate the master reset in the system, which in turn will reset the micro-controller die. A external reset pin is still present and is logically "OR"-ed with the internal Power on reset. This pin will only be used for test modes and OTP programming. The active high reset pin incorporates an internal pull-down, thus it can be left unconnected in application.

Power Saving modes of Operation
There are three Power Saving modes, Idle, Stand-by and Power Down, incorporated into the Painter die. When utilizing either mode, the 3.3v power to the device (Vddp, Vddc & Vdda) should be maintained, since Power Saving is achieved by clock gating on a section by section basis.

STAND-BY MODE
During Stand-by mode, the Acquisition and Display sections of the device are disabled. The following functions remain active:-
- 80c51 CPU Core
- Memory Interface
- I^2C
- Timer/Counters
- WatchDog Timer
- SAD and PWMs

To enter Stand-by mode, the STAND-BY bit in the ROMBANK register must be set. Once in Stand-By, the XTAL oscillator continues to run, but the internal clock to Acquisition and Display are gated out. However, the clocks to the 80c51 CPU Core, Memory Interface, I^2C, Timer/Counters, WatchDog Timer and Pulse Width Modulators are maintained. Since the output values on RGB and VDS are maintained the display output must be disabled before entering this mode.
This mode may be used in conjunction with both Idle and Power-Down modes. Hence, prior to entering either Idle or Power-Down, the STAND-BY bit may be set, thus allowing wake-up of the 80c51 CPU core without fully waking the entire device (This enables detection of a Remote Control source in a power saving mode).

IDLE MODE
During Idle mode, Acquisition, Display and the CPU sections of the device are disabled. The following functions remain active:-
- Memory Interface
- I^2C

- Timer/Counters
- WatchDog Timer
- SAD & PWMs

To enter Idle mode the IDL bit in the PCON register must be set. The WatchDog timer must be disabled prior to entering Idle to prevent the device being reset. Once in Idle mode, the XTAL oscillator continues to run, but the internal clock to the CPU, Acquisition and Display are gated out. However, the clocks to the Memory Interface, I^2C, Timer/Counters, WatchDog Timer and Pulse Width Modulators are maintained. The CPU state is frozen along with the status of all SFRs, internal RAM contents are maintained, as are the device output pin values. Since the output values on RGB and VDS are maintained the Display output must be disabled before entering this mode.

There are three methods available to recover from Idle:-

- Assertion of an enabled interrupt will cause the IDL bit to be cleared by hardware, thus terminating Idle mode. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Idle mode.
- A second method of exiting Idle is via an Interrupt generated by the SAD DC Compare circuit. When Painter is configured in this mode, detection of an analogue threshold at the input to the SAD may be used to trigger wake-up of the device i.e. TV Front Panel Key-press. As above, the interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into Idle.
- The third method of terminating Idle mode is with an external hardware reset. Since the oscillator is running, the hardware reset need only be active for two machine cycles (24 clocks at 12MHz) to complete the reset operation. Reset defines all SFRs and Display memory to a pre-defined state, but maintains all other RAM values. Code execution commences with the Program Counter set to ’0000’.

POWER DOWN MODE

In Power Down mode the XTAL oscillator continue to run, but the internal clock to the CPU, Acquisition, Display, Memory Interface, I^2C, Timer/Counters, WatchDog Timer and SAD & PWMs are gated out. The contents of all SFRs and Data memory are maintained, however, the contents of the Auxiliary/Display memory are lost. The port pins maintain the values defined by their associated SFRs. Since the output values on RGB and VDS are maintained the Display output must be made inactive before entering Power Down mode.

The power down mode is activated by setting the PD bit in the PCON register. It is advised to disable the WatchDog timer prior to entering Power down. There are three methods of exiting power down:-

- An External interrupt provides the first mechanism for waking from Power-Down. Since the clock is stopped, external interrupts needs to be set level sensitive prior to entering Power-Down. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Power-Down mode.
- A second method of exiting Power-Down is via an Interrupt generated by the SAD DC Compare circuit. When Painter is configured in this mode, detection of a certain analogue threshold at the input to the SAD may be used to trigger wake-up of the device i.e. TV Front Panel Key-press. As above, the interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into Power-Down.
- The third method of terminating the Power-Down mode is with an external hardware reset. Reset defines all SFRs and Display memory, but maintains all other RAM values. Code execution commences with the Program Counter set to ’0000’.

I/O Facility

I/O PORTS

The Painter die has 13 I/O lines, each is individually addressable, or form part of 4 parallel addressable ports which are port0, port1, port2 and port3.

PORT TYPE

All individual ports can be programmed to function in one of four modes, the mode is defined by two Port Configuration SFRs. The modes available are Open Drain, Quasi-bidirectional, High Impedance and Push-Pull.

Open Drain

The Open drain mode can be used for bi-directional operation of a port. It requires an external pull-up resistor, the pull-up voltage has a maximum value of 5.5V, to allow connection of the device into a 5V environment.

Quasi bi-directional

The quasi-bidirectional mode is a combination of open drain and push pull. It requires an external pull-up resistor to VDDp (nominally 3.3V). When a signal transition from 0->1 is output from the device, the pad is put into push-pull mode for one clock cycle (166ns) after which the pad goes into open drain mode. This mode is used to speed up the

edges of signal transitions. This is the default mode of operation of the pads after reset.

High Impedance
The high impedance mode can be used for Input only operation of the port. When using this configuration the two output transistors are turned off.

Push-Pull
The push pull mode can be used for output only. In this mode the signal is driven to either 0V or VDDp, which is nominally 3.3V.

Interrupt System
The device has 8 interrupt sources, each of which can be enabled or disabled. When enabled, each interrupt can be assigned one of two priority levels. There are four interrupts that are common to the 80C51, two of these are external interrupts (EX0 and EX1) and the other two are timer interrupts (ET0 and ET1). There is also one interrupt connected to the 80c51 micro-controller IIC peripheral for Transmit and Receive operation.
The TV processors have an additional 16-bit Timer (with 8-bit Pre-scaler). To accommodate this, another interrupt ET2PR has been added to indicate timer overflow.
In addition to the conventional 80c51, two application specific interrupts are incorporated internal to the device which have the following functionality:-
CC (Closed Caption Data Ready Interrupt) - This interrupt is generated when the device is configured for Closed Caption acquisition. The interrupt is activated at the end of the currently selected Slice Line as defined in the CCLIN SFR.
BUSY (Display Busy Interrupt) - An interrupt is generated when the Display enters either a Horizontal or Vertical Blanking Period. i.e. Indicates when the micro-controller can update the Display RAM without causing undesired effects on the screen. This interrupt can be configured in one of two modes using the MMR Configuration Register (Address 87FF, Bit-3 [TXT/V]):-

- TeXT Display Busy: An interrupt is generated on each active horizontal display line when the Horizontal Blanking Period is entered.
- Vertical Display Busy: An interrupt is generated on each vertical display field when the Vertical Blanking Period is entered.

INTERRUPT ENABLE STRUCTURE
Each of the individual interrupts can be enabled or disabled by setting or clearing the relevant bit in the interrupt enable SFRs (IE and IEN1). All interrupt sources can also be globally disabled by clearing the EA bit (IE.7).

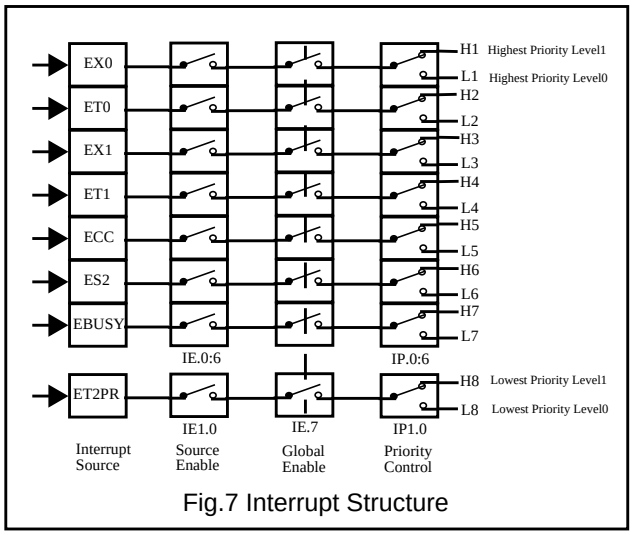


Fig.7 Interrupt Structure

INTERRUPT ENABLE PRIORITY
Each interrupt source can be assigned one of two priority levels. The interrupt priorities are defined by the interrupt priority SFRs (IP and IP1). A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt. A high priority interrupt can not be interrupted by any other interrupt source. If two requests of different priority level are received simultaneously, the request with the highest priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level there is a second priority structure determined by the polling sequence as defined in Table 3.

Source	Priority within level	Interrupt Vector
EX0	Highest	0003H
ET0		000BH
EX1		0013H
ET1		001BH
ECC		0023H
ES2		002BH
EBUSY		0033H
ET2PR	Lowest	003BH

Table 3 Interrupt Priority (within same level)

INTERRUPT VECTOR ADDRESS
The processor acknowledges an interrupt request by executing a hardware generated LCALL to the appropriate servicing routine. The interrupt vector addresses are shown in Table 3.

LEVEL/EDGE INTERRUPT

The external interrupt can be programmed to be either level-activated or transition activated by setting or clearing the IT0/1 bits in the Timer Control SFR(TCON).

ITx	Level	Edge
0	Active low	
1		INT0 = Negative Edge INT1 = Positive and Negative Edge

Table 4 External Interrupt Activation

The external interrupt INT1 differs from the standard 80C51 in that it is activated on both edges when in edge sensitive mode. This is to allow software pulse width measurement for handling remote control inputs.

Timer/Counter

Two 16 bit timers/counters are incorporated Timer0 and Timer1. Both can be configured to operate as either timers or event counters.

In Timer mode, the register is incremented on every machine cycle. It is therefore counting machine cycles. Since the machine cycle consists of 12 oscillator periods, the count rate is 1/12 Fosc = 1MHz.

In Counter mode, the register is incremented in response to a negative transition at its corresponding external pin T0/1. Since the pins T0/1 are sampled once per machine cycle it takes two machine cycles to recognise a transition, this gives a maximum count rate of 1/24 Fosc = 0.5MHz.

There are six special function registers used to control the timers/counters.

TF1	TR	TF0	TR	IE1	IT1	IE0	IT0

Symbol	Position	Name and Significance
TF1	TCON.7	Timer 1 overflow flag. Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR1	TCON.6	Timer 1 Run control bit. Set/cleared by software to turn timer.counter on/off.
TF0	TCON.5	Timer 0 overflow flag. Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR0	TCON.4	Timer 0 Run control bit. Set/cleared by software to turn timer.counter on/off.

Symbol	Position	Name and Significance
IE1	TCON.3	Interrupt 1 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT1	TCON.2	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
IE0	TCON.1	Interrupt 0 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT0	TCON.0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

Fig.8 Timer/Counter Control (TCON) register

Gat	C/T	M1	M0	Gat	C/T	M1	M0

Timer 1 | Timer 0

Gate: Gating control when set. Timer/counter is enabled only while px_int_n is high and TR control bit is set. When cleared timer/counter is enabled whenever TR control bit is set.

C/T: Timer or Counter selector. Cleared for timer operation (input from system clock). Set for counter operation (input from T input pin.

M1	M0	Operating
0	0	8048 Timer, TL serves as 5-bit prescaler.
0	1	16-bit Timer/Counter, TL and TH are cascaded.
1	0	8-bit auto-reload Timer/Counter, TH holds a value which is to be loaded into TL.
1	1	timer 0: two 8-bit Timers/Counters. TL0 is controlled by timer 0 control bits. TH0 is controlled by timer 1 control bits. timer 1: stopped.

Fig.9 Timer/Counter Mode control (TMOD) register

The Timer/Counter function is selected by control bits C/T in the Timer Mode SFR (TMOD). These two Timer/Counter have four operating modes, which are selected by bit-pairs (M1.M0) in the TMOD. Refer to the 80C51 based 8-bit micro-controllers - Philips Semiconductors (ref. IC20) for detail of the modes and operation.

TL0/TL1 and TH0/TH1 are the actual timer/counter registers for timer0 / timer1. TL0/TL1 is the low byte and TH0/TH1 is the high byte.

TIMER WITH PRE-SCALER

An additional 16-bit timer with 8-bit pre-scaler is provided to allow timer periods up to 16.777 seconds. This timer remains active during IDLE mode.
TP2L is the lower timer value and TP2H is the upper timer value. TP2PR provides an 8-bit pre-scaler for timer 2
In Timer mode, the register is incremented on every machine cycle. It is therefore counting machine cycles. Since the machine cycle consists of 12 oscillator periods, the count rate is 1/12 Fosc (1MHz).
TP2CRL is the control and status for timer 2. TP2CRL.0 is the timer enable and TP2CRL.1 is the timer overflow status.
At a count of zero (on TP2CL & TP2CH) the overflow flag is set:-
TP2CRL<1> = '0' : no Timer overflow,
TP2CRL<1> = '1' : Timer overflow.
This overflow flag will need to be reset by software. Upon overflow an interrupt also be generated. The timer is continue after overflow by re-loading the timer with the value of SFRs: TP2PR, TP2H & TP2L. The value on TP2PR, TP2H & TP2L is never changed unless updated by software. If the micro reads TP2PR, TP2H or TP2L at any stage, this return the value written and not the current timer value.
TP2CL and TP2CH are two additional SFRs that indicate the current timer value. These SFRs are readable both when the timer is active and inactive. Once the timer is disable, the Timer value at the timer of disabling are maintained on the SFRs of TP2CL and TP2CH.

WatchDog Timer

The WatchDog timer is a counter that once in an overflow state forces the micro-controller in to a reset condition. The purpose of the WatchDog timer is to reset the micro-controller if it enters an erroneous processor state (possibly caused by electrical noise or RFI) within a reasonable period of time. When enabled, the WatchDog circuitry will generate a system reset if the user program fails to reload the WatchDog timer within a specified length of time known as the WatchDog interval.
The WatchDog timer consists of an 8-bit counter with an 16-bit pre-scaler. The pre-scaler is fed with a signal whose frequency is 1/12 fosc (1MHz).
The 8 bit timer is incremented every 't' seconds where:

$$t=12x65536x1/fosc=12x65536x1/12x10^6 = 65.536ms$$

WATCHDOG TIMER OPERATION

The WatchDog operation is activated when the WLE bit in the Power Control SFR (PCON) is set. The WatchDog can be disabled by Software by loading the value 55H into the WatchDog Key SFR (WDTKEY). This must be performed before entering Idle/Power Down mode to prevent exiting the mode prematurely.
Once activated the WatchDog timer SFR (WDT) must be reloaded before the timer overflows. The WLE bit must be set to enable loading of the WDT SFR, once loaded the WLE bit is reset by hardware, this is to prevent erroneous Software from loading the WDT SFR.
The value loaded into the WDT defines the WatchDog interval.

$$\text{WatchDog interval} = (256 - WDT) * t = (256 - WDT) * 65.536ms.$$

The range of intervals is from WDT=00H which gives 16.777s to WDT=FFH which gives 65.536ms.

PORT Alternate Functions

The Ports 1,2 and 3 are shared with alternate functions to enable control of external devices and circuitry. The alternate functions are enabled by setting the appropriate SFR and also writing a '1' to the Port bit that the function occupies.

PWM PULSE WIDTH MODULATORS

The device has four 6-bit Pulse Width Modulated (PWM) outputs for analogue control of e.g. volume, balance, bass and treble. The PWM outputs generate pulse patterns with a repetition rate of 21.33us, with the high time equal to the PWM SFR value multiplied by 0.33us. The analogue value is determined by the ratio of the high time to the repetition time, a D.C. voltage proportional to the PWM setting is obtained by means of an external integration network (low pass filter).

PWM Control

The relevant PWM is enabled by setting the PWM enable bit PWxE in the PWMx Control register. The high time is defined by the value PWxV<5:0>

TPWM TUNING PULSE WIDTH MODULATOR

The device has a single 14-bit PWM that can be used for Voltage Synthesis Tuning. The method of operation is similar to the normal PWM except the repetition period is 42.66us.

TPWM Control

Two SFRs are used to control the TPWM, they are TDACL and TDACH. The TPWM is enabled by setting the TPWE bit in the TDACH SFR. The most significant bits TD<13:7> alter the high period between 0 and 42.33us. The 7 least significant bits TD<6:0> extend certain pulses by a further 0.33us. e.g. if TD<6:0> = 01H then 1 in 128 periods will be extended by 0.33us, if TD<6:0>=02H then 2 in 128 periods will be extended.

The TPWM will not start to output a new value until TDACH has been written to. Therefore, if the value is to be changed, TACL should be written before TDACH.

SAD SOFTWARE A/D

Four successive approximation Analogue to Digital Converters can be implemented in software by making use of the on board 4-bit Digital to Analogue Converter and Analogue Comparator.

SAD Control

The control of the required analogue input is done using the channel select bits CH<1:0> in the SAD SFR, this selects the required analogue input to be passed to one of the inputs of the comparator. The second comparator input is generated by the DAC whose value is set by the bits SAD<3:0> in the SADB SFRs. A comparison between the two inputs is made when the start compare bit ST in the SAD SFR is set, this must be at least one instruction cycle after the SAD<3:0> value has been set. The result of the comparison is given on VHI one instruction cycle after the setting of ST.

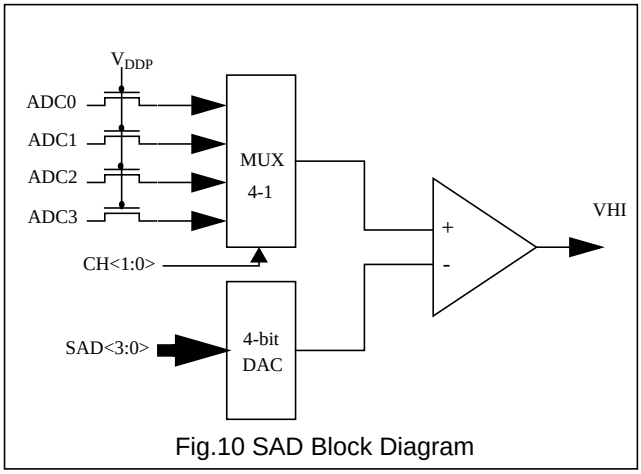


Fig.10 SAD Block Diagram

SAD Input Voltage

The external analogue voltage that is used for comparison with the internally generated DAC voltage, does not have the same voltage range due to the 5 V tolerance of the pin. It is limited to V_{DDP}-V_{tn} where V_{tn} is a maximum of 0.75 V. For further details refer to the SAA55XX and SAA56XX Software Analogue to Digital Converter Application Note: SPG/AN99022.

SAD DC Comparator Mode

The SAD module incorporates a DC Comparator mode which is selected using the 'DC_COMP' control bit in the SADB SFR. This mode enables the micro-controller to detect a threshold crossing at the input to the selected analogue input pin (P3.0, P3.1, P3.2 or P3.3) of the Software A/D Converter. A level sensitive interrupt is generated when the analogue input voltage level at the pin falls below the analogue output level of the SAD D/A converter.

This mode is intended to provide the device with a wake-up mechanism from Power-Down or Idle when a key-press on the front panel of the TV is detected.

The following software sequence should be used when utilizing this mode for Power-Down or Idle:-

1. Disable INT1 using the IE SFR.
2. Set INT1 to level sensitive using the TCON SFR.
3. Set the D/A Converter digital input level to the desired threshold level using the SADB SFR and select the required input pin (P3.0, P3.1, P3.2 or P3,3) using CH1, CH0 in the SAD SFR.
4. Enter DC Compare mode by setting the 'DC_COMP' enable bit in the SADB SFR.
5. Enable INT1 using the IE SFR.
6. Enter Power-Down/Idle. Upon wake-up the SAD should be restored to its conventional operating mode by disabling the 'DC_COMP' control bit.

I^2C Serial I/O Bus

The I^2C bus consists of a serial data line (SDA) and a serial clock line (SCL). The definition of the I^2C protocol can be found in the 80C51 based 8-bit micro-controllers - Philips Semiconductors (ref. IC20).

The device operates in four modes: -

- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver

The micro-controller peripheral is controlled by the Serial Control SFR (S1CON) and its Status is indicated by the status SFR (S1STA). Information is transmitted/received to/from the I^2C bus using the Data SFR (S1DAT) and the Slave Address SFR (S1ADR) is used to configure the slave address of the peripheral.

The byte level I^2C serial port is identical to the I^2C serial port on the 8xC558, except for the clock rate selection bits CR<2:0>. The operation of the subsystem is described in detail in the 8xC558 datasheet and can be found in the 80C51 based 8-bit micro-controllers - Philips Semiconductors (ref. IC20).

Three different IIC selection tables for CR<2:0> can be configured using the ROMBANK SFR (IIC_LUT<1:0>) as follows: -

'558 nominal mode' (iic_lut="00")
This option accommodates the 558 I²C. The various serial rates are shown below: -

CR2	CR1	CR0	f_{clk} (6MHz) divided by	I²C Bit Frequency (KHz) at f_{clk}
0	0	0	60	**100**
0	0	1	1600	3.75
0	1	0	40	150
0	1	1	30	200
1	0	0	240	25
1	0	1	3200	1.875
1	1	0	160	37.5
1	1	1	120	50

Table 5 IIC Serial Rates '558 nominal mode'

'558 fast mode' (iic_lut="01")
This option accommodates the 558 I²C doubled rates as shown below: -

CR2	CR1	CR0	f_{clk} (6MHz) divided by	I²C Bit Frequency (KHz) at f_{clk}
0	0	0	30	200
0	0	1	800	7.5
0	1	0	20	300
0	1	1	15	**400**
1	0	0	120	50
1	0	1	1600	3.75
1	1	0	80	75
1	1	1	60	**100**

Table 6 IIC Serial Rates '558 fast mode'

'558 slow mode' (iic_lut="10")
This option accommodates the 558 I²C rates divided by 2 as shown below: -

CR2	CR1	CR0	f_{clk} (6MHz) divided by	I²C Bit Frequency (KHz) at f_{clk}
0	0	0	120	50
0	0	1	3200	1.875
0	1	0	80	75
0	1	1	60	**100**
1	0	0	480	12.5
1	0	1	6400	0.9375
1	1	0	320	18.75
1	1	1	240	25

Table 7 IIC Serial Rates '558 slow mode'

Note: In the above tables the f_{Clk} relates to the clock rate of the 80c51 IIC module (6MHz).

I²C Port Enable
One external I²C port is available. This port is enabled using TXT21.I2C PORT EN. Any information transmitted to the device can only be acted upon if the port is enabled. Internal communication between the 80c51 micro-controller and the TV Signal Processor will continue regardless of the value written to TXT21.I2C PORT EN.

LED Support
Port pins P0.5 and P0.6 have a 8mA current sinking capability to enable LEDs in series with current limiting resistors to be driven directly, without the need for additional buffering circuitry.

MEMORY INTERFACE
The memory interface controls the access and refresh of the embedded Display DRAM memory. The DRAM is shared between the Display and Microcontroller sections. The Display reads OSD/Closed Caption information from the DRAM and converts it to RGB output values. The Microcontroller uses the DRAM as embedded auxiliary RAM.

Data Capture
The Data Capture section takes in the analogue Composite Video and Blanking Signal (CVBS) from One Chip, and from this extracts the required data, which is then decoded and stored in SFR memory.
The extraction of the data is performed in the digital domain. The first stage is to convert the analogue CVBS signal into a digital form. This is done using an ADC sampling at 12MHz. The data and clock recovery is then performed by a Multi-Rate Video Input Processor (MulVIP). From the recovered data and clock the following data types is extracted: Line Twenty-One Data Services (Closed Caption).

Data Capture Features
- Video Signal Quality detector.
- Data Capture for US Line 21 Data Services (Closed Caption).

- SFR flags indicating reception of US Line 21 Data Services.

Analogue to Digital Converter
The CVBS input is passed through a differential to single ended converter (DIVIS), although in this device it is used in single ended configuration with a reference.The analogue output of DIVIS is converted into a digital representation by a full flash ADC with a sampling rate of 12MHz.

Multi Rate Video Input Processor
The multi rate video input processor is a Digital Signal Processor designed to extract the data and recover the clock from the digital CVBS signal.

Data Standards
The data and clock standard that can be recovered is shown in Table 8 below:-

Data Standard	Clock Rate
Closed Caption	500 KHz

Table 8 Data Slicing Standard

Data Capture Timing
The Data Capture timing section uses the Synchronisation information extracted from the CVBS signal to generate the required Horizontal and Vertical reference timings. The timing section automatically recognises and selects the appropriate timings for either 625 (50Hz) synchronisation or 525 (60Hz) synchronisation. A flag TXT12.Video Signal Quality is set when the timing section is locked correctly to the incoming CVBS signal. When TXT12.Video Signal Quality is set another flag TXT12.625/525 SYNC can be used to identify the standard.

Acquisition
Closed Caption Acquisition
The US Closed Caption data is transmitted on line 21 (525 line timings) and is used for Captioning information, Text information and Extended Data Services. Closed Caption data is only acquired when TXT21.CC ON bit is set.
Two bytes of data are stored per field in SFRs, the first bye is stored in CCDAT1 and the second byte is stored in CCDAT2. The value in the CCDAT registers are reset to 00h at the start of the Closed Caption line defined by CCLIN.CS<4:0>. At the end of the Closed Caption line an interrupt is generated if IE.ECC is active.
The processing of the Closed Caption data to convert into a displayable format is performed by Software.

DISPLAY
The display section is based on the requirements for US Closed Caption. There are some enhancements for use with locally generated On-Screen Displays.
The display section reads the contents of the Display memory and interprets the control/character codes. Using this information and other global settings, the display produces the required RGB signals and Video/Data (Fast Blanking) signal for the TV signal processing.
The display is synchronised to the TV signal processing by way of Horizontal and Vertical sync signals generated within the TV processor. From these signals all display timings are derived.

Display Features
- US Closed Caption features and Enhanced OSD modes.
- Normal, Double Height, Double Width and Double size characters.
- Scrolling of display region.
- Variable flash rate controlled by software.
- Globally selectable scan lines per row 9/10/13/16/18.
- Globally selectable character matrix (HxV) 12x9, 12x10, 12x13, 12x16, 12x18, 16x9, 16x10, 16x13, 16x16 and 16x18.
- Globally selectable horizontal and vertical character spacing.
- Italics, Underline and Overline.
- Soft Colours using CLUT with 64 colour palette.
- Fringing (Shadow) selectable from N-S-E-W direction.
- Fringe colour selectable.
- Contrast reduction of defined area.
- Cursor.
- Special Graphics characters with two planes, allowing four colours per character.
- 16 Software re-definable On-Screen Display characters.

Display Configuration
The display section can be configured as a maximum of 16 rows with up to 48 characters per row. Both the Character matrix, and TV lines per row can be defined. There is an option of 9, 10, 13, 16 & 18 TV lines per display row, and a Character matrix (HxV) of 12x9, 12x10, 12x13, 12x16, 12x18, 16x9, 16x10, 16x13, 16x16 & 16x18. Additionally, up to 4 pixels of character spacing may be introduced between characters in the horizontal direction and up to 7 TV lines may be inserted between display rows.

Not all combinations of TV lines per row and maximum display rows give a sensible OSD display, since there is limited number of TV scan lines available.
Special Function Register, TXT21 is used to control the character matrix and lines per row.

Display Features
The following is a list of features available. Each setting can either be a serial or parallel attribute, and some have a global effect on the display.

Feature	CC
Flash	serial
Boxes	serial
Horizontal Size	x1/x2 (serial)
Vertical Size	x1/x2 (serial)
Italic	serial
Foreground colours	8+8 (parallel)
Background colours	16 (serial)
Soft Colours (CLUT)	16 from 64
Underline	serial
Overline	serial
Fringe	N+S+E+W
Fringe Colour	16 (Serial)
Contrast Reduction	serial
Fast Blanking Polarity	YES
Screen Colour	16 (Global)
DRCS	16 (Global)
Character Height	9/10/13/16/18
Character Width	12/16
Vertical Line Spacing	0-7
Horizontal Character Spacing	0-4
No. of Rows	16
No. of Columns	48
No of Characters displayable	256
Cursor	YES
Special Graphics (2 planes per character)	8
Scroll	One region

Table 9 Display Features

Display Feature Descriptions

FLASH

Flashing causes the foreground colour pixel to be displayed as the background pixels.The flash frequency is controlled by software setting and resetting display register REG0: Status at the appropriate interval. This attribute is valid from the time set (see Table 13) until the end of the row or until otherwise modified.

BOXES

This attribute is valid from the time set until end of row or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, then it is set from the next character onwards.

In CC text mode the background colour is displayed regardless of the setting of the box attribute bit. Boxes take affect only during mixed mode, where boxes are set in this mode the background colour is displayed. Character locations where boxes are not set show video/screen colour (depending on the setting in the display control register. REG0: Display Control) in stead of the background colour.

SIZE

The size of the characters can be modified in both the horizontal and vertical directions. Two sizes are available in both the horizontal and vertical directions. The sizes available are normal (x1), double (x2) height/width and any combination of these. The attribute setting is always valid for the whole row. Mixing of sizes within a row is not possible.

ITALIC

This attribute is valid from the time set until the end of the row or otherwise modified. The attribute causes the character foreground pixels to be offset horizontally by 1 pixel per 4 scan lines (interlaced mode). The base is the bottom left character matrix pixel. The pattern of the character is indented as shown in Fig.11.

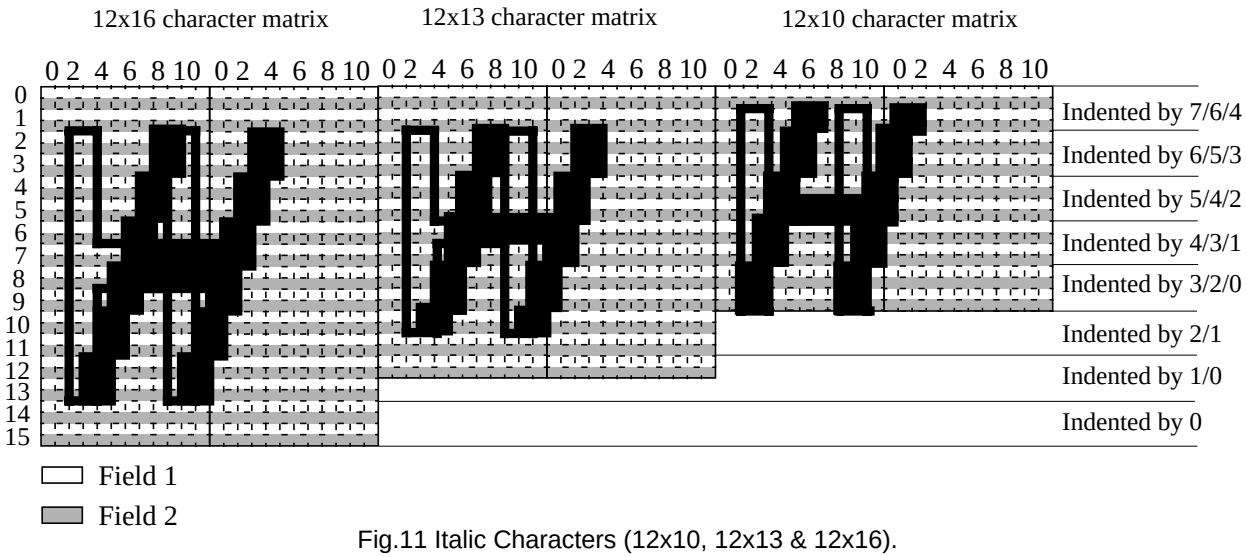


Fig.11 Italic Characters (12x10, 12x13 & 12x16).

COLOURS

CLUT (Colour Look Up Table)

A CLUT (Colour Look Up Table) with 16 colour entries is provided. The colours are programmable out of a palette of 64 (2 bits per R, G and B). The CLUT is defined by writing data to a RAM that resides in the MOVX address space of the 80C51.

RED1-0 b5 . b4	GRN1-0 b3 . b2	BLU1-0 b1 . b0	Colour entry
0 0	0 0	0 0	0
0 0	0 0	1 1	1
...	...	...	...
1 1	1 1	0 0	14
1 1	1 1	1 1	15

Table 10 CLUT Colour values

Foreground Colour
The foreground colour can be chosen from 8 colours on a character by character basis. Two sets of 8 colours are provided. A serial attribute switches between the banks (see Table 13 Serial Mode 1, bit 7). The colours are the CLUT entries 0 to 7 or 8 to 15.

Background Colour
This attribute is valid from the time set until end of row or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, then the colour is set from the next character onwards.
The background colour can be chosen from all 16 CLUT entries.

BACKGROUND DURATION
The attribute when set takes effect from the current position until to the end of the text display defined in REG4:Text Area End. The background duration attribute (see Table 13, Serial Mode 1, bit 8) in combination with the End Of Row attribute (see Table 13, Serial Mode 1, bit 9) forces the background colour to be display on the row until the end of the text area is reached.

UNDERLINE
The underline attribute causes the characters to have the bottom scan line of the character cell forced to foreground colour, including spaces. If background duration is set, then underline is set until the end of the text area. The underline attribute (see Table 13, Serial Mode 0/1, bit 4) is valid from the time set until end of row or otherwise modified.

OVERLINE
The overline attribute causes the characters to have the top scan line of the character cell forced to foreground colour, including spaces. If background duration is set, then overline is set until the end of the text area.
The overline attribute (see Table 13, Serial Mode 0/1, bit 5) is valid from the time set until end of row or otherwise modified. Overlining of Italic characters is not possible

END OF ROW
The number of characters in a row is flexible and can determined by the end of row attribute (see Table 13, Serial Mode 1, bit 9). However the maximum number of character positions displayed is determined by the setting of the REG2:Text Position Horizontal and REG4:Text Area End.
NOTE: When using the end of row attribute the next character location after the attribute should always be occupied by a 'space'.

FRINGING
A fringe (shadow) can be defined around characters. The fringe direction is individually selectable in any of the North, South, East and West direction using REG3:Fringing Control. The colour of the fringe can also be defined as one of the entries in the CLUT, again using REG3:Fringing Control.
The fringe attribute (see Table 13, Serial Mode 0, bit 9) is valid from the time set until the end of the row or otherwise modified.

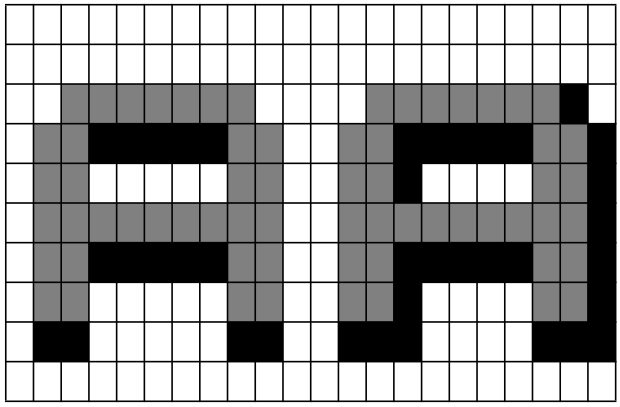


Fig.12 South and Southwest Fringing

CURSOR

The cursor operates by reversing the background and foreground colours in the character position pointed to by the active cursor position. The cursor is enabled using TXT7.CURSOR ON. When active, the row the cursor appears on is defined by TXT9.R<4:0> and the column is defined by TXT10.C<5:0>.

The valid range for row is 0 to 15. The valid range for column is 0 to 47. The cursor remains rectangular at all times, it's shape is not affected by italic attribute, therefore it is not advised to use the cursor with italic characters.

Fig.13 Cursor Display

SPECIAL GRAPHICS CHARACTERS

Several special characters are provided for improved OSD effects. These characters provide a choice of 4 colours within a character cell. The total number of special graphics characters is limited to 8. They are stored in the character codes 8Xh of the character table (16 ROM characters), or in the DRCs which overlay character codes 8Xh. Each special graphics character uses two consecutive normal characters.

Fringing, underline and overline is not possible for special graphics characters. Special graphics characters are activated when TXT20.OSD_PLANE = 1.

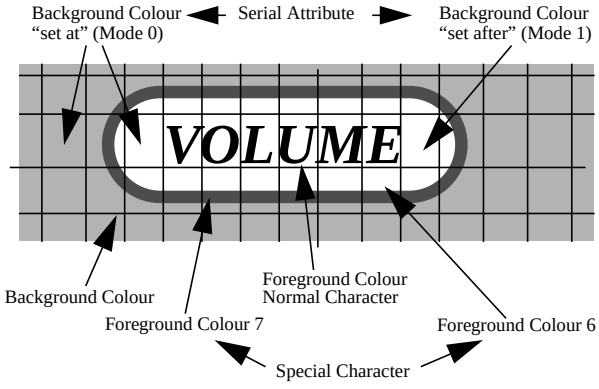


Fig.14 Special Character Example

The example in Fig.14 can be done with 8 special graphics characters.

If the screen colour is transparent (implicit in mixed mode) and inside the object the box attribute is set, then the object is surrounded by video. If the box attribute is not set the background colour inside the object will also be displayed as transparent.

Plane 1 0	Colour Allocation
0 0	Background Colour
0 1	Foreground Colour
1 0	CLUT entry 6
1 1	CLUT entry 7

Table 11 Special Character Colour allocation

SMOOTHING

Smoothing is activated using MMR 87F0<3>. The clarity of Double Height, Double Width and Double Size Characters are all improved when smoothing is enabled.

Smoothing is automatically disable for the duration of any special graphic characters.

Character and Attribute Coding

Character coding is split into character oriented attributes (parallel) and character group coding (serial). The serial attributes take effect either at the position of the attribute (Set At), or at the following location (Set After) and remain effective until either modified by a new serial attribute or until the end of the row. A serial attribute is represented as a space (the space character itself however is not used for this purpose), the attributes that are still active, e.g. overline and underline will be visible during the display of the space. The default setting at the start of a row is:

- 1x size, flash and italics OFF
- overline and underline OFF
- Display mode = superimpose
- fringing OFF
- background colour duration = 0
- end of row = 0
- Contrast Reduction = 0

The coding is done in 13 bit words. The codes are stored sequentially in the display memory. A maximum of 768 character positions can be defined for a single display.

PARALLEL CHARACTER CODING

Bits	Description
0-7	8 bit character code
8-10	3 bits for 8 foreground colours
11	Mode bit: 0 = Parallel code
12	Reserved

Table 12 Parallel Character Coding (bit 11 = 0)

SERIAL CHARACTER CODING

Bits	Description		
	Serial Mode 0 ("set at")	Serial Mode 1	
		Char.Pos. 1 ("set at")	Char.Pos. >1 ("set after")
0-3	4 bits for 16 Background colours	4 bits for 16 Background colours	4 bits for 16 Background colours
4	0 = Underline OFF 1 = Underline ON	Horizontal Size: 0 = normal 1 = x2	0 = Underline OFF 1 = Underline ON
5	0 = Overline OFF 1 = Overline ON	Vertical Size: 0 = normal 1 = x2	0 = Overline OFF 1 = Overline ON
6	Display mode: 0 = Superimpose 1 = Boxing	Display mode: 0 = Superimpose 1 = Boxing	Display mode: 0 = Superimpose 1 = Boxing
7	0 = Flash OFF 1 = Flash ON	Foreground colour switch 0 = Bank 0 (colours 0-7) 1 = Bank 1 (colours 8-15)	Foreground colour switch 0 = Bank 0 (colours 0-7) 1 = Bank 1 (colours 8-15)
8	0 = Italics OFF 1 = Italics ON	Background colour duration: 0 = stop BGC 1 = set BGC to end of row	Background colour duration (set at): 0 = stop BGC 1 = set BGC to end of row
9	0 = Fringing OFF 1 = Fringing ON	End of Row 0 = Continue Row 1 = End Row	End of Row (set at): 0 = Continue Row 1 = End Row
10	Switch for Serial coding mode 0 and 1: 0 = mode 0	Switch for Serial coding mode 0 and 1: 1 = mode 1	Switch for Serial coding mode 0 and 1: 1 = mode 1
11	Mode bit: 1 = Serial code	Mode bit: 1 = Serial code	Mode bit: 1 = Serial code
12	Contrast Reduction: 0 = No COR box 1 = COR box	Contrast Reduction: 0 = No COR box 1 = COR box	Contrast Reduction: 0 = No COR box 1 = COR box

Table 13 Serial Character Coding (bit 11 = 1)

Screen and Global Controls

A number of attributes are available that affect the whole display region, and cannot be applied selectively to regions of the display.

TV SCAN LINES PER ROW

The number of TV scan lines per field used for each display row can be defined, the value is independent of the character size being used. The number of lines can be either 10/13/16/18 per display row. The number of TV scan lines per row is defined TXT21.DISP_LINES<1:0>.
A value of 9 lines per row can be achieved if the display is forced into 525 line display mode by TXT17.DISP_FORCE<1:0>, or if the device is in 10 line mode and the automatic detection circuitry within display finds 525 line display syncs.

CHARACTER MATRIX (HXV)

There are several different character matrices available, these are 12x10, 12x13, 12x16, 12x18, 16x10, 16x13, 16x16 and 16x18. The selection is made using TXT21.CHAR_SIZE<1:0> and TXT10.CHAR_16/12 and is independent of the number of display lines selected per row.
If the character matrix is less than the number of TV scan lines per row then the matrix is padded with blank lines. If the character matrix is greater than the number of TV scan lines then the character is truncated.

CHARACTER SPACING

Characters may be spaced in both the horizontal and vertical directions. Inter character spacing in the horizontal direction can be defined using TXT37.CHAR SPACE<2:0> (0-4 pixels) and the number of TV lines between character rows can be defined using TXT37.TV LINE SPACE<2:0> (0-7 TV lines). These spacing are applied outside the selected character matrix and in addition to the number of TV lines per row.

DISPLAY MODES

When attributes superimpose or when boxing (see Table 13, Serial Mode 0/1, bit 6) is set, the resulting display depends on the setting of the following screen control mode bits in REG0:Display Control.

Display Mode	MOD 1 0	Description
Video	0 0	Video mode disables all display activities and sets the RGB to true black and VDS to video.
Full Text	0 1	Full Text mode displays screen colour at all locations not covered by character foreground or background colour. The box attribute has no effect.
Mixed Screen Colour	1 0	Mixed Screen mode displays screen colour at all locations not covered by character foreground, within boxed areas or, background colour.
Mixed Video	1 1	Mixed Video mode displays video at all locations not covered by character foreground, within boxed areas or, background colour.

Table 14 Display Modes

SCREEN COLOUR

Screen colour is displayed from 10.5 ms to 62.5 ms after the active edge of the HSync input and on TV lines 23 to 310 inclusive, for a 625 line display, and lines 17 to 260 inclusive for a 525 line display.
The screen colour is defined by REG0:Display Control and points to a location in the CLUT table. The screen colour covers the full video width. It is visible when the Full Text or Mixed Screen Colour mode is set and no foreground or background pixels are being displayed.

Text Display Controls

TEXT DISPLAY CONFIGURATION

Two types of area are possible. The one area is static and the other is dynamic. The dynamic area allows scrolling of a region to take place. The areas cannot cross each other. Only one scroll region is possible.

Display Map

The display map allows a flexible allocation of data in the memory to individual rows.
Sixteen words are provided in the display memory for this purpose. The lower 10 bits address the first word in the

memory where the row data starts. This value is an offset in terms of 16-bit words from the start of Display Memory (8000 Hex). The most significant bit enables the display when not within the scroll (dynamic) area.
The display map memory is fixed at the first 16 words in the closed caption display memory.

b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
		Pointer to Row Data									
	Reserved, should be set to 0										
Text Display Enable, valid outside Soft Scroll Area 0 = Disable 1 = Enable											

Table 15 Display map Bit Allocation

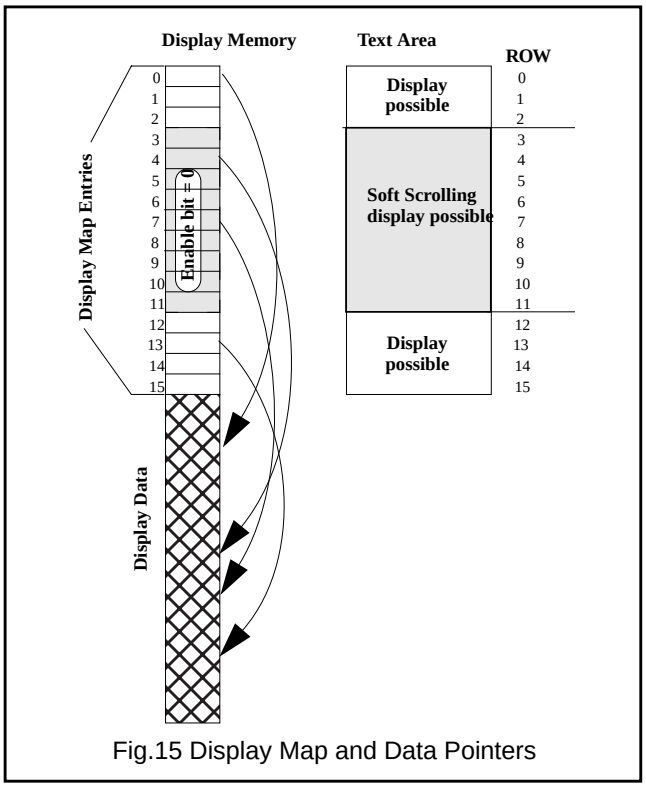


Fig.15 Display Map and Data Pointers

SOFT SCROLL ACTION

The dynamic scroll region is defined by the REG5:Scroll Area, REG6:Scroll Range, REG14:Top Scroll line and the REG8:Status Register. The scroll area is enabled when the SCON bit is set in REG8: Status.
The position of the soft scroll area window is defined using the Soft Scroll Position (SSP<3:0), and the height of the window is defined using the Soft Scroll Height (SSH<3:0>) both are in REG6:Scroll Range. The rows that are scrolled through the window are defined using the Start Scroll Row (STS<3:0>) and the Stop Scroll Row (SPS<3:0>) both are in REG5:Scroll Area.
The soft scrolling function is done by modifying the Scroll Line (SCL<4:0>) in REG14: Top Scroll Line. and the first scroll row value SCR<3:0> in REG8:Status. If the number of rows allocated to the scroll counter is larger than the defined visible scroll area, this allows parts of rows at the top and bottom to be displayed during the scroll function. The registers can be written throughout the field and the values are updated for display with the next field sync. Care should be taken that the register pairs are written to by the software in the same field.
Only a region that contains only single height rows or only double height rows can be scrolled.

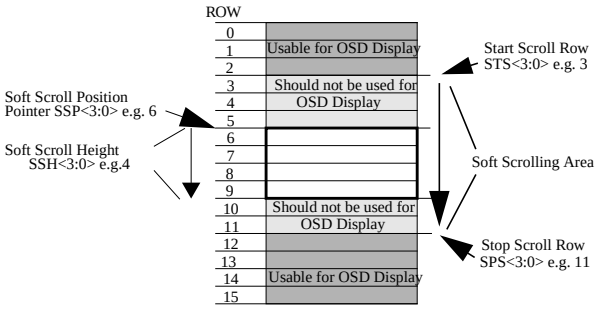


Fig.16 Soft Scroll Area

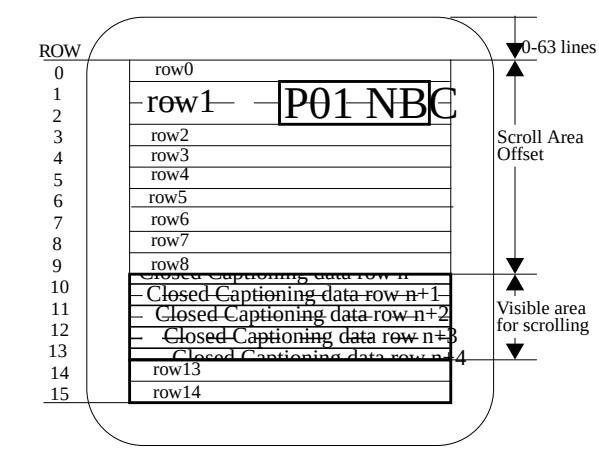


Fig.17 CC Text Areas

Display Positioning

The display consists of the **Screen Colour** covering the whole screen and the **Text Area** that is placed within the visible screen area. The screen colour extends over a large vertical and horizontal range so that no offset is

needed. The text area is offset in both directions relative to the vertical and horizontal sync pulses.

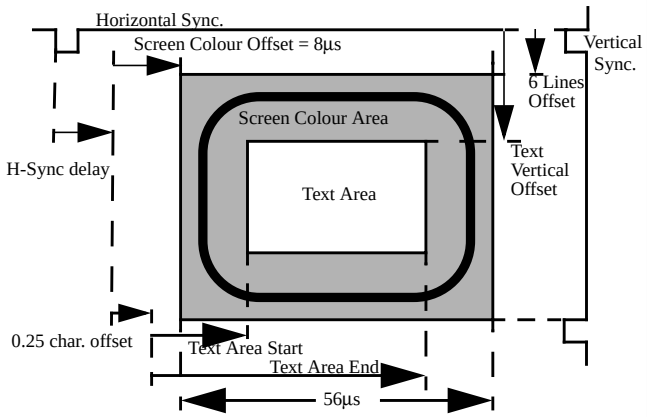


Fig.18 Display Area Positioning

SCREEN COLOUR DISPLAY AREA

This area is covered by the screen colour. The screen colour display area starts with a fixed offset of 8 us from the leading edge of the horizontal sync pulse in the horizontal direction. A vertical offset is not necessary.

Horizontal	starts 8 us after the leading edge of H-Sync for 56 us.
Vertical	line 9, field 1 (321, field 2) with respect to leading edge of vertical sync (line numbering using 625 Standard).

Table 16 Screen Colour Display Area

TEXT DISPLAY AREA

The text area can be defined to start with an offset in both the horizontal and vertical direction.

Horizontal	Up to 48 full sized characters per row. Start position setting from 3 to 64 characters from the leading edge of H-Sync. Fine adjustment in quarter characters.
Vertical	256 lines (nominal 41- 297). Start position setting from leading edge of vertical sync legal values are 4 to 64 lines. (line numbering using 625 Standard)

Table 17 Text Display Area

The horizontal offset is set in REG2: Text Area Start. The offset is done in full width characters using TAS<5:0> and quarter characters using HOP<1:0> for fine setting. The values 00h to 03h for TAS<5:0> will result in a corrupted display.

The width of the text area is defined in REG4:Text Area End by setting the end character value TAE<5:0>. This number determines where the background colour of the Text Area will end if set to extend to the end of the row. It will also terminate the character fetch process thus eliminating the necessity of a ***row end*** attribute. This entails however writing to all positions.

The vertical offset is set in REG1:Text Position Vertical Register. The offset value VOL<5:0> is done in number of TV scan lines.

NOTE: REG1:Text Position Vertical Register should not be set to 00 Hex as the Display Busy interrupt is not generated in these circumstances.

Character Set

To facilitate the global nature of the device the single character set can contain characters with four different character matrix sizes.

CHARACTER MATRICES

The character matrices that can be accommodated are: - (HxVxPlanes) 12x9x1, 12x10x1, 12x13x1, 12x16x1 and 16x18x1.

These modes allow two colours per character position. Three additional character matrices are available to allow four colours per character: -
(HxVxPlanes) 12x13x2, 12x16x2 and 16x18x2.

CHARACTER STORAGE

A single character set is available with up to 256 characters at 16x18x1. Different character matrix sizes may be stored at each character location, but only one character matrix size may be displayed on the screen at any one time.

In applications where only a few OSD characters are required or where the smaller matrices are to be used the unused character memory space may be utilized for the 80c51 micro-controller program memory.

CHARACTER TABLE

The character table is shown in Table 18:-

Character code rows (Bits 0-3)	Character code columns (Bits 4-7)															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		®	SP	0	@	P	ú	p								
1		°	!	1	A	Q	a	q								
2		1/2	"	2	B	R	b	r								
3		¿	#	3	C	S	c	s								
4		™	$	4	D	T	d	t								
5		¢	%	5	E	U	e	u								
6		£	&	6	F	V	f	v								
7		♪	´	7	G	W	g	w								
8		à	(	8	H	X	h	x								
9		_	)	9	I	Y	i	y								
A		è	á	:	J	Z	j	z								
B		â	+	;	K	[	k	ç								
C		ê	,	<	L	é	l									
D		î	-	=	M	]	m	Ñ								
E		ô	.	>	N	í	n	ñ								
F		û	/	?	O	ó	o	n								

Table 18 Closed Caption Character Table

Special Characters are in column 8.

Additional table locations for normal characters

Table locations for normal characters

Re-definable Characters

A number of Dynamically Re-definable Characters (DRC) are available. These are mapped onto the normal character codes, and replace the pre-defined OTP character Rom value.

There are 16 DRCs which occupy character codes 80H to 8FH. Alternatively, These locations can be utilized as 8 special graphics characters. The remapping of the standard OSD to the DRCs is activated when the TXT20.DRCS ENABLE bit is set. The selection of Normal or Special OSD symbols is defined by the TXT20.OSD PLANES.

Each character is stored in a matrix of 16x18x1 (V x H x planes), this allows for all possible character matrices to be defined within a single location.

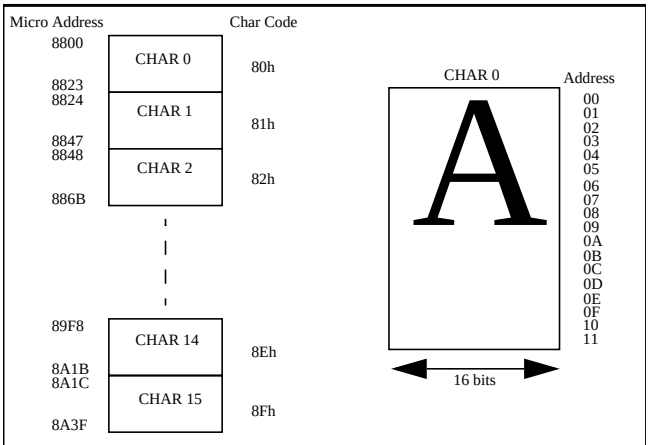


Fig.19 Organisation of DRC RAM

DEFINING CHARACTERS

The DRC RAM is mapped on to the 80C51 RAM address space and starts at location 8800H. The character matrix is 16 bits wide and therefore requires two bytes to be written for each word, the first byte (even addresses), addresses the lower 8 bits and the second byte (odd addresses) addresses the upper 8 bits.

For characters of 9, 10, 16 or 18 lines high the pixel information starts in the first address and continues sequentially for the required number of addresses. Characters of 13 lines high are defined with an initial offset of 1 address, this is to allow for correct generation of fringing across boundaries of clustered characters (see Fig.20). The characters continue sequentially for 13 lines after which a further line can again be used for generation of correct fringing across boundaries of clustered characters.

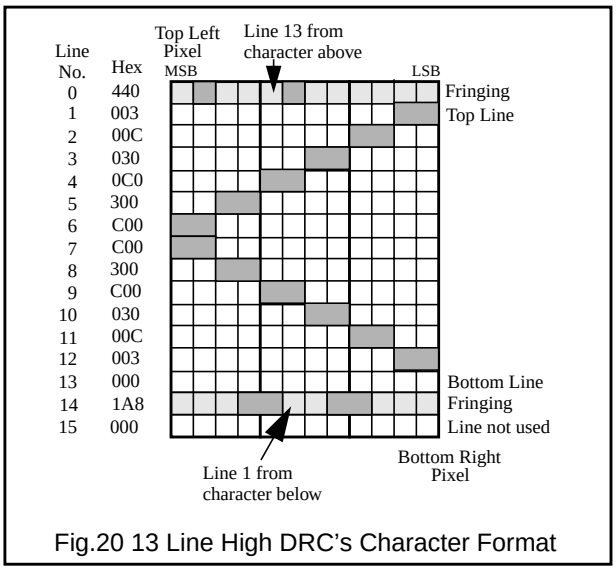


Fig.20 13 Line High DRC's Character Format

DRCs are defined by writing data to the DRC RAM using the 80C51 MOVX command. Setting bits 3 to 9 of the first line of a 12 wide by 16 line character would require setting the high byte of the 80C51 data pointer to 88H, the low byte of the 80C51 data pointer to 00H, using the MOVX command to load address 8800H with data F8H, incrementing the data pointer, and finally using the MOVX command to load address 8801H with data 03H.

Display Synchronization

The horizontal and vertical synchronizing signals from the TV deflection are used as inputs. Both signals can be inverted before being delivered to the Phase Selector section.

The polarity is controlled using either VPOL or HPOL in REG2:Text position Vertical.

A line locked 12 MHz clock is derived from the 12MHz free running oscillator by the Phase Selector. This line locked clock is used to clock the whole of the Display block. The H & V Sync signals are synchronized with the 12 MHz clock before being used in the display section.

Video/Data Switch (Fast Blanking) Polarity

The polarity of the Video/Data (Fast Blanking) signal can be inverted. The polarity is set with the VDSPOL in REG7: VDS Polarity register.

VDSPOL	VDS	Condition
0	1	RGB display
0	0	Video Display
1	0	RGB display
1	1	Video Display

Table 19 Fast Blanking Signal Polarity

Video/Data Switch Adjustment

To take into account the delay between the RGB values and the VDS signal due to external buffering, the VDS signal can be moved in relation to the RGB signals. The VDS signal can be set to be either a clock cycle before or after the RGB signal, or coincident with the RGB signal. This is done using VDEL<2:0> in REG15:Configuration.

Contrast Reduction

The COR bits in SFRs TXT5 control the Contrast Reduction. Contrast Reduction can be enabled either inside or outside OSD boxes.

When contrast reduction is enable, the contrast reduction region can be defined by the Serial Character Coding(bit 12).

Memory Mapped Registers

The memory mapped registers are used to control the display. The registers are mapped into the Micro-controller MOVX address space, starting at address 87F0h and extending to 87FFh.

MMR MAP

ADD	R/W	Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
87F0	R/W	**Display Control**	SRC<3>	SRC<2>	SRC<1>	SRC<0>	SMTH	Reserved	MOD<1>	MOD<0>
87F1	R/W	**Text Position Vertical**	VPOL	HPOL	VOL<5>	VOL<4>	VOL<3>	VOL<2>	VOL<1>	VOL<0>
87F2	R/W	**Text Area Start**	HOP<1>	HOP<0>	TAS<5>	TAS<4>	TAS<3>	TAS<2>	TAS<1>	TAS<0>
87F3	R/W	**Fringing Control**	FRC<3>	FRC<2>	FRC<1>	FRC<0>	FRDN	FRDE	FRDS	FRDW
87F4	R/W	**Text Area End**	VOR<1>	VOR<0>	TAE<5>	TAE<4>	TAE<3>	TAE<2>	TAE<1>	TAE<0>
87F5	R/W	**Scroll Area**	SSH<3>	SSH<2>	SSH<1>	SSH<0>	SSP<3>	SSP<2>	SSP<1>	SSP<0>
87F6	R/W	**Scroll Range**	SPS<3>	SPS<2>	SPS<1>	SPS<0>	STS<3>	STS<2>	STS<1>	STS<0>
87F7	R/W	**VDS Polarity**	VDSPOL	-	-	-	-	-	-	-
87F8	R	**Status read**	BUSY	FIELD	SCON	FLR	SCR<3>	SCR<2>	SCR<1>	SCR<0>
87F8	W	**Status write**	-	-	SCON	FLR	SCR<3>	SCR<2>	SCR<1>	SCR<0>
87FC	R/W	**H-Sync. Delay**	-	HSD<6>	HSD<5>	HSD<4>	HSD<3>	HSD<3>	HSD<1>	HSD<0>
87FD	R/W	**V-Sync. Delay**	-	VSD<6>	VSD<5>	VSD<4>	VSD<3>	VSD<2>	VSD<1>	VSD<0>
87FE	R/W	**Top Scroll Line**	-	-	-	SCL<4>	SCL<3>	SCL<2>	SCL<1>	SCL<0>
87FF	R/W	**Configuration**	CC	VDEL<2>	VDEL<1>	VDEL<0>	TXT/V	-	-	-

Table 20 MMR Memory Map

MMR BIT DEFINITION

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
Display Control.	SRC<3>	SRC<2>	SRC<1>	SRC<0>	SMTH	Reserved	MOD<1>	MOD<0>	00H
SRC<3:0>	Screen Colour definition								
SMTH	0 - Smoothing inactive 1 - Smoothing active for Double Size, Double Height and Double width								
Reserved	Must be kept ’0’ as reset value								
MOD<1:0>	00 - Video 01 - Full Text 10 - Mixed Screen Colour 11 - Mixed Video								
Text Position Vertical	VPOL	HPOL	VOL<5>	VOL<4>	VOL<3>	VOL<2>	VOL<1>	VOL<0>	00H
VPOL	0 - Input polarity 1 - Inverted input polarity								
HPOL	0 - Input Polarity 1 - Inverted input polarity								
VOL<5:0>	Display start Vertical Offset from V-Sync. (lines)								
Text Area Start	HOP<1>	HOP<0>	TAS<5>	TAS<4>	TAS<3>	TAS<2>	TAS<1>	TAS<0>	00H
HOP<1:0>	Fine Horizontal Offset in quarter of characters								
TAS<5:0>	Text area start								
Fringing Control.	FRC<3>	FRC<2>	FRC<1>	FRC<0>	FRDN	FRDE	FRDS	FRDW	00H
FRC<3:0>	Fringing colour, value address of CLUT								
FRDN	0 - No fringe in North direction 1 - Fringe in North direction								
FRDE	0 - No fringe in East direction 1 - Fringe in East direction								
FRDS	0 - No fringe in South direction 1 - Fringe in South direction								
FRDW	0 - No fringe in West direction 1 - Fringe in West direction								
Text Area End	VOR<1>	VOR<0>	TAE<5>	TAE<4>	TAE<3>	TAE<2>	TAE<1>	TAE<0>	00H
VOR<1:0>	Range bits for Display start Vertical Offset from V-Sync. (Equivalent to bit 7&6 of VOL, see MMR 87F1h).								
TAE<5:0>	Text Area End, in full characters								
Scroll Area	SSH<3>	SSH<2>	SSH<1>	SSH<0>	SSP<3>	SSP<2>	SSP<1>	SSP<0>	00H
SSH<3:0>	Soft Scroll Height								
SSP<3:0>	Soft Scroll Position								
Scroll Range	SPS<3>	SPS<2>	SPS<1>	SPS<0>	STS<3>	STS<2>	STS<1>	STS<0>	00H

Table 21 MMR Descriptions

SPS<3:0>	Stop Scroll row								
STS<3:0>	Start Scroll row								
VDS Polarity	VDSPOL	-	-	-	-	-	-	-	00H
VDSPOL	VDS Polarity 0 - RGB (1), Video (0) 1 - RGB (0), Video (1)								
Status read	BUSY	FIELD	SCON	FLR	SCR<3>	SCR<2>	SCR<1>	SCR<0>	00H
BUSY	0 - Access to display memory will not cause display problems 1 - Access to display memory could cause display problems.								
FIELD	0 - Odd Field 1 - Even Field								
FLR	0 - Active flash region foreground and background displayed 1 - Active flash region background only displayed								
SCR<3:0>	First scroll row								
Status write	-	-	SCON	FLR	SCR<3>	SCR<2>	SCR<1>	SCR<0>	00H
SCON	0 - Scroll area disabled 1 - Scroll area enabled								
FLR	0 - Active flash region foreground and background colour displayed 1 - Active flash region background colour only displayed								
SCR<3:0>	First Scroll Row								
H-Sync. delay	-	HSD<6>	HSD<5>	HSD<4>	HSD<3>	HSD<3>	HSD<1>	HSD<0>	00H
HSD<6:0>	H-Sync delay, in full size characters								
V-Sync Delay	-	VSD<6>	VSD<5>	VSD<4>	VSD<3>	VSD<2>	VSD<1>	VSD<0>	00H
VSD<6:0>	V-Sync delay in step of 8 clock cycles								
Top Scroll Line	-	-	-	SCL<4>	SCL<3>	SCL<2>	SCL<1>	SCL<0>	00H
SCL<4:0>	Top line for scroll								
Configuration	CC	VDEL<2>	VDEL<1>	VDEL<0>	TXT/V	-	-	-	00H
CC	0 - OSD mode 1 - Closed Caption mode								
VDEL<2:0>	Pixel delay between VDS and RGB output 000 - VDS switched to video, not active 001 - VDS active one pixel earlier then RGB 010 - VDS synchronous to RGB 100 - VDS active one pixel after RGB								
TXT/V	BUSY Signal switch 1 - Horizontal 0 - Vertical								

Table 21 MMR Descriptions

OTP MEMORY

The Painter die has one OTP module: -
User: 32K x 16-bit (55Kbyte of Program ROM and 4.5K word Character ROM).
Test: 0.5K x 16-bit.
These may be programmed by using the Parallel Programming Interface

Parallel Programming

The following pins form the parallel programming interface:-

Pin	Name	Function
P0.5	IO(0)	Bit 0:- Address/Data/Mode
P0.6	IO(1)	Bit 1:- Address/Data/Mode
P1.0	IO(2)	Bit 2:- Address/Data/Mode
P1.1	IO(3)	Bit 3:- Address/Data/Mode
P1.2	IO(4)	Bit 4:- Address/Data/Mode
P1.3	IO(5)	Bit 5:- Address/Data/Mode
P3.1	IO(6)	Bit 6:- Address/Data/Mode
P3.2	IO(7)	Bit 7:- Address/Data/Mode
P2.0	OEB	Output Enable 0 = IO is output 1 = IO is input
P3.0	WEB	Write Enable, programming pulse >100us 0 = Program
P1.6	MODE	0 = IO(7:0) defined by A/DB 1 = IO(7:0) contains mode information
P1.7	A/DB	0 = IO(7:0) contains Data 1 = IO(7:0) contains Address Information
P3.3		Unused
VPE	VPE	9V Programming Voltage
RESET	RESET	Device reset/ mode selection
XTALIN	CLK	Clock 4 MHz

Table 22 Parallel Programming Interface

Security Bits

The family of devices have a set of security bits for the combined OTP Program ROM and Character ROM. The security bits are used to prevent the ROM from being overwritten once programmed, and also the contents being verified once programmed. The security bits are one-time programmable and CANNOT be erased.

The memory and security bits are structured as follows:-

MEMORY			SECURITY BITS INTERACTION		
			USER ROM Programming (Enable/Disable)	TEST ROM Programming (Enable/Disable)	Verify (Enable/Disable)
PROGRAM ROM and CHARACTER ROM	USER ROM (i.e. 32k x 16bits)	=	Yes	No	Yes
	TEST ROM RESERVED (1k x 8 bits)	=	No	Yes	Yes

Table 23 Security bit structure

The security bits are set as follows for production programmed devices (i.e. programmed by Philips):-

MEMORY		SECURITY BITS SET		
		USER ROM Programming (Enable/Disable)	TEST ROM Programming (Enable/Disable)	Verify (Enable/Disable)
PROGRAM ROM and CHAR ROM	=	DISABLED	DISABLED	ENABLED

Table 24 Security bits for production devices

The security bits are set as follows for production un-programmed (blank) devices:-

MEMORY		SECURITY BITS SET		
		USER ROM Programming (Enable/Disable)	TEST ROM Programming (Enable/Disable)	Verify (Enable/Disable)
PROGRAM ROM and CHAR ROM	=	ENABLED	DISABLED	ENABLED

Table 25 Security bits for Blank devices

FUNCTIONAL DESCRIPTION OF VIDEO PROCESSOR

Vision IF amplifier

The vision IF amplifier can demodulate signals with negative modulation. The PLL demodulator is completely alignment-free.

The VCO of the PLL circuit is internal and the frequency is fixed to the required value by using the clock frequency of the μ-Controller as a reference. The setting of the various frequencies (38, 38.9, 45.75 and 58.75 MHz) can be made via the control bits IFB-IFC in subaddress 27H. Because of the internal VCO the IF circuit has a high immunity to EMC interferences.

FM demodulator

The FM demodulator is realised as narrow-band PLL with external loop filter, which provides the necessary selectivity without using an external band-pass filter. To obtain a good selectivity a linear phase detector and a constant input signal amplitude are required. For this reason the intercarrier signal is internally supplied to the demodulator via a gain controlled amplifier and AGC circuit. To improve the selectivity an internal bandpass filter is connected in front of the PLL circuit.

The nominal frequency of the demodulator is tuned to the required frequency (4.5/5.5/6.0/6.5 MHz) by means of a calibration circuit which uses the clock frequency of the μ-Controller as a reference. The setting to the wanted frequency is realised by means of the control bits FMA/FMB in the control bit 29H.

From the output status bytes it can be read whether the PLL frequency is inside or outside the window and whether the PLL is in lock or not. With this information it is possible to make an automatic search system for the incoming sound frequency. This can be realised by means of a software loop which switches the demodulator to the various frequencies and then select the frequency on which a lock condition has been found.

The amplitude deemphasis output signal changed with 6 dB by means of the AGN bit. In this way output signal differences between the 4.5 MHz standard (frequency deviation ±25 kHz) and the other standards (frequency deviation ±50 kHz) can be compensated.

Audio circuit and input signal selection

The audio control circuit contains an audio switch with 1 external input and a volume control circuit. The selection of the input is made by means of the ADX bit.

When required the Automatic Volume Levelling (AVL) function can be activated. The capacitor which is required for this function must be connected to combination pin AVL/REFO/SNDIF. This choice is made via the CBM0/1 bits (in subaddress 22H). When the AVL is active it automatically stabilises the audio output signal to a certain level.

It is possible to use the deemphasis pin as additional audio input. In that case the internal signal must, of course, be switched off. This can be realised by means of the sound mute bits (SM0/SM1 in subaddress 29H).

CVBS and Y/C input signal selection

The ICs have 2 inputs for external CVBS signals and one input can also be used as one Y/C input (see Fig. 21).

It is possible to supply the selected CVBS signal to the demodulated IF video output pin. This mode is selected by means of the SVO bit in subaddress 22H. The vision IF amplifier is switched off in this mode.

The video ident circuit can be connected to the incoming ‘internal’ video signal or to the selected signal. This ident circuit is independent of the synchronisation and can be used to switch the time-constant of the horizontal PLL depending on the presence of a video signal (via the VID bit). In this way a very stable OSD can be realised.

The subcarrier output is combined with a 3-level output switch (0 V, 2.3 V and 4.5 V). The output level and the availability of the subcarrier signal is controlled by the CMB1 and CMB0 bits. The output can be used to switch sound traps etc. It is also possible to use this pin for the connection of the AVL capacitor.

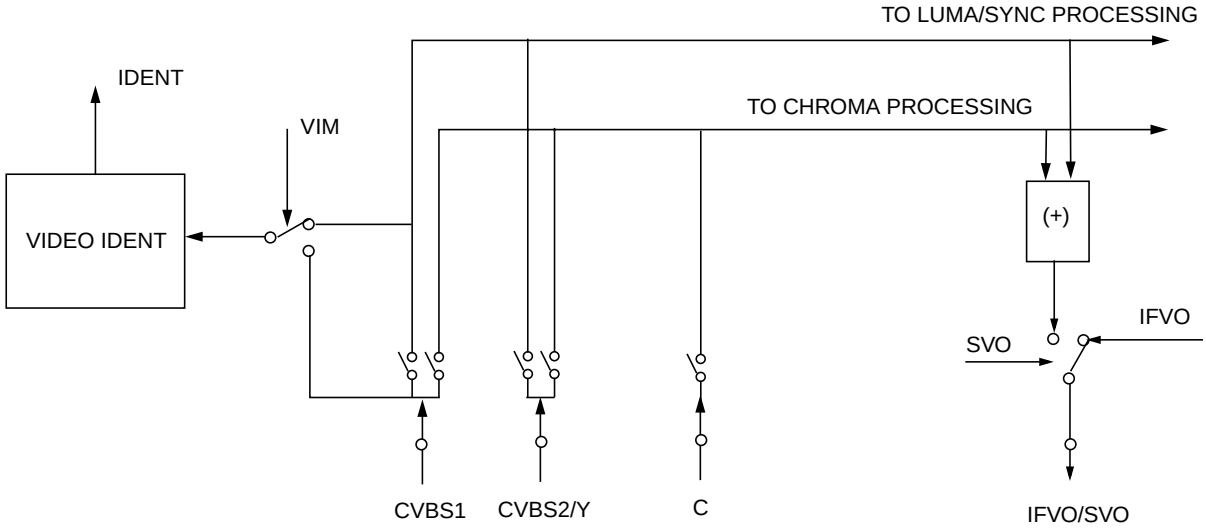


Fig.21 CVBS switch and interfacing of video ident

Synchronisation circuit

The IC contains separator circuits for the horizontal and vertical sync pulses and a data-slicing circuit which extracts the digital closed caption data from the analog signal.

The horizontal drive signal is obtained from an internal VCO which is running at a frequency of 25 MHz. This oscillator is stabilised to this frequency by using a 12 MHz signal coming from the reference oscillator of the μ-Controller.

The horizontal drive is switched on and off via the soft start/stop procedure. This function is realised by means of variation of the T_{ON} of the horizontal drive pulses. In addition the horizontal drive circuit has a 'low-power start-up' function.

The vertical synchronisation is realised by means of a divider circuit. The vertical ramp generator needs an external resistor and capacitor. For the vertical drive a differential output current is available. The outputs must be DC coupled to the vertical output stage.

The following geometry parameters can be adjusted:

- Horizontal shift
- Vertical amplitude
- Vertical slope
- S-correction
- Vertical shift
- EW width
- EW parabola width
- EW upper and lower corner parabola correction
- EW trapezium correction
- Vertical zoom
- Horizontal parallelogram and bow correction.

When the vertical amplitude is compressed (zoom factor <1) it is still possible to display the black current measuring lines in the overscan. This function is activated by means of the bit OSVE in subaddress 26H.

Chroma, luminance and feature processing

The chroma band-pass and trap circuits are realised by means of gyrators and are tuned to the right frequency by comparing the tuning frequency with the reference frequency of the colour decoder. The luminance delay line and the delay cells for the peaking circuit are also realised with gyrators.

The circuits contain the following picture improvement features:

- Peaking control circuit. The ratio of the positive and negative overshoots of the peaking can be adjusted by means of the bits RPO1/RPO0 in subaddress 2EH.
- Video dependent coring in the peaking circuit. The coring can be activated only in the low-light parts of the screen. This effectively reduces noise while having maximum peaking in the bright parts of the picture.
- Black stretch. This function corrects the black level for incoming signals which have a difference between the black level and the blanking level.
- Blue-stretch. This circuit is intended to shift colour near 'white' with sufficient contrast values towards more blue to obtain a brighter impression of the picture.
- Dynamic skin tone (flesh) control. This function is realised in the YUV domain by detecting the colours near to the skin tone.

Colour decoder

The ICs can decode PAL and NTSC signals. The PAL/NTSC decoder does not need external reference crystals but has an internal clock generator which is stabilised to the required frequency by using the 12 MHz clock signal from the reference oscillator of the μ-Controller.

Under bad-signal conditions (e.g. VCR-playback in feature mode), it may occur that the colour killer is activated although the colour PLL is still in lock. When this killing action is not wanted it is possible to overrule the colour killer by forcing the colour decoder to the required standard and to activate the FCO-bit (Forced Colour On) in subaddress 21H.

The Automatic Colour Limiting (ACL) circuit (switchable via the ACL bit in subaddress 20H) prevents that oversaturation occurs when PAL/NTSC signals with a high chroma-to-burst ratio are received. The ACL circuit is designed such that it only reduces the chroma signal and not the burst signal. This has the advantage that the colour sensitivity is not affected by this function.

The base-band delay line is integrated. This delay line is also active during NTSC to obtain a good suppression of cross colour effects. The demodulated colour difference signals are internally supplied to the delay line.

RGB output circuit and black-current stabilization

In the RGB control circuit the signal is controlled on contrast, brightness and saturation. The ICs have a linear input for external RGB/YUV signals. Switching between RGB and the YUV/YP_RP_B mode can be realised via the YUV0/YUV1 bits in subaddress 2BH. The signals for OSD and text are internally supplied to the control circuit. The output signal has an amplitude of about 2 V black-to-white at nominal input signals and nominal settings of the various controls.

To obtain an accurate biasing of the picture tube the 'Continuous Cathode Calibration' (CCC) system has been included in these ICs. When required the operation of the CCC system can be changed into a one-point black current system. The switching between the 2 possibilities is realised by means of the OPC bit in subaddress 2BH.

When used as one-point control loop the system will control the black level of the RGB output signals to the 'low' reference current and not on the cut off point of the cathode. In this way spreads in the picture tube characteristics will not taken into account. A further consequence is that the RGB output signals have a fixed amplitude (2 V_{P-P} under nominal conditions) and that the 'cathode drive level' bits (CL3-CL0) have no effect on these amplitudes. For this reason the gain of the RGB output stages has to be adapted to the required drive level of the cathodes.

A black level off-set can be made with respect to the level which is generated by the black current stabilization system. In this way different colour temperatures can be obtained for the bright and the dark part of the picture. In the V_{g2} adjustment mode (AVG = 1) a certain black level is inserted at the RGB outputs and the black current stabilization system checks the feedback current of the 3 channels and indicates whether the current level is in a certain window (WBC-bit) or below or above this window (HBC-bit). This indication can be read from the status byte 01 and can be used for automatic adjustment of the V_{g2} voltage during the production of the TV receiver. During this test the vertical scan remains active so that the indication of the 2 bits can be made visible on the TV screen.

The control circuit contains a beam current limiting circuit and a peak white limiting circuit. The peak white level is adjustable via the I²C-bus. To prevent that the peak white limiting circuit reacts on the high frequency content of the video signal a low-pass filter is inserted in front of the peak detector. The circuit also contains a soft-clipper which prevents that the high frequency peaks in the output signal become too high. The difference between the peak white limiting level and the soft clipping level is adjustable via the I²C-bus in a few steps.

During switch-off of the TV receiver a fixed beam current is generated by the black current control circuit. This current ensures that the picture tube capacitance is discharged. During the switch-off period the vertical deflection can be placed in an overscan position so that the discharge is not visible on the screen.

A wide blanking pulse can be activated in the RGB outputs by means of the HBL bit in subaddress 2BH. The timing of this blanking can be adjusted by means of the bits WBF/R bits in subaddress 03H.

I²C BUS USER INTERFACE DESCRIPTION

The TV processor is fully controlled via the I²C bus. Control is exercised by writing data to one or more internal registers. Status information can be read from a set of info registers to enable the controlling microcontroller determine whether any action is required. The device has an I²C-bus slave transceiver, in accordance with the fast-mode specification, with a maximum speed of 400 kbits/s. Information concerning the I²C-bus can be found in brochure “I²C-bus and how to use it” (order number 9398 393 40011).

Slave address

SLAVE ADDRESS A6 TO A0
1 0 0 0 1 0 1

The device will not respond to a ‘general call’ on the I²C-bus, i.e. when a slave address of 0000000 is sent by a master.

Read/Write registers

ADDRESS	WORDS	WORD LENGTH	DESCRIPTION
$02 to $30	47 words	1 byte	I²C addresses enabled and usable for customers
$31 to $FB	-	-	Not used
$FC to $FF	4 words	1 byte	I²C addresses enabled not usable for customers

Each address of the address space (see below) can only be written. Correct operation is not guaranteed if registers in the range $FC to $FF will be addressed! The output registers of the TV processor are only available via auto-increment mode, no address can be used and all registers must be read.

DESCRIPTION OF THE I²C-BUS SUBADDRESSES

Table 26 Inputs TV-processor

FUNCTION	SUBADDR (HEX)	DATA BYTE								POR
		D7	D6	D5	D4	D3	D2	D1	D0	Value
Tint control	02	0	0	A5	A4	A3	A2	A1	A0	00
Timing of 'wide blanking'	03	WBF3	WBF2	WBF1	WBF0	WBR3	WBR2	WBR1	WBR0	88
Peak white limiting	04	0	0	SOC1	SOC0	A3	A2	A1	A0	08
Off-set IF demodulator	05	0	0	A5	A4	A3	A2	A1	A0	20
Horizontal parallelogram	06	0	0	A5	A4	A3	A2	A1	A0	20
Horizontal bow	07	0	0	A5	A4	A3	A2	A1	A0	20
Hue	08	0	0	A5	A4	A3	A2	A1	A0	00
Horizontal shift (HS)	09	0	0	A5	A4	A3	A2	A1	A0	20
EW width (EW)	0A	0	0	A5	A4	A3	A2	A1	A0	20
EW parabola/width (PW)	0B	0	0	A5	A4	A3	A2	A1	A0	20
EW upper corner parabola	0C	0	0	A5	A4	A3	A2	A1	A0	20
EW lower corner parabola	0D	0	0	A5	A4	A3	A2	A1	A0	20
EW trapezium (TC)	0E	0	0	A5	A4	A3	A2	A1	A0	20
Vertical slope (VS)	0F	0	0	A5	A4	A3	A2	A1	A0	20
Vertical amplitude (VA)	10	0	0	A5	A4	A3	A2	A1	A0	20
S-correction (SC)	11	0	0	A5	A4	A3	A2	A1	A0	20
Vertical shift (VSH)	12	0	0	A5	A4	A3	A2	A1	A0	20
Vertical zoom (VX)	13	0	0	A5	A4	A3	A2	A1	A0	20
Black level offset R	14	0	0	A5	A4	A3	A2	A1	A0	20
Black level offset G	15	0	0	A5	A4	A3	A2	A1	A0	20
White point R	16	0	0	A5	A4	A3	A2	A1	A0	20
White point G	17	0	0	A5	A4	A3	A2	A1	A0	20
White point B	18	0	0	A5	A4	A3	A2	A1	A0	20
Peaking	19	PF1	PF0	A5	A4	A3	A2	A1	A0	20
Luminance delay time	1A	0	0	0	0	YD3	YD2	YD1	YD0	00
Brightness	1B	0	0	A5	A4	A3	A2	A1	A0	20
Saturation	1C	0	0	A5	A4	A3	A2	A1	A0	20
Contrast	1D	0	0	A5	A4	A3	A2	A1	A0	20
AGC take-over	1E	0	0	A5	A4	A3	A2	A1	A0	20
Volume control	1F	0	0	A5	A4	A3	A2	A1	A0	20

FUNCTION	SUBADDR (HEX)	DATA BYTE								POR
		D7	D6	D5	D4	D3	D2	D1	D0	Value
Colour decoder 0	20	CM3	CM2	CM1	CM0	MAT	MUS	ACL	CB	00
Colour decoder 1	21	0	0	0	0	0	PSNS	BPS	FCO	00
AV-switch 0	22	0	0	SVO	CMB1	CMB0	INA	INB	0	00
AV-switch 1	23	0	0	0	0	0	0	0	RGBL	00
Synchronisation 0	24	0	HP2	FOA	FOB	POC	STB	VIM	VID	00
Synchronisation 1	25	0	RED	FSL	OSO	FORF	FORS	DL	NCIN	00
Deflection	26	OSVE	AFN	DFL	XDT	SBL	AVG	EVG	HCO	00
Vision IF 0	27	0	IFB	IFC	VSW	0	AFW	IFS	STM	00
Vision IF 1	28	SIF	0	0	IFLH	0	AGC1	AGC0	FFI	00
Sound 0	29	AGN	SM1	FMWS	0	SM0	0	FMB	FMA	00
Control 0	2A	0	IE2	RBL	AKB	CL3	CL2	CL1	CL0	00
Control 1	2B	OPC	0	VSD	SOY	0	YUV1	YUV0	HBL	00
Sound 1	2C	0	0	ADX	0	0	AVL[1]	0	0	00
Features 0	2D	0	0	COR1	COR0	DSK	0	BLS	BKS	00
Features 1	2E	0	BPB	RPO1	RPO0	0	0	0	0	00
Features 2	2F	0	CMSS	MVK	FMWS1	0	TUV	AAS	BSD	00
Features 3	30	0	0	0	RE6DB	0	YGN	LCT1	LCT0	00

Note

1. The AVL function can be activated only when the subcarrier output is used for the connection of the AVL capacitor (via the bits CMB1 and CMB0 in subaddress 22H).

Table 27 Outputs TV-processor

FUNCTION	SUBADDR	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	IFI	LOCK	SL	CD3	CD2	CD1	CD0
	01	XPR	NDF	FSI	IVW	WBC	HBC	BCF	IN2
	02	SUP	AGC	X	X	AFA	AFB	FMW	FML
	03	X	X	X	X	X	X	X	X
	04	SN1	SN0	X	X	X	X	X	X

Explanation input control data TV-processor

Table 28 Base-band tint control

DAC SETTING	CONTROL
0	–30°
20	0°
3F	+30°

Table 29 Timing of 'wide blanking'

DAC SETTING	SETTING
0	3.5 / 7.8 μs
F	5.9 / 10.2 μs

Table 30 Soft clipping level

SOC1	SOC0	VOLTAGE DIFFERENCE BETWEEN SOFT CLIPPING AND PWL
0	0	0% above PWL level
0	1	5% above PWL level
1	0	10% above PWL level
1	1	soft clipping off

Table 31 Peak White Limiting; note 1

DAC SETTING	CONTROL
00	0.55 V_{BL-WH}
0F	0.85 V_{BL-WH}

Note

1. CVBS input signal at which the Peak White Limiting is activated. Nominal input signal: 1.0 V_{P-P}.

Table 32 Off-set IF demodulator

DAC SETTING	CONTROL
0	negative correction
20	no correction
3F	positive correction

Table 33 Horizontal parallelogram

DAC SETTING	CONTROL
0	screen top 0.5 μs delayed and screen bottom 0.5 μs advanced with respect to centre
20	no correction
3F	screen top 0.5 μs advanced and screen bottom 0.5 μs delayed with respect to centre

Table 34 Horizontal bow

DAC SETTING	CONTROL
0	screen top and bottom 0.5 μs delayed with respect to centre
20	no correction
3F	screen top and bottom 0.5 μs advanced with respect to centre

Table 35 Hue control

DAC SETTING	CONTROL
0	–40°
20	0°
3F	+40°

Table 36 Horizontal shift

DAC SETTING	CONTROL
0	–2 μs
20	0
3F	+2 μs

Table 37 EW width

DAC SETTING	CONTROL
0	output current 700 μA
3F	output current 0 μA

Table 38 EW parabola/width

DAC SETTING	CONTROL
0	output current 0 μA
3F	output current 440 μA at top and bottom of screen

Table 39 EW upper/lower corner parabola

DAC SETTING	CONTROL
0	output current +76 μA
11	output current 0 μA
3F	output current –207 μA

Table 40 EW trapezium

DAC SETTING	CONTROL
0	output current at top of screen 100 μA lower that at bottom
20	no correction
3F	output current at top of screen 100 μA higher than at bottom

Table 41 Vertical slope

DAC SETTING	CONTROL
0	correction –20%
20	no correction
3F	correction +20%

Table 42 Vertical amplitude

DAC SETTING	CONTROL
0	amplitude 80%
20	amplitude 100%
3F	amplitude 120%

Table 43 S-correction

DAC SETTING	CONTROL
0	correction –10%
0E	no correction
3F	correction 25%

Table 44 Vertical shift

DAC SETTING	CONTROL
0	shift –5%
20	no correction
3F	shift +5%

Table 45 Vertical zoom

DAC SETTING	CONTROL
0	amplitude 75%
19	amplitude 100%
3F	amplitude 138%

Table 46 Black level off-set R/G

DAC SETTING	CONTROL
0	off-set of –160 mV
20	no off-set
3F	off-set of +160 mV

Table 47 White point R/G/B

DAC SETTING	CONTROL
0	gain –3 dB
20	no correction
3F	gain +3 dB

Table 48 Peaking centre frequency

PF1	PF0	CENTRE FREQUENCY	DELAY
0	0	2.7 MHz	190 ns
0	1	3.1 MHz	160 ns
1	0	3.5 MHz	143 ns
1	1	4.0 MHz	125 ns

Table 49 Peaking control (overshoot in direction ‘black’)

DAC SETTING	CONTROL
0	depeaking (overshoot –22%)
10	no peaking
3F	overshoot 80%

Table 50 Y-delay adjustment; note 1

YD0 to YD3	Y-DELAY
YD3	YD3 × 160 ns +
YD2	YD2 × 80 ns +
YD1	YD1 × 80 ns +
YD0	YD0 × 40 ns

Note

1. For an equal delay of the luminance and chrominance signal the delay must be set at a value of 160 ns. This is only valid for a CVBS signal without group delay distortions.

Table 51 Brightness control

DAC SETTING	CONTROL
0	correction –0.7V
20	no correction
3F	correction +0.7V

Table 52 Saturation control

DAC SETTING	CONTROL
0	colour off (–52 dB)
17	saturation nominal
3F	saturation +300%

Table 53 Contrast control

DAC SETTING	CONTROL
0	RGB amplitude –14 dB
20	RGB amplitude nominal
3F	RGB amplitude +6 dB

Table 54 AGC take-over

DAC SETTING	CONTROL
0	tuner take-over at IF input signal of 0.4 mV
3F	tuner take-over at IF input signal of 80 mV

Table 55 Volume control

DAC SETTING	CONTROL
0	attenuation 80 dB
3F	no attenuation

Table 56 Colour decoder mode, note 1

CM3	CM2	CM1	CM0	DECODER MODE	FREQ
0	0	0	0	PAL/NTSC	A
0	0	0	1	spare	A
0	0	1	0	PAL	A
0	0	1	1	NTSC	A
0	1	0	0	spare	
0	1	0	1	PAL/NTSC	B
0	1	1	0	PAL	B
0	1	1	1	NTSC	B
1	0	0	0	PAL/NTSC	ABCD
1	0	0	1	PAL/NTSC	C
1	0	1	0	PAL	C
1	0	1	1	NTSC	C
1	1	0	0	PAL/NTSC (Tri-Norma)	BCD
1	1	0	1	PAL/NTSC	D
1	1	1	0	PAL	D
1	1	1	1	NTSC	D

Note

1. The decoder frequencies for the various standards are obtained from an internal clock generator which is synchronised by a 12 MHz reference signal which is obtained from the μ-Controller clock generator.

   These frequencies are:

   a) A: 4.433619 MHz

   b) B: 3.582056 MHz (PAL-N)

   c) C: 3.575611 MHz (PAL-M)

   d) D: 3.579545 MHz (NTSC-M)

2. In the auto modes (CM3-CM0 setting 1000 and 1100) PAL with frequency D is not possible.

Table 57 PAL/NTSC matrix

MAT	MATRIX POSITION
0	adapted to standard
1	PAL matrix

Table 58 NTSC matrix

MUS	MATRIX POSITION
0	Japanese matrix
1	USA matrix

Table 59 Automatic colour limiting

ACL	COLOUR LIMITING
0	not active
1	active

Table 60 Chroma bandpass centre frequency

CB	CENTRE FREQUENCY
0	F_{SC}
1	$1.1 \times F_{SC}$

Table 61 Identification sensitivity PAL/NTSC decoder

PSNS	CONDITION
0	normal operation
1	increased identification sensitivity

Table 62 Bypass of chroma base-band delay line

BPS	DELAY LINE MODE
0	active
1	bypassed

Table 63 Forced Colour-On

FCO	CONDITION
0	off
1	on

Table 64 Selected video out

SVO	CONDITION
0	IF video available at output
1	selected CVBS available at output

Table 65 Condition AVL/SNDIF/REFO

CMB1	CMB0	CONDITION
0	0	AVL/SNDIF active (depends on SIF bit)
0	1	output voltage 2.3 V + subcarrier;
1	0	output voltage low (<0.8 V)
1	1	output voltage high (>4.5V)

Table 66 Source select

INA	INB	SELECTED SIGNALS
0	0	CVBS1
0	1	CVBS2
1	0	Y/C

Table 67 Blanking of RGB outputs

RGBL	CONDITION
0	normal operation
1	RGB outputs blanked continuously

Table 68 Synchronization of OSD/TEXT display

HP2	μ-CONTROLLER COUPLED TO
0	φ1 loop
1	φ2 loop

Table 69 Phase 1 (φ_1) time constant

FOA	FOB	MODE
0	0	normal
0	1	slow
1	0	slow/fast
1	1	fast

Table 70 Synchronization mode

POC	MODE
0	active
1	not active

Table 71 Stand-by

STB	MODE
0	stand-by
1	normal

Table 72 Video ident mode source (see fig. 21)

VIM	VIDEO IDENT COUPLING
0	ident coupled to internal CVBS (pin 40)
1	ident coupled to selected CVBS

Table 73 Video ident mode

VID	VIDEO IDENT MODE
0	φ1 loop dependent on video ident system
1	φ1 loop not dependent on video ident system

Table 74 Disable reference oscillator check in the SUP output bit (see also Table 140)

RED	CONDITION
0	reference oscillator check enabled
1	reference oscillator check disabled

Table 75 Forced slicing level for vertical sync

FSL	SLICING LEVEL
0	slicing level dependent on noise detector
1	fixed slicing level of 60%

Table 76 Switch-off in vertical overscan

OSO	MODE
0	Switch-off undefined
1	Switch-off in vertical overscan

Table 77 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto (60 Hz when line not in sync)
0	1	60 Hz
1	0	keep last detected field frequency
1	1	auto (50 Hz when line not in sync)

Table 78 Interlace

DL	STATUS
0	interlace
1	de-interlace

Table 79 Vertical divider mode

NCIN	VERTICAL DIVIDER MODE
0	normal operation
1	switched to search window

Table 80 Black current measuring lines in overscan (for vertical zoom setting < 1)

OSVE	MODE
0	normal operation
1	measuring lines in overscan

Table 81 AFC switch

AFN	MODE
0	normal operation
1	AFC not active

Table 82 Disable flash protection

DFL	MODE
0	flash protection active
1	flash protection disabled

Table 83 X-ray detection

XDT	MODE
0	protection mode, when a too high EHT is detected the receiver is switched to stand-by and the XPR-bit is set to 1
1	detection mode, the receiver is not switched to stand-by and only the XPR-bit is set to 1

Table 84 Service blanking

SBL	SERVICE BLANKING MODE
0	off
1	on

Table 85 Adjustment V_{g2} voltage

AVG	MODE
0	normal operation
1	V_{g2} adjustment (WBC and HBC bits in output byte 01 can be read)

Table 86 Enable vertical guard (RGB blanking)

EVG	VERTICAL GUARD MODE
0	not active
1	active

Table 87 EHT tracking mode

HCO	TRACKING MODE
0	EHT tracking only on vertical
1	EHT tracking on vertical and EW

Table 88 PLL demodulator frequency adjust

IFB	IFC	IF FREQUENCY
0	0	58.75 MHz
0	1	45.75 MHz
1	0	38.90 MHz
1	1	38.00 MHz

Table 89 Video mute

VSW	STATE
0	normal operation
1	IF-video signal switched off

Table 90 AFC window

AFW	AFC WINDOW
0	normal
1	enlarged

Table 91 IF sensitivity

IFS	IF SENSITIVITY
0	normal
1	reduced

Table 92 Search tuning mode

STM	MODE
0	normal operation
1	reduced sensitivity of video indent circuit

Table 93 Selection external input for sound IF circuit

SIF	MODE
0	2nd Sound IF input not selected
1	2nd Sound IF input selected

Table 94 Calibration of IF PLL demodulator

IFLH	MODE
0	calibration system active
1	calibration system not active

Table 95 IF AGC speed

AGC1	AGC0	AGC SPEED
0	0	$0.7 \times$ norm
0	1	norm
1	0	$3 \times$ norm
1	1	$6 \times$ norm

Table 96 Fast filter IF-PLL

FFI	CONDITION
0	normal time constant
1	increased time constant

Table 97 Gain FM demodulator

AGN	MODE
0	normal operation
1	gain +6 dB, to be used for the demodulation of mono signals in the NTSC system

Table 98 Sound mute

SM1	SM0	CONDITION
0	1	sound enhancer; note 1
1	0	mute on
1	1	mute off

Note

1. The noise which is generated by the digital acquisition circuit is limited

Table 99 Window selection of Narrow-band sound PLL

FMWS	FUNCTION
0	small window (± 225 kHz)
1	large window (± 450 kHz)

Table 100 Window selection of Narrow-band sound PLL

FMWS1	CONDITION
0	window as selected with FMWS
1	extra large window (± 600 kHz)

Table 101 Nominal frequency FM demodulator

FMB	FMA	FREQUENCY
0	0	5.5 MHz
0	1	6.0 MHz
1	0	4.5 MHz
1	1	6.5 MHz

Table 102 Enable fast blanking ext.RGB/YUV

IE2	FAST BLANKING
0	not active
1	active

Table 103 RGB blanking

RBL	RGB BLANKING
0	not active
1	active

Table 104 Black current stabilization

AKB	MODE
0	active
1	not active

Table 105 Cathode drive level (15 steps; 3.5 V/step)

CL3	CL2	CL1	CL0	SETTING CATHODE DRIVE AMPLITUDE; NOTE 1
0	0	0	0	50 V_{BL-WH}
0	1	1	1	75 V_{BL-WH}
1	1	1	1	95 V_{BL-WH}

Note

1. The given values are valid for the following conditions:
   a) - Nominal CVBS input signal
   b) - Nominal settings for contrast, WPA and peaking
   c) - Black- and blue-stretch switched-off
   d) - Gain of output stage such that no clipping occurs
   e) - Beam current limiting not active
   f) - AKB = 0; OPC = 0
   g) - The tolerance on these values is about ± 3 V.

Table 106 1- or 2- point black current system

OPC	MODE
0	2-point black current system
1	1-point black current system

Table 107 Vertical scan disable

VSD	MODE
0	normal operation
1	vertical scan disabled

Table 108 Synchronisation on YUV input

SOY	MODE
0	sync coupled to CVBS (Y) input
1	sync coupled to Y input

Table 109 RGB/YUV switch

YUV1	YUV0	MODE
0	0	RGB input activated
0	1	spare
1	0	YUV input; input conditions: note 1
1	1	YP_RP_B input; input conditions: note 2

Note

1. YUV input with the specification:
   Y = +1.4 V_{P-P}; U = –1.33 V_{P-P}; V = –1.05 V_{P-P}.
   These signal amplitudes are based on a colour bar signal with 75% saturation.
2. YP_RP_B input with the specification:
   Y = +1.0 V_{P-P}; P_B = +0.7 V_{P-P}; P_R = +0.7 V_{P-P}.
   These signal amplitudes are based on a colour bar signal with 100% saturation.

Table 110 RGB blanking mode

HBL	MODE
0	normal blanking (horizontal flyback)
1	wide blanking

Table 111 Audio signal selection

ADX	SELECTED SIGNAL
0	internal audio signal
1	external audio signal

Table 112 Auto Volume Levelling

AVL	MODE
0	not active
1	active

Table 113 Video dependent coring (peaking)

COR1	COR0	SETTING
0	0	off
0	1	coring active between 0 and 20 IRE
1	0	coring active between 0 and 40 IRE
1	1	coring active between 0 and 100 IRE

Table 114 Dynamic skin control on/off

DSK	MODE
0	off
1	on

Table 115 Blue stretch

BLS	BLUE STRETCH MODE
0	off
1	on

Table 116 Black stretch

BKS	BLACK STRETCH MODE
0	off
1	on

Table 117 Bypass of sound bandpass filter

BPB	CONDITION
0	normal operation
1	sound bandpass filter bypassed

Table 118 Ratio pre- and overshoot

RPO1	RPO0	RATIO PRE-/OVERSHOOT
0	0	1 : 1
0	1	1 : 1.25
1	0	1 : 1.5
1	1	1 : 1.8

Table 119 Selection of sync input signal for the video ident circuit

CMSS	CONDITION
0	IF ident circuit uses own sync separator
1	input IF ident circuit from main sync separator

Table 120 MacroVision Keying

MVK	MODE
0	Macrovision keying not active
1	Macrovision keying active

Table 121 Tint control on UV signals

TUV	MODE
0	not active
1	active

Table 122 Black area to switch off the black stretch

AAS	BLACK STRETCH MODE
0	10% back ground needed
1	20% background needed

Table 123 Black stretch depth (A-A in Fig.34)

BSD	BLACK STRETCH MODE
0	20 IRE
1	30 IRE

Table 124 Contrast reduction of main picture during OSD/TXT insertion

RE6DB	MODE
0	10dB OSD contrast reduction
1	6 dB OSD contrast reduction

Table 125 External Y (Luminance) input gain during YP_RP_B

YGN	MODE
0	gain 0 dB reduced
1	gain 3 dB reduced

Table 126 OSD / TEXT gain reduction

LCT1	LCT0	SETTING
0	0	0 %
0	1	25 %
1	0	37 %
1	1	50 %

Explanation output control data TV-processor

Table 127 Power-on-reset

POR	MODE
0	normal
1	power-down

Table 128 Output video identification

IFI	VIDEO SIGNAL
0	no video signal identified
1	video signal identified

Table 129 IF-PLL lock indication

LOCK	INDICATION
0	not locked
1	locked

Table 130 Phase 1 (φ_1) lock indication

SL	INDICATION
0	not locked
1	locked

Table 131 Colour decoder mode, note 1

CD3	CD2	CD1	CD0	STANDARD
0	0	0	0	no colour standard identified
0	0	0	1	NTSC with freq. A
0	0	1	0	PAL with freq. A
0	0	1	1	NTSC with freq. B
0	1	0	0	PAL with freq. B
0	1	0	1	NTSC with freq. C
0	1	1	0	PAL with freq. C
0	1	1	1	NTSC with freq. D
1	0	0	0	PAL with freq. D

Note

1. The values for the various frequencies can be found in the note of table 56.

Table 132 X-ray protection

XPR	OVERVOLTAGE
0	no overvoltage detected
1	overvoltage detected

Table 133 Output vertical guard

NDF	VERTICAL OUTPUT STAGE
0	OK
1	failure

Table 134 Field frequency indication

FSI	FREQUENCY
0	50 Hz
1	60 Hz

Table 135 Condition vertical divider

IVW	STANDARD VIDEO SIGNAL
0	no standard video signal
1	standard video signal (525 or 625 lines)

Table 136 Indication output black level in/out window

WBC	CONDITION
0	black current stabilisation outside window
1	black current stabilisation inside window

Table 137 Indication output black level

HBC	CONDITION
0	black current stabilisation below window
1	black current stabilisation above window

Table 138 Condition black current loop

BCF	CONDITION
0	black current loop is stabilised
1	black current loop is not stabilised

Table 139 Indication RGB-2 input condition

IN2	RGB INSERTION
0	no
1	yes

Table 140 Supply voltage and reference oscillator indication

SUP	CONDITION
0	supply voltage (8 Volt) not present or reference oscillator not OK
1	supply voltage (8 Volt) present and reference oscillator OK, note 1

Note

1. When RED = 1 only the supply voltage condition is checked.

Table 141 Indication tuner AGC

AGC	CONDITION
0	no gain control of tuner
1	tuner gain control active

Table 142 AFC output

AFA	AFB	CONDITION
0	0	outside window; RF too low
0	1	outside window; RF too high
1	0	in window; below reference
1	1	in window; above reference

Table 143 Indication FM-PLL in/out window

FMW	CONDITION
0	FM-PLL in window
1	FM-PLL out of window

Table 144 Indication FM-PLL in/out lock

FML	CONDITION
0	FM-PLL out of lock
1	FM-PLL locked

Table 145 Signal-to-Noise ratio

SN1	SN0	CONDITION
0	0	S/N ≤ 24 dB
0	1	S/N ≥ 24 dB and ≤ 27 dB
1	0	S/N ≥ 27 dB and ≤ 31 dB
1	1	S/N ≥ 31 dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	9	V
V_{DD}	supply voltage (all digital supplies)		–0.5	5.0	V
V_I	digital inputs	note 1	–0.5	V_{DD}+ 0.5	V
V_O	digital outputs	note 1	–0.5	V_{DD}+ 0.5	V
I_O	output current (each output)		–	±10	mA
I_{IOK}	DC input or output diode current		–	±20	mA
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_{sol}	soldering temperature	for 5 s	–	260	°C
T_j	operating junction temperature		–	150	°C
V_{es}	electrostatic handling	HBM; all pins; notes 2 and 3	–2000	+2000	V
		MM; all pins; notes 2 and 4	–300	+300	V

Notes

1. This maximum value has an absolute maximum of 5.5 V independent of V_{DD}.
2. All pins are protected against ESD by means of internal clamping diodes.
3. Human Body Model (HBM): R = 1.5 kΩ; C = 100 pF.
4. Machine Model (MM): R = 0 Ω; C = 200 pF.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	35	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*.

Latch-up

At an ambient temperature of 70 °C all pins meet the following specification:

For pins associated to V_P:

- $I_{trigger} \geq 100$ mA or ≥11V
- $I_{trigger} \leq -100$ mA or $\leq -0.5V_{P(max)}$.

For pins associated to V_{DD}:

- $I_{trigger} \geq 100$ mA or $\geq 1.5V_{DD(max)}$
- $I_{trigger} \leq -100$ mA or $\leq -0.5V_{DD(max)}$.

CHARACTERISTICS OF MICRO-COMPUTER AND TEXT DECODER

V_{DD} = 3.3 V ± 10%; V_{SS} = 0 V; T_{amb} = –20 to +70 °C; unless otherwise specified

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
VM.1.1	supply voltage ($V_{DDA/P/C}$)		3.0	3.3	3.6	V
VM.1.2	periphery supply current (I_{DDP})	note 1	1	–	–	mA
VM.1.3	core supply current (I_{DDC})		–	15	–	mA
VM.1.4	analog supply current (I_{DDA})		–	45	–	mA
Digital inputs						
RESET						
I.1.1	low level input voltage		–	–	0.8	V
I.1.2	high level input voltage		2.0	–	5.5	V
I.1.3	hysteresis of Schmitt Trigger input		0.4	–	0.7	V
I.1.4	input leakage current	V_I = 0	–	–	1	µA
I.1.5	equivalent pull down resistance	V = V_{DD}	–	33	–	kΩ
I.1.6	capacitance of input pin		–	–	10	pF
Digital input/outputs						
P1.0 TO P1.3, P2.0 AND P3.0 TO P3.3						
IO.1.1	low level input voltage		–	–	0.8	V
IO.1.2	high level input voltage		2.0	–	5.5	V
IO.1.3	hysteresis of Schmitt Trigger input		0.4	–	0.7	V
IO.1.4	low level output voltage	I_{OL} = 4 mA	–	–	0.4	V
IO.1.5	high level output voltage	open drain	–	–	5.5	V
IO.1.6	high level output voltage	I_{OH} = 4 mA	2.4	–	–	V
IO.1.7	output rise time (push-pull only) 10% to 90%	load 100 pF	–	16	–	ns
IO.1.8	output fall time 10% to 90%	load 100pF	–	14	–	ns
IO.1.9	load capacitance		–	–	100	pF
IO.1.10	capacitance of input pin		–	–	10	pF

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P0.5 AND P0.6						
IO.2.1	low level input voltage		–	–	0.8	V
IO.2.2	high level input voltage		2.0	–	5.5	V
IO.2.3	hysteresis of Schmitt Trigger input		0.4	–	0.7	V
IO.2.4	low level output voltage	I_{OL} = 8mA	–	–	0.4	V
IO.2.5	high level output voltage	open drain	–	–	5.5	V
IO.2.6	high level output voltage	I_{OH} = 8mA	2.4	–	–	V
IO.2.7	output rise time (push-pull only) 10% to 90%	load 100 pF	–	16	–	ns
IO.2.8	output fall time 10% to 90%	load 100pF	–	14	–	ns
IO.2.9	load capacitance		–	–	100	pF
IO.2.10	capacitance of input pin		–	–	10	pF
P1.6 AND P1.7						
IO.3.1	low level input voltage (V_{IL})		–	–	1.5	V
IO.3.2	high level input voltage (V_{IH})		3.0	–	5.5	V
IO.3.3	hysteresis of Schmitt-trigger input		0.2	–	–	V
IO.3.4	low level output voltage	sink current 8mA	0	–	0.4	V
IO.3.5	high level output voltage	open drain	–	–	5.5	V
IO.3.6	output fall time (V_{IH} to V_{IL} for C_L)		20+0.1× C_L	–	250	ns
IO.3.7	bus load capacitance		10	–	400	pF
IO.3.8	capacitance of IO pin		–	–	10	pF
Crystal oscillator						
OSCIN; NOTE 2						
X.1.1	resonator frequency		–	12	–	MHz
X.1.2	input capacitance (C_i)		–	4.0	–	pF
X.1.3	output capacitance (C_o)		–	5.0	–	pF
X.1.4	C_{x1} = C_{x2}		12	–	56	pF
X.1.5	R_i (crystal)		–	–	100	Ω

Note

1. Peripheral current is dependent on external components and voltage levels on I/Os
2. The simplified circuit diagram of the oscillator is given in Fig.22.

   A suitable crystal for this oscillator is the Saronix type 9922 520 00169. The nominal tuning of the crystal is important to obtain a symmetrical catching range for the PLL in the colour decoder. This tuning can be adapted by means of the values of the capacitors C_{x1} and C_{x2} in Fig.22. Good results were obtained with capacitor values of 39 pF, however, for a new application the optimum value should be determined by checking the symmetry of the catching range of the colour decoder.

CHARACTERISTICS OF TV-PROCESSORS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
MAIN SUPPLY; NOTE 1						
V.1.1	supply voltage		7.2	8.0	8.4	V
V.1.2	total supply current		–	135	–	mA
V.1.4	total power dissipation		–	1085	–	mW
IF circuit						
VISION IF AMPLIFIER INPUTS						
	input sensitivity (RMS value)	note 2				
M.1.1		f_i = 38.90 MHz	–	75	150	μV
M.1.2		f_i = 45.75 MHz	–	75	150	μV
M.1.3		f_i = 58.75 MHz	–	75	150	μV
M.1.4	input resistance (differential)	note 3	–	2	–	kΩ
M.1.5	input capacitance (differential)	note 3	–	3	–	pF
M.1.6	gain control range		64	–	–	dB
M.1.7	maximum input signal (RMS value)		150	–	–	mV
PLL DEMODULATOR; NOTES 4 AND 5						
M.2.1	Free-running frequency of VCO	PLL not locked, deviation from nominal setting	–500	–	+500	kHz
M.2.2	Catching range PLL	without SAW filter	–	±1	–	MHz
M.2.3	delay time of identification	via LOCK bit	–	–	20	ms
VIDEO AMPLIFIER OUTPUT; NOTES 7 AND 8						
M.3.1	zero signal output level	note 9	–	4.7	–	V
M.3.3	top sync level		1.9	2.1	2.3	V
M.3.6	video output impedance		–	50	–	Ω
M.3.7	internal bias current of NPN emitter follower output transistor		1.0	–	–	mA
M.3.8	maximum source current		–	–	5	mA
M.3.9	bandwidth of demodulated output signal	at –3 dB	6	7	–	MHz
M.3.10	differential gain	note 10	–	2	5	%
M.3.11	differential phase	notes 10 and 6	–	–	5	deg

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO AMPLIFIER (CONTINUED)						
M.3.12	video non-linearity	note 11	–	–	5	%
M.3.13	white spot clamp level		–	5.3	–	V
M.3.14	noise inverter clamping level	note 12	–	1.5	–	V
M.3.15	noise inverter insertion level (identical to black level)	note 12	–	2.8	–	V
	intermodulation	notes 6 and 13				
M.3.16	blue	V_o = 0.92 or 1.1 MHz	60	66	–	dB
M.3.17		V_o = 2.66 or 3.3 MHz	60	66	–	dB
M.3.18	yellow	V_o = 0.92 or 1.1 MHz	56	62	–	dB
M.3.19		V_o = 2.66 or 3.3 MHz	60	66	–	dB
	signal-to-noise ratio	notes 6 and 14				
M.3.20		weighted	56	60	–	dB
M.3.21		unweighted	49	53	–	dB
M.3.22	residual carrier signal	note 6	–	5.5	–	mV
M.3.23	residual 2nd harmonic of carrier signal	note 6	–	2.5	–	mV
IF AND TUNER AGC; NOTE 15						
Timing of IF-AGC						
M.4.1	modulated video interference	30% AM for 1 mV to 100 mV; 0 to 200 Hz (system B/G)	–	–	10	%
M.4.2	response time to IF input signal amplitude increase of 52 dB		–	2	–	ms
M.4.3	response to an IF input signal amplitude decrease of 52 dB		–	50	–	ms
Tuner take-over adjustment (via I^2C-bus)						
M.5.1	minimum starting level for tuner take-over (RMS value)		–	0.4	0.8	mV
M.5.2	maximum starting level for tuner take-over (RMS value)		80	150	–	mV
Tuner control output						
M.6.1	maximum tuner AGC output voltage	maximum tuner gain; note 3	–	–	8	V
M.6.2	output saturation voltage	minimum tuner gain; I_O = 2 mA	–	–	300	mV
M.6.3	maximum tuner AGC output swing		5	–	–	mA
M.6.4	leakage current RF AGC		–	–	1	μA
M.6.5	input signal variation for complete tuner control		0.5	2	4	dB

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC OUTPUT (VIA I^2C-BUS); NOTE 16						
M.7.1	AFC resolution		–	2	–	bits
M.7.2	window sensitivity		–	125	–	kHz
M.7.3	window sensitivity in large window mode		–	275	–	kHz
VIDEO IDENTIFICATION OUTPUT (VIA IFI BIT IN OUTPUT BYTE 00)						
M.8.1	delay time of identification after the AGC has stabilized on a new transmitter		–	–	10	ms

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator and audio amplifier						
FM-PLL DEMODULATOR; NOTE 17						
G.1.2	gain control range AGC amplifier		26	30	–	dB
G.1.3	catching range PLL	FMWS = 0	–	±225	–	kHz
G.1.31	catching range PLL	FMWS = 1	–	±450	–	kHz
G.1.4	maximum phase detector output current		–	±100	–	μA
G.1.5	VCO steepness $\Delta f_{FM}/\Delta V_C$ (K_0)		–	3.3	–	MHz/V
G.1.6	phase detector steepness $\Delta I_C/\Delta\varphi_{VFM}$ (K_D)		–	9	–	μA/rad
G.1.7	AM rejection	note 19	40	46	–	dB
EXTERNAL SOUND IF INPUT (SNDIF, WHEN SELECTED)						
G.1.8	input limiting for lock-in of PLL (RMS value)	Resistor parallel at input needed 470 < R < 4700 kΩ	–	1	2	mV
G.1.9	input resistance	note 3	–	50	–	kΩ
G.1.10	input capacitance	note 3	–	–	1.0	pF
DE-EMPHASIS OUTPUT; NOTE 21						
G.2.1	output signal amplitude (RMS value)	notes 18 and 20	–	500	–	mV
G.2.2	output resistance		–	15	–	kΩ
G.2.3	DC output voltage		–	3.2	–	V
G.2.31	signal-to-noise ratio (RMS value)	note 22	–	50	–	dB
AUDIO INPUT VIA DEEMPHASIS OUTPUT; NOTE 21						
G.2.4	input signal amplitude (RMS value)		–	500	–	mV
G.2.5	input resistance		–	15	–	kΩ
G.2.6	voltage gain between input and output	maximum volume	–	9	–	dB

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio Amplifier						
AUDIO OUTPUT						
A.1.1	controlled output signal amplitude (RMS value)	−6 dB; nominal audio input signal	500	700	900	mV
A.1.2	output resistance		–	500	–	Ω
A.1.3	DC output voltage		–	3.6	–	V
A.1.4	total harmonic distortion	note 23	–	–	0.5	%
A.1.6	power supply rejection	note 6	–	25	–	dB
A.1.7	internal signal-to-noise ratio	note 6 + 22 + 24	–	50	–	dB
A.1.8	external signal-to-noise ratio	note 6 + 24	–	60	–	dB
A.1.10	control range	see also Fig.23	–	80	–	dB
A.1.11	suppression of output signal when mute is active		–	80	–	dB
A.1.12	DC shift of the output when mute is active	note 25	–	10	50	mV
EXTERNAL AUDIO INPUT						
A.2.1	input signal amplitude (RMS value)		–	500	2000	mV
A.2.2	input resistance		–	25	–	kΩ
A.2.3	voltage gain between input and output	maximum volume	–	9	–	dB
A.2.4	crosstalk between internal and external audio signals		60	–	–	dB
AUTOMATIC VOLUME LEVELLING; NOTE 26						
A.3.1	gain at maximum boost		–	6	–	dB
A.3.2	gain at minimum boost		–	-14	–	dB
A.3.3	charge (attack) current		–	1	–	mA
A.3.4	discharge (decay) current		–	200	–	nA
A.3.5	control voltage at maximum boost		–	1	–	V
A.3.6	control voltage at minimum boost		–	5	–	V

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS, Y/C and RGB/YUV INPUTS						
CVBS-Y/C SWITCH						
S.1.1	CVBS or Y input voltage (peak-to-peak value)	note 27	–	1.0	1.4	V
S.1.2	CVBS or Y input current		–	4	–	μA
S.1.3	suppression of non-selected CVBS input signal	notes 6 and 28	50	–	–	dB
S.1.4	chrominance input voltage (burst amplitude)	note 3 and 29	–	0.3	1.0	V
S.1.5	chrominance input impedance		–	50	–	kΩ
CVBS OUTPUT						
S.1.9	output signal amplitude (peak-to-peak value)		–	2.0	–	V
S.1.10	top sync level		–	1.8	–	V
S.1.11	output impedance		–	–	50	Ω
EXTERNAL RGB / YUV (YP_BP_R) INPUT						
S.2.1	RGB input signal amplitude for an output signal of 2 V (black-to-white) (peak-to-peak value)	note 30	–	0.7	0.8	V
S.2.2	RGB input signal amplitude before clipping occurs (peak-to-peak value)	note 6	1.0	–	–	V
S.2.3	Y input signal amplitude (peak-to-peak value)	input signal amplitude for an output signal of 2 V (black-to-white); when activated via the YUV1/YUV0 bits; note 31	–	1.4/1.0	2.0	V
S.2.4	U/P_B input signal amplitude (peak-to-peak value)		–	–1.33/ +0.7	2.0	V
S.2.5	V/P_R input signal amplitude (peak-to-peak value)		–	–1.05/ +0.7	1.5	V
S.2.6	difference between black level of internal and external signals at the outputs		–	–	20	mV
S.2.7	input currents	no clamping; note 3	–	0.1	1	μA
S.2.8	delay difference for the three channels	note 6	–	0	20	ns
BASE-BAND TINT CONTROL						
S2.9	tint control range	63 steps; see Fig.27	–	±30	–	deg

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST INSERTION						
S.3.1	input voltage	no data insertion	–	–	0.4	V
S.3.2		data insertion	0.9	–	–	V
S.3.3	maximum input pulse	insertion	–	–	3.0	V
S.3.4	delay time from RGB in to RGB out	data insertion; note 6	–	–	20	ns
S.3.5	delay difference between insertion to RGB out and RGB in to RGB out	data insertion; note 6	–	–	20	ns
S.3.6	input current		–	–	0.2	mA
S.3.7	suppression of internal RGB signals	notes 6 and 28; insertion; f_i = 0 to 5 MHz	–	55	–	dB
S.3.8	suppression of external RGB signals	notes 6 and 28; no insertion; f_i = 0 to 5 MHz	–	55	–	dB
Chrominance and Luminance filters						
CHROMINANCE TRAP CIRCUIT; NOTE 32						
F.1.1	trap frequency		–	f_{osc}	–	MHz
F.1.2	Bandwidth at f_{SC} = 3.58 MHz	–3 dB	–	2.8	–	MHz
F.1.3	Bandwidth at f_{SC} = 4.43 MHz	–3 dB	–	3.4	–	MHz
F.1.4	colour subcarrier rejection		24	26	–	dB
CHROMINANCE BANDPASS CIRCUIT						
F.2.1	centre frequency (CB = 0)		–	f_{osc}	–	MHz
F.2.2	centre frequency (CB = 1)		–	$1.1 \times f_{osc}$	–	MHz
F.2.3	bandpass quality factor		–	3	–	
Y DELAY LINE						
F.4.1	delay time	note 6	–	480	–	ns
F.4.2	tuning range delay time	8 steps	–160	–	+160	ns
F.4.3	bandwidth of internal delay line	note 6	8	–	–	MHz
Picture Improvement Features						
PEAKING CONTROL; NOTE 33						
P.1.1	width of preshoot or overshoot	note 3	–	160	–	ns
P.1.2	peaking signal compression threshold		–	50	–	IRE
P.1.3	overshoot at maximum peaking	positive	–	45	–	%
P.1.4		negative	–	80	–	%
P.1.5	Ratio negative/positive overshoot; note 34		–	1.8	–	
P.1.6	peaking control curve	63 steps	see Fig.24			

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P.1.7	peaking centre frequency	setting PF1/PF0 = 0/0	–	2.7	–	MHz
P.1.8		setting PF1/PF0 = 0/1	–	3.1	–	MHz
P.1.9		setting PF1/PF0 = 1/0	–	3.5	–	MHz
P1.10		setting PF1/PF0 = 1/1	–	4.0	–	MHz
CORING STAGE; NOTE 35						
P.1.11	coring range		–	10	–	IRE
BLACK LEVEL STRETCHER; NOTE 36						
P.2.1	Maximum black level shift	BSD=0	16	20	24	IRE
P.2.11	Maximum black level shift	BSD=1	25	30	35	IRE
P.2.2	level shift at 100% peak white		–1	0	1	IRE
P.2.3	level shift at 50% peak white		–1	–	3	IRE
P.2.4	level shift at 15% peak white	BSD=0	6	8	10	IRE
P.2.4.1	level shift at 15% peak white	BSD=1	12	16	20	IRE
DYNAMIC SKIN TONE (FLESH) CONTROL; NOTE 37						
P.4.1	control angle		–	123	–	deg
P.4.2	correction range (angle)		–	45	–	deg
BLUE STRETCH; NOTE 38						
P.7.1	decrease of small signal gain for the channel	BLS = 1	–	40	–	%
P.7.2	decrease of small signal gain for the green channel	BLS = 1	–	20	–	%

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal and vertical synchronization and drive circuits						
SYNC VIDEO INPUT						
H.1.1	sync pulse amplitude	note 3	50	300	350	mV
H.1.2	slicing level for horizontal sync	note 39	–	50	–	%
H.1.3	slicing level for vertical sync	note 39	–	35	–	%
HORIZONTAL OSCILLATOR						
H.2.1	free running frequency		–	15625	–	Hz
H.2.2	spread on free running frequency		–	–	±2	%
H.2.3	frequency variation with respect to the supply voltage	V_P = 8.0 V ±10%; note 6	–	0.2	0.5	%
H.2.4	frequency variation with temperature	T_{amb} = 0 to 70 °C; note 6	–	–	80	Hz
FIRST CONTROL LOOP; NOTE 40						
H.3.1	holding range PLL		–	±0.9	±1.2	kHz
H.3.2	catching range PLL	note 6	±0.6	±0.9	–	kHz
H.3.3	signal-to-noise ratio of the video input signal at which the time constant is switched		–	24	–	dB
H.3.4	hysteresis at the switching point		–	3	–	dB
SECOND CONTROL LOOP						
H.4.1	control sensitivity		–	150	–	μs/μs
H.4.2	control range from start of horizontal output to flyback at nominal shift position		–	19	–	μs
H.4.3	horizontal shift range	63 steps	±2	–	–	μs
H.4.4	control sensitivity for dynamic compensation		–	7.6	–	μs/V
H.4.5	Voltage to switch-on the ‘flash’ protection	note 41	6.0	–	–	V
H.4.6	Input current during protection		–	–	1	mA
H.4.7	control range of the parallelogram correction	note 42	–	±0.5	–	μs
H.4.8	control range of the bow correction	note 42	–	±0.5	–	μs

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HORIZONTAL OUTPUT; NOTE 43						
H.5.1	LOW level output voltage	I_O = 10 mA	–	–	0.3	V
H.5.2	maximum allowed output current		10	–	–	mA
H.5.3	maximum allowed output voltage		–	–	V_P	V
H.5.4	duty factor	V_{OUT} = LOW (T_{ON})	–	55	–	%
H.5.5	switch-on time of horizontal drive pulse		–	1175	–	ms
H.5.6	switch-off time of horizontal drive pulse		–	43	–	ms
FLYBACK PULSE INPUT AND SANDCASTLE OUTPUT						
H.6.1	required input current during flyback pulse	note 3	100	–	300	µA
H.6.2	output voltage	during burst key	4.8	5.3	5.8	V
		during blanking	2.3	2.5	2.7	V
H.6.3	clamped input voltage during flyback		2.6	3.0	3.4	V
H.6.4	pulse width	burst key pulse	3.3	3.5	3.7	µs
H.6.5		vertical blanking, note 44	–	14/9.5	–	lines
H.6.6	delay of start of burst key to start of sync		4.8	5.0	5.2	µs
VERTICAL OSCILLATOR; NOTE 45						
H.7.1	free running frequency		–	50/60	–	Hz
H.7.2	locking range		45	–	64.5/72	Hz
H.7.3	divider value not locked		–	625/525	–	lines
H.7.4	locking range		434/488	–	722	lines/ frame
VERTICAL RAMP GENERATOR						
H.8.1	sawtooth amplitude (peak-to-peak value)	VS = 1FH; C = 100 nF; R = 39 kΩ	–	3.0	–	V
H.8.2	discharge current		–	1	–	mA
H.8.3	charge current set by external resistor	note 46	–	16	–	µA
H.8.4	vertical slope	63 steps; see Fig. 45	–20	–	+20	%
H.8.5	charge current increase	f = 60 Hz	–	19	–	%
H.8.6	LOW level of ramp		–	2.3	–	V
VERTICAL DRIVE OUTPUTS						
H.9.1	differential output current (peak-to-peak value)	VA = 1FH	–	0.95	–	mA
H.9.2	common mode current		–	400	–	µA
H.9.3	output voltage range		0	–	4.0	V

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EHT TRACKING/OVERVOLTAGE PROTECTION						
H.10.1	input voltage		1.2	–	2.8	V
H.10.2	scan modulation range		–5	–	+5	%
H.10.3	vertical sensitivity		–	6.3	–	%/V
H.10.4	EW sensitivity	when switched-on	–	–6.3	–	%/V
H.10.5	EW equivalent output current		+100	–	–100	μA
H.10.6	overvoltage detection level	note 41	–	3.9	–	V
DE-INTERLACE						
H.11.1	first field delay		–	0.5H	–	
EW WIDTH; NOTE 47						
H.12.1	control range	63 steps; see Fig. 48	100	–	65	%
H.12.2	equivalent output current		0	–	700	μA
H.12.3	EW output voltage range		1.0	–	5.0	V
H.12.4	EW output current range		0	–	1200	μA
EW PARABOLA/WIDTH						
H.13.1	control range	63 steps; see Fig. 49	0	–	23	%
H.13.2	equivalent output current	EW=3FH; CP=11H; TC=1FH	0	–	450	μA
EW UPPER/LOWER CORNER/PARABOLA						
H.14.1	control range	63 steps; see Fig. 50	–46	–	+17	%
H.14.2	equivalent output current	PW=3FH; EW=3FH; TC=1FH	–207	–	+76	μA
EW TRAPEZIUM						
H.15.1	control range	63 steps; see Fig. 51	–5	–	+5	%
H.15.2	equivalent output current	EW=1FH; CP=11H; PW=1FH	–100	–	+100	μA
VERTICAL AMPLITUDE						
H.16.1	control range	63 steps; see Fig. 44	80	–	120	%
H.16.2	equivalent differential vertical drive output current (peak-to-peak value)	SC = 0EH	760	–	1140	μA
VERTICAL SHIFT						
H.17.1	control range	63 steps; see Fig. 46	–5	–	+5	%
H.17.2	equivalent differential vertical drive output current (peak-to-peak value)		–50	–	+50	μA
S-CORRECTION						
H.18.1	control range	63 steps; see Fig. 47	–10	–	25	%
VERTICAL ZOOM MODE (OUTPUT CURRENT VARIATION WITH RESPECT TO NOMINAL SCAN); NOTE 48						
H.19.1	vertical expand factor		0.75	–	1.38	
H.19.2	output current limiting and RGB blanking		–	1.05	–	

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Colour demodulation part						
CHROMINANCE AMPLIFIER						
D.1.1	ACC control range	note 49	26	–	–	dB
D.1.2	change in amplitude of the output signals over the ACC range		–	–	2	dB
D.1.3	threshold colour killer ON		–30	–	–	dB
D.1.4	hysteresis colour killer OFF	strong signal conditions; S/N ≥ 40 dB; note 6	–	+3	–	dB
D.1.5		noisy input signals; note 6	–	+1	–	dB
ACL CIRCUIT; NOTE 50						
D.2.1	chrominance burst ratio at which the ACL starts to operate		–	3.0	–	
REFERENCE PART						
Phase-locked loop						
D.3.1	catching range		±500	–	–	Hz
D.3.2	phase shift for a ±400 Hz deviation of the oscillator frequency	note 6	–	–	2	deg
HUE CONTROL						
D.5.1	hue control range	63 steps; see Fig.25	±35	±40	–	deg
D.5.2	hue variation for ±10% V_P	note 6	–	0	–	deg
D.5.3	hue variation with temperature	T_{amb} = 0 to 70 °C; note 6	–	0	–	deg
DEMODULATORS						
General						
D.6.3	spread of signal amplitude ratio between standards	note 6	–1	–	+1	dB
D.6.5	bandwidth of demodulators	–3 dB; note 51	–	650	–	kHz
PAL/NTSC demodulator						
D.6.6	gain between both demodulators G(B–Y) and G(R–Y)		1.60	1.78	1.96	
D.6.12	change of output signal amplitude with temperature	note 6	–	0.1	–	%/K
D.6.13	change of output signal amplitude with supply voltage	note 6	–	–	±0.1	dB
D.6.14	phase error in the demodulated signals	note 6	–	–	±5	deg

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Base-band delay line						
D.8.1	variation of output signal for adjacent time samples at constant input signals		–0.1	–	0.1	dB
D.8.2	residual clock signal (peak-to-peak value)		–	–	5	mV
D.8.3	delay of delayed signal		63.94	64.0	64.06	μs
D.8.4	delay of non-delayed signal		40	60	80	ns
D.8.5	difference in output amplitude with delay on or off		–	–	5	%
COLOUR DIFFERENCE MATRICES (IN CONTROL CIRCUIT)						
PAL mode; (R–Y) and (B–Y) not affected						
D.9.1	ratio of demodulated signals (G–Y)/(R–Y)		–	–0.51 ±10%	–	
D.9.2	ratio of demodulated signals (G–Y)/(B–Y)		–	–0.19 ±25%	–	
NTSC mode; the matrix results in the following signals (nominal hue setting)						
MUS-bit = 0						
D.9.6	(B–Y) signal: 2.03/0°			$2.03U_R$		
D.9.7	(R–Y) signal: 1.59/95°			$-0.14U_R + 1.58V_R$		
D.9.8	(G–Y) signal: 0.61/240°			$-0.31U_R - 0.53V_R$		
MUS-bit = 1						
D.9.9	(B–Y) signal: 2.20/–1°			$2.20U_R - 0.04V_R$		
D.9.10	(R–Y) signal: 1.53/99°			$-0.24U_R + 1.51V_R$		
D.9.11	(G–Y) signal: 0.70/223°			$-0.51U_R - 0.48V_R$		
REFERENCE SIGNAL OUTPUT/SWITCH OUTPUT; NOTE 52						
D.10.1	reference frequency	CMB1/CMB0 = 01		3.58/4.43		MHz
D.10.2	output signal amplitude (peak-to-peak value)	CMB1/CMB0 = 01	0.2	0.25	0.3	V
D.10.3	output level (mid position)	CMB1/CMB0 = 01	2.3	2.5	2.7	V
D.10.4	output level LOW	CMB1/CMB0 = 10	–	–	0.8	V
D.10.5	output level HIGH	CMB1/CMB0 = 11	4.5	–	–	V

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Control part						
SATURATION CONTROL; NOTE 30						
C.1.1	saturation control range	63 steps; see Fig.26	52	–	–	dB
CONTRAST CONTROL; NOTE 30						
C.2.1	contrast control range	63 steps; see Fig.28	–	20	–	dB
C.2.2	tracking between the three channels over a control range of 10 dB		–	–	0.5	dB
C.2.61	contrast reduction	RE6DB = 0	–	10	–	dB
C.2.62		RE6DB = 1	–	6	–	dB
BRIGHTNESS CONTROL						
C.3.1	brightness control range	63 steps; see Fig.29	–	±0.7	–	V
RGB AMPLIFIERS						
C.4.1	output signal amplitude (peak-to-peak value)	at nominal luminance input signal, nominal settings for contrast, white-point adjustment and cathode drive level(CL3-CL0 = 0111)	–	2.0	–	V
C.4.2	maximum signal amplitude (black-to-white)	note 53	–	3.0	–	V
C.4.3	maximum peak white level		–	5.5	–	V
C.4.4	output signal amplitude for the ‘red’ channel (peak-to-peak value)	at nominal settings for contrast and saturation control and no luminance signal to the input (R–Y, PAL)	–	2.1	–	V
C.4.5	nominal black level voltage		–	2.5	–	V
C.4.6	black level voltage	when black level stabilisation is switched-off (via AKB bit)	–	2.5	–	V
C.4.61	black level voltage control range	AVG bit active; note 54	1.8	2.5	3.2	V
C.4.71	timing of video blanking with respect to mid sync (HBL = 1)	start of blanking; note 55	3.5	–	5.9	µs
C.4.72		end of blanking; note 55	7.8	–	10.2	µs
C.4.8	control range of the black-current stabilisation		–	±1	–	V
C.4.81	RGB output level when RGBL=1		–	0.8	–	V
C.4.9	blanking level	difference with black level, note 53	–	–0.5	–	V
C.4.10	level during leakage measurement		–	–0.1	–	V
C.4.11	level during ‘low’ measuring pulse		–	0.25	–	V
C.4.12	level during ‘high’ measuring pulse; note 56		–	0.5	–	V
C.4.13	adjustment range of the cathode drive level	note 53	–	±3	–	dB

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C.4.131	gain control range to compensate spreads in picture tube characteristics for the 2-point black -current stabilization system; note 56		–	±6	–	dB
C.4.14	variation of black level with temperature	note 6	–	1.0	–	mV/K
C.4.141	black level off-set adjustment on the Red and Green channel	63 steps	–	±160	–	mV
C.4.21	signal-to-noise ratio of the output signals	RGB input; note 57	60	–	–	dB
C.4.22		CVBS input; note 57	50	–	–	dB
C.4.23	residual voltage at the RGB outputs (peak-to-peak value)	at f_{osc}	–	–	15	mV
C.4.24		at $2f_{osc}$ plus higher harmonics	–	–	15	mV
C.4.25	bandwidth of output signals	RGB input; at –3 dB	–	15	–	MHz
C.4.26		CVBS input; at –3 dB; f_{osc} = 3.58 MHz	–	2.8	–	MHz
C.4.27		CVBS input; at –3 dB; f_{osc} = 4.43 MHz	–	3.4	–	MHz
C.4.28		S-VHS input; at –3 dB	5	–	–	MHz
WHITE-POINT ADJUSTMENT						
C.5.1	I^2C-bus setting for nominal gain	HEX code	–	20H	–	
C.5.2	adjustment range of the relative R, G and B drive levels		–	±3	–	dB
2-POINT BLACK-CURRENT STABILIZATION, NOTES 58						
C.6.1	amplitude of ‘low’ reference current		–	8	–	μA
C.6.2	amplitude of ‘high’ reference current; note 56		–	40	–	μA
C.6.3	acceptable leakage current		–	±75	–	μA
C.6.4	maximum current during scan		–	2	–	mA
C.6.5	input impedance		–	500	–	Ω
C.6.7	minimum input current to activate the guard circuit	note 59	–	0.1	–	mA
BEAM CURRENT LIMITING						
C.7.1	contrast reduction starting voltage		–	2.8	–	V
C.7.2	voltage difference for full contrast reduction		–	1.8	–	V
C.7.3	brightness reduction starting voltage		–	1.7	–	V
C.7.4	voltage difference for full brightness reduction		–	0.9	–	V
C.7.5	internal bias voltage		–	3.3	–	V

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C.7.8	maximum allowable current		–	1	–	mA
FIXED BEAM CURRENT SWITCH-OFF; NOTE 60						
C.8.1	discharge current during switch-off		0.85	1.0	1.15	mA
C.8.2	discharge time of picture tube		–	38	–	ms
PEAK WHITE LIMITER AND SOFT CLIPPING; NOTES 61 AND 62						
C.9.1	CVBS signal amplitude at which peak white limiter is activated (black-to-white value)	PWL range (15 steps); at max. contrast	0.55	–	0.85	V
C.9.2	soft clipper gain reduction	maximum contrast; note 62, see Fig.41	–	8	–	dB

Notes

1. When the 3.3 V supply is present and the μ-Controller is active a ‘low-power start-up’ mode can be activated. When all sub-address bytes have been sent and the POR and XPR flags have been cleared the horizontal output can be switched-on via the STB-bit (subaddress 24H). In this condition the horizontal drive signal has the nominal T_{OFF} and the T_{ON} grows gradually from zero to the nominal value. As soon as the 8 V supply is present the switch-on procedure (e.g. closing of the second loop) is continued.
2. On set AGC.
3. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
4. Loop bandwidth BL = 60 kHz (natural frequency fN = 15 kHz; damping factor d = 2; calculated with top sync level as FPLL input signal level).
5. The IF-PLL demodulator uses an internal VCO (no external LC-circuit required) which is calibrated by means of a digital control circuit which uses the clock frequency of the μ-Controller as a reference. The required IF frequency for the various standards is set via the IFB-IFC bits in subaddress 27H. When the system is locked the resulting IF frequency is very accurate with a deviation from the nominal value of less than 25 kHz.
6. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
7. Measured at 10 mV (RMS) top sync input signal.
8. Via this pin both the demodulated IF signal and the selected CVBS (or Y+C) signal can be supplied to the output. The selection between both signals is realised by means of the SVO bit in subaddress 22H.
9. So called projected zero point, i.e. with switched demodulator.
10. Measured in accordance with the test line given in Fig.30. For the differential phase test the peak white setting is reduced to 87%.

    The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.

    The phase difference is defined as the difference in degrees between the largest and smallest phase angle.
11. This figure is valid for the complete video signal amplitude (peak white-to-black), see Fig.31.
12. The noise inverter is only active in the ‘strong signal mode’ (no noise detected in the incoming signal)
13. The test set-up and input conditions are given in Fig.32. The figures are measured with an input signal of 10 mV RMS. This test can only be carried out in a test set-up in which the test options of the IC can be activated. This because the IF-AGC control input is not available in this IC.

14. Measured at an input signal of 10 mV_{RMS}. The S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value). B = 5 MHz. Weighted in accordance with CCIR 567.
15. The time-constant of the IF-AGC is internal and the speed of the AGC can be set via the bits AGC1 and AGC0 in subaddress 28H. The AGC response time is also dependent on the acquisition time of the PLL demodulator. The values given are valid for the 'norm' setting (AGC1-AGC0 = 0-1) and when the PLL is in lock.
16. The AFC control voltage is generated by the digital tuning system of the PLL demodulator. This system uses the clock frequency of the μ-Controller as a reference and is therefore very accurate. For this reason no maximum and minimum values are given for the window sensitivity figures (parameters M.7.2 and M.7.3). The tuning information is supplied to the tuning system via the AFA and AFB bits in output byte 02H. The AFC value is valid only when the LOCK-bit is 1.
17. Calculation of the FM-PLL filter can be done approximately by use of the following equations:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{K_0 K_D}{C_P}}$$

$$\upsilon = \frac{1}{2R\sqrt{K_0 K_D C_P}}$$

$BL_{-3dB} = f_0(1.55 - \upsilon^2)$

These equations are only valid under the conditions that $\upsilon \leq 1$ and $C_S > 5C_P$.

Definitions:

K_0 = VCO steepness in rad/V

K_D = phase detector steepness μA/rad

R = loop filter resistor

C_S = series capacitor

C_P = parallel capacitor

f_0 = natural frequency of PLL

BL_{-3dB} = loop bandwidth for −3dB

υ = damping factor

Some examples for these values are given in table 146

18. f = 5.5 MHz; modulation frequency: 1 kHz, $\Delta f = \pm 50$ kHz.
19. f = 4.5/5.5 MHz; FM: 70 Hz, ± 50 kHz deviation; AM: 1.0 kHz, 30% modulation.
20. The amplitude of the output signal can be increased with 6 dB by means of the AGN bit in subaddress 29H.
21. The deemphasis pin can also be used as additional audio input. In that case the internal (demodulated FM signal) must be switched off. This can be realised by means of the SM1/SM0 (sound mute) bits. The external signal must be switched off when the internal signal is selected.
22. The signal-to-noise ratio is measured under the following conditions:
    a) Input signal to the SNDIF pin (activated via SIF bit) with an amplitude of 100mV_{RMS}, f_{MOD} = 1 kHz and Δf = 27 kHz
    b) Output signal measured at the AUDEEM pin. The noise (RMS value) is measured according to the CCIR 468 definition.
23. Audio input signal 200 mV_{RMS}. Measured with a bandwidth of 15 kHz and the audio attenuator at −6 dB.
24. Unweighted RMS value, audio input signal 500 mV_{RMS}, audio attenuator at −6 dB.
25. Test conditions: Modulation frequency: 1 kHz, Δf = 27 kHz, AGN = 0 and audio attenuator at -9 dB

26. The capacitor for the Automatic Volume Levelling circuit must be connected to the AVL/SNDIF/REFO multi function pin. The selection of the function must be made by means of the CMB0 and CMB1 bit in subaddress 22H. More details about the sub-carrier output are given in the parameters D.10.

    The Automatic Volume Levelling (AVL) circuit stabilises automatically the audio output signal to a certain level which can be set by means of the volume control. This AVL function prevents big audio output fluctuations due to variation of the modulation depth of the transmitter. The AVL can be switched on and off via the AVL bit in subaddress 29H.

    The AVL is active over an input voltage range (measured at the deemphasis output) of 150 to 1500 mV_{RMS}. The AVL control curve is given in Fig.33. The control range of +6 dB to −14 dB is valid for input signals with 50% of the maximum frequency deviation.
27. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
28. This parameter is measured at nominal settings of the various controls.
29. Indicated is a signal for a colour bar with 75% saturation (chroma : burst ratio = 2.2 : 1).
30. The contrast and saturation control is active on the internal signal (YUV) and on the external RGB/YUV input. The Text/OSD input can be controlled on brightness only. Nominal contrast is specified with the DAC in position 20 HEX. Nominal saturation as maximum −10 dB.
31. The YUV/YP_BP_R input signal amplitudes are based on a colour bar signal with 75/100% saturation.
32. When the decoder is forced to a fixed subcarrier frequency (via the CM-bits) the chroma trap is always switched-on, also when no colour signal is identified. In the automatic mode the chroma trap is switched-off when no colour signal is identified.
33. Valid for a signal amplitude on the Y-input of 0.7 V black-to-white (100 IRE) with a rise time (10% to 90%) of 70 ns and the video switch in the Y/C mode. During production the peaking function is not tested by measuring the overshoots but by measuring the frequency response of the Y output.
34. The ratio between the positive and negative peaks can be varied by means of the bits RPO1 and RPO0 in subaddress 2EH (see Table 118). For ratios which are smaller than 1.8 the positive peak is not affected and the negative peak is reduced.
35. The coring can be activated in the low-light part of the picture. This effectively reduces the noise while having maximum peaking in the bright parts of the picture. The setting the video content at which the coring is active can be adapted by means of the COR1/COR0 bits in subaddress 2DH.
36. For video signals with a black level which deviates from the back-porch blanking level the signal is “stretched” to the blanking level. The amount of correction depends on the IRE value of the signal (see Fig.34). The black level is detected by means of an internal capacitor. The black level stretcher can be switched on and off via the BKS bit in subaddress 2DH. The values given in the specification are valid only when the luminance input signal has an amplitude of 1 V_{p-p}.
37. The Dynamic Skin Tone Correction circuit is designed such that it corrects (instantaneously and locally) the hue of those colours which are located in the area in the UV plane that matches to skin tones. The correction is dependent on the luminance, saturation and distance to the preferred axis. Because the amount of correction is dependent on the parameters of the incoming YUV signal it is not possible to give exact figures for the correction angle. The correction angle of 45 (±22.5) degrees is just given as an indication and is valid for an input signal with a luminance signal amplitude of 75% and a colour saturation of 50%. A graphical representation of the control behaviour is given in Figure 35 on page 95.
38. Via the ‘blue stretch’ (BLS bit) function the colour temperature of the bright scenes (amplitudes which exceed a value of 80% of the nominal amplitude) can be increased. This effect is obtained by decreasing the small signal gain of the red and green channel signals which exceed the 80% level. The effect is illustrated in Figure 37 on page 96.
39. The slicing level is independent of sync pulse amplitude. The given percentage is the distance between the slicing level and the black level (back porch). When the amplitude of the sync pulse exceeds the value of 350 mV the sync separator will slice the sync pulse at a level of 175 mV above top sync. The maximum sync pulse amplitude is 4 V_{p-p}.

The vertical slicing level is dependent on the S/N ratio of the incoming video signal. For a S/N ≤ 24 dB the slicing level is 35%, for a S/N ≥ 24 dB the slicing level is 60%. With the bit FSL (Forced Slicing Level) the vertical slicing level can be forced to 60%.

40. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition and the condition of the POC, FOA, FOB and VID bits in subaddress 24H. The circuit contains a noise detector and the time constant is switched to 'slow' when too much noise is present in the signal. In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible. Switching of the time constant can be automatically or can be set by means of the control bits.

    The circuit contains a video identification circuit which is independent of the first loop. This identification circuit can be used to close or open the first control loop when a video signal is present or not present on the input. This enables a stable On Screen Display (OSD) when just noise is present at the input.

    To prevent that the horizontal synchronisation is disturbed by anti copy signals like Macrovision the phase detector is gated during the vertical retrace period so that pulses during scan have no effect on the output voltage. The width of the gate pulse is about 22 μs. During weak signal conditions (noise detector active) the gating is active during the complete scan period and the width of the gate pulse is reduced to 5.7 μs so that the effect of noise is reduced to a minimum.

    The output current of the phase detector in the various conditions are shown in Table 147.

41. The ICs have 2 protection inputs. The protection on the second phase detector pin is intended to be used as 'flash' protection. When this protection is activated the horizontal drive is switched-off immediately and then switched-on again via the slow start procedure.

    The protection on the EHT input is intended for overvoltage (X-ray) protection. When this protection is activated the horizontal drive is directly switched-off (via the slow stop procedure).

    The EHT protection input can also be used to switch-off the TV receiver in a correct way when it is switched off via the mains power switch or when the power supply is interrupted by pulling the mains plug. This can be realised by means of a detection circuit which monitors the main supply voltage of the receiver. When this voltage suddenly decreases the EHT protection input must be pulled HIGH and then the horizontal drive is switched off via the slow stop procedure. Whether the EHT capacitor is discharged in the overscan or not during the switch-off period depends on the setting of the OSO bit (subaddress 25H, D4). See also note 60.

42. The control range indicates the maximum phase difference at the top and the bottom of the screen. Compared with the phase position at the centre of the screen the maximum phase difference at the top and the bottom of the screen is ±0.5 μs for both the parallelogram and the bow correction.

43. During switch-on the horizontal drive starts-up in a soft-start mode. The horizontal drive starts with a very short T_{ON} time of the horizontal output transistor, the 'off time' of the transistor is identical to the 'off time' in normal operation. The starting frequency during switch-on is therefore about 2 times higher than the normal value. The 'on time' is slowly increased to the nominal value in a time of about 1175 ms (see Fig.39). The rather slow rise of the T_{ON} between 75% and 100% of T_{ON} is introduced to obtain a sufficiently slow rise of the EHT for picture tubes with Dynamic Astigmatic Focus (DAF) guns. When the nominal frequency is reached the PLL is closed in such a way that only very small phase corrections are necessary. This ensures a safe operation of the output stage.

    During switch-off the soft-stop function is active. This is realised by decreasing the T_{ON} of the output transistor complimentary to the start-up behaviour. The switch-off time is about 43 ms (see Fig.39). When the 'switch off command' is received the soft-stop procedure is started after a delay of about 2 ms. During the switch-off time the EHT capacitor of the picture tube is discharged with a fixed beam current which is forced by the black current loop (see also note 60). The discharge time is about 38 ms.

    The horizontal output is gated with the flyback pulse so that the horizontal output transistor cannot be switched-on during the flyback time.

44. The vertical blanking pulse in the RGB outputs has a width of 27 or 22 lines (50 or 60 Hz system). The vertical pulse in the sandcastle pulse has a width of 14 or 9.5 lines (50 or 60 Hz system). This to prevent a phase distortion on top of the picture due to a timing modulation of the incoming flyback pulse.
45. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. During TV reception this divider circuit has 3 modes of operation:
    a) Search mode ‘large window’.

       This mode is switched on when the circuit is not synchronized or when a non-standard signal (number of lines per frame outside the range between 311 and 314(50 Hz mode) or between 261 and 264 (60 Hz mode) is received). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz).

    b) Standard mode ‘narrow window’.

       This mode is switched on when more than 15 succeeding vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

    c) Standard TV-norm (divider ratio 525 (60 Hz) or 625 (50 Hz).

       When the system is switched to the narrow window it is checked whether the incoming vertical sync pulses are in accordance with the TV-norm. When 15 standard TV-norm pulses are counted the divider system is switched to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing.

       When 3 vertical sync pulses are missed the system switches back to the narrow window and when also in this window no sync pulses are found (condition 3 missing pulses) the system switches over to the search window.

    The vertical divider needs some waiting time during channel-switching of the tuner. When a fast reaction of the divider is required during channel-switching the system can be forced to the search window by means of the NCIN bit in subaddress 25H.

    When RGB signals are inserted the maximum vertical frequency is increased to 72 Hz. This has the consequence that the circuit can also be synchronised by signals with a higher vertical frequency like VGA.
46. Conditions: frequency is 50 Hz; normal mode; VS = 1F.
47. The output range percentages mentioned for E-W control parameters are based on the assumption that 400 μA variation in E-W output current is equivalent to 20% variation in picture width.
48. The ICs have a zoom adjustment possibility for the horizontal and vertical deflection. For this reason an extra DAC has been added in the vertical amplitude control which controls the vertical scan amplitude between 0.75 and 1.38 of the nominal scan. At an amplitude of 1.06 of the nominal scan the output current is limited and the blanking of the RGB outputs is activated. This is illustrated in Fig. 36.

    When the vertical amplitude is compressed (zoom factor <1) it is still possible to display the black-current measuring lines in the vertical overscan. The feature is activated by means of the OSVE-bit in sub-address 26H. Because the vertical deflection output stage needs some time for the excursion from the top of the picture to the required position on the screen the vertical blanking is increased when the OSVE-bit is activated. The shape of the vertical deflection current for a zoom factor of 0.75 with OSVE activated is given in Fig. 38. The exact timing of the measuring pulses and vertical blanking for the various conditions is given in Fig. 40.

    The nominal scan height must be adjusted at a position of 19 HEX of the vertical ‘zoom’ DAC.
49. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) the dynamic range of the ACC is +6 and −20 dB.
50. The ACL function can be activated by via the ACL bit in the subaddress 20H. The ACL circuit reduces the gain of the chroma amplifier for input signals with a chroma-to-burst ratio which exceeds a value of 3.0.

51. This parameter indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the low-pass filter of the demodulator is approximately 1 MHz.
52. The subcarrier output is combined with a 3-level switch output which can be used to switch external circuits like sound traps etc. This output is controlled by the CMB1 and CMB0 bits in control byte 22H. The subcarrier signal is available when CMB1/0 are set to 0/1.
53. Because of the 2-point black current stabilization circuit both the black level and the amplitude of the RGB output signals depend on the drive characteristic of the picture tube. The system checks whether the returning measuring currents meet the requirement and adapts the output level and gain of the circuit when necessary. Therefore the typical value of the black level and amplitude at the output are just given as an indication for the design of the RGB output stage.

    The 2-point black level system adapts the drive voltage for each cathode in such a way that the 2 measuring currents have the right value. This has the consequence that a change in the gain of the output stage will be compensated by a gain change of the RGB control circuit. Because different picture tubes may require different drive voltage amplitudes the ratio between the output signal amplitude and the inserted measuring pulses can be adapted via the I^2C-bus. This is indicated in the parameter ‘Adjustment range of the cathode drive level’.

    Because of the dependence of the output signal amplitude on the application the soft clipping limiting has been related to the input signal amplitude.
54. The alignment system for the V_{g2} voltage of the picture tube can be activated by means of the AVG bit. In that condition a certain black level is inserted at the RGB outputs during a few lines. The value of this level can be adjusted by means of the brightness control DAC. An automatic adjustment of the V_{g2} of the picture tube can be realised by using the WBC and HBC bits in output byte 01. For a black level feedback current between 12 and 20 μA the WBC = 1, for a higher or lower current WBC = 0. Whether the current is too high or too low can be found from the HBC bit. The indication of these bits can be made visible on the screen via OSD so that this alignment procedure can also be used for service purposes.
55. When the reproduction of 4 : 3 pictures on a 16 : 9 picture tube is realised by means of a reduction of the horizontal scan amplitude the edges of the picture may slightly be disturbed. This effect can be prevented by adding an additional blanking to the RGB signals. The blanking pulse is derived form the horizontal oscillator and is directly related to the incoming video signal (independent of the flyback pulse). This blanking is activated with the HBL bit (see Fig. 42).
56. This parameter is valid only when the CCC loop is active.
57. Signal-to-noise ratio (S/N) is specified as peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz).
58. This is a current input. The timing of the measuring pulses and the vertical blanking for the 50/60 Hz standard are given in Fig.40

    The start-up procedure is as follows.

    When the TV receiver is switched-on the RGB outputs are blanked and the black-current loop will try to adjust the picture tube to the right bias levels. The RGB drive signals are switched-on as soon as the black current loop is stabilised. This results in the shortest switch-on time.

    When this switch-on system results in a visible disturbance of the picture it is possible to add a further switch-on delay via a software routine. In that case the RGB outputs must be blanked by means of the RBL bit. As soon as the black current loop is stabilised the BCF-bit is set to 0 (output byte 01). This information can then be used to switch-on the RGB outputs with some additional delay.
59. The vertical guard function has been combined with the black current measuring input. For a reliable operation of the protection system and to avoid that the black current stabilization system is disturbed the end of the protection pulse during normal operation should not overlap the measuring pulses (see also Fig.40). Therefore this pulse must end before line 14.

60. During switch-off the magnitude of the discharge current of the picture tube is controlled by the black current loop. Dependent on the setting of the OSO bit the vertical scan can be stopped in an overscan position during that time so that the discharge is not visible on the screen. The switch-off procedure is as follows:
    a) When the switch-off command is received the RGB outputs are blanked for a time of about 2 ms.
    b) If OSO = 1 the vertical scan is placed in an overscan position
    c) If OSO = 0 the vertical deflection will keep running during the switch-off time
    d) The soft-stop procedure is started with a reduction of the T_{ON} of the output stage from nominal to zero
    e) The fixed beam current is forced via the black current loop
    f) The soft-stop time has a value of 43 ms, the fixed beam current is flowing during a time of 38 ms.
61. The control circuit contains a Peak White Limiting (PWL) circuit and a soft clipper.
    a) The detection level of the PWL is adjustable via the I^2C-bus and has a control range between 0.55 and 0.85 V_{BL-WH} (this amplitude is related to the CVBS input signal (typical amplitude 1.0 V_{P-P}) at maximum contrast setting). The high frequency components of the video signal are suppressed so that they do not activate the limiting action. The contrast reduction of the PWL is obtained by discharging the capacitor of the beam current limiting input.
    b) In addition to the PWL circuit the IC contains a soft clipper function which limits the high frequency signals when they exceed the peak white limiting level. The difference between the peak white limiting level and the soft clipping level is adjustable via the I^2C-bus and can be varied between 0 and 10% in 3 steps (soft clipping level equal or higher than the PWL level). It is also possible to switch-off the soft clipping function.
62. The soft clipper gain reduction is measured by applying a sawtooth signal with rising slope and 0.7 V_{BL-WH} at the CVBS input. To prevent the beam current limiter from operating a DC voltage of 3.5V must be applied to BCLIN pin. The contrast is set at the maximum value, the PWL (peak white limiting) level at the minimum value, and the soft clipping level is set at 0% above the PWL level (SOC_{10}=00). The tangents of the sawtooth waveform at one of the RGB outputs is now determined at begin and end of the sawtooth. The soft clipper gain reduction is defined as the ratio of the slopes of the tangents for black and white, see Fig.41.

Table 146 Some examples for the FM-PLL filter

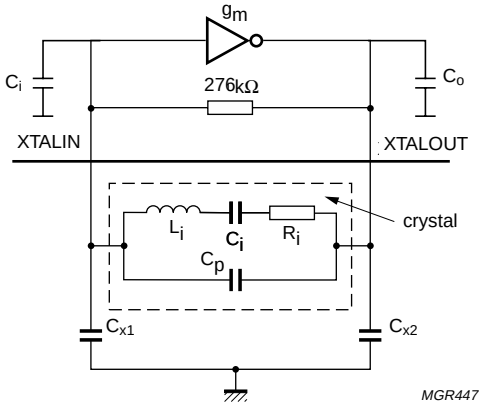
BL_{-3dB} (kHz)	C_S (nF)	C_P (pF)	R (kΩ)	ν
150	1.2	330	3.9	0.5

Table 147 Output current of the phase detector in the various conditions

I^2C-BUS COMMANDS				IC CONDITIONS			φ-1 CURRENT/MODE			
VID	POC	FOA	FOB	IFI	SL	NOISE	SCAN	V-RETR	GATING	MODE
–	0	0	0	yes	yes	no	200	300	yes (1)	normal
–	0	0	0	yes	yes	yes	30	30	yes(2)	normal
–	0	0	0	yes	no	–	200	300	no	normal
–	0	0	1	yes	yes	–	30	30	yes(2)	slow
–	0	0	1	yes	no	–	200	300	no	slow
–	0	1	0	yes	yes	no	200	300	yes(2)	slow/fast
–	0	1	0	yes	yes	yes	30	30	yes(2)	slow/fast
–	–	1	1	–	–	–	200	300	yes(1)	fast
0	0	–	–	no	–	–	6	6	no	OSD
–	1	–	–	–	–	–	–	–	–	off

Note

1. Gating is active during vertical retrace, the width is 22 μs. This gating prevents disturbance due to Macro Vision Anti Copy signals.
2. Gating is continuously active and is 5.7 μs wide



$$f_{osc} = \frac{1}{2\pi\sqrt{L_i \times \frac{C_i \times C_{tot}}{C_i + C_{tot}}}}$$

$$C_{tot} = C_p + \frac{C_a \times C_b}{C_a + C_b}$$

$$C_a = C_i + C_{x1}$$
$$C_b = C_o + C_{x2}$$

Fig.22 Simplified diagram crystal oscillator.

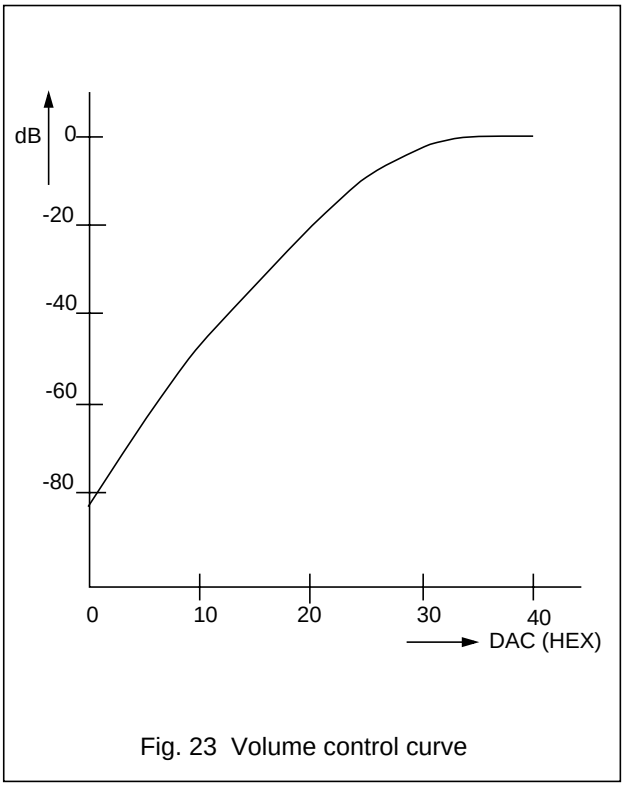
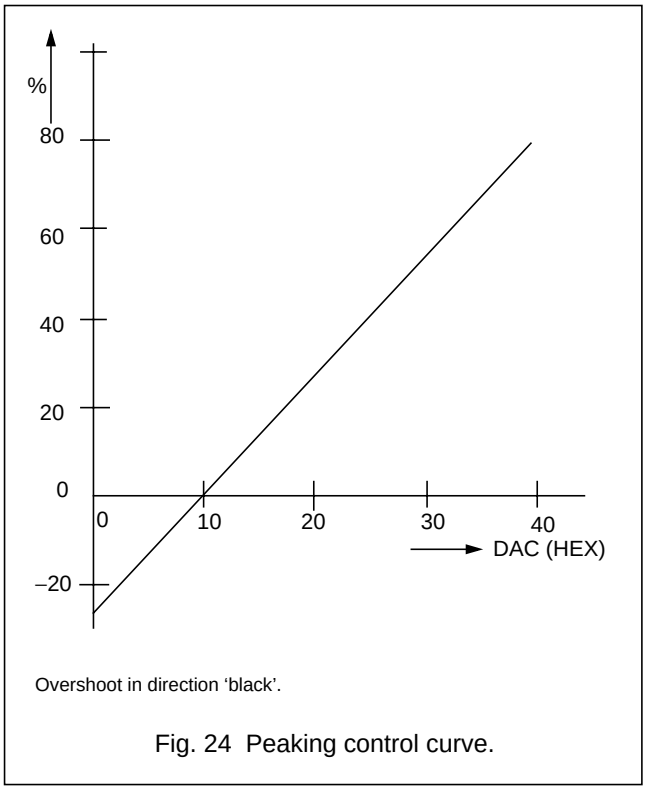


Fig. 23 Volume control curve



Overshoot in direction ‘black’.

Fig. 24 Peaking control curve.

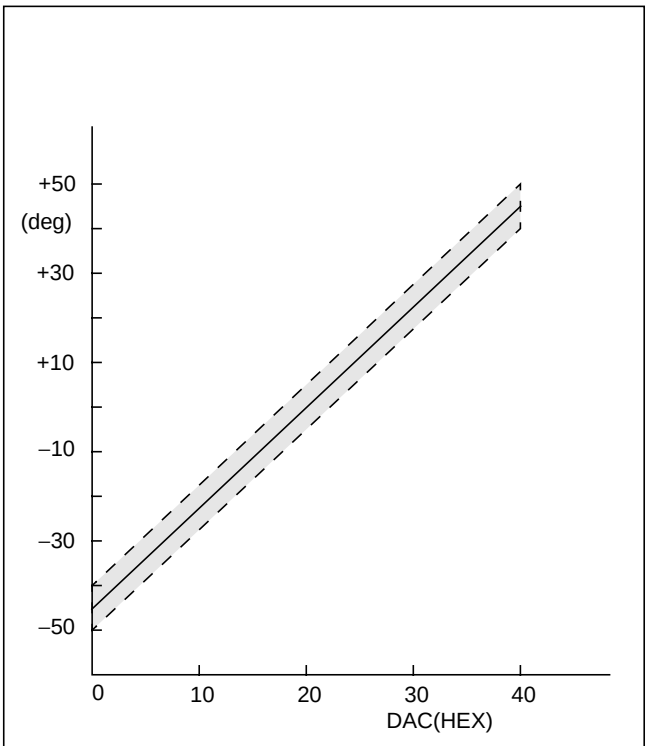


Fig.25 Hue control curve.

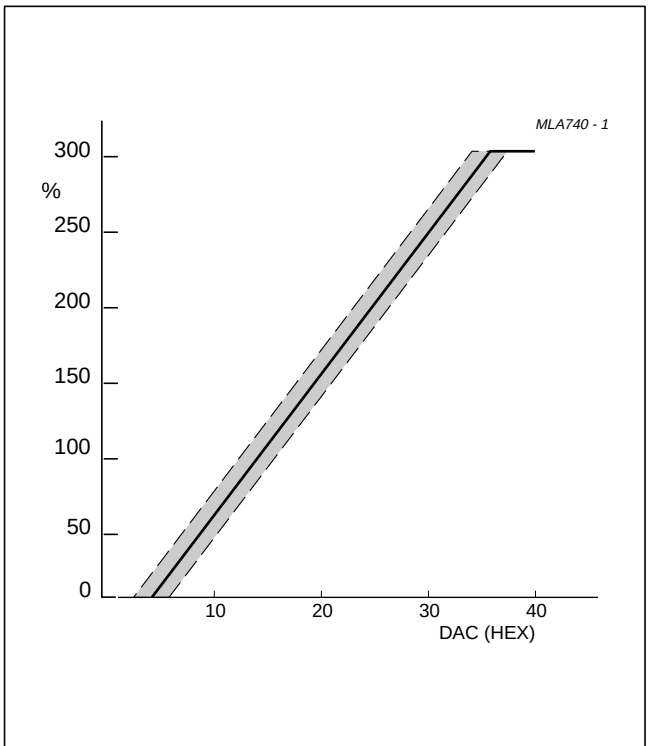


Fig. 26 Saturation control curve.

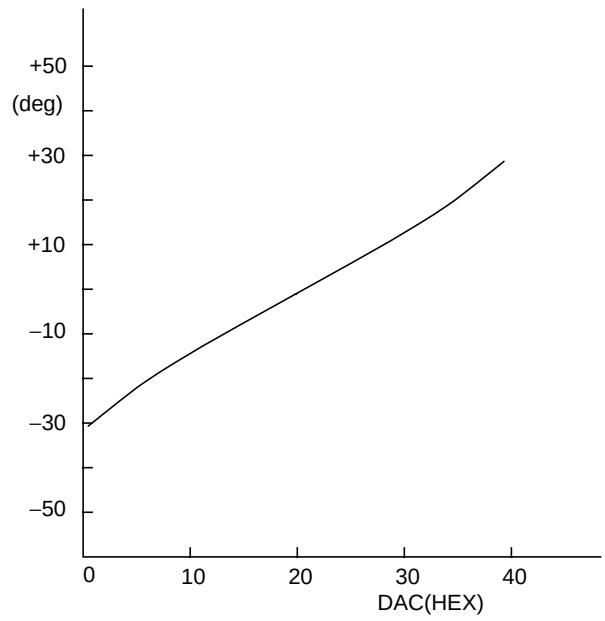


Fig.27 Base-band tint control curve.

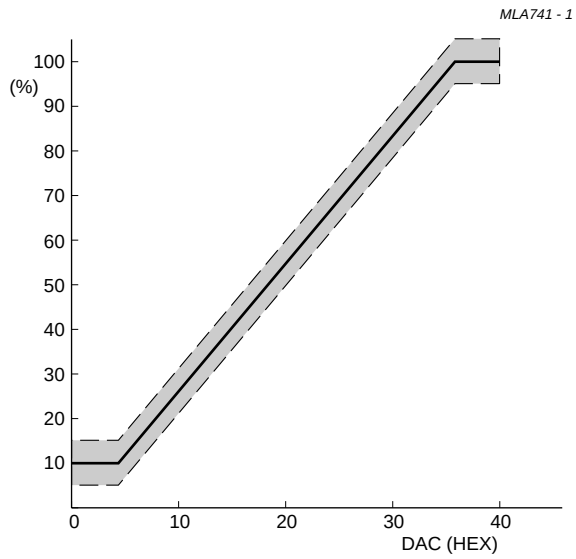


Fig. 28 Contrast control curve.

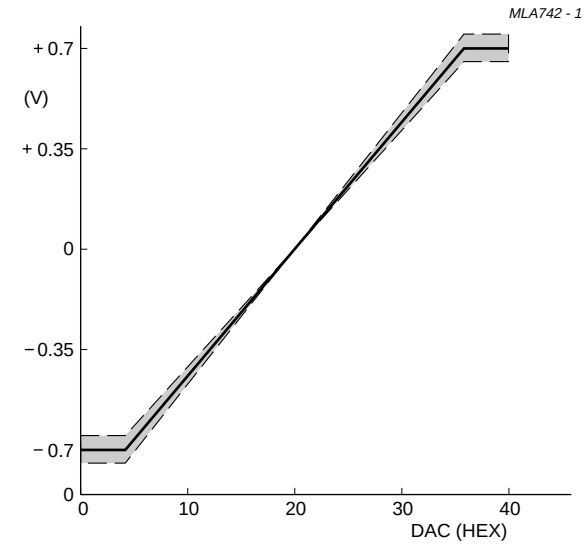


Fig. 29 Brightness control curve.

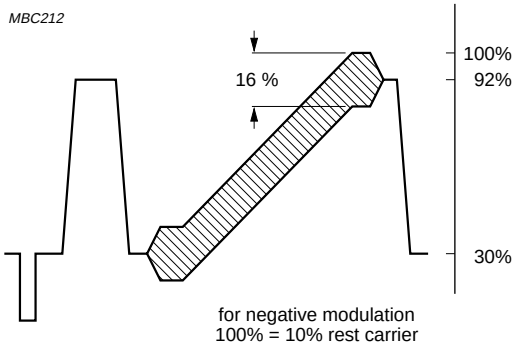


Fig. 30 Video output signal.

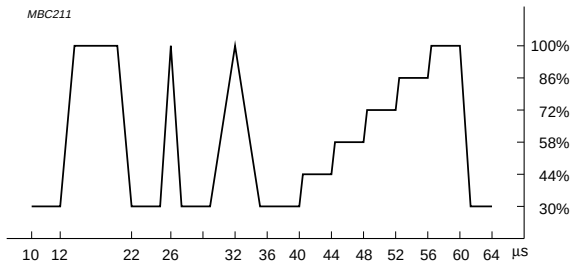
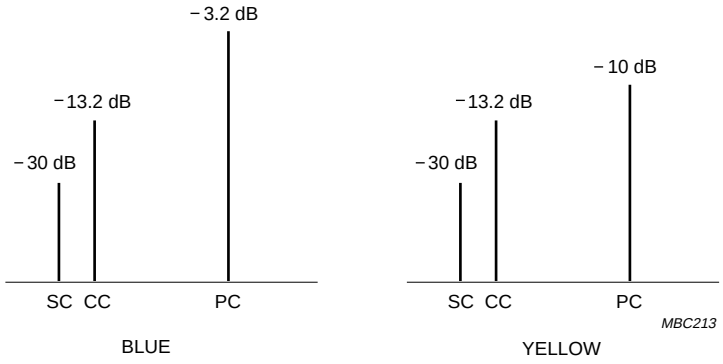
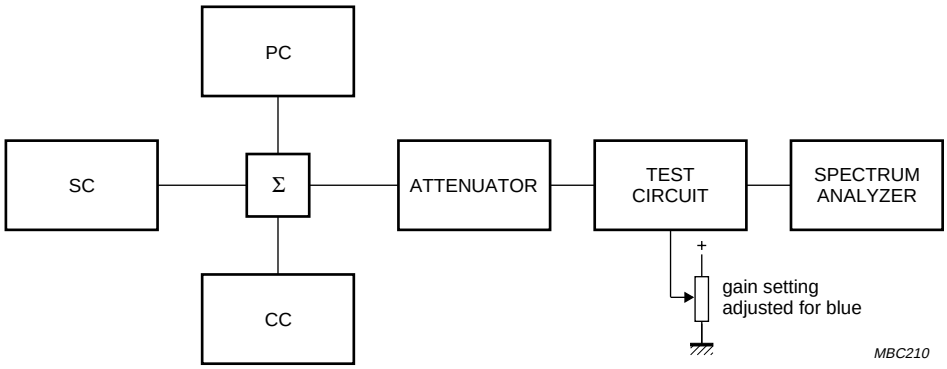


Fig. 31 Test signal waveform.





Input signal conditions: SC = sound carrier; CC = colour carrier; PC = picture carrier.
All amplitudes with respect to top sync level.

$$\text{Value at 0.92 or 1.1 MHz} = 20 \log \frac{V_O \text{ at 3.58 or 4.4 MHz}}{V_O \text{ at 0.92 or 1.1 MHz}} + 3.6 \text{ dB}$$

$$\text{Value at 2.66 or 3.3 MHz} = 20 \log \frac{V_O \text{ at 3.58 or 4.4 MHz}}{V_O \text{ at 2.66 or 3.3 MHz}}$$

Fig. 32 Test set-up intermodulation.

CHARACTERISTIC POINTS AVL	A	B	C	D	UNIT
Deemphasis voltage	150	300	500	1500	mV_{RMS}
FM swing	15	30	50	150	kHz

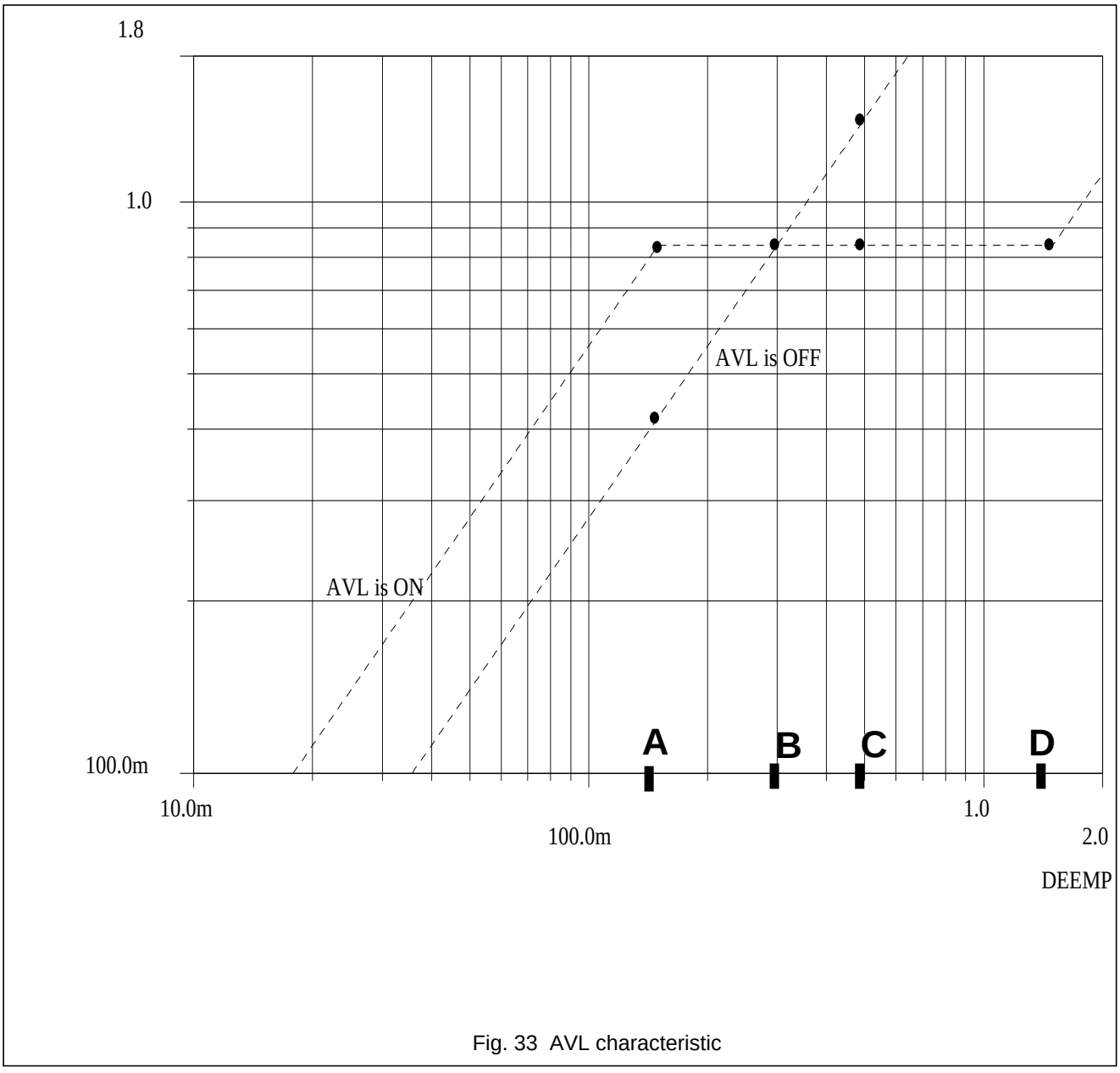
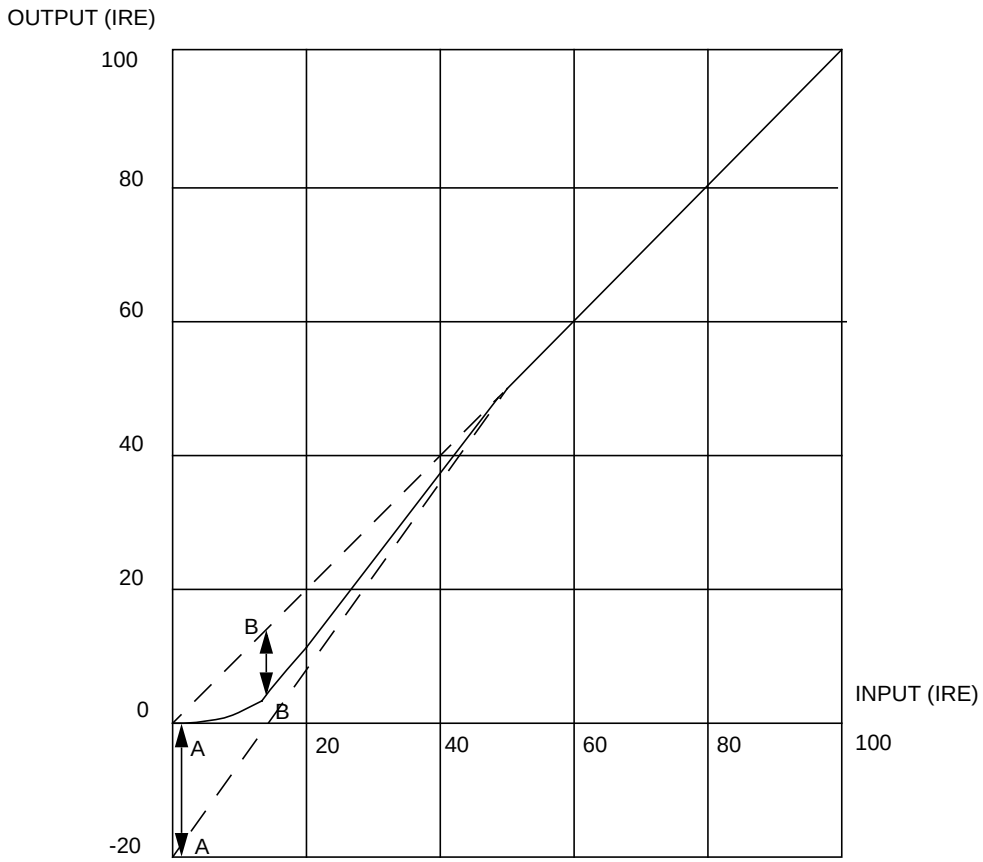


Fig. 33 AVL characteristic



A-A: MAXIMUM BLACK LEVEL SHIFT

B-B: LEVEL SHIFT AT 15% OF PEAK WHITE

Fig. 34 I/O relation of the black level stretch circuit

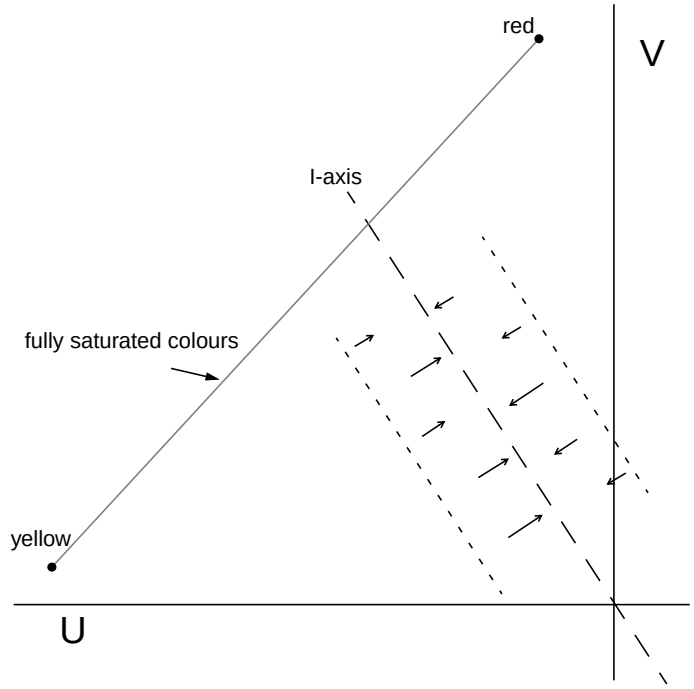


Fig.35 Skin tone correction range for the correction angle of 123 deg.

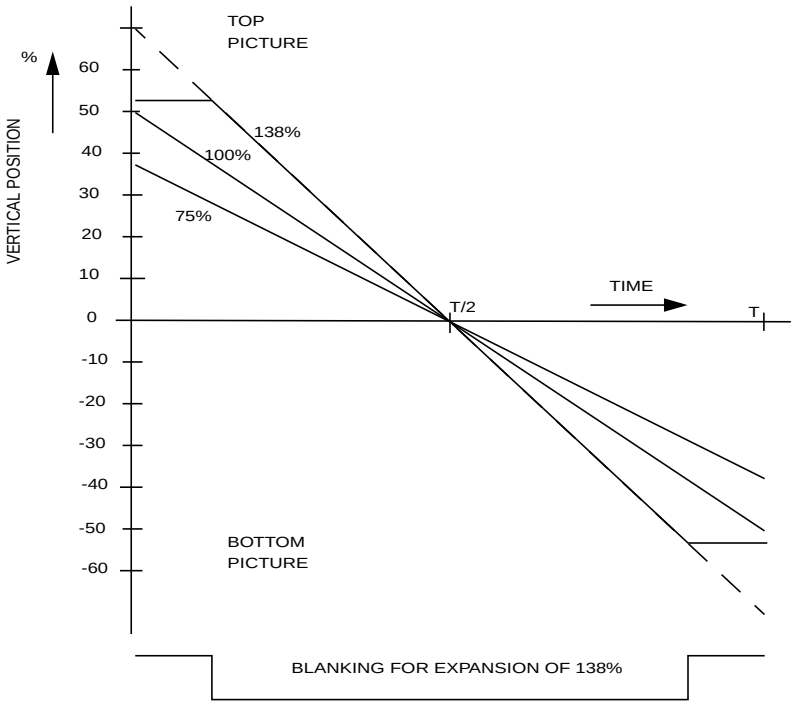


Fig. 36 Vertical position and blanking pulse

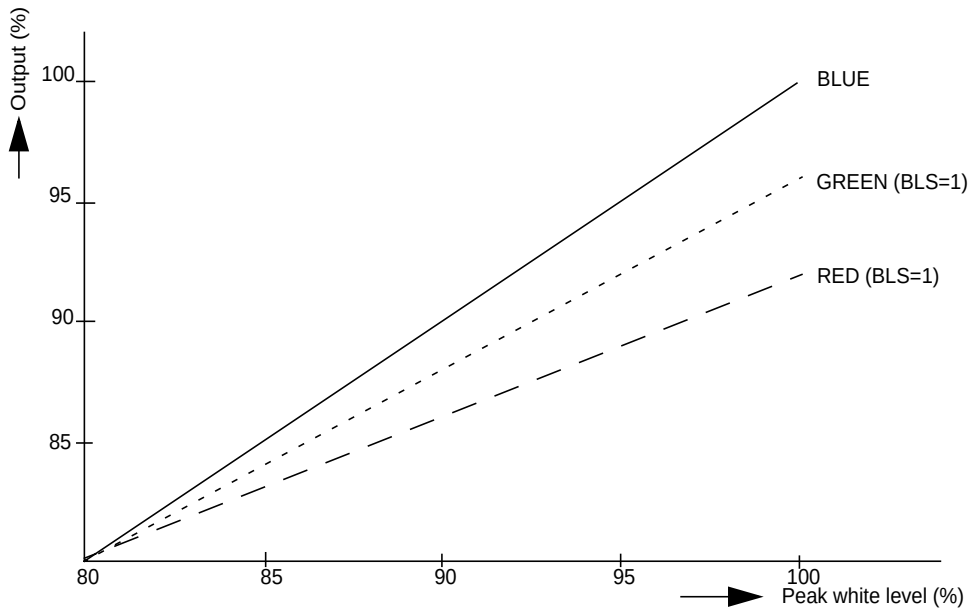


Fig.37 Blue stretch characteristic

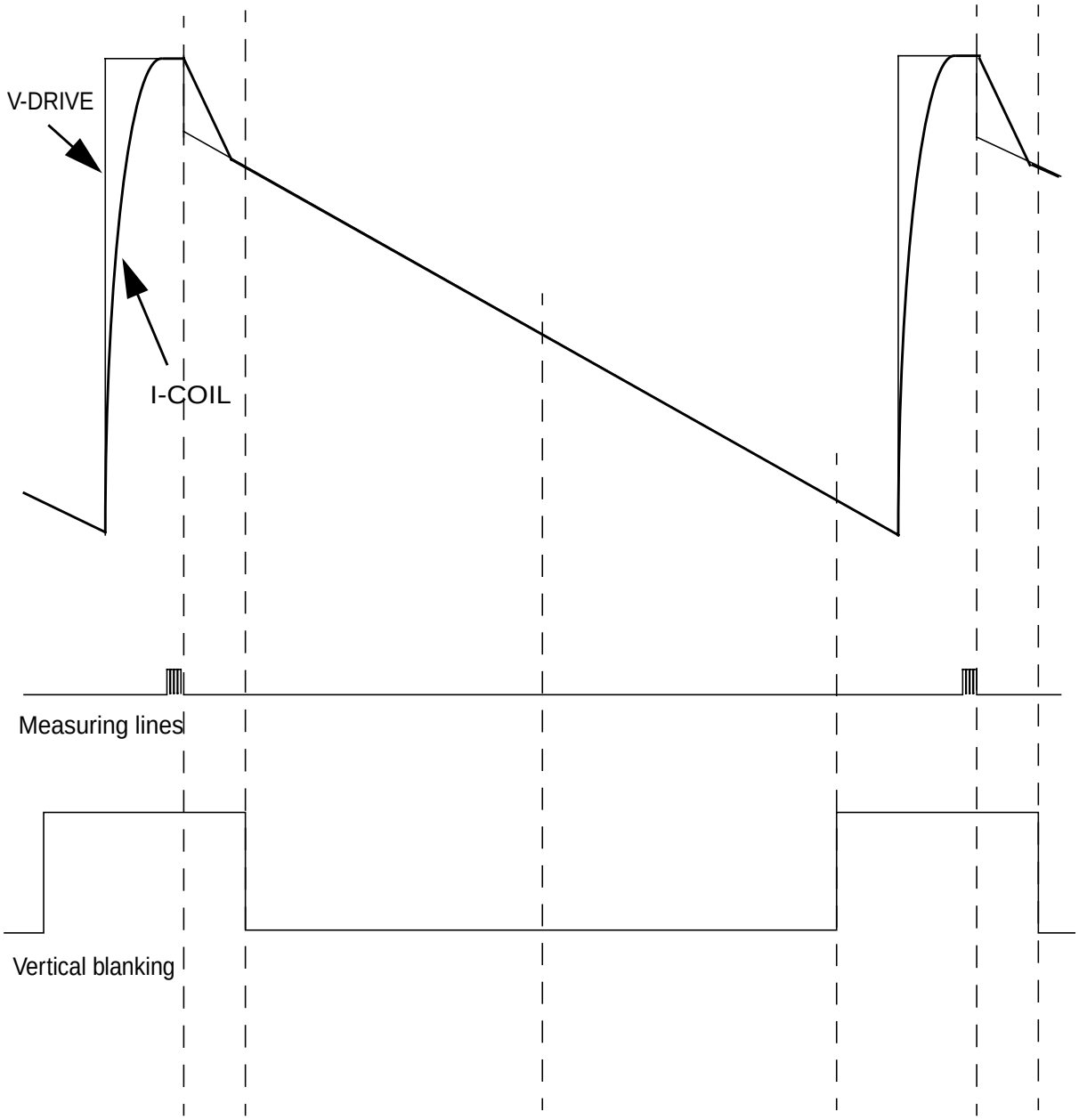


Fig.38 Measuring lines in vertical overscan for vertical compressed scan

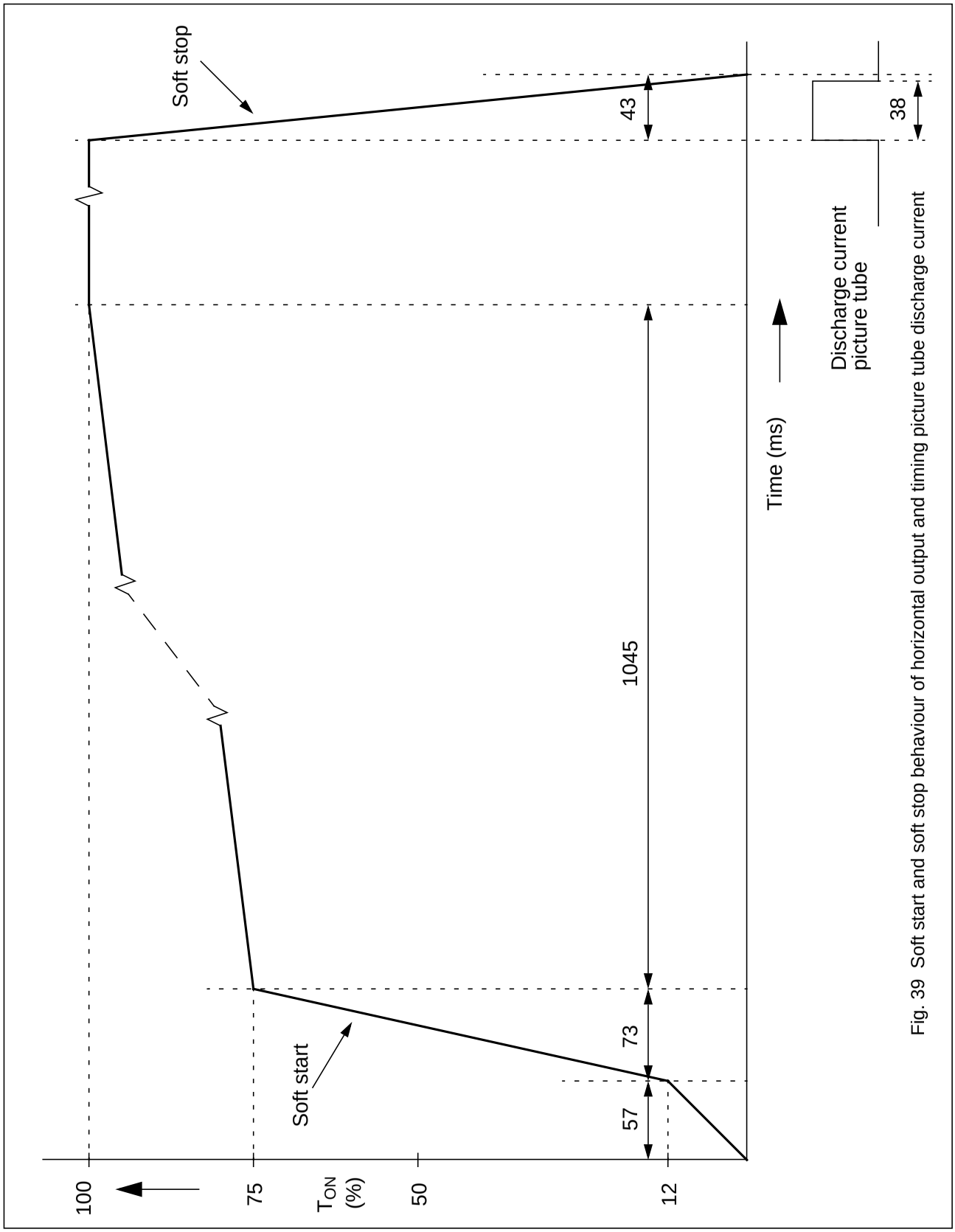


Fig. 39 Soft start and soft stop behaviour of horizontal output and timing picture tube discharge current

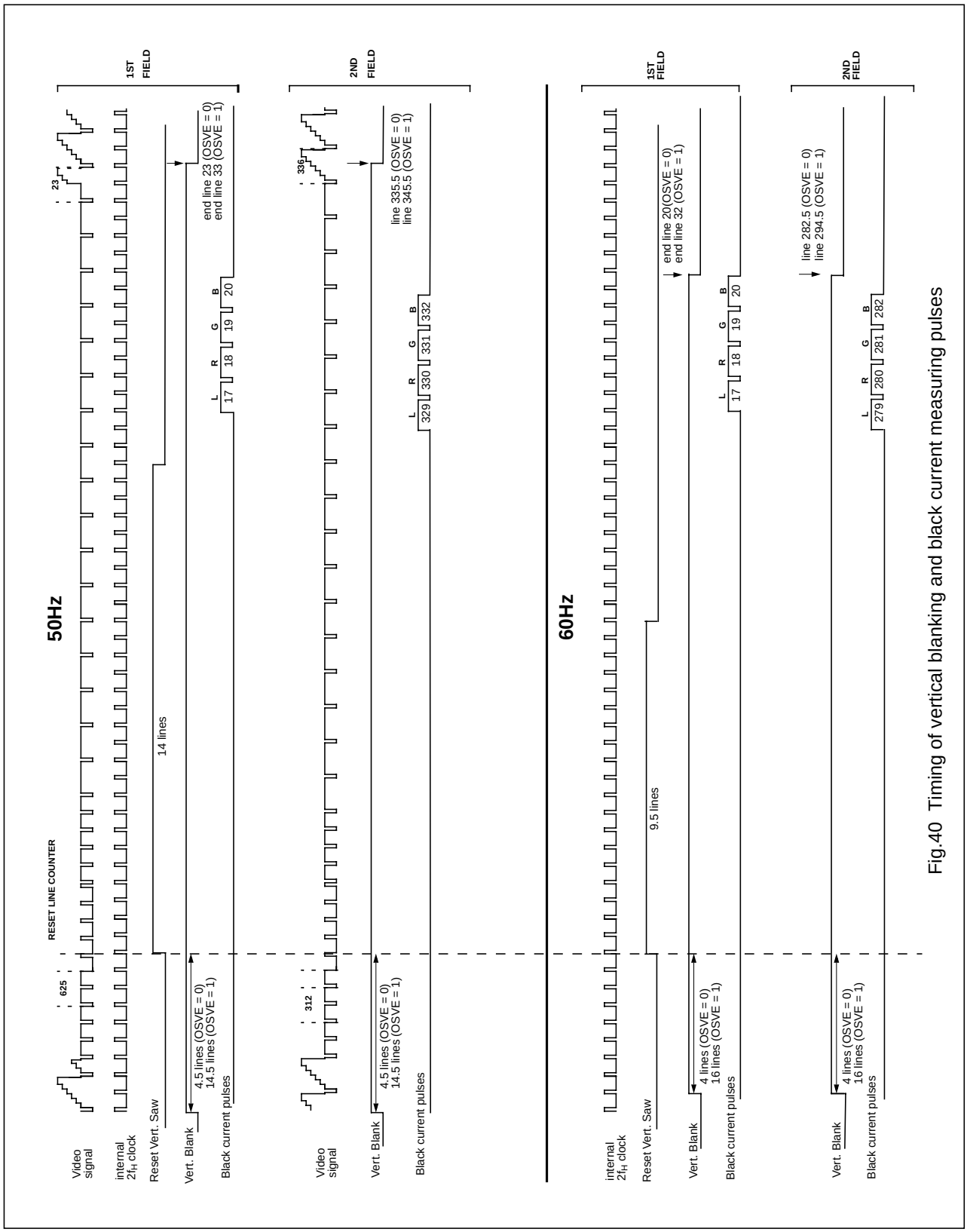


Fig.40 Timing of vertical blanking and black current measuring pulses

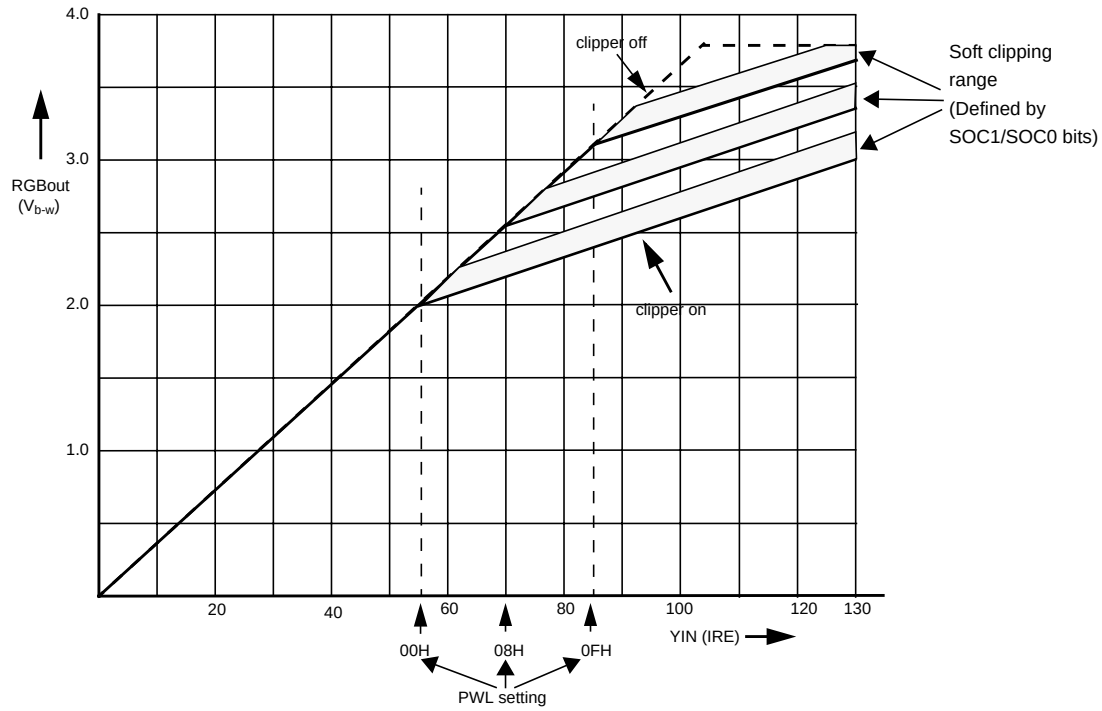


Fig.41 Peak White Limiting / Soft clipper characteristic.

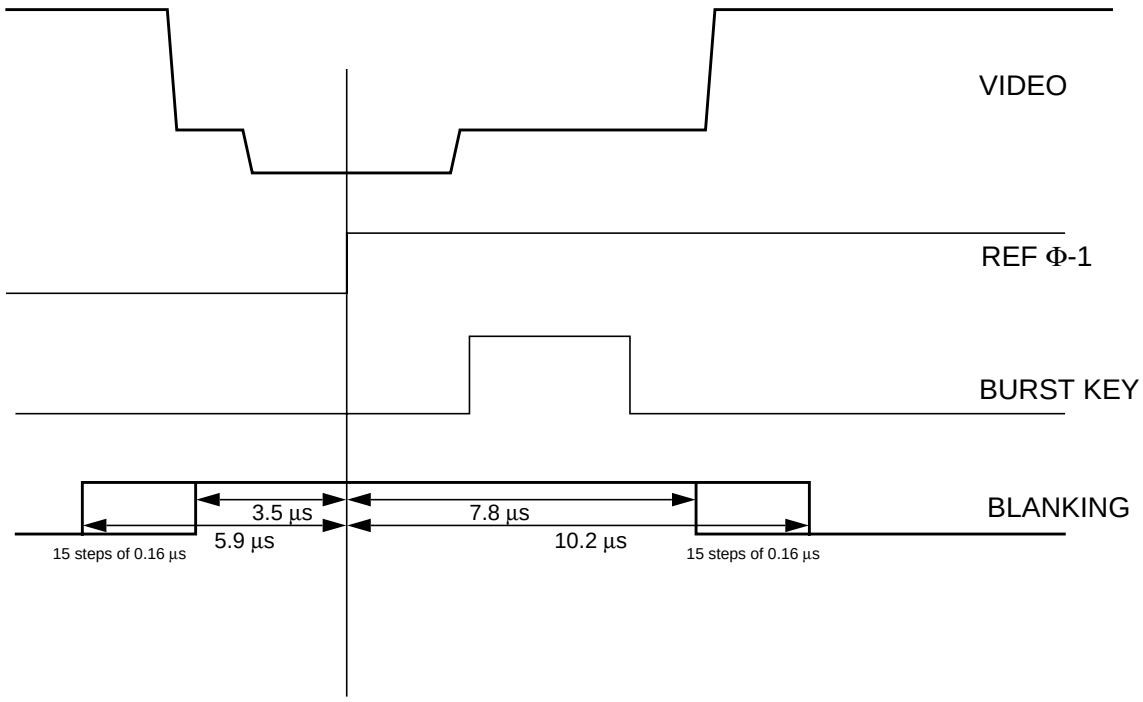


Fig.42 Timing of horizontal wide blanking

TEST AND APPLICATION INFORMATION

East-West output stage

In order to obtain correct tracking of the vertical and horizontal EHT-correction, the EW output stage should be dimensioned as illustrated in Fig.43.

Resistor R_{EW} determines the gain of the EW output stage. Resistor R_c determines the reference current for both the vertical sawtooth generator and the geometry processor. The preferred value of R_c is 39 kΩ which results in a reference current of 100 μA (V_{ref} = 3.9 V).

The value of R_{EW} must be:

$$R_{EW} = R_c \times \frac{V_{scan}}{18 \times V_{ref}}$$

Example: With V_{ref} = 3.9 V; R_c = 39 kΩ and V_{scan} = 120 V then R_{EW} = 68 kΩ.

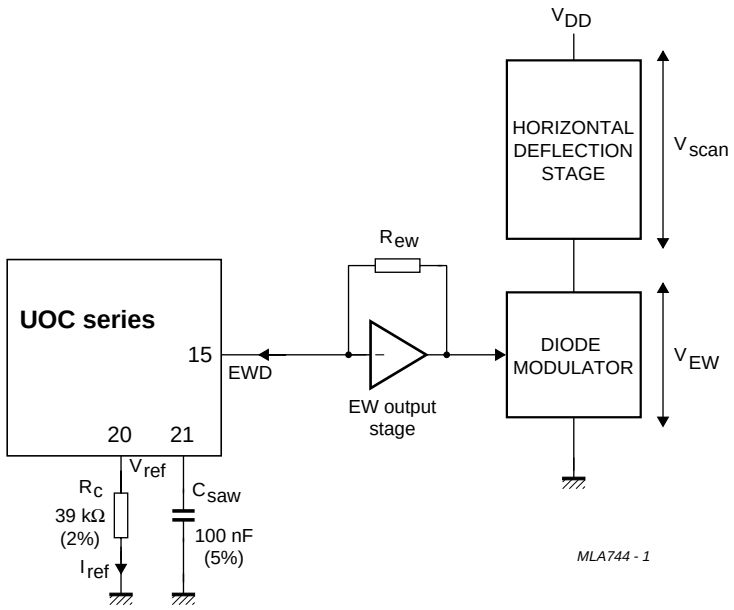
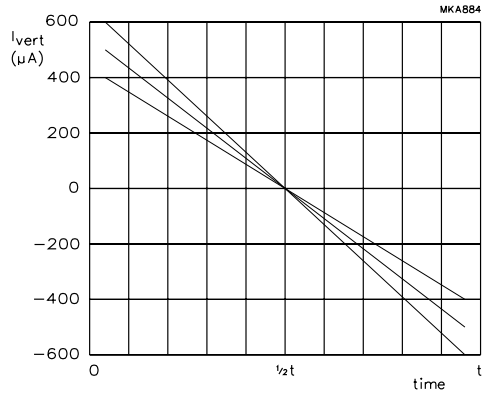
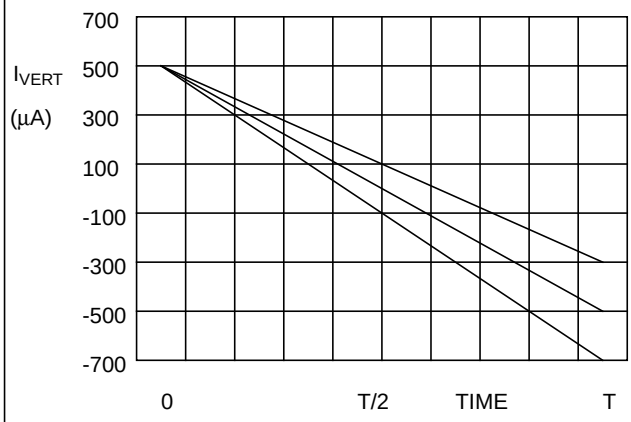


Fig. 43 East-West output stage.



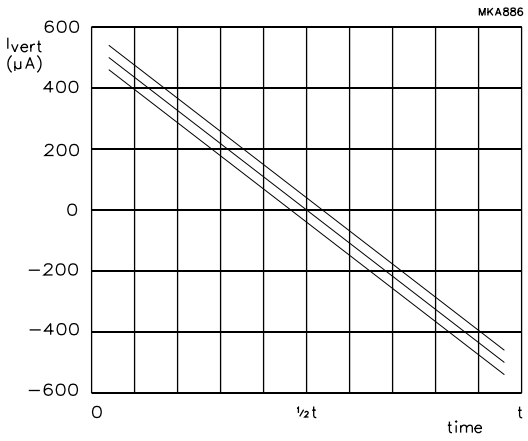
VA = 0, 1FH and 3FH; VSH = 1FH; SC = 0EH.

Fig. 44 Control range of vertical amplitude.



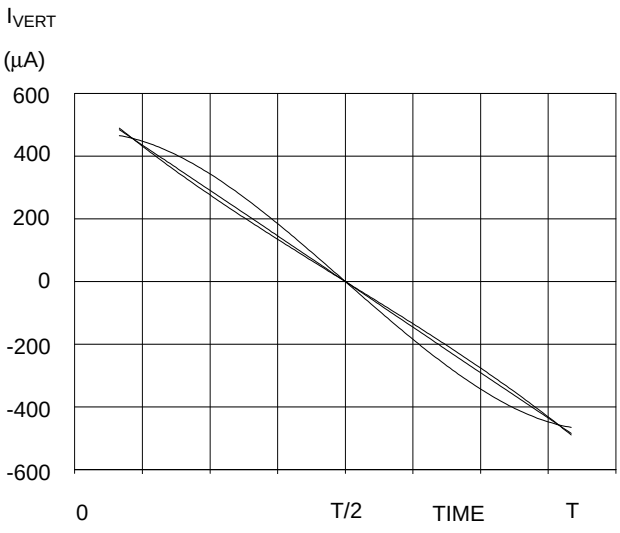
VS = 0, 1FH and 3FH; VA = 1FH; VSH = 1FH; SC = 0EH.

Fig. 45 Control range of vertical slope.



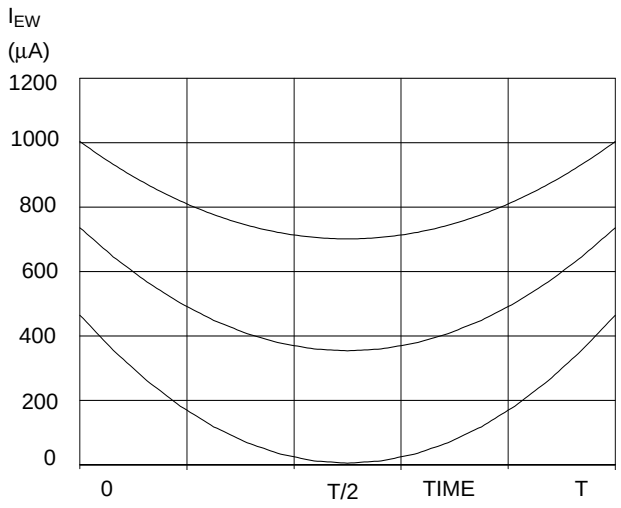
VSH = 0, 1FH and 3FH; VA = 1FH; SC = 0EH.

Fig. 46 Control range of vertical shift.



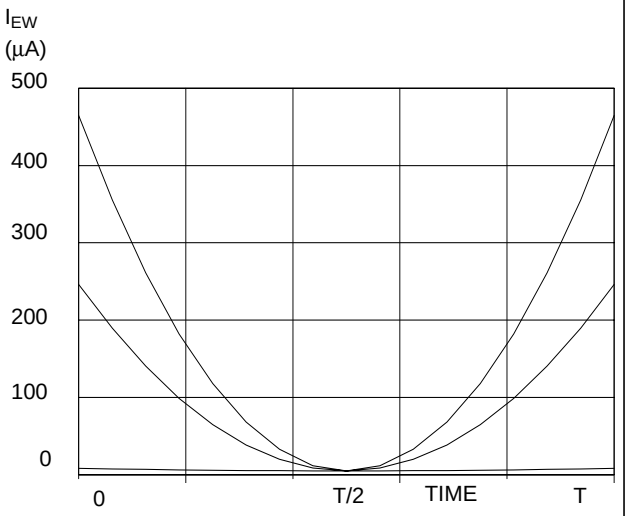
SC = 0, 0EH and 3FH; VA = 1FH; VSH = 1FH.

Fig. 47 Control range of S-correction.



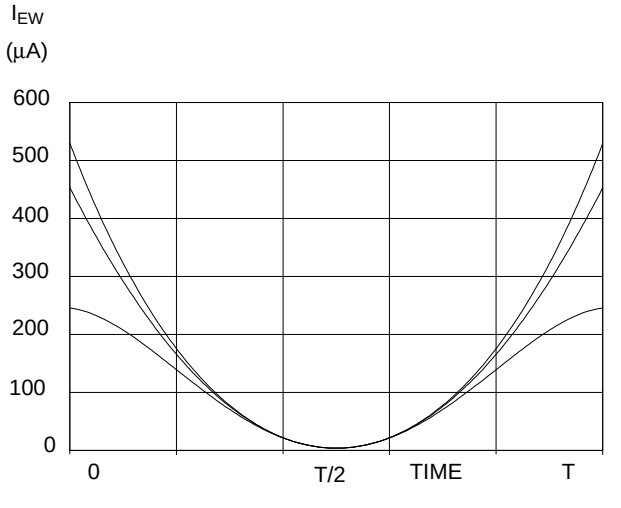
EW = 0, 1FH and 3FH; PW = 3FH; TC = 1FH; CP = 11H.

Fig. 48 Control range of EW width.



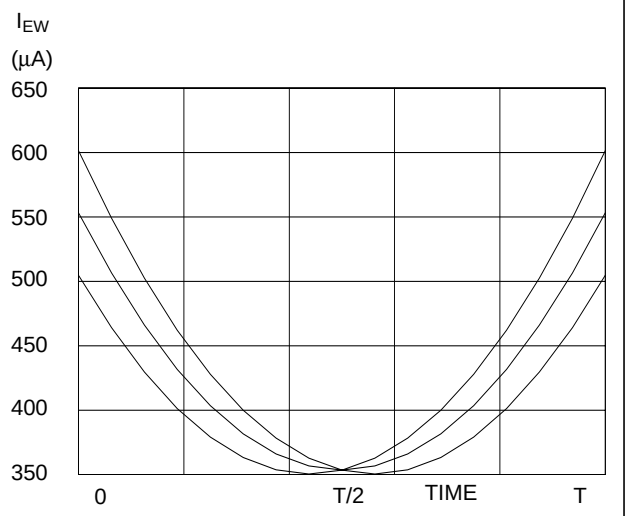
PW = 0, 1FH and 3FH; EW = 3FH; TC = 1FH; CP = 11H.

Fig. 49 Control range of EW parabola/width ratio.



CP = 0, 11H and 3FH; EW = 3FH; PW = 3FH; TC = 1FH.

Fig. 50 Control range of EW corner/parabola ratio.



TC = 0, 1FH and 3FH; EW = 1FH; PW = 1FH; CP = 11H.

Fig. 51 Control range of EW trapezium correction.

Adjustment of geometry control parameters

The deflection processor offers 11 control parameters for picture alignment, viz:

- S-correction
- vertical amplitude
- vertical slope
- vertical shift
- horizontal shift.
- EW width
- EW parabola width
- EW upper/lower corner parabola
- EW trapezium correction.
- Vertical zoom
- Horizontal parallelogram and bow correction

It is important to notice that the ICs are designed for use with a DC-coupled vertical deflection stage. This is the reason why a vertical linearity alignment is not necessary (and therefore not available).

For a particular combination of picture tube type and vertical output stage it is determined which are the required values for the settings of the S-correction. This parameters can be preset via the I^2C-bus, and do not need any additional adjustment. The rest of the parameters are preset with the mid-value of their control range (i.e. 1FH), or with the values obtained by previous TV-set adjustments.

The vertical shift control is meant for compensation of off-sets in the external vertical output stage or in the picture tube. It can be shown that without compensation these off-sets will result in a certain linearity error, especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the value of the off-set, and to the square of the S-correction needed. The necessity to use the vertical shift alignment depends on the expected off-sets in vertical output stage and picture tube, on the required value of the S-correction, and on the demands upon vertical linearity.

For adjustment of the vertical shift and vertical slope independent of each other, a special service blanking mode can be entered by setting the SBL bit HIGH. In this mode the RGB-outputs are blanked during the second half of the picture. There are 2 different methods for alignment of the picture in vertical direction. Both methods make use of the service blanking mode.

The first method is recommended for picture tubes that have a marking for the middle of the screen. With the vertical shift control the last line of the visible picture is positioned exactly in the middle of the screen. After this adjustment the vertical shift should not be changed. The top of the picture is placed by adjustment of the vertical amplitude, and the bottom by adjustment of the vertical slope.

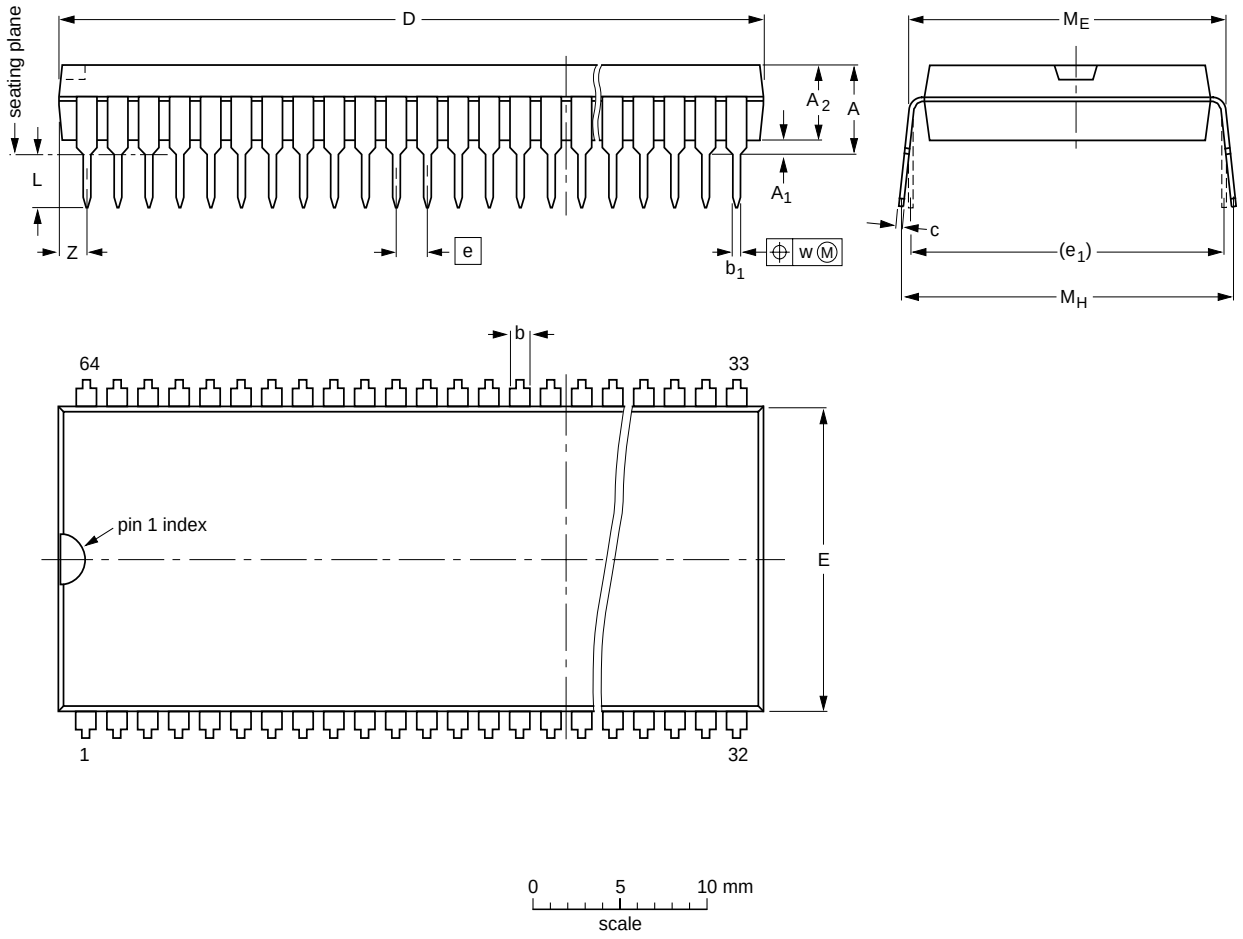
The second method is recommended for picture tubes that have no marking for the middle of the screen. For this method a video signal is required in which the middle of the picture is indicated (e.g. the white line in the circle test pattern). With the vertical slope control the beginning of the blanking is positioned exactly on the middle of the picture. Then the top and bottom of the picture are placed symmetrical with respect to the middle of the screen by adjustment of the vertical amplitude and vertical shift. After this adjustment the vertical shift has the right setting and should not be changed.

If the vertical shift alignment is not required VSH should be set to its mid-value (i.e. VSH = 1F). Then the top of the picture is placed by adjustment of the vertical amplitude and the bottom by adjustment of the vertical slope. After the vertical picture alignment the picture is positioned in the horizontal direction by adjustment of the horizontal shift.

To obtain the full range of the vertical zoom function the adjustment of the vertical geometry should be carried out at a nominal setting of the zoom DAC at position 19 HEX.

PACKAGE OUTLINE

SDIP64: plastic shrink dual in-line package; 64 leads (750 mil) **SOT274-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.84	0.51	4.57	1.3 0.8	0.53 0.40	0.32 0.23	58.67 57.70	17.2 16.9	1.778	19.05	3.2 2.8	19.61 19.05	20.96 19.71	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT274-1						~~92-10-13~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC package Databook"* (order code 9398 652 90011).

SDIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

QFP

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.